CIRRUS LOGIC

CL-GD5320

Data Sheet

FEATURES

- 100-pin QFP single-chip VGA
- Two 256K x 4 DRAM interface
- 100% hardware-register- and BIOS-compatible with VGA, EGA, CGA, MDA and Hercules® HGC
- Fully compatible motherboard VGA solution for IBM® PS/2™ Model 30
- Motherboard VGA solution with only seven ICs
- Equivalent interleave ratio of 1:2.5
- 8/16-bit CPU interface
- Multiple FIFO sequencer design
- CPU-to-video-memory read/write cache
- Auto monitor/bus width detection support
- No external PALs required
- Independent video and DRAM timings
- 800 x 600 x 16 resolution — VESA-compatible
- 132-column support for PS/2 and multifrequency monitors
- 36 or 40 MHz dot clock
- Low-power CMOS technology
- Board-level testability *(CL-GD5325* only)*

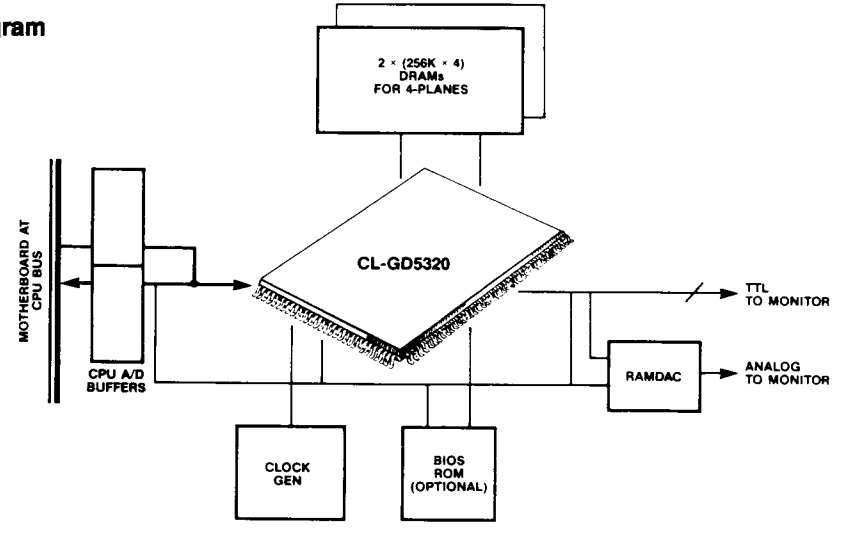
Enhanced VGA-Compatible Graphics Chip

OVERVIEW

The single-chip CL-GD5320 VGA graphics controller is hardware-compatible with the IBM VGA, EGA, CGA, and MDA standards, as well as Hercules HGC, and provides improved performance and additional functionality.

Operating at dot clock rates up to 40 MHz, the CL-GD5320 chip supports high-resolution graphics and alphanumeric display modes for both monochrome and color, and for high-resolution variable frequency and PS/2 monitors. Video outputs are provided in four bits per pixel (all resolutions) and eight bits per pixel (320 x 200, 320 x 240, 360 x 480). Using analog video output and an external RAMDAC, selection may be made from 256K colors.

System Block Diagram



OVERVIEW (cont.)

The CL-GD5320 implements all control and data registers in the current graphics standards, including those of the 6845 CRT Controller. The chip also implements all data manipulation capabilities and data paths, providing complete hardware and software compatibility.

Relative to the IBM VGA standard, the CL-GD5320 design provides extra memory cycles to the CPU. Memory cycles not used to refresh the display or video memory are allocated to process CPU memory requests. Speed improvements are obtained by using page mode access to DRAMs for consecutive locations on the same row.

The hardware supports graphics cursor. Additional text cursor controls include blink disable and replace/invert mode control. The hardware supports simultaneous and independent smooth scrolling of two separate text screens.

The CL-GD5320 is designed for minimum external circuitry support and is ideal for integrated systems. Support circuitry can include timing sources, memory, and RAMDAC. A minimum motherboard implementation of seven ICs can be achieved with the CL-GD5320.

* Otherwise identical to the CL-GD5320, the CL-GD5325 provides a board-level testability feature.

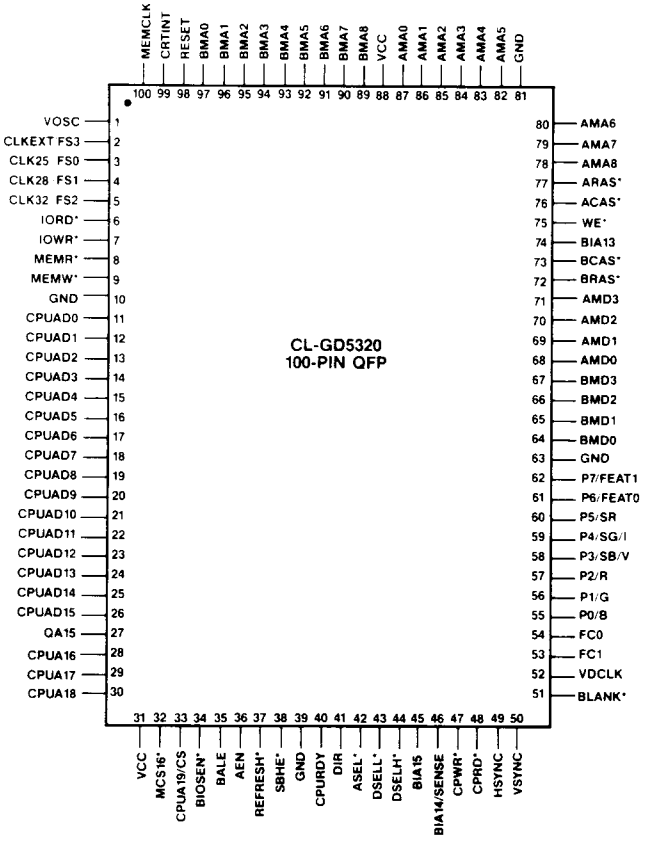
ADVANTAGES

Unique Features	Benefits
• *Interface to two 1 Mbit DRAMs*	Minimum chip count design for a very cost-effective implementation.
• *Hardware compatibility with VGA, EGA, CGA, MDA, and HGC standards*	True backward compatibility for installed software base.
• *Support for PS/2 analog monitors, multi-frequency monitors, color and monochrome TTL monitors*	Drives most IBM-PC-compatible monitors; end user isn't forced to upgrade
• *Page mode access to DRAMs*	Improved performance on video memory access.
• *Independent video and DRAM timing*	Allows flexible video subsystems design.
• *Multiple FIFO sequencer design*	Fast host access to video memory.
• *CPU-to-video memory cache*	More bandwidth available to the host.
• *Enhanced split screen capability*	Simplifies driver software while improving performance.
• *Hardware graphics cursor*	Dramatically reduces software overhead for mouse pointer. Graphics applications and environments (e.g., Microsoft® Windows™ and DR™ GEM™) run faster.
• *Flexible vertical interrupt mechanism*	Allows programs to perform where there is a need to execute synchronously with video.
• *Nonintrusive software ID of devices*	Simplifies installation of device-specific drivers and applications.
• *Four pages of memory for mode 13h (320 x 200 resolution mode)*	Permits 256-color images to be switched rapidly to produce color animation.
• *Read back capability of all registers*	Eliminates the need for shadow registers, and allows graphics controller state-save for multi-tasking applications.

Table of Contents

1. PIN INFORMATION

1.1 Pin Diagram



(*) Denotes negative true signal

1.2 Pin Assignment Table

NAME	CL-GD5320 PIN NO.	TYPE	FUNCTION	Analog	ECD	CD	MD
PROCESSOR INTERFACE							
BIOSEN*	34	O	BIOS output enable				
MEMR*, MEMW*	8, 9	I	CPU read/write of video memory				
IORD*, IOWR*	6, 7	I	I/O R/W strobes				
CPUAD [15:0]	26..11	I/O	Bidirectional multiplexed address data to/from host CPU				
BIA [15:13]	45, 46, 74	I/O	Bidirectional multiplexed BIOS address programmable inputs				
CPUA [18:16]	30..28	I	Upper three bits of CPU address bus				
CPUA19/CS	33	I	MSB of CPU address bus or CS input				
QA15	27	I	Address 15 lookahead				
MCS16*	32	O	16-bit acknowledge				
RESET	98	I	System reset				
REFRESH*	37	I	System refresh				
CPURDY	40	O	Data available signal for wait state logic				
CRTINT	99	O	Display retrace interrupt				
DIR	41	O	Bidirectional CPU data bus transceiver control (I = Write, O = Read)				
AEN	36	I	Prevent I/O during DMA cycles				
SBHE*	38	I	Bus high enable from host				
ASEL*, DSELL*, DSELH*	42, 43, 44	O	Address and data select (low and high byte) enable				
BALE	35	I	Buffered Address Latch Enable				
DISPLAY MEMORY DATA INTERFACE							
AMD[3:0]	71..68	I/O	4-bit-wide bidirectional data bus to planes 0 and 1				
BMD[3:0]	67..64	I/O	4-bit-wide bidirectional data bus to planes 2 and 3				
DISPLAY MEMORY CONTROL INTERFACE							
AMA[8:0]	78..80, 82..87	O	Address bus to byte planes 0 and 1				
BMA[8:0]	89..97	O	Address bus to byte planes 2 and 3				
ARAS*, BRAS*	77, 72	O	Row address strobes to planes 0, 1 and 2, 3				
ACAS*, BCAS*	76, 73	O	Column address strobes to planes 0, 1 and 2, 3				
WE*	75	O	Video memory write enable				
MEMCLK	100	I	Independent video memory clock**				
EXTERNAL INTERFACE							
CPRD*	48	O	Color Palette read signal				
CPWR*	47	O	Color Palette write signal				
VOSC	1	I	Oscillator input, must be connected to a clock				
BIA14/SENSE	46	I/O	BIOS address 14 or monochrome/color monitor detect				
FC [1:0]	53, 54	O	Programmable output pins, normally drive feature connectors				
CLKEXT/FS3, CLK32/FS2, CLK28/FS1, CLK25/FS0	2, 5..3	I/O	Programmable I/O pins for clocks/frequency select lines				
VIDEO INTERFACE							
VDCLK	52	O	Video data clock				
VSYNC	50	O	CRT horizontal sync				
HSYNC	49	O	CRT horizontal sync				
BLANK*	51	O	Video blanking signal				
P7/FEAT1	62	I/O	Pixel data MSB/Feature Bit 1	P7			
P6/FEAT0	61	I/O	Pixel data 6/Feature Bit 0	P6			
P5/SR	60	O	Pixel data 5/Secondary Red	P5	SR		
P4/SG/I	59	O	Pixel data 4/Secondary Green/Intensity	P4	SG	I	I
P3/SB/V	58	O	Pixel data 3/Secondary Blue/Video	P3	SB		V
P2/R	57	O	Pixel data 2/Primary Red	P2	R	R	
P1/G	56	O	Pixel data 1/Primary Green	P1	G	G	
P0/B	55	O	Pixel data LSB/Primary Blue	P0	B	B	

** 44 MHz MEMCLK for 80 ns, 36.4 MHz for 100 ns, and 31 MHz for 120 ns page mode DRAMs

2. DETAILED SIGNAL DESCRIPTION

2.1 Processor Interface

Name	Pin No.	CL-GD5320	Description
CPUAD [15:0]	26..11	I/O	Bidirectional multiplexed address/data bus between the CPU and the CL-GD5320 for video memory and I/O.
BIA [15:13]	45, 46, 74	I/O	Bidirectional multiplexed BIOS page address outputs. The BIOS Page Addresses [BIA15:BIA13] need to be used only when there is a requirement for physical BIOS ROM size greater than 32K x 8 bytes. BIA14 is multiplexed with SENSE, for monitor detection.
CPUA [18:16]	30..28	INPUT	Upper CPU addresses from the CPU for all required decoding.
CPUA19/CS	33	INPUT	Connected to SA19 (8-bit bus system) or CS (LA[23..LA19], 16-bit bus system) for all required decoding.
QA15	27	INPUT	Connected to local address 15 for fast MCS16* response.
CPURDY	40	OUTPUT	Inactive (tri-state) when no video memory CPU request is pending. The request may be either MEMR* or MEMW*. At the beginning of a CPU access to video memory, CPURDY may drop low, putting the CPU in a wait-state. This condition is held until the video memory sequencer fits the memory request into the next available 'slot'. At completion of the sequencer CPU memory cycle, CPURDY is driven high until MEMR* and MEMW* go inactive and then returns to tri-state condition.
CRTINT	99	OUTPUT	Enabled by setting Bit 5 of the Vertical Retrace End Register to '0' and cleared by setting Bit 4 of the Vertical Retrace End Register to '0'. When enabled, the CRTINT pin will go high at the start of the vertical retrace interval and remain high until cleared by a write of '0' to Bit 4 of the Vertical Retrace End Register (CR11). CRTINT is enabled by setting bit 5 of CR11 to '0' and setting Bit 4 of CR11 to '1'. If Bit 4 is not set to '1' after clearing the initial CRTINT, interrupts will cease. Register CR11 is also readable. This feature greatly simplifies the task of ORing in the proper value for the remaining bits of CR11 (not the case for an IBM EGA or VGA controller).
DIR	41	OUTPUT	Controls the direction of the data flow on the bidirectional CPUAD bus. Driven low when the CPU is performing an I/O or memory read cycle. This signal can also be used for PC XT slot-8 control.

(*) Denotes negative true signal.

2.1 Processor Interface *(cont.)*

Name	Pin No.	CL-GD5320	Description
MCS16*	32	OUTPUT	Acknowledge for 16-bit-wide accesses. It is generated by the CL-GD5320 only if the 16-bit peripheral mode is enabled and a valid memory address range has been decoded. It may be generated by a full internal decode (LA [19:17], SA [16:14]) and partial internal decode with QA15 for fastest response time.
IORD*, IOWR*	6 7	INPUT	When low, indicates that an IORD* or IOWR* cycle is taking place within the proper I/O address range.
RESET	98	INPUT	Normally connected to the system reset bus signal and is used as a hardware reset of the CL-GD5320 chips. An identical reset state can be accomplished via software by setting SR0-bit 0 to '0'.
MEMR*, MEMW*	8	INPUT	Video memory read and write strobes. These inputs are driven low during CPU memory read/write access to the video memory.
BIOSEN*	34	OUTPUT	Typically connected to a ROM BIOS OE* input. Enables the BIOS ROMs output if a memory address in the C000:0000-C000:7FFF range has been internally decoded and ROM control register Bit 7 is cleared.
BALE	35	INPUT	Buffered Address Latch Enable. High indicates valid unlatched 'LA' addresses on the bus.
AEN	36	INPUT	Host CPU bus signal that distinguishes between DMA and non-DMA bus cycles. The signal is high for a DMA cycle.
REFRESH*	37	INPUT	Indicates host system refresh of bus attached main memory and tells CL-GD5320 to ignore memory addresses on the bus.
SBHE*	38	INPUT	Host CPU System Byte High Enable. If no SBHE input is available, this pin should be pulled up with 4.7K resistor.
ASEL*	42	OUTPUT	Low active output signal; used to enable the 16-bit CPU address bus.
DSELL*	43	OUTPUT	Low active output signal; used to enable the low byte D[7:0] the CPU data bus access.
DSELH*	44	OUTPUT	Low active output signal; used to enable the high byte D[15:8] of the CPU data bus access.

(*) Denotes negative true signal.

2.2 Display Memory Data/Control Interface

Name	Pin No.	CL-GD5320	Description
AMA [8:0]	78..80, 82..87	OUTPUT	Multiplexed video memory address bus A. This bus contains the row/column address information required by the DRAMs in the video memory for 64K byte memory planes 0 and 1.
BMA [8:0]	89..97	OUTPUT	Multiplexed video memory address bus B. This bus contains the row/column address information required by the DRAMs in the video memory for 64K byte memory planes 2 and 3.
AMD[3:0]	71..68	I/O	Bidirectional video memory data bus; controlled by the CL-GD5320 for read/write operations into video memory planes 0 and 1, which store graphics data for color plane 0 and 1 or character/attribute codes in the text modes. The CL-GD5320 uses these character codes in Text Mode to produce the proper address on the BMA bus to access the character generator fonts.
BMD [3:0]	67..64	I/O	Bidirectional video memory data bus; controlled by CL-GD5320 for read/write operations into video memory planes 2 and 3, which store graphics data for color planes 2 and 3 or character fonts in text modes.
ARAS*, BRAS*	77, 72	OUTPUT	Video memory DRAM row address strobes. A low-going edge on these signals latches the row address (contained on the AMA and BMA memory address buses) into the video memory DRAMs.
ACAS*, BCAS*	76, 73	OUTPUT	Video memory DRAM column address strobes. A low-going edge on these signals latches the column address (contained on the AMA and BMA memory address buses) into the video memory DRAMs.
WE*	75	OUTPUT	When low, this signal enables a video memory write to the bank selected by the appropriate RAS* signal(s).
MEMCLK	100	INPUT	Display memory sequencer clock. 44 MHz for 80 ns (all resolutions, including 800 x 600 x 16), 36.4 MHz for 100 ns (all resolutions, excluding 800 x 600 x 16), and 31 MHz for 120 ns (standard resolutions only) with page mode 256K x 4 DRAMs.

(*) Denotes negative true signal.

2.3 Video Interface

The PIXEL DATA bits drive the analog or digital inputs of color or monochrome displays. P0-P5 bits are always 'on' if video out is enabled by AR-12 (Attribute Register 12) Bit 4. P6 and P7 are also enabled by this register and bit, but are AND'ed with the 8-bit Video Enable Bit (Extension Index 87, Bit 4). P0-P7 pins are described in the following table:

Name		Description	Pin No.	Analog RAMDAC Interface	ECD 64-color Digital	CD 16-color Digital	MD Mono-chrome	GD5320
P7/FEAT1	Pixel Bit 7/	Feature Bit 1**	62	P7	–	–	–	OUTPUT INPUT
P6/FEAT0	Pixel Bit 6/	Feature Bit 0**	61	P6	–	–	–	OUTPUT INPUT
P5/SR	Pixel Bit 5/	Secondary Red	60	P5	SR	–	Note	OUTPUT
P4/SG/I	Pixel Bit 4/	Secondary Green/ Intensity	59	P4	SG	I	I, Note	OUTPUT
P3/SB/V	Pixel Bit 3/	Secondary Blue/Video	58	P3	SB	–	V, Note	OUTPUT
P2/R	Pixel Bit 2/	Primary Red	57	P2	R	R	Note	OUTPUT
P1/G	Pixel Bit 1/	Primary Green	56	P1	G	G	Note	OUTPUT
P0/B	Pixel Bit 0/	Primary Blue	55	P0	B	B	Note	OUTPUT

** FEAT1 and FEAT0 (Feature Bits 1 and 0) are programmable as inputs to the FC Register (Feature Control) and can be read at port address 3CA.

NOTE: In monochrome modes, video outputs are driven from CL-GD5320 Palette Registers 0, 7, 8, 15 as follows:

Intensity	Video	Palette Register Selected	Mode
0	0	0	Monochrome, Text or HGC Graphics
0	1	7	Monochrome, Text or HGC Graphics
1	0	8	Monochrome, Text Only
1	1	15	Monochrome, Text Only

Intensity = Text Mode attribute byte, Bit 3
Video = Normal output to monochrome display

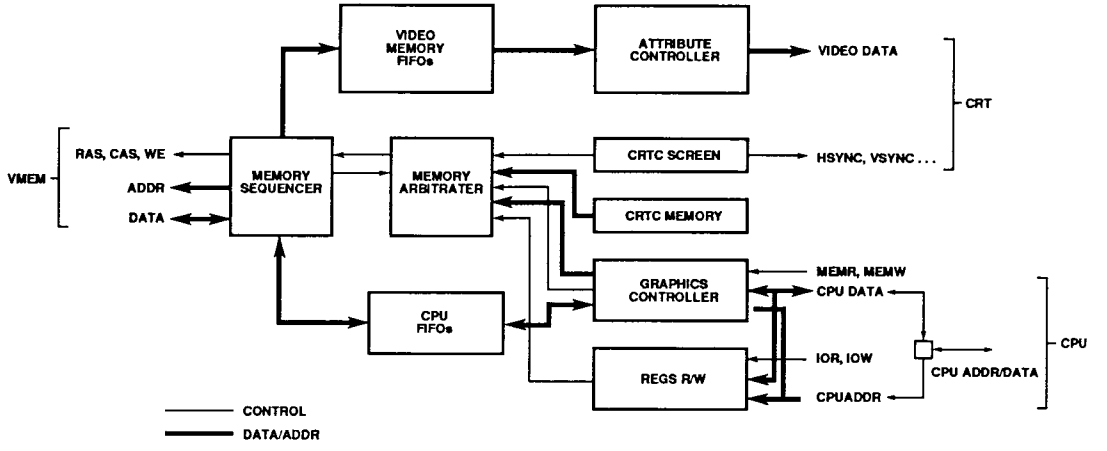
2.3 Video Interface *(cont.)*

Name	Pin No.	CL-GD5320	Description
HSYNC	49	OUTPUT	Horizontal Sync. The active polarity of this signal can be selected by Bit 6 of the Miscellaneous Output Register (I/O address 3C2H) or Bit 6 of the Timing Control Register (extension address 85H).
VSYNC	50	OUTPUT	Vertical Sync. The active polarity of this signal can be selected by Bit 7 of the Miscellaneous Output Register (I/O address 3C2H) or Bit 7 of the Timing Control Register (extension address 85H).
VDCLK	52	OUTPUT	Video Clock. Used to clock data through the horizontal shift registers. This signal should be used for all video timing purposes.
BLANK*	51	OUTPUT	Blanking pulse to the external RAMDAC to maintain video synchronization. During the active state of this signal the RGB lines are blanked.

2.4 External Interface

Name	Pin No.	CL-GD5320	Description
FC[1:0]	53, 54	OUTPUT	Programmable output pins, normally used to drive feature connector.
BIA14/SENSE	46	I/O	Programmable input pin typically used to detect whether a monitor is connected and whether it is monochrome or color. This pin is multiplexed with BIA14 for BIOS page addressing.
CPWR*, CPRD*	47 48	OUTPUT OUTPUT	Color palette read/write strobes. These pins are active when valid I/O reads or writes to port addresses xC6H-xC9H are decoded.
VOSC	1	INPUT	Oscillator input, which must be connected to a clock, typically 14.318 MHz from the system bus. If an external clock synthesizer or multiplexer is used, this pin becomes the video clock source input. Pixel clock of up to 40 MHz can be supplied.
CLKEXT/FS3 CLK32/FS2 CLK28/FS1 CLK25/FS0	2 5 4 3	I/O I/O I/O I/O	These pins are configured as inputs or outputs based on the state of CPUAD14 latched from the bus on the falling edge of RESET*. They can be driven from crystal oscillators to provide 32.514, 28.322, and 25.172 MHz inputs to the CL-GD5320 internal mux (when required, a 16.257 MHz clock is internally generated). Thirty-six and 40 MHz clock oscillators can be connected to the CLK32/FS2 Pin. When configured as outputs, they provide select signals to an external PLL-based multifrequency synthesizer circuit.

(*) Denotes negative true signal.



CL-GD5320 Chip Block Diagram

3. FUNCTIONAL DESCRIPTION

3.1 General

The CL-GD5320 offers a complete solution for VGA, EGA, CGA, MDA and Hercules HGC graphics standards. All the hardware required to implement CPU updates to memory, screen refresh, and DRAM refresh are included in the CL-GD5320. It interfaces directly to the host system bus, to the display memory, and to the monitor. The host interface can be either eight or sixteen bits wide. The CL-GD5320 chip requires no external PAL for address decoding and control logic handshaking. The following functional blocks have been integrated into the CL-GD5320:

- **The Graphics Controller**

The Graphics Controller interfaces to the CPU and the display memory planes to perform text manipulations, data rotating, color mapping, and miscellaneous operations.

- **The Sequencer**

The Sequencer generates all of the required timing for display memory interfacing. This includes RAS and CAS timings for the display memory, bit map, character mapping, and DRAM refresh.

- **The CRT Controller**

The CRT Controller generates all the required timings for monitor interfacing. It supports all the 6845 CRT controller functions.

- **The Attribute Controller**

The Attribute Controller formats the display data to the screen. Display color selection, text blinking, underlining, and horizontal timing display generation are performed by the Attribute Controller.

A 32-x-32-bit hardware cursor, which is also responsible for pixel panning, is generated in this unit. Foreground and background attributes are specified for each character in alphanumeric mode. Cursors and borders are also controlled by the CL-GD5320.

3.2 Functional Operation

The four major operations supported by the CL-GD5320 are:

- **Host access to all CL-GD5320 registers**
- **Host access to display memory**
- **Memory refresh**
- **Screen refresh**

Memory bandwidth is allocated to each process according to the actual realtime needs of the process, ensuring efficient use of the available bandwidth. The display is blanked during horizontal and vertical retrace intervals, freeing memory bandwidth for host access and/or memory refresh. Unlike early VGA implementations that gave the host only 1:7 interleave ratio, the CL-GD5320 can give the host up to 1:2.5 interleave ratio to video memory. This is achieved by virtue of proprietary algorithms and multiple FIFO sequencer design.

Host Access to Registers

The host (typically an 8088/80286/80386SX/80386DX/80486 processor in an IBM PC/XT/AT-bus-compatible environment) can access CL-GD5320 registers by setting up 16-bit addresses and generating IORD*/IOWR* signals to read or write eight bits of data.

DRAM and screen refresh occur concurrently and independently (unless display parameters are being changed by the host CPU actions on CL-GD5320 registers).

The registers that may be accessed by the host are listed in Sections 4 and 5. They include all the registers of IBM VGA, EGA, CGA, MDA, and Hercules HGC standard, including those of the 6845 CRT controller. All registers, including non-VGA registers, have been made host-readable in order to allow BIOS and driver software to determine the state of the graphics adapter.

Host Access to Display Memory

Host access to Display Memory is channeled via the CL-GD5320. The host must set up the proper address/data parameters in CL-GD5320 registers, and then handshake with the CL-GD5320 in order to access the Display Memory.

Data Interface between the Display Memory and the host is bridged through a cache inside the CL-GD5320.

Memory planes 0 and 1 share address bus AMA; planes 2 and 3 share address bus BMA. The CL-GD5320 takes up to 20-bit addresses (or external address decoding for higher address requirements) from the host, and transforms them into multiplexed addresses AMA and BMA. ACAS*, BCAS*, ARAS*, BRAS*, and WE* signals are also generated within the CL-GD5320.

Memory Refresh

A programmable number of memory refresh cycles are generated during every horizontal scan.

Screen Refresh

During this process a multiple FIFO architecture is employed to efficiently assemble alphanumeric and graphics display data. Intelligent algorithm utilizes page mode features of the two 256K x 4 DRAMs to deliver up to 32 bits of data through an 8-bit data path. Once assembled, pixel data are transferred to internal shift registers.

An internal color look up table is then utilized before the data is sent to the video output pins. The CL-GD5320 keeps track of the active and unused areas of the screen and cursor position by constantly supplying HSYNC, VSYNC and BLANK* signals.

3.3 Performance

The CL-GD5320, using an 8-bit memory bus, offers a performance level improved or equal (depending on the modes) to its predecessor, the CL-GD510A/520A, which uses a 32-bit memory bus. This is achieved by an efficient utilization of the DRAM page mode feature, by a multiple FIFO sequencer design, by host access cacheing and by the 16-bit CPU data interface. An interleave ratio of 1:2.5 or better is achieved on all standard VGA modes using 100 ns DRAMs.

3.4 Compatibility Modes

The CL-GD5320 includes all registers and data paths required for VGA/EGA, CGA, MDA, and HGC controllers. VGA enhancements to baseline EGA functionality include 320 x 200 8-bit/pixel modes and support for an external color palette, eight simultaneously loadable text fonts, Write Mode 3, and readable registers.

Extended graphics resolutions beyond the 640 x 480 IBM VGA standard are also possible using either multiple frequency monitors such as the NEC® MultiSync™ or Sony® MultiScan™ or single-frequency PS/2 monitors such as the IBM 8512. These include a 720 x 540 mode, which has a 4:3 aspect ratio (square pixels on typical monitors). This mode is supported on both PS/2 monitors as well as multifrequency displays. In addition, the CL-GD5320 supports 800 x 600 graphics and 132-column text modes, which require multifrequency display.

The CL-GD5320 supports an extended mode 13 where four pages of 64K byte blocks of memory can be switched and displayed instead of the IBM VGA single page. This allows for animation using 256 displayable colors without requiring a large amount of data to be manipulated (64K byte maximum size per image).

The extended resolution capabilities of the CL-GD5320 are listed on the next page following the listing of the standard screen formats.

3.5 Board-Level Testability *(CL-GD5325)*

The CL-GD5325 provides board-level testing functionality by allowing all the outputs and the I/O pads of the controller to be tristated, or forced into a 'walking 0' mode (all outputs and I/O pads forced to '1' except one pin, which is forced to '0'). This feature greatly enhances the board-level testability of a system based on the CL-GD5325 by allowing the designer to effectively disconnect the chip from the rest of the system (tristate outputs and I/O pads) and test for connectivity on the PCB layout ('walking 0').

3.6 Supported Screen Formats

Mode No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Video Mode	Display Mode	Dot CLK MHz†	H. Freq KHz†	V. Freq Hz†	Buffer Start
PS/2 (Single-Frequency Analog Display, IBM 85xx Series-compatible)										
0	16/256K	40 x 25	8 x 8	320 x 200	CGA	Text	25	31.5	70.1	B8000
0*	16/256K	40 x 25	8 x 14	320 x 350	EGA	Text	25	31.5	70.1	B8000
0/1+	16/256K	40 x 25	9 x 16	360 x 400	VGA	Text	28	31.5	70.1	B8000
1	16/256K	40 x 25	8 x 8	320 x 200	CGA	Text	25	31.5	70.1	B8000
1*	16/256K	40 x 25	8 x 14	320 x 350	EGA	Text	25	31.5	70.1	B8000
2	16/256K	80 x 25	8 x 8	640 x 200	CGA	Text	25	31.5	70.1	B8000
2*	16/256K	80 x 25	8 x 14	640 x 350	EGA	Text	25	31.5	70.1	B8000
2/3+	16/256K	80 x 5	9 x 16	720 x 400	VGA	Text	28	31.5	70.1	B8000
3	4/256K	80 x 25	8 x 8	640 x 200	CGA	Text	25	31.5	70.1	B8000
3*	16/256K	80 x 25	8 x 14	640 x 350	EGA	Text	25	31.5	70.1	B8000
4	4/256K	40 x 25	8 x 8	320 x 200	CGA	Graphics	25	31.5	70.1	B8000
5	4/256K	40 x 25	8 x 8	320 x 200	CGA	Graphics	25	31.5	70.1	B8000
6	2/256K	80 x 25	8 x 8	640 x 200	CGA	Graphics	25	31.5	70.1	B8000
7	4	80 x 25	9 x 14	720 x 350	HGC/MDA	Text	28	31.5	70.1	B0000
7+	4	80 x 25	9 x 16	720 x 400	VGA	Text	28	31.5	70.1	B0000
10*	16 x 256K	80 x 25	8 x 14	640 x 350	EGA	Graphics	25	31.5	70.1	A0000
11	2/256K	80 x 30	8 x 16	640 x 480	VGA	Graphics	25	31.5	59.9	A0000
12	16/256K	30 x 30	8 x 16	640 x 480	VGA	Graphics	25	31.5	59.9	A0000
13	256/256K	40 x 25	8 x 8	320 x 200	VGA	Graphics	25	31.5	70.1	A0000
40	16/256K	100 x 30	8 x 13	800 x 390	Extended	Text	32††	31.5	70.0	B8000
41	16/256K	100 x 50	8 x 8	800 x 400	Extended	Text	32††	31.5	70.0	B8000
42	16/256K	100 x 60	8 x 8	800 x 480	Extended	Text	32††	31.5	60.0	B8000
50	16/256K	132 x 30	8 x 13	1056 x 390	Extended	Text	40	31.5	70.1	B8000
51	16/256K	132 x 50	8 x 8	1056 x 400	Extended	Text	40	31.5	70.0	B8000
52	16/256K	132 x 60	8 x 8	1056 x 480	Extended	Text	40	31.5	60.0	B8000
53	16/256K	80 x 60	9 x 8	640 x 480	Extended	Text	28	31.5	60.0	B8000
61	2/256K	80 x 25	8 x 16	640 x 400	Extended	Graphics	25	31.5	70.0	A0000
62	16/256K	80 x 25	8 x 16	640 x 450	Extended	Graphics	25	31.5	60.0	A0000
63	16/256K	90 x 33	8 x 16	720 x 540	Extended	Graphics	32††	31.5	56.0	A0000
70	256/256K	45 x 30	8 x 16	360 x 480	Extended	Graphics	28	31.5	60.0	A0000
74	256/256K	40 x 30	8 x 8	320 x 240	Extended	Graphics	25	31.5	60.0	A0000
D	16/256K	40 x 25	8 x 8	320 x 200	EGA	Graphics	25	31.5	70.1	A0000
E	16/256K	80 x 25	8 x 14	640 x 200	EGA	Graphics	25	31.5	70.1	A0000
F*	4	80 x 25	8 x 14	640 x 350	EGA	Graphics	25	31.5	70.1	A0000
HGC	2			720 x 348	HGC	Graphics	32††	31.5	70.0	B8000
Multifrequency Display (NEC® Multisync™, Sony® Multiscan™, or Compatible)										
0	4/256K	40 x 25	8 x 8	320 x 200	CGA	Text	25	30.3	60.6	B8000
0*	16/256K	40 x 25	8 x 14	320 x 350	EGA	Text	25	30.3	60.6	B8000
0/1+	16/256K	4 x 25	9 x 16	360 x 400	VGA	Text	28	30.3	60.6	B8000
1	4/256K	40 x 25	8 x 8	320 x 200	CGA	Text	25	30.3	60.6	B8000
1*	16/256K	40 x 25	8 x 14	320 x 350	EGA	Text	25	30.3	60.6	B8000
2	4/256K	80 x 25	8 x 8	640 x 200	CGA	Text	25	30.0	60.1	B8000
2*	16/256K	80 x 25	8 x 14	640 x 350	EGA	Text	25	30.0	60.1	B8000
2/3+	16/256K	80 x 25	9 x 16	720 x 400	VGA	Text	28	30.0	60.1	B8000
3	4/256K	80 x 25	8 x 8	640 x 200	CGA	Text	25	30.0	60.1	B8000
3*	16/256K	80 x 25	8 x 14	640 x 350	EGA	Text	25	30.0	60.1	B8000
4	4/256K	40 x 25	8 x 8	320 x 200	CGA	Graphics	25	30.3	60.6	A0000
5	4/256K	40 x 25	8 x 8	320 x 200	CGA	Graphics	25	30.3	60.6	A0000
6	2/256K	80 x 25	8 x 8	640 x 200	CGA	Graphics	25	30.0	60.1	A0000
7	4	80 x 25	9 x 14	720 x 350	HGC/MDA	Text	28	30.0	60.1	B0000
7+	4	80 x 25	9 x 16	720 x 400	VGA	Text	28	30.0	60.1	B0000
10*	16/256K	80 x 25	8 x 14	640 x 350	EGA	Graphics	25	30.0	60.1	A0000
11	2/256K	80 x 30	8 x 16	640 x 480	VGA	Text	25	30.0	60.1	B0000
12	16/256K	80 x 30	8 x 16	640 x 480	VGA	Text	25	30.0	60.1	B0000

3.6 Supported Screen Formats *(cont.)*

Mode No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Video Mode	Display Mode	Dot CLK MHz†	H.Freq KHz†	V. Freq Hz†	Buff. Start
Multifrequency Display (NEC® Multisync™, Sony® Multiscan™, or Compatible) *(cont.)*										
13	256/256K	40 x 25	8 x 8	320 x 200	VGA	Graphics	25	30.0	60.1	A0000
40	16/256K	100 x 30	8 x 13	800 x 390	Extended	Text	32††	29.9	60.0	B8000
41	16/256K	100 x 50	8 x 8	800 x 400	Extended	Text	32††	29.9	60.0	B8000
42	16/256K	100 x 60	8 x 8	800 x 480	Extended	Text	32††	29.9	60.0	B8000
43	16/256K	100 x 75	8 x 8	800 x 600	Extended	Text	32††	33.3	54.0	B8000
50	16/256K	132 x 30	8 x 13	1056 x 390	Extended	Text	32††	25.2	60.0	B8000
51	16/256K	132 x 50	8 x 8	1056 x 400	Extended	Text	32††	25.2	60.0	B8000
52	16/256K	132 x 60	8 x 8	1056 x 480	Extended	Text	32††	26.2	53.1	B8000
53	16/256K	80 x 60	8 x 8	640 x 480	Extended	Text	25	31.9	60.0	B8000
61	16/256K	80 x 25	8 x 16	640 x 400	Extended	Graphics	25	29.9	60.0	A0000
62	16/256K	80 x 28	8 x 16	640 x 400	Extended	Graphics	25	29.9	60.0	A0000
63	16/256K	90 x 33	8 x 16	720 x 540	Extended	Graphics	32††	34.7	60.0	A0000
64	16/256K	100 x 37	8 x 16	800 x 600	Extended	Graphics	32††	33.0	53.6	A0000
6A	16/256K	100 x 37	8 x 16	800 x 600	Extended	Graphics	32††	33.0	53.6	A0000
70	256/256K	45 x 30	8 x 16	360 x 480	Extended	Graphics	28	31.6	60.0	A0000
73	256/256K	40 x 25	8 x 8	320 x 200	Extended	Graphics	14	15.7	60.0	A0000
74	256/256K	40 x 30	8 x 8	320 x 240	Extended	Graphics	14	15.7	60.0	A0000
D	16/256K	40 x 25	8 x 8	320 x 200	EGA	Graphics	25	30.3	60.6	A0000
E	16/256K	80 x 25	8 x 8	640 x 200	EGA	Graphics	25	30.1	60.1	A0000
F*	4	80 x 25	8 x 14	640 x 350	EGA	Graphics	25	30.1	60.1	A0000
HGC	2			720 x 348	HGC	Graphics	32††	33.0	60.0	A0000
IBM Enhanced Color Display (Model 5154) or Compatible										
0	4	40 x 25	8 x 8	320 x 200	CGA	Text	14.3	15.75	60.0	B8000
0*	16/64	40 x 25	8 x 14	320 x 350	EGA	Text	16.2	21.85	60.0	B8000
1	4	40 x 25	8 x 8	320 x 200	CGA	Text	14.3	15.75	60.0	B8000
1*	16/64	40 x 25	8 x 14	320 x 350	EGA	Text	16.2	21.85	60.0	B8000
2	4	80 x 25	8 x 8	640 x 200	CGA	Text	14.3	15.75	60.0	B8000
2*	16/64	80 x 25	8 x 14	640 x 350	EGA	Text	16.2	21.85	60.0	B8000
3	4	80 x 25	8 x 8	640 x 200	CGA	Text	14.3	15.75	60.0	B8000
3*	16/64	80 x 25	8 x 14	640 x 350	EGA	Text	16.2	21.85	60.0	B8000
4	4			320 x 200	CGA	Graphics	14.3	15.75	60.0	A0000
5	4			320 x 200	CGA	Graphics	14.3	15.75	60.0	A0000
6	2			640 x 200	CGA	Graphics	14.3	15.75	60.0	A0000
10*	16/64			640 x 350	EGA	Graphics	16.2	21.85	60.0	A0000
D	16/64			320 x 200	EGA	Graphics	14.3	15.75	60.0	A0000
E	16/64			640 x 200	EGA	Graphics	14.3	15.75	60.0	A0000
F*	4			640 x 350	EGA	Graphics	16.2	21.85	60.0	A0000
IBM Color Display (Model 5153) or Compatible										
0	4	40 x 25	8 x 8	320 x 200	CGA	Text	14.3	15.75	70.1	B8000
1	4	40 x 25	8 x 8	320 x 200	CGA	Text	14.3	15.75	70.1	B8000
2	4	80 x 25	8 x 8	640 x 200	CGA	Text	14.3	15.75	70.1	B8000
3	4	80 x 25	8 x 8	640 x 200	CGA	Text	14.3	15.75	70.1	B8000
4	4			320 x 200	CGA	Graphics	14.3	15.75	70.1	A0000
5	4			320 x 200	CGA	Graphics	14.3	15.75	70.1	A0000
6	2			640 x 200	CGA	Graphics	14.3	15.75	70.1	A0000
D	16/64			320 x 200	EGA	Graphics	14.3	15.75	70.1	A0000
E	16/64			640 x 200	EGA	Graphics	14.3	15.75	70.1	A0000
IBM Monochrome Display (Model 5151) or Compatible										
7	4	80 x 25	9 x 14	720 x 350	HGC/MDA	Text	16.2	18.4	50.0	B0000
F*	4			640 x 350	EGA	Graphics	16.2	18.4	50.0	A0000
HGC	2			720 x 348	HGC	Graphics	16.2	18.4	50.0	B0000

NOTES: Modes 40h–52h and 63h–64h require a 32.514 MHz dot clock and 100 ns or faster DRAM.
In monochrome modes, four colors is defined as Black, White, 'Blinking' White, and 'Intensified' White.
' * ' and '+' are part of the IBM mode names.
† These values vary depending upon the monitors and monitor parameters used in the BIOS.
†† With customized parameters, these modes can also be used with dotclocks of 36 and 40 MHz.

4. VGA, EGA, CGA, AND HGC REGISTER PORT MEMORY MAP

Address	VGA/EGA Port	CGA Port	HGC Port
3B0	CRTC Index (R/W)		6845 Index (R/W)
3B1	CRTC Data (R/W)		6845 Data (R/W)
3B2	CRTC Index (R/W)		6845 Index (R/W)
3B3	CRTC Data (R/W)		6845 Data (R/W)
3B4	CRTC Index (R/W)		6845 Index (R/W)
3B5	CRTC Data (R/W)		6845 Data (R/W)
3B6	CRTC Index (R/W)		6845 Index (R/W)
3B7	CRTC Data (R/W)		6845 Data (R/W)
3B8			Mode Control (R/W)
3B9			
3BA	Feature Control(W), Display Status(R)		Display Status (R)
3BB			
3BC			
3BD			
3BE			
3BF			Configuration (R/W)
3C0	Attribute Controller Index/Data (R/W)		
3C1	Attribute Controller Index/Data (R/W)		
3C2	Misc Output (W), Feature (R)		
3C3	Misc Output (W), Feature (R)		
3C4	Sequencer/Extensions Index (R/W)		
3C5	Sequencer/Extensions Data (R/W)		
3C6	Palette Pixel Mask (R/W)		
3C7	Palette Address Register R Mode (R/W)		
3C8	Palette Address Register W Mode (R/W)		
3C9	Palette Data (R/W)		
3CA	G. Pos. 2 (W) (EGA Only)		
3CB	(Reserved)		
3CC	G. Pos. 1 (W) (EGA Only) Misc Output (R)		
3CD	(Reserved)		
3CE	Graphics Controller Index (R/W)		
3CF	Graphics Controller Data (R/W)		
3D0	CRTC Index (R/W)	6845 Index (R/W)	
3D1	CRTC Data (R/W)	6845 Data (R/W)	
3D2	CRTC Index (R/W)	6845 Index (R/W)	
3D3	CRTC Data (R/W)	6845 Data (R/W)	
3D4	CRTC Index (R/W)	6845 Index (R/W)	
3D5	CRTC Data (R/W)	6845 Data (R/W)	

4. VGA, EGA, CGA, AND HGC REGISTER PORT MEMORY MAP *(cont.)*

Address	VGA/EGA Port	CGA Port	HGC Port
3D6	CRTC Index (R/W)	6845 Index (R/W)	
3D7	CRTC Data (R/W)	6845 Data (R/W)	
3D8		Mode Control (R/W)	
3D9		Color Select (R/W)	
3DA	Feature Control (W), Display Status (R)	Display Status (R)	
3DB			
3DC			
3DD			
3DE			
3DF			

5. CGA, MDA, AND HGC REGISTERS

5.1 Color-Graphics-Adapter (CGA)-Compatible Registers

ABBREV.	CGA REGISTER NAME	READ/ WRITE BITS	REG/ WRITE	INDEX	PORT ADDRESS
MODE	Mode Control	7	R/W	–	3D8
COLOR	Color Select	6	R/W	–	3D9
STAT	Display Status	7	R	–	3DA
CRX	6845 Index	5	R/W	–	3D4 (3D0,3D2,3D6)†
R0	Horizontal Total	8	R/W	00	3D5 (3D1,3D3,3D7)†
R1	Horizontal Displayed	8	R/W	01	3D5 (3D1,3D3,3D7)†
R2	Horizontal Sync Position	8	R/W	02	3D5 (3D1,3D3,3D7)†
R3	Sync Width	8	R/W	03	3D5 (3D1,3D3,3D7)†
R4	Vertical Total	7	R/W	04	3D5 (3D1,3D3,3D7)†
R5	Vertical Total Adjust	5	R/W	05	3D5 (3D1,3D3,3D7)†
R6	Vertical Displayed	7	R/W	06	3D5 (3D1,3D3,3D7)†
R7	Vertical Sync Position	7	R/W	07	3D5 (3D1,3D3,3D7)†
R8	Interlace Mode	2	R/W	08	3D5 (3D1,3D3,3D7)†
R9	Character Cell Height	5	R/W	09	3D5 (3D1,3D3,3D7)†
RA	Cursor Start	7	R/W	0A	3D5 (3D1,3D3,3D7)†
RB	Cursor End	5	R/W	0B	3D5 (3D1,3D3,3D7)†
CRC	Start Address High	8	R/W	0C	3D5 (3D1,3D3,3D7)†
CRD	Start Address Low	8	R/W	0D	3D5 (3D1,3D3,3D7)†
CRE	Cursor Address High	8	R/W	0E	3D5 (3D1,3D3,3D7)†
CRF	Cursor Address Low	8	R/W	0F	3D5 (3D1,3D3,3D7)†

† Valid alternate register addresses are presented in parentheses.

5.2 Monochrome-Display-Adapter (MDA)- and Hercules-Graphics-Adapter (HGC)-Compatible Registers

ABBREV.	MDA/HGC REGISTER NAME	BITS	READ/ WRITE	REG/ INDEX	PORT ADDRESS
MODE	Mode Control	7	R/W	–	3B8
STAT	Display Status	7	R	–	3BA
CONFIG	Configuration	2	R/W	–	3BF
CRX	6845 Index	5	R/W	–	3B4 (3B0,3B2,3B6)†
R0	Horizontal Total	8	R/W	00	3B5 (3B1,3B3,3B7)†
R1	Horizontal Displayed	8	R/W	01	3B5 (3B1,3B3,3B7)†
R2	Horizontal Sync Position	8	R/W	02	3B5 (3B1,3B3,3B7)†
R3	Sync Width	8	R/W	03	3B5 (3B1,3B3,3B7)†
R4	Vertical Total	7	R/W	04	3B5 (3B1,3B3,3B7)†
R5	Vertical Total Adjust	5	R/W	05	3B5 (3B1,3B3,3B7)†
R6	Vertical Displayed	7	R/W	06	3B5 (3B1,3B3,3B7)†
R7	Vertical Sync Position	7	R/W	07	3B5 (3B1,3B3,3B7)†
R8	Interlace Mode	2	R/W	08	3B5 (3B1,3B3,3B7)†
R9	Character Cell Height	5	R/W	09	3B5 (3B1,3B3,3B7)†
RA	Cursor Start	7	R/W	0A	3B5 (3B1,3B3,3B7)†
RB	Cursor End	5	R/W	0B	3B5 (3B1,3B3,3B7)†
CRC	Start Address High	8	R/W	0C	3B5 (3B1,3B3,3B7)†
CRD	Start Address Low	8	R/W	0D	3B5 (3B1,3B3,3B7)†
CRE	Cursor Address High	8	R/W	0E	3B5 (3B1,3B3,3B7)†
CRF	Cursor Address Low	8	R/W	0F	3B5 (3B1,3B3,3B7)†

† Valid alternate register addresses are presented in parentheses.

6. VGA/EGA REGISTERS

6.1 VGA/EGA-Compatible Register Table

ABBREV.	EGA REGISTER NAME	BITS	R/W	REG/ INDEX	MONO. PORT	COLOR PORT
VSSM	Video System Sleep Mechanism	1	R/W	–	102	102
VSE	Video System Enable	2	R/W	–	46E8/3C3	46E8/3C3
MISC	Miscellaneous Output	8	W	–	3C2	3C2
FEAT	Input Status 0 (Feature Read)	4	R	–	3C2	3C2
STAT	Input Status 1 (Display Status)	7	R	–	3BA	3DA
FC	Feature Control	3	W	–	3BA	3DA
GPOS1/MISC	Graphics 1 Pos (W), Misc (R)	2,8	R/W	–	3CC	3CC
GPOS2/FC	Graphics 2 Pos (W), FeatCtrl (R)	2,3	R/W	–	3CA	3CA
GRX	Graphics Controller Index	4	R/W	–	3CE	3CE
GR0	Set/Reset	4	R/W	00	3CF	3CF
GR1	Enable Set/Reset	4	R/W	01	3CF	3CF
GR2	Color Compare	4	R/W	02	3CF	3CF
GR3	Data Rotate	5	R/W	03	3CF	3CF
GR4	Read Map Select	3	R/W	04	3CF	3CF
GR5	Mode	7	R/W	05	3CF	3CF

6.1 VGA/EGA-Compatible Register Table *(cont.)*

ABBREV.	EGA REGISTER NAME	BITS	R/W	REG/ INDEX	MONO. PORT	COLOR PORT
GR6	Miscellaneous	4	R/W	06	3CF	3CF
GR7	Color Don't Care	4	R/W	07	3CF	3CF
GR8	Bit Mask	8	R/W	08	3CF	3CF
ARX	Attribute Controller Index	6	R/W	–	3C0	3C0
AR0-F	Color Palette Regs 0-15	8	R/W	00-0F	3C0	3C0
AR10	Mode Control	7	R/W	10	3C0	3C0
AR11	Overscan Color	8	R/W	11	3C0	3C0
AR12	Color Plane Enable	6	R/W	12	3C0	3C0
AR13	Horizontal Pixel Panning	4	R/W	13	3C0	3C0
AR14	Color Select	4	R/W	14	3C0	3C0
SERX	Sequencer/Extension Reg. Index	7	R/W	–	3C4	3C4
SR0	Reset	2	R/W	00	3C5	3C5
SR1	Clocking Mode	6	R/W	01	3C5	3C5
SR2	Plane Mask	4	R/W	02	3C5	3C5
SR3	Character Map Select	6	R/W	03	3C5	3C5
SR4	Memory Mode	3	R/W	04	3C5	3C5
SR6	Extensions Control (see Ext. Table)	1	R/W	06	3C5	3C5
SR7	Reset H. Character Counter	1	W	07	3C5	3C5
CRX	CRTC Index	6/5	R/W	–	3B4	3D4
CR0	Horizontal Total	8	R/W	00	3B5	3D5
CR1	Horizontal Display End	8	R/W	01	3B5	3D5
CR2	Horizontal Blanking Start	8	R/W	02	3B5	3D5
CR3	Horizontal Blanking End	8	R/W	03	3B5	3D5
CR4	Horizontal Retrace Start	8	R/W	04	3B5	3D5
CR5	Horizontal Retrace End	8	R/W	05	3B5	3D5
CR6	Vertical Total	8	R/W	06	3B5	3D5
CR7	Overflow	8	R/W	07	3B5	3D5
CR8	Screen A Preset Row Scan	7	R/W	08	3B5	3D5
CR9	Character Cell Height	8	R/W	09	3B5	3D5
CRA	Cursor Start	6	R/W	0A	3B5	3D5
CRB	Cursor End	7	R/W	0B	3B5	3D5
CRC	Screen A Start Address High	8	R/W	0C	3B5	3D5
CRD	Screen A Start Address Low	8	R/W	0D	3B5	3D5
CRE	Cursor Location High	8	R/W	0E	3B5	3D5
CRF	Cursor Location Low	8	R/W	0F	3B5	3D5
CR10	Vertical Retrace Start	8	W	10	3B5	3D5
CR11	Vertical Retrace End	8	W	11	3B5	3D5
CR12	Vertical Display End	8	R/W	12	3B5	3D5
CR13	Offset	8	R/W	13	3B5	3D5
CR14	Underline Location	7	R/W	14	3B5	3D5
CR15	Vertical Blanking Start	8	R/W	15	3B5	3D5
CR16	Vertical Blanking End	8	R/W	16	3B5	3D5
CR17	CRT Mode Control	7	R/W	17	3B5	3D5
CR18	Line Compare	8	R/W	18	3B5	3D5
CR22	Readback CRT Latches	8	R	22	3B5	3D5
CR24	Attribute Index Toggle	7	R	24	3B5	3D5
CR30-CR3F	Frame Blank	1	W	3X	3B5	3D5

NOTE: Unlike VGA, EGA supports sparse decoding.

6.2 Extension Register Table

ABBREV.	EXTENSION REGISTER	BITS	READ/WRITE	REG/INDEX	PORT ADDR.
SERX	Sequencer Extensions Register Index	7	R/W	–	3C4
SR6	Extension Control	1	R/W	06	3C5
CR7F	Identification	8	R	7F	3B5/3D5
MC1	Misc. Control 1	8	R/W	80	3C5
GPOS1	Graphics 1 Position	2	R/W	81	3C5
GPOS2	Graphics 2 Position	2	R/W	82	3C5
ARX	Attribute Controller Index	7	R/W	83	3C5
WRC	Write Control	8	R/W	84	3C5
TC	Timing Control	7	R/W	85	3C5
	-reserved-	–	–	86	3C5
MC2	Misc. Control 2	8	R/W	87	3C5
	-reserved-	–	–	88	3C5
FONTC	CGA, HGC Font Control	4	R/W	89	3C5
	-reserved-	0	–	8A	3C5
SBPR	Screen B Preset Row Scan	5	R/W	8B	3C5
SBSH	Screen B Start Address High	8	R/W	8C	3C5
SBSL	Screen B Start Address Low	8	R/W	8D	3C5
REV	Revision Code	8	R	8E	3C5
CR10	Vertical Retrace Start	8	R/W	90	3C5
CR11	Vertical Retrace End	8	R/W	91	3C5
PPAH	Pointer Pattern Address High	8	R/W	94	3C5
CADJ	Cursor Height Adjust	8	R/W	95	3C5
	-reserved-	–	–	96	3C5
	-reserved-	–	–	97	3C5
	-reserved-	–	–	98	3C5
	-reserved-	–	–	99	3C5
	-reserved-	–	–	9A	3C5
	-reserved-	–	–	9B	3C5
PXH	Pointer Horizontal Position High	3	R/W	9C	3C5
PXL	Pointer Horizontal Position Low	8	R/W	9D	3C5
PYH	Pointer Vertical Position High	2	R/W	9E	3C5
PYL	Pointer Vertical Position Low	8	R/W	9F	3C5
GRL0	Graphics Controller Memory Latch 0	8	R/W	A0	3C5
GRL1	Graphics Controller Memory Latch 1	8	R/W	A1	3C5
GRL2	Graphics Controller Memory Latch 2	8	R/W	A2	3C5
GRL3	Graphics Controller Memory Latch 3	8	R/W	A3	3C5
CLK	Clock Select	6,1	R/W	A4,A7	3C5
CURS	Cursor Attributes	8	R/W	A5	3C5
ISS	Internal Switch Source	8	R/W	A6	3C5
256 CPC	256 Color Page Control	4	R/W	AD	3C5
STATE	Active Adapter State	7	R/W	AF	3C5
	-reserved-	–	–	B0-BA	3C5
SCRBB-BF	Scratch register BB-BF	8	R/W	BB-BF	3C5
	-reserved-	–	–	C0-C3	3C5
SWRH	Switch Register High	8	R	C4	3C5
SWRL	Switch Register Low	8	R	C5	3C5
	-reserved-	–	–	C6	3C5
BUSW	Bus Width Enable 16-Bit Bus	1	R/W	C7	3C5
FIFOC	FIFO Threshold Control	8	R/W	C8	3C5
TREG	Test REG	2	R/W	C9	3C5
ROMPC	BIOS ROM Paging Control	8	R/W	CA	3C5
ROMPD	BIOS ROM Page Data	2	R/W	CB	3C5
	-reserved-	–	–	CC-CF	3C5

6.3 Extension Switch Settings

The external hardware configurations are sensed through the extension switch setting registers SWRH and SWRL at I/O Port Address 3C5H with index C4H and C5H consecutively. These registers are initialized at power-up to store switch settings. The setting of these switches is incorporated by the BIOS. These switches can be omitted for motherboard applications.

6.3.1 SWRH Switch Setting Register High

The SWRH register can be accessed at extension register C4H. Every bit in this register is readable by the BIOS.

The following hardware configurations are expected:

Bit #	Description	Access	Reset State
7 (MSB)	BIOS Location 0: BIOS at C000 (respond to 46E8 sleep mechanism) 1: BIOS at E000 (respond to 3C3 sleep mechanism)	R	CPUAD15
6	External Multifrequency Oscillator Select: 0: pins 3, 4, 5 and 2 are inputs from individual oscillators 1: pins 3, 4, 5 and 2 are Frequency Select outputs	R	CPUAD14
5	BIOS Width. '0' = 8 bit / '1' = 16 bit	R	CPUAD13
4	'0' = VGA is Primary '1' = VGA is Secondary Adapter	R	CPUAD12
3	reserved	–	CPUAD11
2..0	State Control 001: CGA Locked State 010: MGA Locked State 011: EGA Locked State 100: VGA Locked State	R	CPUAD10..CPUAD8

6.3.2 SWRL Switch Setting Register Low

The SWRL can be accessed at extension register C5H. The following hardware configurations are expected:

Bit #	Description	Access	Reset Status
7..5	Reserved	–	CPUAD7..CPUAD5
4..3	Monitor type 00: MD 18.432 kHz 01: Color 15.75 kHz 10: Enhanced Color Display 11: Digital Multifrequency Display	R	CPUAD4..CPUAD3
2..0	PS/2 Monitor ID Bits 010: 8514 Monitor 101: 8503 Monitor 110: 8512/8513 Monitor 111: No Monitor Connected		CPUAD2..CPUAD0

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Stresses above those listed here may cause permanent damage to system components. Note that these are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Ambient Temperature Under Bias ..... 0° C to 70° C
Storage Temperature ..... -65° C to 150° C
Voltage On Any Pin With Respect To Ground ..... GND -0.5 to VCC +0.5 Volts
Operating Power Dissipation ..... 0.375 Watt
Standby Power Dissipation ..... 0.055 Watt
Power Supply Voltage ..... 7 Volts
Injection Current (Latch-up) ..... 25 mA

7.2 CL–GD5320 DC Characteristics

(V_{CC} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{CC}	Power Supply Voltage	4.75	5.25	V	Normal Operations
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = -2 mA†*
					I_{OL} = 8 mA for CPUAD[15:0]
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 400 µA
					I_{OH} = .8 mA for VSYNC, HSYNC
I_{CC}	Operating Supply Current		55	mA	@ 33 MHz, 5V nominal
I_{CCpd}	Power-Down Mode Current		1.5	mA	@ 33 MHz, 5V nominal
I_L	Input Leakage	-10	10	µA	$0 < V_{IN} < V_{CC}$
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

† I_{OL} maximum for CL-GD5320 = 12 mA CPURDY, CRTINT @ .4 V_{OL}
= 24 mA MCS16* @ .4 V_{OL}

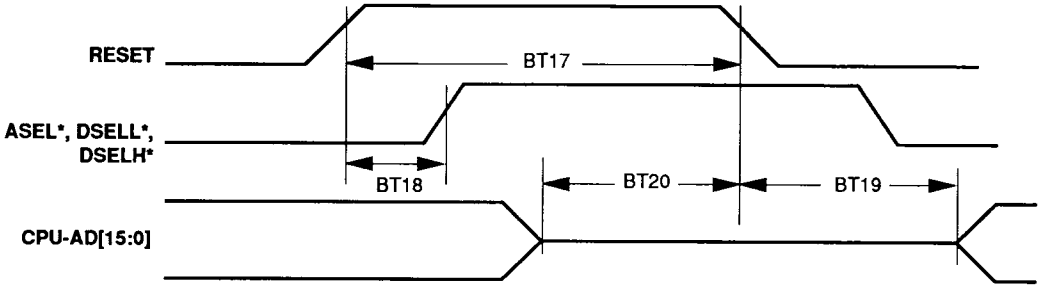
* -4 mA for Revision C silicon

7.3 AC Characteristics/Timing Information

The following timing information assumes that all outputs will drive one Schottky TTL load in parallel with 50 pF and all inputs are at TTL level. The MIN and MAX timings are those conforming to the operating ranges of a power supply voltage of 5V ± 5% and an ambient temperature of 0° C to 70° C.

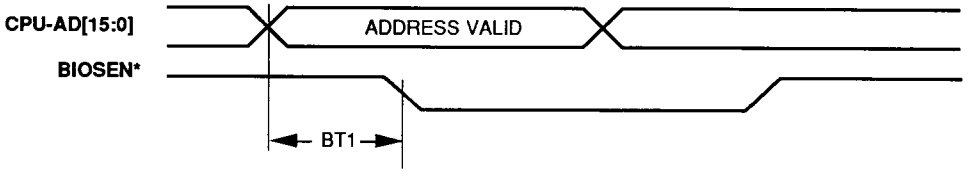
Index of Timing Information

I/O Bus Timing at RESET

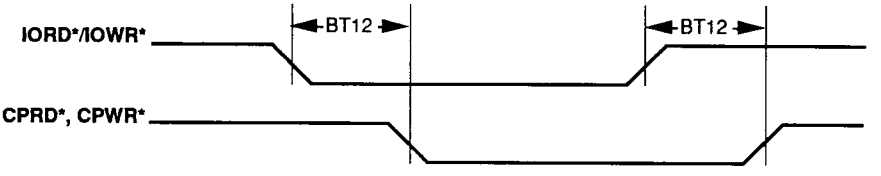


NOTE: High-Z state unless controlled by switch pullups/downs.

BIOS Addressing Timing



RAMDAC Interface Timing

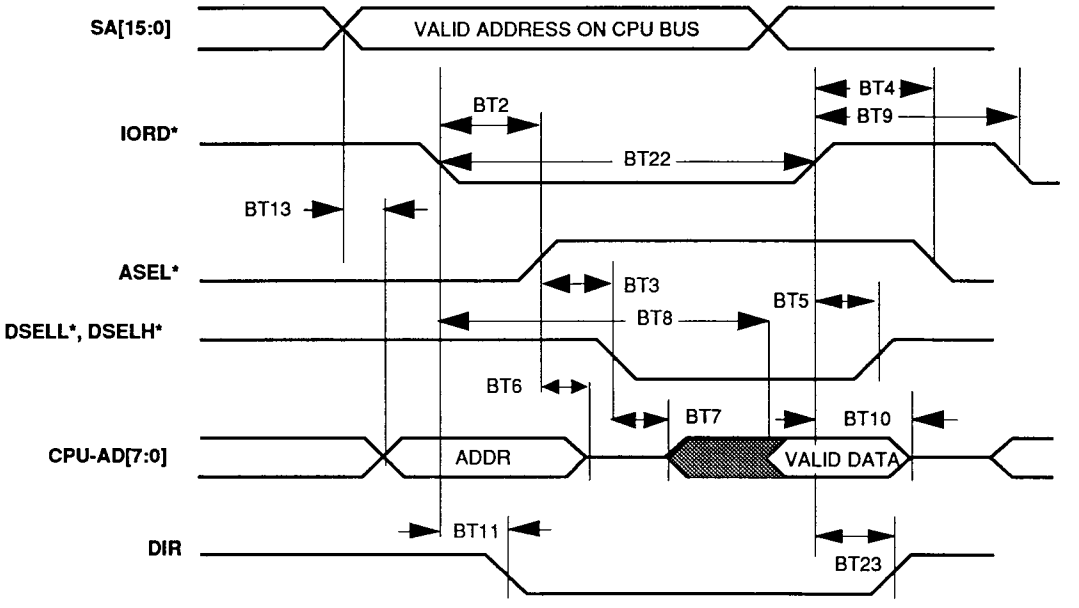


BIOS Interface, I/O Port, and RAMDAC Timing Table

SYMBOL	PARAMETER	5320/5325 MIN	5320/5325 MAX	UNITS
BT1	Address to BIOSEN* Delay		40	ns
BT2	ASEL* delay after command active delay	25	40/48	ns
BT3	DSELL/H* low from ASEL* high delay	4	15/18	ns
BT4	ASEL* delay after command inactive delay	25	40	ns
BT5	DSEL* high after command inactive delay	20	40	ns
BT6	Allowable Address hold time after ASEL* inactive	4	20	ns
BT7	Allowable Data drive delay from DSELL/H* active		20	ns
BT8	IORD* access time	80	150	ns
BT9	Inter-command delay for IORD*	80		ns
BT10	Data tri-state after IORD*inactive	16	32	ns
BT11	DIR low active from IORD* command	30	50	ns
BT12	CPRD*/CPWR* delay from command		30	ns
BT13	Bus Address to CPU-AD[7:0] delay	20	50	ns
BT14	Inter-command delay for IOWR*	80		ns
BT15	Data setup time to IOWR* trailing edge	60	120	ns
BT16	IOWR* to I/O Port output delay (FC[0,1], CLKxx)		80	ns
BT17	RESET pulse width	500		ns
BT18	Select lines inactive after RESET active		100	ns
BT19	Select lines inactive hold time after RESET low	30	100	ns
BT20	CPU-AD bus High-Z setup time to RESET low	400		ns
BT21	Address hold time from IOWR* inactive	0	50	ns
BT22	IORD*, IOWR* Pulse Width	150		ns
BT23	IORD* Inactive to DIR Inactive	30	50	ns

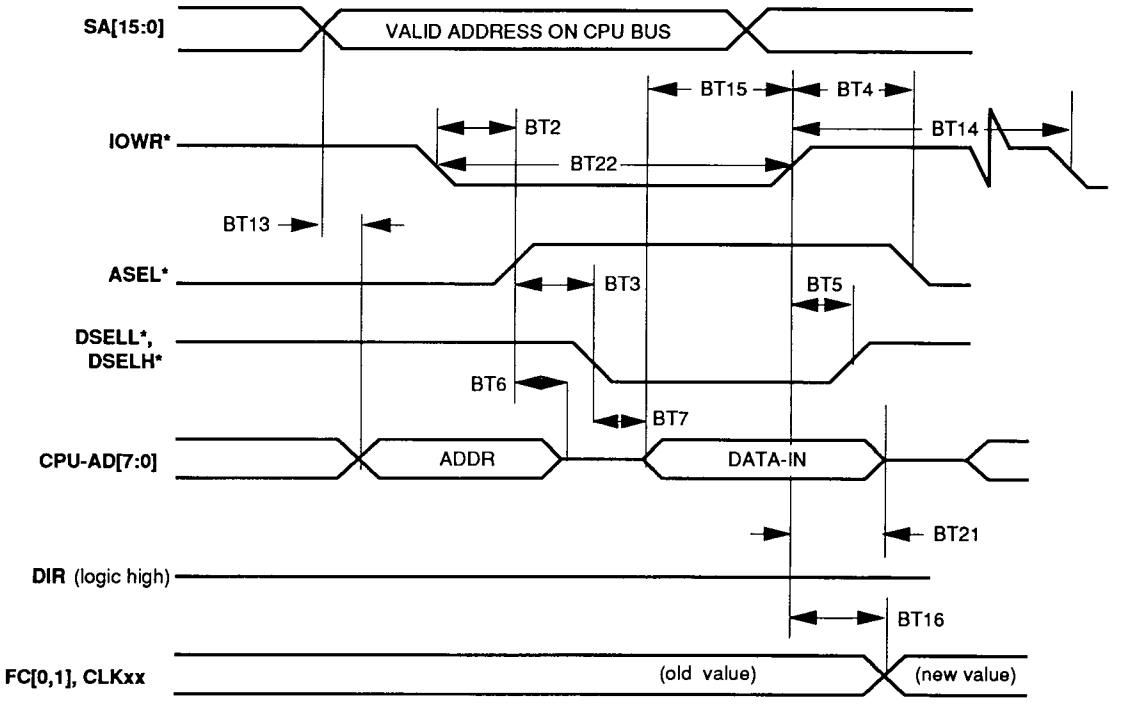
NOTES: BT2 depends on ROM access time from enable and bidirectional buffer propagation delay time.
BT4, BT7, BT8, BT9 depend on external components selected. Maximum delays shown here for reference only.
'Command' implies IOWR*/IORD* or MEMR*/MEMW*; I/O command means IOWR*/IORD*.

IORD* Cycle Timing



NOTES: The delay of CPU-AD[AD7:0] from ASEL*, DSELL*, and DSELH* is dependent on the speed of the external components selected. Maximum allowable delays are shown here for reference only.

IOWR* Cycle Timing



NOTES: The delay of CPU-AD[AD7:0] from ASEL*, DSELL*, and DSELH* is dependent on the speed of the external components selected. Maximum allowable delays are shown here for reference only.

CPU Memory Read Cycle Timing

SYMBOL	PARAMETER	8 Dots	9 Dots	ns
MT1	CPURDY* Low from MEMR*	15	15	TYP
MT2	MEMR* Inactive to CPURDY* Tristate	25	25	MAX
MT3	CPU Read Cycle End to CPURDY* Inactive	50	50	TYP
MT4	CS Valid to MCS16* Active	24	24	TYP
MT5	MEMR* Active to ASEL* Inactive	40/25	40/25	MAX/MIN
MT6	CS Hold Time After Command	45	45	MIN
MT7	ASEL* Inactive to DSEL* Active Delay	4/18	4/18	MIN/MAX
MT8	Tristate after Data MEMR* Inactive	32/16	32/16	MAX/TYP
MT16	MEMR* Inactive to ASEL Active	40/25	40/25	MAX/MIN
MT17	MEMR* Inactive to DIR Inactive	25	25	MAX
MT19	MEMR* Pulse Width	150	150	MIN
MT21	MEMR* Active to DIR Active	50	50	MAX

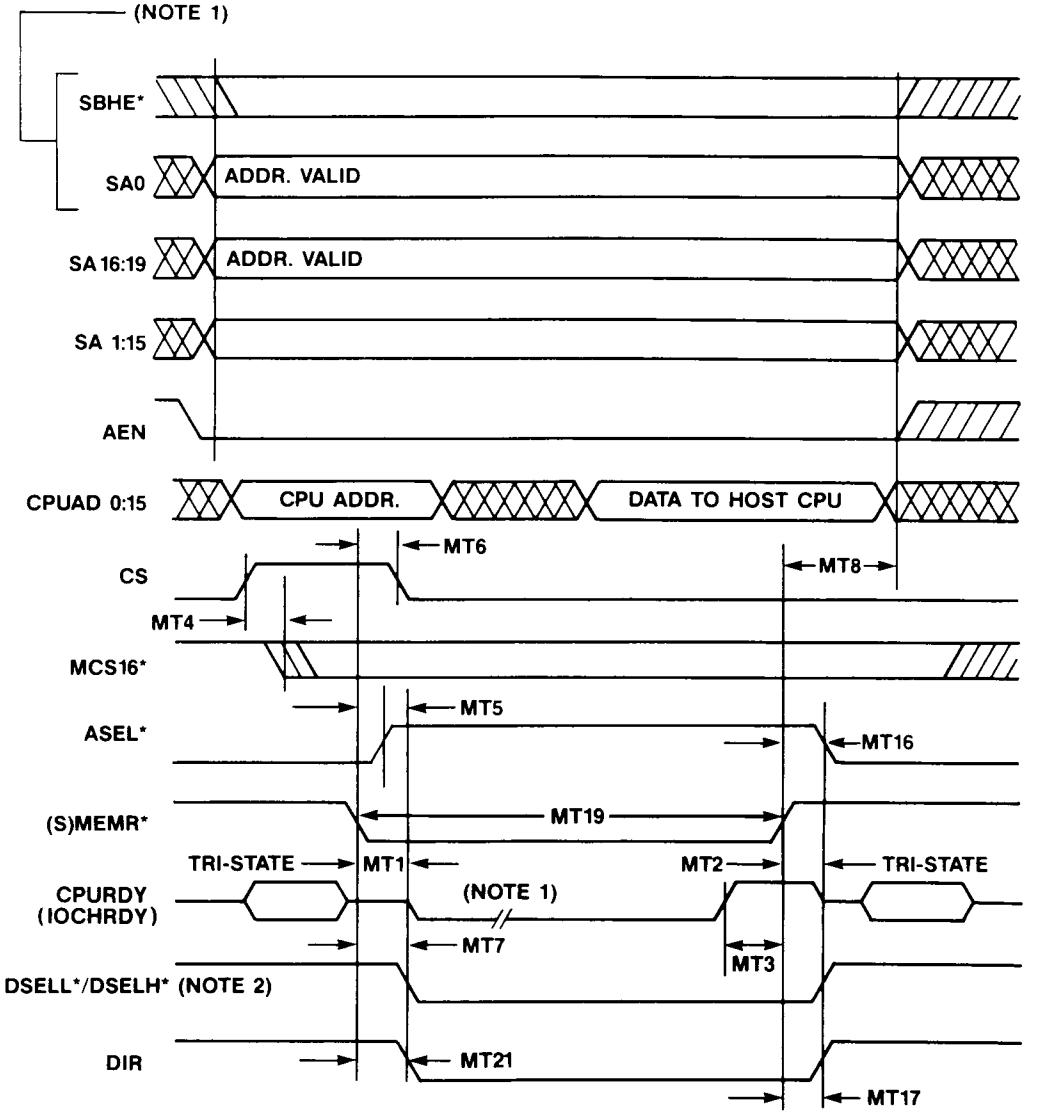
NOTE: All times are in nanoseconds (ns) unless otherwise noted; 50 pF load capacitance is assumed. Command implies IORD*/IOWR* or MEMR*/MEMWR*; I/O command implies IORD* or IOWR*.

CPU Memory Write Cycle Timing

SYMBOL	PARAMETER	8 Dots	9 Dots	ns
MT9	CPURDY* Low from MEMW*	15	15	TYP
MT10	MEMW* Inactive to CPURDY* Tristate	25	25	MAX
MT11	CS Active to MCS16* Active Delay	20	20	TYP
MT12	CS Hold Time After Command	45	45	TYP
MT13	MEMW* Active to ASEL* Inactive	40/25	40/25	MAX/TYP
MT14	ASEL* Inactive to MEMW* Active to DSELL*, DSELH* Active	4/18	4/18	MIN/MAX
MT15	MEMW* to CPU Write Data Hold Time	32/16	32/16	MAX/TYP
MT18	MEMW* Inactive to ASEL Active	50	50	MAX
MT19	MEMR* Pulse Width	150	150	MIN

NOTE: All times are in nanoseconds (ns) unless otherwise noted; use parameter MT14 with I/O port parameters BT5, BT6.

CPU Memory Read Cycle Timing

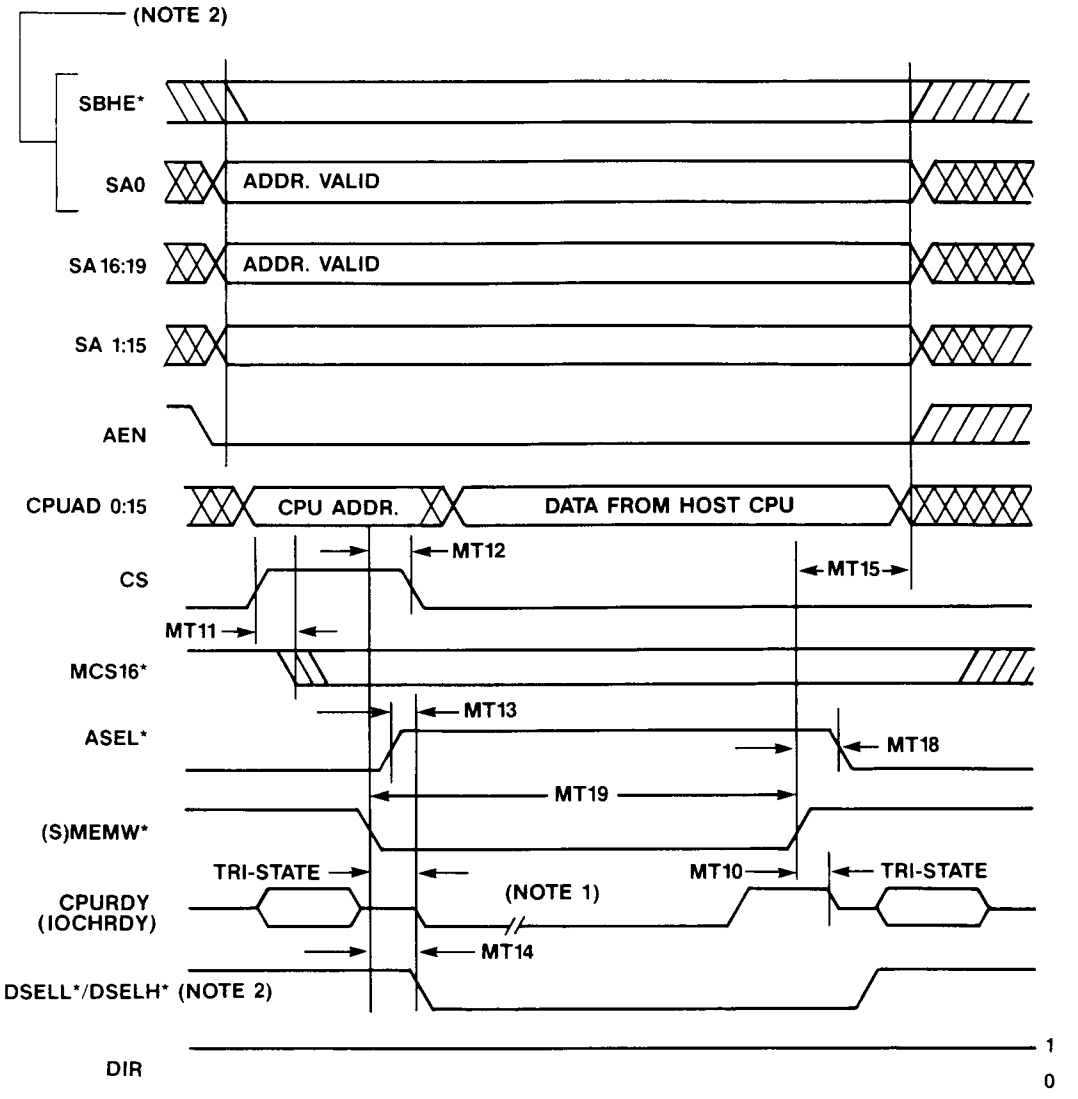


NOTE 1: 8/16-Bit Bus Cycle Control

SBHE*	A0	DSELL*	DSELH*	Operation
0	0	0	0	16-Bit WRD
0	1	1	0	Odd Byte
1	0	0	1	Even Byte
1	1	X	X	Reserved

NOTE 2: A CPU read cycle will go in a wait state if a CRT cycle is in progress. The interleave will determine the wait length.

CPU Memory Write Cycle Timing



NOTE 1: 8/16-Bit Bus Cycle Control

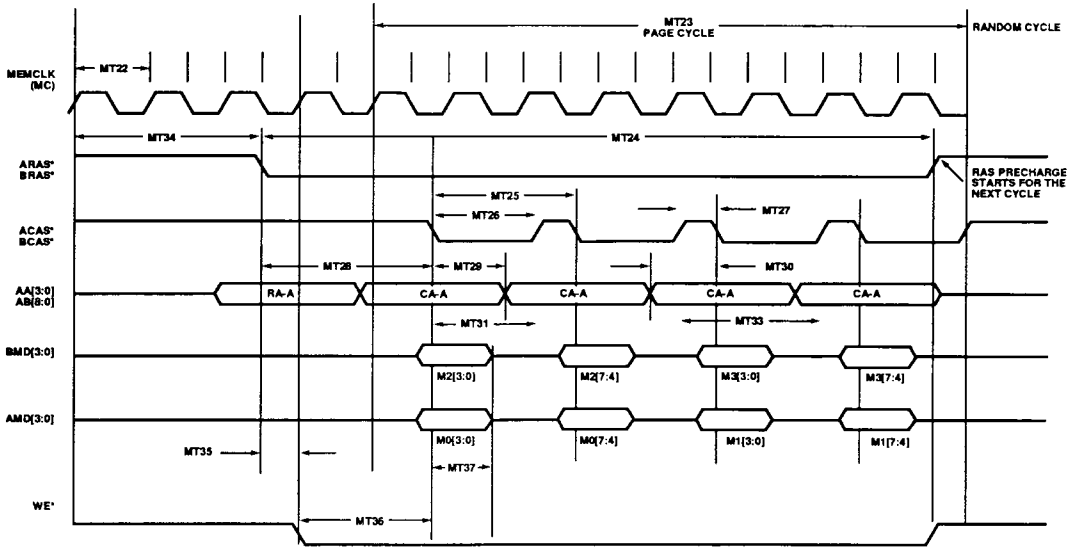
SBHE*	A0	DSELL*	DSELH*	Operation
0	0	0	0	16-Bit WRD
0	1	1	0	Odd Byte
1	0	0	1	Even Byte
1	1	X	X	Reserved

NOTE 2: A CPU write cycle will go in a wait state if a CRT cycle is in progress. The interleave will determine the wait length.

Display Memory Write Cycle Table

SYMBOL	PARAMETER	DRAMs 120	DRAMs 100	DRAMs 80	Units ns (MIN)
MT22	Memory Clock Cycle Time	32	27.5	22.5	ns
MT23	Page Mode Cycle	270	220	180	ns
MT24	Random Access Planes 0, 1, 2 & 3 R/W	390	330	270	ns
MT25	Fast Page Cycle Time	70	60	50	ns
MT26	CAS* Pulse Width	50	40	30	ns
MT27	CAS* Precharge	15	15	10	ns
MT28	RAS-to-CAS Delay	70	60	50	ns
MT29	Column Address Hold Time	30	25	20	ns
MT30	Column Address Setup Time	15	15	10	ns
MT31	Access Time from CAS* Falling Edge	30	25	20	ns
MT33	Access Time from CAS* Precharge Rising Edge	65	55	45	ns
MT34	RAS* Precharge	90	80	70	ns
MT35	RAS* to Command Delay	42	37	33	ns
MT36	Command to CAS* Delay	24	22	20	ns
MT37	Data Hold Time from CAS* Falling Edge	39	34	30	ns

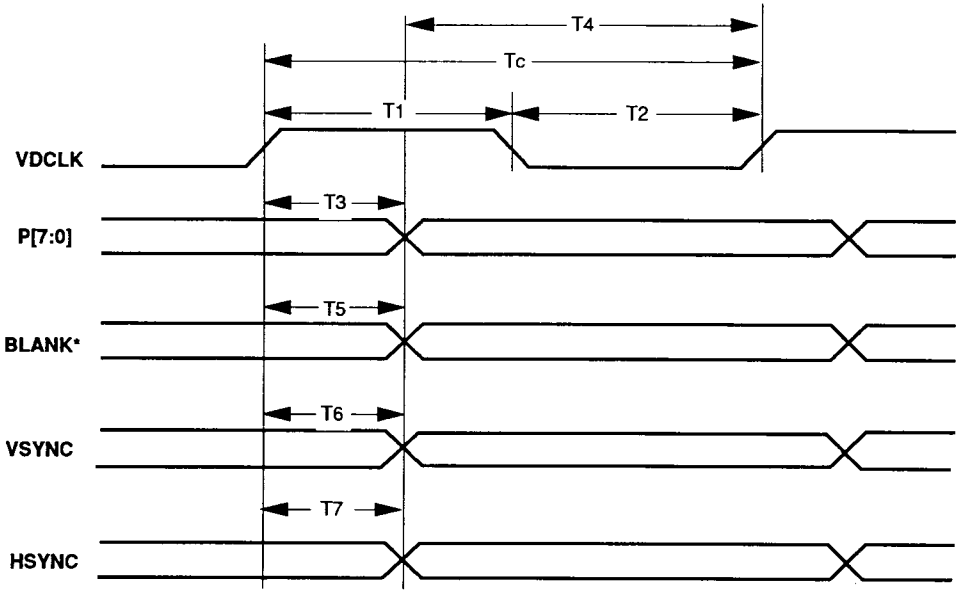
Display Memory Write Cycle



Video Timing Table

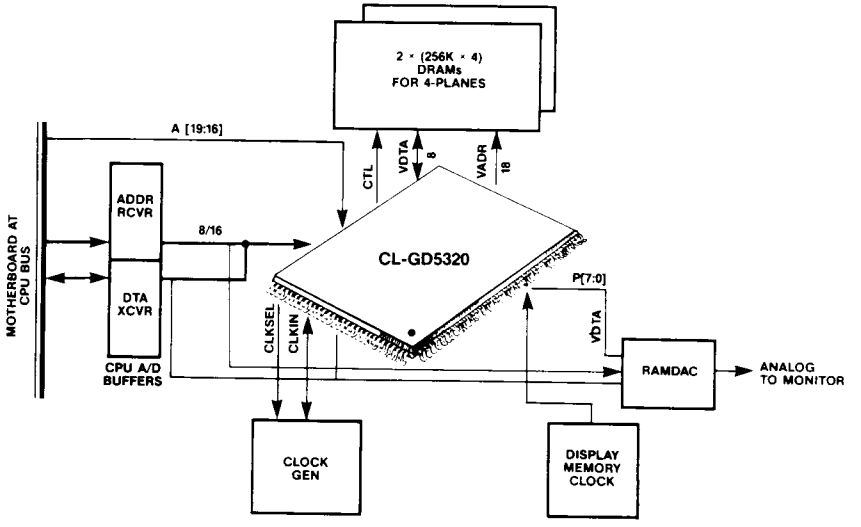
SYMBOL	PARAMETER	MIN	MAX	UNITS
Tc	VDCLK Cycle (36 MHz MAX)	27.5		ns
	VDCLK Cycle (40 MHz MAX)	25		ns
T1	VDCLK High (measured @ 2.0V; 40 MHz MAX)	[Tc/2] - 5%		
T2	VDCLK Low (measured @ 0.4V)	[Tc/2] - 5%		
T3	P[7:0] Delay (hold time)	4	20	ns
T4	P[7:0] Setup Time (Tc - T3) (36 MHz MAX)	7.5		ns
	P[7:0] Setup Time (Tc - T3) (40 MHz MAX)	5		ns
T5	BLANK* Delay	10	30	ns
T6	VSYNC Delay	10	60	ns
T7	HSYNC Delay	10	40	ns

Video Timing



8. TYPICAL APPLICATION

8.1 Motherboard Block Diagram (Minimal 8/16-bit Configuration) — BIOS at Segment E000

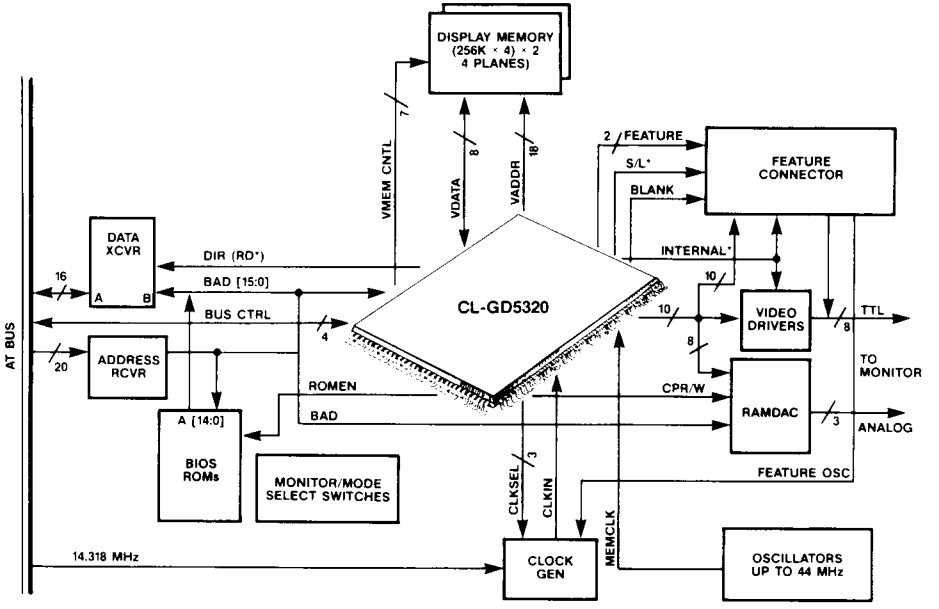


Parts List for Motherboard Implementation

ICs:	8 Bits	16 Bits
• CL-GD5320	1	1
• PC AT Address Bus Receivers	2	2
• PC AT Data Transceivers	1	2
• Two 256K x 4 DRAMs	2	2
• RAMDAC	1	1
• 74F260	—	1
Total ICs	7	9
Clocks:		
• Clock Generator	1	1
• Display Memory Clock	1	1
Total Components	9	11

8. TYPICAL APPLICATION *(cont.)*

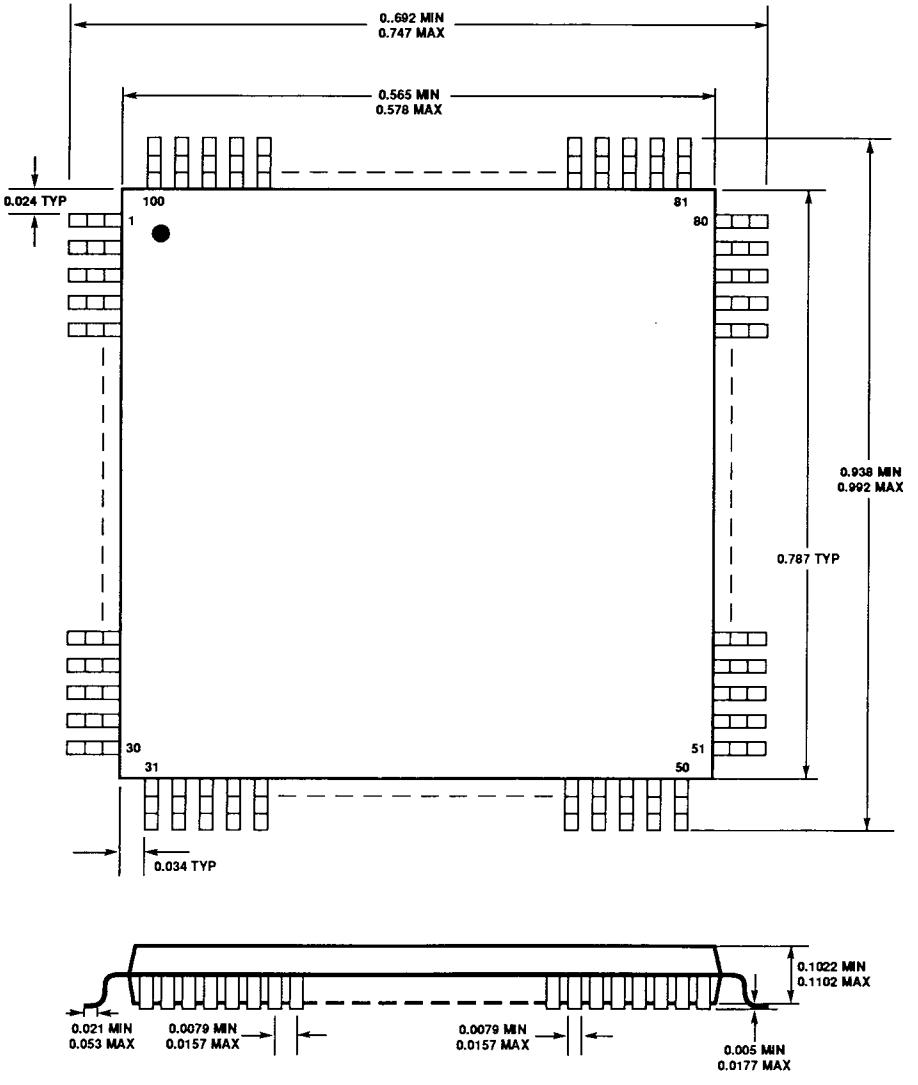
8.2 Add-in Card Block Diagram (Full 8/16-bit Configuration)



ICs:	8 Bits	16 Bits
• CL-GD5320	1	1
• PC Bus Address Receiver	2	2
• PC Bus Data Transceiver	1	2
• Two 256K x 4 DRAMs	2	2
• RAMDAC (for VGA only)	1	1
• Video Transceivers	2	2
• 74F260	—	1
• BIOS EPROM(s)	1	2
Total ICs:	10	13
Clocks:		
• Clock Generator	1	1
• Display Memory Clock	1	1
Total Components:	12	15

9. PACKAGE INFORMATION

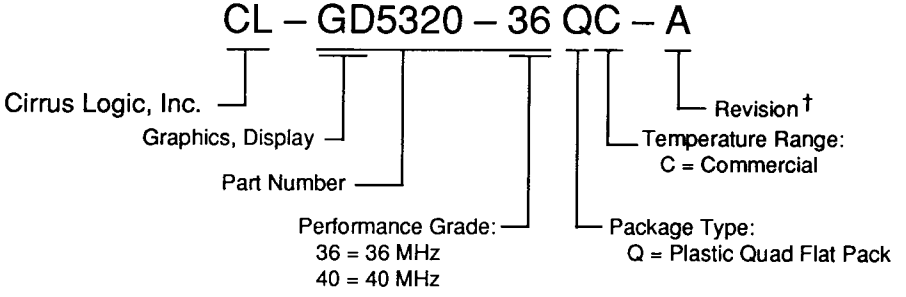
9.2 100-Pin QFP (Quad Flat Pack)



NOTE: All dimensions are in inches and are nominal unless otherwise stated.

10. ORDERING INFORMATION

10.1 Package Numbering Guide



† Contact Cirrus Logic, Inc. for up-to-date information on revisions.

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† U.S. Patent No. 4,293,783

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