



# Intel<sup>®</sup> G31/P31 Express Chipset

## Datasheet

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— *For the Intel<sup>®</sup> 82G31 Graphics and Memory Controller Hub (GMCH) and the Intel<sup>®</sup> 82P31 Memory Controller Hub (MCH)*

*July 2007*



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# Contents

|       |   |    |
|-------|---|----|
| 1     | Introduction .....  | 15 |
| 1.1   | Terminology .....   | 18 |
| 1.2   | Reference Documents .....                                       | 20 |
| 1.3   | (G)MCH Overview .....   | 21 |
| 1.3.1 | Host Interface .....  | 21 |
| 1.3.2 | System Memory Interface .....                                   | 22 |
| 1.3.3 | Direct Media Interface (DMI) .....                              | 23 |
| 1.3.4 | PCI Express* Interface .....                                    | 23 |
| 1.3.5 | Graphics Features (Intel® 82G31 GMCH Only) .....                | 24 |
| 1.3.6 | SDVO and Analog Display Features (Intel® 82G31 GMCH Only) ..... | 24 |
| 1.3.7 | (G)MCH Clocking .....   | 25 |
| 1.3.8 | Power Management .....  | 26 |
| 1.3.9 | Thermal Sensor .....  | 26 |
| 2     | Signal Description .....  | 27 |
| 2.1   | Host Interface Signals .....                                    | 28 |
| 2.2   | System Memory (DDR2) Interface Signals .....                    | 31 |
| 2.2.1 | System Memory Channel A Interface Signals .....                 | 31 |
| 2.2.2 | System Memory Channel B Interface Signals .....                 | 32 |
| 2.2.3 | DDR2 DRAM Reference and Compensation Signals .....              | 33 |
| 2.3   | PCI Express* Interface Signals .....                            | 33 |
| 2.4   | Analog Display Signals (Intel® 82G31 GMCH Only) .....           | 34 |
| 2.5   | Clocks, Reset, and Miscellaneous .....                          | 35 |
| 2.6   | Direct Media Interface .....                                    | 36 |
| 2.7   | Serial DVO Interface (Intel® 82G31 GMCH Only) .....             | 36 |
| 2.7.1 | SDVO/PCI Express* Signal Mapping .....                          | 38 |
| 2.8   | Power and Ground .....  | 39 |
| 3     | System Address Map .....  | 41 |
| 3.1   | Legacy Address Range .....                                      | 44 |
| 3.1.1 | DOS Range (0h – 9_FFFFh) .....                                  | 45 |
| 3.1.2 | Legacy Video Area (A_0000h-B_FFFFh) .....                       | 45 |
| 3.1.3 | Expansion Area (C_0000h-D_FFFFh) .....                          | 46 |
| 3.1.4 | Extended System BIOS Area (E_0000h-E_FFFFh) .....               | 47 |
| 3.1.5 | System BIOS Area (F_0000h-F_FFFFh) .....                        | 47 |
| 3.1.6 | PAM Memory Area Details .....                                   | 47 |
| 3.2   | Main Memory Address Range (1MB – TOLUD) .....                   | 48 |
| 3.2.1 | ISA Hole (15 MB-16 MB) .....                                    | 49 |
| 3.2.2 | TSEG .....  | 49 |
| 3.2.3 | Pre-allocated Memory .....                                      | 49 |
| 3.3   | PCI Memory Address Range (TOLUD – 4 GB) .....                   | 50 |
| 3.3.1 | APIC Configuration Space (FEC0_0000h–FECF_FFFFh) .....          | 51 |
| 3.3.2 | HSEG (FEDA_0000h–FEDB_FFFFh) .....                              | 52 |
| 3.3.3 | FSB Interrupt Memory Space (FEE0_0000–FEEF_FFFF) .....          | 52 |
| 3.3.4 | High BIOS Area .....  | 52 |



|        |   |    |
|--------|---|----|
| 3.4    | Main Memory Address Space (4 GB to TOUUD) .....                   | 52 |
| 3.4.1  | Memory Re-claim Background .....                                  | 53 |
| 3.4.2  | Memory Reclaiming .....   | 53 |
| 3.5    | PCI Express* Configuration Address Space.....                     | 53 |
| 3.6    | PCI Express* Graphics Attach (PEG).....                           | 54 |
| 3.7    | Graphics Memory Address Ranges (Intel® 82G31 GMCH Only) .....     | 55 |
| 3.8    | System Management Mode (SMM) .....                                | 55 |
| 3.8.1  | SMM Space Definition .....  | 56 |
| 3.8.2  | SMM Space Restrictions.....                                       | 56 |
| 3.8.3  | SMM Space Combinations .....                                      | 57 |
| 3.8.4  | SMM Control Combinations .....                                    | 57 |
| 3.8.5  | SMM Space Decode and Transaction Handling.....                    | 57 |
| 3.8.6  | Processor WB Transaction to an Enabled SMM Address Space .....    | 57 |
| 3.8.7  | SMM Access Through GTT TLB (Intel® 82G31 GMCH Only) .....         | 58 |
| 3.9    | Memory Shadowing .....  | 58 |
| 3.10   | I/O Address Space.....  | 59 |
| 3.10.1 | PCI Express* I/O Address Mapping .....                            | 59 |
| 3.11   | (G)MCH Decode Rules and Cross-Bridge Address Mapping .....        | 60 |
| 3.11.1 | Legacy VGA and I/O Range Decode Rules .....                       | 60 |
| 4      | (G)MCH Register Description .....                                 | 61 |
| 4.1    | Register Terminology .....  | 62 |
| 4.2    | Configuration Process and Registers.....                          | 64 |
| 4.2.1  | Platform Configuration Structure .....                            | 64 |
| 4.3    | Configuration Mechanisms .....                                    | 65 |
| 4.3.1  | Standard PCI Configuration Mechanism .....                        | 65 |
| 4.3.2  | PCI Express* Enhanced Configuration Mechanism .....               | 65 |
| 4.4    | Routing Configuration Accesses .....                              | 67 |
| 4.4.1  | Internal Device Configuration Accesses.....                       | 68 |
| 4.4.2  | Bridge Related Configuration Accesses.....                        | 68 |
| 4.5    | I/O Mapped Registers .....  | 69 |
| 4.5.1  | CONFIG_ADDRESS—Configuration Address Register .....               | 69 |
| 4.5.2  | CONFIG_DATA—Configuration Data Register .....                     | 71 |
| 5      | DRAM Controller Registers (D0:F0).....                            | 73 |
| 5.1    | DRAM Controller (D0:F0) .....                                     | 73 |
| 5.1.1  | VID—Vendor Identification.....                                    | 75 |
| 5.1.2  | DID—Device Identification .....                                   | 75 |
| 5.1.3  | PCICMD—PCI Command.....   | 76 |
| 5.1.4  | PCISTS—PCI Status .....   | 77 |
| 5.1.5  | RID—Revision Identification .....                                 | 78 |
| 5.1.6  | CC—Class Code.....  | 79 |
| 5.1.7  | MLT—Master Latency Timer .....                                    | 79 |
| 5.1.8  | HDR—Header Type .....   | 80 |
| 5.1.9  | SVID—Subsystem Vendor Identification.....                         | 80 |
| 5.1.10 | SID—Subsystem Identification .....                                | 80 |
| 5.1.11 | CAPPTR—Capabilities Pointer .....                                 | 81 |
| 5.1.12 | PXPEPBAR—PCI Express* Egress Port Base Address .....              | 81 |
| 5.1.13 | MCHBAR—(G)MCH Memory Mapped Register Range Base .....             | 82 |
| 5.1.14 | GGC—GMCH Graphics Control Register (Intel® 82G31 GMCH Only) ..... | 82 |
| 5.1.15 | DEVEN—Device Enable.....  | 84 |
| 5.1.16 | PCIEXBAR—PCI Express* Register Range Base Address .....           | 86 |
| 5.1.17 | DMIBAR—Root Complex Register Range Base Address .....             | 88 |



|        |   |     |
|--------|---|-----|
| 5.1.18 | PAM0—Programmable Attribute Map 0.....                  | 89  |
| 5.1.19 | PAM1—Programmable Attribute Map 1.....                  | 91  |
| 5.1.20 | PAM2—Programmable Attribute Map 2.....                  | 92  |
| 5.1.21 | PAM3—Programmable Attribute Map 3.....                  | 93  |
| 5.1.22 | PAM4—Programmable Attribute Map 4.....                  | 94  |
| 5.1.23 | PAM5—Programmable Attribute Map 5.....                  | 95  |
| 5.1.24 | PAM6—Programmable Attribute Map 6.....                  | 96  |
| 5.1.25 | LAC—Legacy Access Control.....                          | 97  |
| 5.1.26 | REMAPBASE—Remap Base Address Register.....              | 98  |
| 5.1.27 | REMAPLIMIT—Remap Limit Address Register.....            | 98  |
| 5.1.28 | SMRAM—System Management RAM Control.....                | 99  |
| 5.1.29 | ESMRAMC—Extended System Management RAM Control.....     | 100 |
| 5.1.30 | TOM—Top of Memory.....                                  | 101 |
| 5.1.31 | TOUUD—Top of Upper Usable Dram.....                     | 102 |
| 5.1.32 | GBSM—Graphics Base of Stolen Memory.....                | 103 |
| 5.1.33 | BGSM—Base of GTT stolen Memory.....                     | 104 |
| 5.1.34 | TSEGMB—TSEG Memory Base.....                            | 104 |
| 5.1.35 | TOLUD—Top of Low Usable DRAM.....                       | 105 |
| 5.1.36 | ERRSTS—Error Status.....                                | 106 |
| 5.1.37 | ERRCMD—Error Command.....                               | 108 |
| 5.1.38 | SMICMD—SMI Command.....                                 | 109 |
| 5.1.39 | SKPD—Scratchpad Data.....                               | 109 |
| 5.1.40 | CAPID0—Capability Identifier.....                       | 110 |
| 5.2    | MCHBAR.....   | 114 |
| 5.2.1  | CHDECMISC—Channel Decode Miscellaneous.....             | 116 |
| 5.2.2  | CODRBO—Channel 0 DRAM Rank Boundary Address 0.....      | 117 |
| 5.2.3  | COCYCTRKPCHG—Channel 0 CYCTRK PCHG.....                 | 118 |
| 5.2.4  | COCYCTRKACT—Channel 0 CYCTRK ACT.....                   | 119 |
| 5.2.5  | COCYCTRKWR—Channel 0 CYCTRK WR.....                     | 120 |
| 5.2.6  | COCYCTRKRD—Channel 0 CYCTRK READ.....                   | 121 |
| 5.2.7  | COCYCTRKREFR—Channel 0 CYCTRK REFR.....                 | 121 |
| 5.2.8  | COCKECTRL—Channel 0 CKE Control.....                    | 122 |
| 5.2.9  | COREFRCTRL—Channel 0 DRAM Refresh Control.....          | 123 |
| 5.2.10 | COODTCTRL—Channel 0 ODT Control.....                    | 124 |
| 5.2.11 | C1DRBO—Channel 1 DRAM Rank Boundary Address 0.....      | 125 |
| 5.2.12 | C1DRB1—Channel 1 DRAM Rank Boundary Address 1.....      | 125 |
| 5.2.13 | C1DRB2—Channel 1 DRAM Rank Boundary Address 2.....      | 126 |
| 5.2.14 | C1DRB3—Channel 1 DRAM Rank Boundary Address 3.....      | 126 |
| 5.2.15 | C1DRA01—Channel 1 DRAM Rank 0,1 Attributes.....         | 127 |
| 5.2.16 | C1DRA23—Channel 1 DRAM Rank 2,3 Attributes.....         | 127 |
| 5.2.17 | C1CYCTRKPCHG—Channel 1 CYCTRK PCHG.....                 | 128 |
| 5.2.18 | C1CYCTRKACT—Channel 1 CYCTRK ACT.....                   | 129 |
| 5.2.19 | C1CYCTRKWR—Channel 1 CYCTRK WR.....                     | 130 |
| 5.2.20 | C1CYCTRKRD—Channel 1 CYCTRK READ.....                   | 131 |
| 5.2.21 | C1CKECTRL—Channel 1 CKE Control.....                    | 132 |
| 5.2.22 | C1REFRCTRL—Channel 1 DRAM Refresh Control.....          | 133 |
| 5.2.23 | C1ODTCTRL—Channel 1 ODT Control.....                    | 135 |
| 5.2.24 | EPCODRB1—EP Channel 0 DRAM Rank Boundary Address 1..... | 136 |
| 5.2.25 | EPCODRB2—EP Channel 0 DRAM Rank Boundary Address 2..... | 136 |
| 5.2.26 | EPCODRB3—EP Channel 0 DRAM Rank Boundary Address 3..... | 136 |
| 5.2.27 | EPCODRA01—EP Channel 0 DRAM Rank 0,1 Attribute.....     | 137 |
| 5.2.28 | EPCODRA23—EP Channel 0 DRAM Rank 2,3 Attribute.....     | 137 |
| 5.2.29 | EPDCYCTRKWRTPRE—EPD CYCTRK WRT PRE.....                 | 138 |
| 5.2.30 | EPDCYCTRKWRTACT—EPD CYCTRK WRT ACT.....                 | 138 |
| 5.2.31 | EPDCYCTRKWRTWR—EPD CYCTRK WRT WR.....                   | 139 |



|        |  |     |
|--------|--|-----|
| 5.2.32 | EPDCYCTRKWRTRD—EPD CYCTRK WRT READ.....                      | 140 |
| 5.2.33 | EPDCKECONFIGREG—EPD CKE Related Configuration Register ..... | 141 |
| 5.2.34 | EPDREFCONFIG—EP DRAM Refresh Configuration.....              | 143 |
| 5.2.35 | TSC1—Thermal Sensor Control 1 .....                          | 145 |
| 5.2.36 | TSC2—Thermal Sensor Control 2 .....                          | 146 |
| 5.2.37 | TSS—Thermal Sensor Status.....                               | 148 |
| 5.2.38 | TSTTP—Thermal Sensor Temperature Trip Point.....             | 149 |
| 5.2.39 | TCO—Thermal Calibration Offset.....                          | 150 |
| 5.2.40 | THERM1—Hardware Throttle Control .....                       | 151 |
| 5.2.41 | TIS—Thermal Interrupt Status .....                           | 152 |
| 5.2.42 | TSMICMD—Thermal SMI Command.....                             | 154 |
| 5.2.43 | PMSTS—Power Management Status .....                          | 155 |
| 5.3    | EPBAR .....  | 156 |
| 5.3.1  | EPESD—EP Element Self Description .....                      | 156 |
| 5.3.2  | EPL1D—EP Link Entry 1 Description.....                       | 157 |
| 5.3.3  | EPL1A—EP Link Entry 1 Address .....                          | 157 |
| 5.3.4  | EPL2D—EP Link Entry 2 Description.....                       | 158 |
| 5.3.5  | EPL2A—EP Link Entry 2 Address .....                          | 159 |
| 6      | PCI Express* Registers (D1:F0) .....                         | 161 |
| 6.1    | PCI Express* Configuration Register Details (D1:F0) .....    | 164 |
| 6.1.1  | VID1—Vendor Identification .....                             | 164 |
| 6.1.2  | DID1—Device Identification .....                             | 164 |
| 6.1.3  | PCICMD1—PCI Command .....                                    | 165 |
| 6.1.4  | PCISTS1—PCI Status .....                                     | 167 |
| 6.1.5  | RID1—Revision Identification .....                           | 168 |
| 6.1.6  | CC1—Class Code .....   | 168 |
| 6.1.7  | CL1—Cache Line Size .....                                    | 169 |
| 6.1.8  | HDR1—Header Type .....                                       | 169 |
| 6.1.9  | PBUSN1—Primary Bus Number .....                              | 169 |
| 6.1.10 | SBUSN1—Secondary Bus Number.....                             | 170 |
| 6.1.11 | SUBUSN1—Subordinate Bus Number.....                          | 170 |
| 6.1.12 | IOBASE1—I/O Base Address .....                               | 171 |
| 6.1.13 | IOLIMIT1—I/O Limit Address.....                              | 171 |
| 6.1.14 | SSTS1—Secondary Status .....                                 | 172 |
| 6.1.15 | MBASE1—Memory Base Address.....                              | 173 |
| 6.1.16 | MLIMIT1—Memory Limit Address .....                           | 174 |
| 6.1.17 | PMBASE1—Prefetchable Memory Base Address .....               | 175 |
| 6.1.18 | PMLIMIT1—Prefetchable Memory Limit Address.....              | 176 |
| 6.1.19 | PMBASEU1—Prefetchable Memory Base Address .....              | 177 |
| 6.1.20 | PMLIMITU1—Prefetchable Memory Limit Address.....             | 178 |
| 6.1.21 | CAPPTR1—Capabilities Pointer.....                            | 179 |
| 6.1.22 | INTRLINE1—Interrupt Line.....                                | 179 |
| 6.1.23 | INTRPIN1—Interrupt Pin.....                                  | 179 |
| 6.1.24 | BCTRL1—Bridge Control .....                                  | 180 |
| 6.1.25 | PM_CAPID1—Power Management Capabilities.....                 | 182 |
| 6.1.26 | PM_CS1—Power Management Control/Status .....                 | 183 |
| 6.1.27 | SS_CAPID—Subsystem ID and Vendor ID Capabilities .....       | 184 |
| 6.1.28 | SS—Subsystem ID and Subsystem Vendor ID .....                | 184 |
| 6.1.29 | MSI_CAPID—Message Signaled Interrupts Capability ID.....     | 185 |
| 6.1.30 | MC—Message Control.....                                      | 185 |
| 6.1.31 | MA—Message Address.....                                      | 186 |
| 6.1.32 | MD—Message Data.....   | 186 |
| 6.1.33 | PEG_CAPL—PCI Express*-G Capability List.....                 | 187 |
| 6.1.34 | PEG_CAP—PCI Express*-G Capabilities.....                     | 187 |



|        |  |     |
|--------|--|-----|
| 6.1.35 | DCAP—Device Capabilities .....   | 188 |
| 6.1.36 | DCTL—Device Control .....  | 189 |
| 6.1.37 | DSTS—Device Status .....   | 190 |
| 6.1.38 | LCAP—Link Capabilities .....   | 191 |
| 6.1.39 | LCTL—Link Control .....  | 193 |
| 6.1.40 | LSTS—Link Status .....   | 195 |
| 6.1.41 | SLOTCAP—Slot Capabilities.....   | 196 |
| 6.1.42 | SLOTCTL—Slot Control.....  | 197 |
| 6.1.43 | SLOTSTS—Slot Status.....   | 200 |
| 6.1.44 | RCTL—Root Control .....  | 201 |
| 6.1.45 | RSTS—Root Status .....   | 202 |
| 6.1.46 | PEGLC—PCI Express*-G Legacy Control.....                               | 203 |
| 6.1.47 | VCECH—Virtual Channel Enhanced Capability Header .....                 | 204 |
| 6.1.48 | PVCCAP1—Port VC Capability Register 1 .....                            | 204 |
| 6.1.49 | PVCCAP2—Port VC Capability Register 2 .....                            | 205 |
| 6.1.50 | PVCCTL—Port VC Control.....  | 205 |
| 6.1.51 | VCORCAP—VC0 Resource Capability .....                                  | 206 |
| 6.1.52 | VCORCTL—VC0 Resource Control .....                                     | 207 |
| 6.1.53 | VCORSTS—VC0 Resource Status.....                                       | 208 |
| 6.1.54 | RCLDECH—Root Complex Link Declaration Enhanced.....                    | 209 |
| 6.1.55 | ESD—Element Self Description.....                                      | 209 |
| 6.1.56 | LE1D—Link Entry 1 Description .....                                    | 210 |
| 6.1.57 | LE1A—Link Entry 1 Address .....  | 210 |
| 6.1.58 | PEGSSTS—PCI Express*-G Sequence Status .....                           | 211 |
| 7      | Direct Memory Interface (DMI) Registers.....                           | 213 |
| 7.1    | Direct Memory Interface (DMI) Configuration Register Details.....      | 214 |
| 7.1.1  | DMIVCECH—DMI Virtual Channel Enhanced Capability .....                 | 214 |
| 7.1.2  | DMIPVCCAP1—DMI Port VC Capability Register 1 .....                     | 215 |
| 7.1.3  | DMIPVCCAP2—DMI Port VC Capability Register 2 .....                     | 215 |
| 7.1.4  | DMIPVCCTL—DMI Port VC Control.....                                     | 216 |
| 7.1.5  | DMIVCORCAP—DMI VC0 Resource Capability .....                           | 216 |
| 7.1.6  | DMIVCORCTL0—DMI VC0 Resource Control .....                             | 217 |
| 7.1.7  | DMIVCORSTS—DMI VC0 Resource Status.....                                | 218 |
| 7.1.8  | DMIVC1RCAP—DMI VC1 Resource Capability .....                           | 218 |
| 7.1.9  | DMIVC1RCTL1—DMI VC1 Resource Control .....                             | 219 |
| 7.1.10 | DMIVC1RSTS—DMI VC1 Resource Status.....                                | 220 |
| 7.1.11 | DMILCAP—DMI Link Capabilities .....                                    | 220 |
| 7.1.12 | DMILCTL—DMI Link Control .....   | 221 |
| 7.1.13 | DMILSTS—DMI Link Status .....  | 222 |
| 8      | Integrated Graphics Registers (D2:F0,F1) (Intel® 82G31 GMCH Only)..... | 223 |
| 8.1    | Integrated Graphics Register Details (D2:F0).....                      | 223 |
| 8.1.1  | VID2—Vendor Identification .....                                       | 224 |
| 8.1.2  | DID—Device Identification .....  | 225 |
| 8.1.3  | PCICMD2—PCI Command .....  | 225 |
| 8.1.4  | PCISTS2—PCI Status .....   | 227 |
| 8.1.5  | RID2—Revision Identification .....                                     | 228 |
| 8.1.6  | CC—Class Code.....   | 228 |
| 8.1.7  | CLS—Cache Line Size.....   | 229 |
| 8.1.8  | MLT2—Master Latency Timer.....   | 229 |
| 8.1.9  | HDR2—Header Type .....   | 230 |
| 8.1.10 | GMADR—Graphics Memory Range Address.....                               | 230 |
| 8.1.11 | IOBAR—I/O Base Address.....  | 231 |
| 8.1.12 | SVID2—Subsystem Vendor Identification .....                            | 231 |



|        |  |     |
|--------|--|-----|
| 8.1.13 | SID2—Subsystem Identification .....                            | 232 |
| 8.1.14 | ROMADR—Video BIOS ROM Base Address .....                       | 232 |
| 8.1.15 | CAPPOINT—Capabilities Pointer .....                            | 233 |
| 8.1.16 | INTRLINE—Interrupt Line .....                                  | 233 |
| 8.1.17 | INTRPIN—Interrupt Pin .....                                    | 233 |
| 8.1.18 | MINGNT—Minimum Grant .....                                     | 234 |
| 8.1.19 | MAXLAT—Maximum Latency .....                                   | 234 |
| 8.1.20 | CAPID0—Capability Identifier .....                             | 235 |
| 8.1.21 | MGGC—GMCH Graphics Control Register .....                      | 236 |
| 8.1.22 | DEVEN—Device Enable .....                                      | 238 |
| 8.1.23 | SSRW—Software Scratch Read Write .....                         | 239 |
| 8.1.24 | BSM—Base of Stolen Memory .....                                | 239 |
| 8.1.25 | HSRW—Hardware Scratch Read Write .....                         | 239 |
| 8.1.26 | MC—Message Control .....                                       | 240 |
| 8.1.27 | MA—Message Address .....                                       | 241 |
| 8.1.28 | MD—Message Data .....  | 241 |
| 8.1.29 | GDRST—Graphics Debug Reset .....                               | 242 |
| 8.1.30 | PMCAPID—Power Management Capabilities ID .....                 | 243 |
| 8.1.31 | PMCAP—Power Management Capabilities .....                      | 243 |
| 8.1.32 | PMCS—Power Management Control/Status .....                     | 244 |
| 8.1.33 | SWSMI—Software SMI .....                                       | 245 |
| 8.2    | IGD Configuration Register Details (D2:F1) .....               | 246 |
| 8.2.1  | VID2—Vendor Identification .....                               | 248 |
| 8.2.2  | DID2—Device Identification .....                               | 248 |
| 8.2.3  | PCICMD2—PCI Command .....                                      | 249 |
| 8.2.4  | PCISTS2—PCI Status .....                                       | 250 |
| 8.2.5  | RID2—Revision Identification .....                             | 251 |
| 8.2.6  | CC—Class Code Register .....                                   | 251 |
| 8.2.7  | CLS—Cache Line Size .....                                      | 252 |
| 8.2.8  | MLT2—Master Latency Timer .....                                | 252 |
| 8.2.9  | HDR2—Header Type .....   | 253 |
| 8.2.10 | MMADR—Memory Mapped Range Address .....                        | 253 |
| 8.2.11 | SVID2—Subsystem Vendor Identification .....                    | 254 |
| 8.2.12 | SID2—Subsystem Identification .....                            | 254 |
| 8.2.13 | ROMADR—Video BIOS ROM Base Address .....                       | 255 |
| 8.2.14 | CAPPOINT—Capabilities Pointer .....                            | 255 |
| 8.2.15 | MINGNT—Minimum Grant .....                                     | 256 |
| 8.2.16 | MAXLAT—Maximum Latency .....                                   | 256 |
| 8.2.17 | CAPID0—Mirror of Dev0 Capability Identifier .....              | 256 |
| 8.2.18 | MGGC—Mirror of Dev 0 GMCH Graphics Control Register .....      | 257 |
| 8.2.19 | DEVEN—Device Enable .....                                      | 259 |
| 8.2.20 | SSRW—Mirror of Fun 0 Software Scratch Read Write .....         | 260 |
| 8.2.21 | BSM—Mirror of Func0 Base of Stolen Memory .....                | 260 |
| 8.2.22 | HSRW—Mirror of Dev2 Func0 Hardware Scratch Read Write .....    | 261 |
| 8.2.23 | GDRST—Mirror of Dev2 Func0 Graphics Reset .....                | 261 |
| 8.2.24 | PMCAPID—Mirror of Fun 0 Power Management Capabilities ID ..... | 262 |
| 8.2.25 | PMCAP—Mirror of Fun 0 Power Management Capabilities .....      | 263 |
| 8.2.26 | PMCS—Power Management Control/Status .....                     | 264 |
| 8.2.27 | SWSMI—Mirror of Func0 Software SMI .....                       | 265 |
| 9      | Functional Description .....                                   | 267 |
| 9.1    | Host Interface .....   | 267 |
| 9.1.1  | FSB IOQ Depth .....  | 267 |
| 9.1.2  | FSB OoQ Depth .....  | 267 |
| 9.1.3  | FSB GTL+ Termination .....                                     | 267 |



|        |   |     |
|--------|---|-----|
| 9.1.4  | FSB Dynamic Bus Inversion .....   | 267 |
| 9.1.5  | APIC Cluster Mode Support .....   | 268 |
| 9.2    | System Memory Controller.....   | 268 |
| 9.2.1  | System Memory Organization Modes .....                                      | 268 |
| 9.2.2  | System Memory Technology Supported .....                                    | 270 |
| 9.3    | PCI Express* .....  | 271 |
| 9.3.1  | Intel® Serial Digital Video Output (sDVO)<br>(Intel® 82G31 GMCH Only) ..... | 272 |
| 9.4    | Integrated Graphics Controller (Intel® 82G31 GMCH Only) .....               | 276 |
| 9.4.1  | 3D Graphics Pipeline .....  | 276 |
| 9.5    | Display Interfaces (Intel® 82G31 GMCH Only) .....                           | 278 |
| 9.5.1  | Analog Display Port Characteristics .....                                   | 279 |
| 9.5.2  | Digital Display Interface .....   | 280 |
| 9.5.3  | Multiple Display Configurations.....  | 283 |
| 9.6    | Power Management .....  | 283 |
| 9.7    | Thermal Sensor.....   | 284 |
| 9.7.1  | PCI Device 0, Function 0 .....  | 284 |
| 9.7.2  | MCHBAR Thermal Sensor Registers .....                                       | 284 |
| 9.8    | Clocking.....   | 285 |
| 10     | Electrical Characteristics .....  | 287 |
| 10.1   | Absolute Minimum and Maximum Ratings .....                                  | 287 |
| 10.1.1 | Current Consumption.....  | 289 |
| 10.2   | Signal Groups.....  | 291 |
| 10.3   | Buffer Supply and DC Characteristics .....                                  | 294 |
| 10.3.1 | I/O Buffer Supply Voltages .....  | 294 |
| 10.3.2 | General DC Characteristics .....  | 296 |
| 10.4   | R, G, B / CRT DAC Display DC Characteristics (Intel® 82G31 GMCH Only) ...   | 300 |
| 11     | Ballout and Package Information .....                                       | 301 |
| 11.1   | Ballout.....  | 301 |
| 11.2   | Package Information.....  | 316 |
| 12     | Testability.....  | 317 |
| 12.1   | XOR Test Mode Initialization .....  | 317 |
| 12.2   | XOR Chain Definition .....  | 319 |
| 12.3   | XOR Chains .....  | 320 |



## Figures

|   |     |
|---|-----|
| Figure 1-1. Intel® G31 Express Chipset System Block Diagram Example .....   | 16  |
| Figure 1-2. Intel® P31 Express Chipset System Block Diagram Example .....   | 17  |
| Figure 3-1. System Address Ranges.....                                      | 43  |
| Figure 3-2. DOS Legacy Address Range.....                                   | 44  |
| Figure 3-3. Main Memory Address Range.....                                  | 48  |
| Figure 3-4. PCI Memory Address Range.....                                   | 51  |
| Figure 4-1. Memory Map to PCI Express* Device Configuration Space.....      | 66  |
| Figure 4-2. GMCH Configuration Cycle Flow Chart.....                        | 67  |
| Figure 9-1. sDVO Conceptual Block Diagram .....                             | 273 |
| Figure 9-2. Concurrent sDVO / PCI Express* Non-Reversed Configurations..... | 275 |
| Figure 9-3. Concurrent sDVO / PCI Express* Reversed Configurations .....    | 275 |
| Figure 9-4. Integrated 3D Graphics Pipeline .....                           | 277 |
| Figure 9-5. Intel® G31/P31 Express Chipset System Clock Diagram.....        | 286 |
| Figure 11-1. (G)MCH Ballout Diagram (Top View Left – Columns 43–30) .....   | 302 |
| Figure 11-2. (G)MCH Ballout Diagram (Top View Middle – Columns 29–15) ..... | 303 |
| Figure 11-3. (G)MCH Ballout Diagram (Top View Right – Columns 14–0).....    | 304 |
| Figure 11-6. (G)MCH Package Drawing.....                                    | 316 |
| Figure 12-1. XOR Test Mode Initialization Cycles .....                      | 317 |



## Tables

|  |     |
|--|-----|
| Table 3-1. Expansion Area Memory Segments .....  | 46  |
| Table 3-2. Extended System BIOS Area Memory Segments .....   | 47  |
| Table 3-3. System BIOS Area Memory Segments .....  | 47  |
| Table 3-4. Pre-allocated Memory Example for 64 MB DRAM, 1 MB VGA, 1 MB<br>GTT stolen and 1 MB TSEG .....                 | 49  |
| Table 3-5. Pre-Allocated Memory Example for 64-MB DRAM, 1-MB VGA and<br>1-MB TSEG .....                                  | 56  |
| Table 3-6. SMM Space Table .....   | 57  |
| Table 5-1. DRAM Controller Register Address Map (D0:F0) .....  | 73  |
| Table 5-2. MCHBAR Register Address Map .....   | 114 |
| Table 5-3. EPBAR Register Address Map .....  | 156 |
| Table 6-1. PCI Express* Register Address Map (Device 1, Function 0) .....  | 161 |
| Table 7-1. DMI Register Address Map .....  | 213 |
| Table 8-1. Integrated Graphics Device Register Address Map<br>(Device 2, Function 0) .....                               | 223 |
| Table 8-2. Integrated Graphics Device Register Address Map (D2:F1) .....   | 246 |
| Table 9-1. Sample System Memory Dual Channel Symmetric Organization<br>Mode with Intel® Flex Memory Mode Enabled .....   | 269 |
| Table 9-2. Sample System Memory Dual Channel Asymmetric Organization<br>Mode with Intel® Flex Memory Mode Disabled ..... | 269 |
| Table 9-3. Supported DIMM Module Configurations .....  | 270 |
| Table 9-4. Concurrent sDVO / PCI Express* Configuration Strap Controls .....   | 274 |
| Table 10-1. Absolute Minimum and Maximum Ratings .....   | 287 |
| Table 10-2. Current Consumption in S0 .....  | 289 |
| Table 10-4. Signal Groups .....  | 291 |
| Table 10-5. I/O Buffer Supply Voltage .....  | 295 |
| Table 10-6. DC Characteristics .....   | 296 |
| Table 10-7. R, G, B / CRT DAC Display DC Characteristics: Functional<br>Operating Range (VCCA_DAC = 3.3 V ± 5%) .....    | 300 |
| Table 11-1. (G)MCH Ballout Sorted by Signal Name .....   | 305 |
| Table 12-1. XOR Chain 14 functionality .....   | 318 |
| Table 12-2. XOR Chain Outputs .....  | 319 |
| Table 12-3. XOR Chain 0 .....  | 320 |
| Table 12-4. XOR Chain 1 .....  | 321 |
| Table 12-5. XOR Chain 2 .....  | 321 |
| Table 12-6. XOR Chain 3 .....  | 322 |
| Table 12-7. XOR Chain 4 .....  | 322 |
| Table 12-8. XOR Chain 5 .....  | 322 |
| Table 12-9. XOR Chain 6 .....  | 323 |
| Table 12-10. XOR Chain 8 .....   | 324 |
| Table 12-11. XOR Chain 9 .....   | 325 |
| Table 12-12. XOR Chain 10 .....  | 325 |
| Table 12-13. XOR Chain 12 .....  | 326 |
| Table 12-14. XOR Chain 13 .....  | 326 |
| Table 12-15. XOR Chain 14 .....  | 326 |



## *Revision History*

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| Revision Number | Description     | Revision Date |
|-----------------|-----------------|---------------|
| -001            | Initial release | July 2007     |

§



# Intel® 82G31/82P31 (G)MCH Features

- Processor/Host Interface (FSB)
  - Supports Intel® Core™2 Duo desktop processors and Intel® Core™2 Quad processors
  - 800/1067 MT/s (200/266 MHz) FSB
  - Hyper-Threading Technology (HT Technology)
  - FSB Dynamic Bus Inversion (DBI)
  - 36-bit host bus addressing
  - 12-deep In-Order Queue
  - 1-deep Defer Queue
  - GTL+ bus driver with integrated GTL termination resistors
  - Supports cache Line Size of 64 bytes
- System Memory Interface
  - One or two channels (each channel consisting of 64 data lines)
  - Single or Dual Channel memory organization
  - DDR2-800/667 frequencies
  - Unbuffered, non-ECC DIMMs only
  - Supports 1-Gb, 512-Mb DDR2 technologies for x8 and x16 devices
  - 4 GB maximum memory
- Direct Media Interface (DMI)
  - Chip-to-chip connection interface to Intel ICH7
  - 2 GB/s point-to-point DMI to ICH9 (1 GB/s each direction)
  - 100 MHz reference clock (shared with PCI Express graphics attach)
  - 32-bit downstream addressing
  - Messaging and Error Handling
- PCI Express\* Interface
  - One x16 PCI Express port
  - Compatible with the *PCI Express Base Specification, Revision 1.1*
  - Raw bit rate on data pins of 2.5 Gb/s resulting in a real bandwidth per pair of 250 MB/s
- Integrated Graphics Device (82G31 GMCH only)
  - Core frequency of 400 MHz
  - 1.6 GP/s pixel rate
  - High-Quality 3D Setup and Render Engine
  - High-Quality Texture Engine
  - 3D Graphics Rendering Enhancements
  - 2D Graphics
  - Video Overlay
  - Multiple Overlay Functionality
- Analog Display (82G31 GMCH only)
  - 350 MHz Integrated 24-bit RAMDAC
  - Up to 2048x1536 @ 75 Hz refresh
  - Hardware Color Cursor Support
  - DDC2B Compliant Interface
- Digital Display (82G31 GMCH only)
  - SDVO ports in single mode supported
  - 225 MHz dot clock on each 12-bit interface
  - Flat panels up to 1920x1200 @ 60 Hz or digital CRT/HDTV at 1400x1050 @ 85Hz
  - Dual independent display options with digital display
  - Multiplexed digital display channels (supported with ADD2 Card).
  - Supports TMDS transmitters or TV-Out encoders
  - ADD2/MEC card uses PCI Express graphics x16 connector
  - Two channels multiplexed with PCI Express\* Graphics port
  - Supports Hot-Plug and Display
- Thermal Sensor
  - Catastrophic Trip Point support
  - Hot Trip Point support for SMI generation
- Power Management
  - PC99 suspend to DRAM support (“STR”, mapped to ACPI state S3)
  - ACPI Revision 2.0 compatible power management
  - Supports processor states: C0, C1, C2
  - Supports System states: S0, S1, S3, and S5
  - Supports processor Thermal Management 2
- Package
  - FC-BGA. 34 mm × 34 mm. The 1226 balls are located in a non-grid pattern





# 1 Introduction

---

The Intel® G31/P31 Express Chipset is designed for use with Intel® Core™2 Duo desktop processor and Intel® Core™2 Quad processor based platforms. The chipsets each contain two components: GMCH (or MCH) for the host bridge and I/O Controller Hub 7 (ICH7) for the I/O subsystem. The 82G31 GMCH is part of the Intel® G31 Express Chipset. The 82P31 MCH is part of the Intel® P31 Express chipset. The ICH7 is the seventh generation I/O Controller Hub and provides a multitude of I/O related functions. Figure 1-1 and Figure 1-2 show examples system block diagrams for the Intel® G31 and P31 Express Chipsets.

This document is the datasheet for the Intel® 82G31 Graphics and Memory Controller Hub (GMCH) and Intel® 82P31 Memory Controller Hub (MCH). Topics covered include; signal description, system memory map, PCI register description, a description of the (G)MCH interfaces and major functional units, electrical characteristics, ballout definitions, and package characteristics.

The primary difference between the Intel® 82G31 GMCH and 82P31 MCH is that the 82G31 GMCH has an integrated graphics device (IGD) plus the associated display interfaces. The 82P31 does not contain an IGD and the associated interfaces.

**Note:** Unless otherwise specified, the information in this document applies to the Intel® 82G31 Graphics and Memory Controller Hub (GMCH) and Intel® 82P31 Memory Controller Hub (MCH).

**Note:** The term (G)MCH refers to the 82G31 GMCH and 82P31 MCH.

**Note:** Unless otherwise specified, ICH7 refers to the Intel® 82801GB ICH7, Intel® 82801GR ICH7R, and Intel® 82801GDH ICH7DH I/O Controller Hub 7 components.

Figure 1-1. Intel® G31 Express Chipset System Block Diagram Example

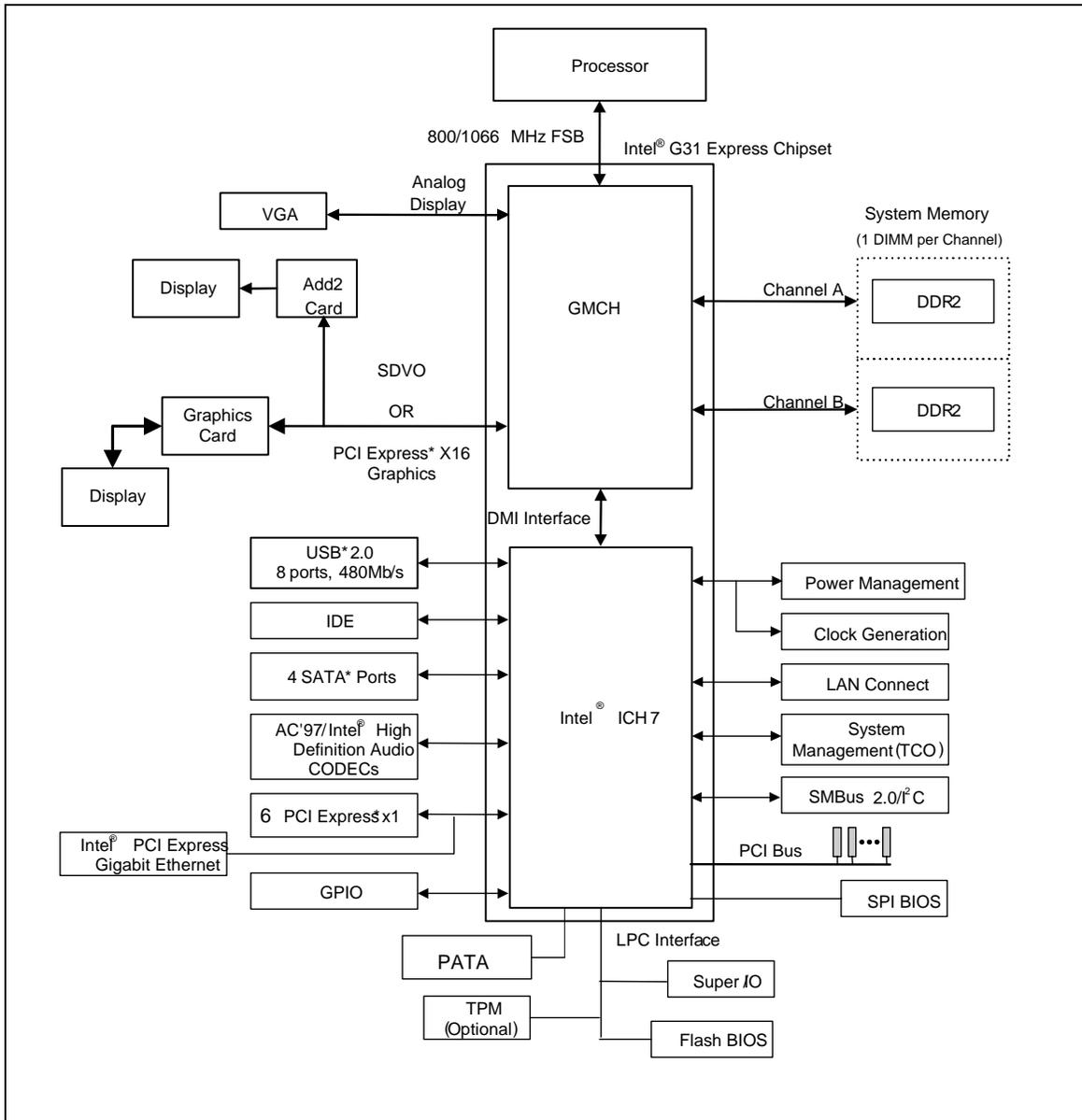
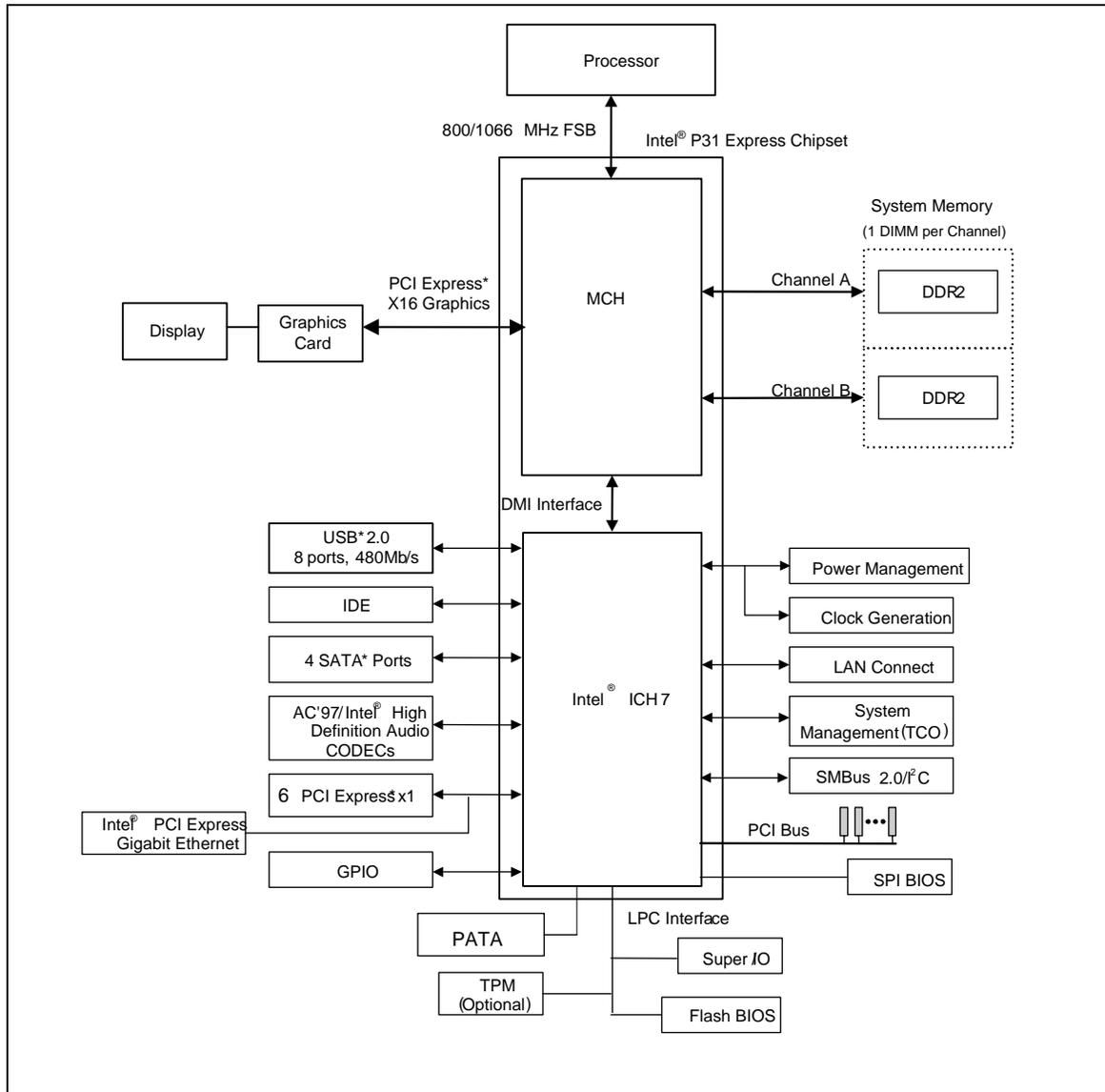




Figure 1-2. Intel® P31 Express Chipset System Block Diagram Example





## 1.1 Terminology

| Term                     | Description  |
|--------------------------|--|
| ADD Card                 | Advanced Digital Display Card. Provides digital display options for an Intel Graphics Controller that supports ADD cards (have DVOs multiplexed with AGP interface). Keyed like an AGP 4x card and plugs into an AGP connector. Will <b>not</b> work with an Intel Graphics Controller that implements Intel® SDVO.  |
| ADD2 Card                | Advanced Digital Display Card – 2 <sup>nd</sup> Generation. Provides digital display options for an Intel graphics controller that supports ADD2 cards. Plugs into an x16 PCI Express* connector but utilizes the multiplexed SDVO interface. Will <b>not</b> work with an Intel Graphics Controller that supports Intel® DVO and ADD cards.   |
| Chipset / Root – Complex | Used in this specification to refer to one or more hardware components that connect processor complexes to the I/O and memory subsystems. The chipset may include a variety of integrated devices.   |
| Core                     | The internal base logic in the (G)MCH  |
| CPU                      | Refers to the processors.  |
| CRT                      | Cathode Ray Tube   |
| DBI                      | Dynamic Bus Inversion  |
| DDR2                     | A second generation Double Data Rate SDRAM memory technology   |
| DMI                      | (G)MCH-Intel® ICH7 Direct Media Interface  |
| DVI                      | Digital Video Interface. Specification that defines the connector and interface for digital displays.  |
| DVMT                     | Dynamic Video Memory Technology  |
| FSB                      | Front Side Bus, synonymous with Host or processor bus  |
| Full Reset               | Full reset is when PWROK is deasserted. Warm reset is when both RSTIN# and PWROK are asserted.   |
| GMCH                     | Graphics Memory Controller Hub component that contains the processor interface, DRAM controller, display interfaces, integrated graphics device, and x16 PCI Express port (typically the external graphics interface). It communicates with the I/O controller hub (Intel® ICH7) over the DMI interconnect.  |
| HAW                      | Host Address Width. This refers to the maximum host physical address that can be accessed by a given processor / root-complex implementation. The host BIOS typically reports the host system address map.   |
| Host                     | This term is used synonymously with processor  |
| HPA                      | Host Physical Address  |
| IGD                      | Internal Graphics Device   |
| Intel® ICH7              | Seventh generation I/O Controller Hub component that contains additional functionality compared to previous Intel® ICHs, The Intel® I/O Controller Hub 7 component contains the primary PCI interface, LPC interface, USB2, SATA, ATA-100 and other I/O functions. It communicates with the (G)MCH over a proprietary interconnect called DMI. For this (G)MCH, the term Intel® ICH refers to Intel® ICH7. |



| Term                       | Description   |
|----------------------------|---|
| INTx                       | An interrupt request signal where X stands for interrupts A, B, C and D   |
| IOQ                        | In Order Queue  |
| MCH                        | Memory Controller Hub component that contains the processor interface, DRAM controller, and x16 PCI Express port (typically the external graphics interface). It communicates with the I/O controller hub (Intel® ICH7) over the DMI interconnect.  |
| Media Expansion Card (MEC) | Media Expansion Card –. Provides digital display options for an Intel Graphics Controller that supports MEC cards. Plugs into an x16 PCI Express connector but utilizes the multiplexed sDVO interface. Adds Video In capabilities to platform. Will <b>not</b> work with an Intel Graphics Controller that supports DVO and ADD cards. Will function as an ADD2 card in an ADD2 supported system, but Video In capabilities will not work.                                     |
| MSI                        | Message Signaled Interrupt. A transaction conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.®  |
| OOQ                        | Out of Order Queuing  |
| PCI Express*               | A high-speed serial interface whose configuration is software compatible with the legacy PCI specifications.  |
| Primary PCI                | The physical PCI bus that is driven directly by the Intel® ICH7 component. Communication between Primary PCI and the (G)MCH occurs over DMI. Note that the Primary PCI bus is <b>not</b> PCI Bus 0 from a configuration standpoint.   |
| Rank                       | A unit of DRAM corresponding to eight x8 SDRAM devices in parallel or four x16 SDRAM devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DIMM.  |
| SCI                        | System Control Interrupt. Used in ACPI protocol.  |
| sDVO                       | Serial Digital Video Out (sDVO). Digital display channel that serially transmits digital display data to an external sDVO device. The sDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e., TMDS, LVDS, and TV-Out). This interface is not electrically compatible with the previous digital display channel - DVO. For 82G31 GMCH, it will be multiplexed on a portion of the x16 graphics PCI Express interface. |
| sDVO Device                | Third party codec that utilizes sDVO as an input. May have a variety of output formats, including DVI, LVDS, HDMI, TV-out, etc.   |
| SERR                       | System Error. An indication that an unrecoverable error has occurred on an I/O bus.   |
| SMI                        | System Management Interrupt. Used to indicate any of several system conditions such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity.  |
| TMDS                       | Transition Minimized Differential Signaling. Signaling interface from Silicon Image that is used in DVI and HDMI.   |
| UMA                        | Unified Memory Architecture used for system memory.. Typically used by IGD or ME functionality.   |
| VCO                        | Voltage Controlled Oscillator   |



## 1.2 Reference Documents

| Document Name   | Location  |
|---|---|
| <i>Intel® G31/P31 Express Chipset Specification Update</i>  | <a href="http://www.intel.com/design/chipsets/specupdt/317496.htm">http://www.intel.com/design/chipsets/specupdt/317496.htm</a>               |
| <i>Intel® G31/P31 Express Chipset Thermal and Mechanical Design Guide.</i>                                      | <a href="http://www.intel.com/design/chipsets/designex/317497.htm">http://www.intel.com/design/chipsets/designex/317497.htm</a>               |
| <i>Intel® Core™ 2 Duo Processor and Intel® Pentium® Dual Core Processor Thermal and Mechanical Design Guide</i> | <a href="http://www.intel.com/design/processor/designex/317804.htm">http://www.intel.com/design/processor/designex/317804.htm</a>             |
| <i>Intel® I/O Controller Hub 7 (ICH7) Family Thermal Mechanical Design Guide.</i>                               | <a href="http://developer.intel.com//design/chipsets/designex/307015.htm">http://developer.intel.com//design/chipsets/designex/307015.htm</a> |
| <i>Intel® I/O Controller Hub 7 (ICH7) Family Datasheet</i>  | <a href="http://developer.intel.com//design/chipsets/datashts/307013.htm">http://developer.intel.com//design/chipsets/datashts/307013.htm</a> |
| <i>Designing for Energy Efficiency White Paper</i>  | <a href="http://www.intel.com/design/chipsets/applnots/316970.htm">www.intel.com/design/chipsets/applnots/316970.htm</a>                      |
| <i>Intel® P35/G33 Express Chipset Memory Technology and Configuration Guide White Paper</i>                     | <a href="http://www.intel.com/design/chipsets/applnots/316971.htm">www.intel.com/design/chipsets/applnots/316971.htm</a>                      |
| <i>Advanced Configuration and Power Interface Specification, Version 2.0</i>                                    | <a href="http://www.acpi.info/">http://www.acpi.info/</a>   |
| <i>Advanced Configuration and Power Interface Specification, Version 1.0b</i>                                   | <a href="http://www.acpi.info/">http://www.acpi.info/</a>   |
| <i>The PCI Local Bus Specification, Version 2.3</i>   | <a href="http://www.pcisig.com/specifications">http://www.pcisig.com/specifications</a>   |
| <i>PCI Express* Specification, Version 1.1</i>  | <a href="http://www.pcisig.com/specifications">http://www.pcisig.com/specifications</a>   |



## 1.3 (G)MCH Overview

The Intel® 82G31 GMCH and 82P31 MCH are designed for use with the Intel® Core™2 Duo processors and Intel® Core™2 Quad processors in desktop platforms. The role of a (G)MCH in a system is to manage the flow of information between its four interfaces: the processor interface, the system memory interface, the external graphics interface, and the I/O controller through DMI interface. This includes arbitrating between the four interfaces when each initiates transactions. The (G)MCH supports one or two channels of DDR2 SDRAM. It also supports the PCI Express based external graphics attach. The Intel® G31/P31 platform supports the seventh generation I/O Controller Hub (Intel® ICH7).

### 1.3.1 Host Interface

The (G)MCH can use a single LGA775 socket processor. The (G)MCH supports a FSB frequency of 800/1066 MHz. Host-initiated I/O cycles are decoded to PCI Express, DMI, or the (G)MCH configuration space. Host-initiated memory cycles are decoded to PCI Express, DMI or system memory. PCI Express device accesses to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from PCI Express using PCI semantics and from DMI to system SDRAM will be snooped on the host bus.

Capabilities of the Host Interface include:

- Supports Intel Core™2 Duo processors and Intel® Core™2 Quad processors
- Supports Front Side Bus (FSB) at the following Frequency Ranges:
  - 800/1066 (200/266MHz)
- Supports FSB Dynamic Bus Inversion (DBI)
- Supports 36-bit host bus addressing, allowing the processor to access the entire 64 GB of the host address space.
- Has a 12-deep In-Order Queue to support up to twelve outstanding pipelined address requests on the host bus
- Has a 1-deep Defer Queue
- Uses GTL+ bus driver with integrated GTL termination resistors
- Supports a Cache Line Size of 64 bytes



### 1.3.2 System Memory Interface

The (G)MCH integrates a system memory DDR2 controller with two, 64-bit wide interfaces. The buffers support SSTL\_1.8 (Stub Series Terminated Logic for 1.8 V) signal interfaces. The memory controller interface is fully configurable through a set of control registers.

Capabilities of the system memory interface include:

- Directly supports one or two channels of DDR2 memory with a maximum of one DIMM per channel
- Supports single and dual channel memory organization modes
- Supports a data burst length of eight for all memory organization modes
- Supports memory data transfer rates of 667 and 800 MHz for DDR2
- I/O Voltage of 1.8 V for DDR2
- Supports only un-buffered non-ECC DDR2 DIMMs
- Supports maximum memory bandwidth of 6.4 GB/s in single-channel or dual-channel asymmetric mode, or 12.8 GB/s in dual-channel symmetric mode assuming DDR2 800MHz
- Supports 512 Mb and 1 Gb DDR2 DRAM technologies for x8 and x16 devices
- Using 512 Mb device technologies, the smallest memory capacity possible is 256 MB, assuming Single Channel Mode with a single x16 single sided un-buffered non-ECC DIMM memory configuration
- Using 1 Gb device technologies, the largest memory capacity possible is 4 GB, assuming Dual Channel Mode with two x8 double sided un-buffered non-ECC DIMM memory configuration
- Supports up to 16 simultaneous open pages per channel (assuming 2 ranks of 8 bank devices)
- Supports opportunistic refresh scheme
- Supports Partial Writes to memory using Data Mask (DM) signals
- Supports a memory thermal management scheme to selectively manage reads and/or writes. Memory thermal management can be triggered either by on-die thermal sensor, or by preset limits. Management limits are determined by weighted sum of various commands that are scheduled on the memory interface



### 1.3.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the (G)MCH and ICH7. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

To provide for true isochronous transfers and configurable Quality of Service (QoS) transactions, the ICH7 supports two virtual channels on DMI: VC0 and VC1. These two channels provide a fixed arbitration scheme where VC1 is always the highest priority. VC0 is the default conduit of traffic for DMI and is always enabled. VC1 must be specifically enabled and configured at both ends of the DMI link (i.e., the ICH7 and (G)MCH).

- A chip-to-chip connection interface to Intel ICH7
- 2 GB/s point-to-point DMI to ICH7 (1 GB/s each direction)
- 100 MHz reference clock (shared with PCI Express Graphics Attach)
- 32-bit downstream addressing
- APIC and MSI interrupt messaging support. Will send Intel-defined "End Of Interrupt" broadcast message when initiated by the processor.
- Message Signaled Interrupt (MSI) messages
- SMI, SCI and SERR error indication

### 1.3.4 PCI Express\* Interface

The (G)MCH contains one 16-lane (x16) PCI Express port intended for an external PCI Express graphics card. The PCI Express port is compliant to the *PCI Express\* Base Specification* revision 1.1. The x16 port operates at a frequency of 2.5 GB/s on each lane while employing 8b/10b encoding, and supports a maximum theoretical bandwidth of 40 GB/s in each direction. The 82G31 GMCH multiplexes a PCI Express interface with the Intel® sDVO ports.

- One, 16-lane PCI Express port intended for graphics attach, compatible to the PCI Express\* Base Specification revision 1.1.
- PCI Express frequency of 1.25 GHz resulting in 2.5 GB/s each direction per lane.
- Raw bit-rate on the data pins of 2.5 GB/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface
- Maximum theoretical realized bandwidth on the interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when x16.
- PCI Express\* Graphics Extended Configuration Space. The first 256 bytes of configuration space alias directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4 KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express Enhanced Addressing Mechanism. Accessing the device configuration space in a flat memory mapped fashion.



- Automatic discovery, negotiation, and training of link out of reset
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, PCI Express-relaxed ordering)
- Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e., normal PCI 2.3 Configuration space as a PCI-to-PCI bridge)
- Supports “static” lane numbering reversal. This method of lane reversal is controlled by a Hardware Reset strap, and reverses both the receivers and transmitters for all lanes (e.g., TX[15]->TX[0], RX[15]->RX[0]). This method is transparent to all external devices and is different than lane reversal as defined in the PCI Express Specification. In particular, link initialization is not affected by static lane reversal.

### 1.3.5 Graphics Features (Intel® 82G31 GMCH Only)

The GMCH provides an integrated graphics device (IGD) delivering cost competitive 3D, 2D and video capabilities. The GMCH contains an extensive set of instructions for 3D operations, 2D operations, motion compensation, overlay, and display control. The GMCH’s video engines support video conferencing and other video applications. The GMCH uses a UMA configuration with DVMT for graphics memory. The GMCH also has the capability to support external graphics accelerators via the PCI Express Graphics (PEG) port but cannot work concurrently with the integrated graphics device. High bandwidth access to data is provided through the system memory port.

### 1.3.6 SDVO and Analog Display Features (Intel® 82G31 GMCH Only)

The GMCH provides interfaces to a progressive scan analog monitor and two SDVO ports. For the GMCH, the SDVO ports are multiplexed with PCI Express x16 graphics port signals. The GMCH supports two multiplexed SDVO ports that each drive pixel clocks up to 225 MHz. The SDVO ports can each support a single-channel SDVO device. If both ports are active in single-channel mode, they can have different display timing and data.

The digital display channels are capable of driving a variety of SDVO devices (e.g., TMDS, TV-Out). Note that SDVO only works with the Integrated Graphics Device (IGD). The GMCH is capable of driving an Advanced Digital Display (ADD2) card or Media Expansion Card. The Media Expansion Card adds video-in capabilities. The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display (e.g., flat panel or digital CRT).

The GMCH is compliant with HDMI specification 1.1. When combined with a HDMI compliant external device and connector, the external HDMI device can support standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.



Capabilities of the SDVO and Analog Display interfaces include:

- SDVO Support
  - SDVO ports in either single modes supported
  - 3x3 Built In full panel scalar
  - 180 degree Hardware screen rotation
  - Multiplexed Digital Display Channels (Supported with ADD2/MEC)
  - Two channels multiplexed with PCI Express\* Graphics port
  - 200 MHz dot clock on each 12-bit interface
  - Supports flat panels up to 1920 x 1200 @ 60 Hz or digital CRT/HDTV at 1400 x1050 @ 85 Hz
  - Supports Hot-Plug and Display
  - Supports TMDS transmitters or TV-out encoders
  - ADD2/Media Expansion card utilizes PCI Express Graphics x16 connector
- Analog Display Support
  - 350 MHz Integrated 24-bit RAMDAC
  - Up to 2048x1536 @ 75 Hz refresh
  - Hardware Color Cursor Support
  - DDC2B Compliant Interface
- Dual Independent Display options with digital display

### 1.3.7 (G)MCH Clocking

- Differential Host clock of 200/266 MHz (HCLKP/HCLKN). Supports transfer rates of 800/1066 MT/s.
- Memory clocks of 333 and 400 MHz generated from (G)MCH PLLs that use the Host clock as a reference.
- The PCI Express\* PLL of 100MHz Serial Reference Clock (GCLKP/GCLKN) generates the PCI Express core clock of 250 MHz
- Display timings are generated from display PLLs that use a 96MHz differential non-spread spectrum clock as a reference. Display PLLs can also use the sDVO\_TVCLKIN[+/-] from an SDVO device as a reference.
- All of the above clocks are capable of tolerating Spread Spectrum clocking.
- Host, Memory, and PCI Express Graphics PLLs and all associated internal clocks are disabled until PWROK is asserted.



### 1.3.8 Power Management

(G)MCH Power Management support includes:

- PC99 suspend to DRAM support ("STR", mapped to ACPI state S3)
- SMRAM space remapping to A0000h (128 KB)
- Supports extended SMRAM space above 256 MB, additional 1 MB TSEG from the Base of graphics stolen memory (BSM) when enabled, and cacheable (cacheability controlled by processor)
- ACPI Rev 1.0b compatible power management
- Supports processor states: C0, C1, and C2
- Supports System states: S0, S1, S3 and S5
- Supports processor Thermal Management 2 (TM2)

### 1.3.9 Thermal Sensor

(G)MCH Thermal Sensor support includes:

- Catastrophic Trip Point support for emergency clock gating for the (G)MCH at 115 °C
- Hot Trip Point support for SMI generation between 85 °C and 105 °C

§



## 2 Signal Description

This chapter provides a detailed description of (G)MCH signals. The signals are arranged in functional groups according to their associated interface.

The following notations are used to describe the signal type:

| Signal Type  | Description  |
|--------------|--|
| PCI Express* | PCI Express interface signals. These signals are compatible with PCI Express 1.1 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = $( D+ - D- ) * 2 = 1.2V_{max}$ . Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.   |
| DMI          | Direct Media Interface signals. These signals are compatible with PCI Express 1.1 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = $( D+ - D- ) * 2 = 1.2V_{max}$ . Single-ended maximum = 1.25 V. Single-ended minimum = 0 V. |
| CMOS         | CMOS buffers. 1.5 V tolerant.  |
| COD          | CMOS Open Drain buffers. 3.3 V tolerant.   |
| HVCMOS       | High Voltage CMOS buffers. 3.3 V tolerant.   |
| HVIN         | High Voltage CMOS input-only buffers. 3.3 V tolerant.  |
| SSTL_1.8     | Stub Series Termination Logic. These are 1.8 V output capable buffers. 1.8 V tolerant.   |
| A            | Analog reference or output. May be used as a threshold voltage or for buffer compensation.   |
| GTL+         | Gunning Transceiver Logic signaling technology. Implements a voltage level as defined by VTT of 1.2V.  |



## 2.1 Host Interface Signals

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (Vtt).

| Signal Name | Type        | Description  |
|-------------|-------------|--|
| HADS#       | I/O<br>GTL+ | <b>Address Strobe:</b> The processor bus owner asserts HADS# to indicate the first of two cycles of a request phase. The (G)MCH can assert this signal for snoop cycles and interrupt messages.  |
| HBNR#       | I/O<br>GTL+ | <b>Block Next Request:</b> Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.   |
| HBPRI#      | O<br>GTL+   | <b>Priority Agent Bus Request:</b> The (G)MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.  |
| HBREQ0#     | I/O<br>GTL+ | <b>Bus Request 0:</b> The (G)MCH pulls the processor's bus HBREQ0# signal low during HCPURST#. The processor samples this signal on the active-to-inactive transition of HCPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs. HBREQ0# should be tristated after the hold time requirement has been satisfied.   |
| HCPURST#    | O<br>GTL+   | <b>CPU Reset:</b> The HCPURST# pin is an output from the (G)MCH. The (G)MCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is de-asserted. The HCPURST# allows the processors to begin execution in a known state.<br><br>Note that the Intel® ICH7 must provide processor frequency select strap set-up and hold times around HCPURST#. This requires strict synchronization between (G)MCH HCPURST# de-assertion and the ICH7 driving the straps. |
| HDBSY#      | I/O<br>GTL+ | <b>Data Bus Busy:</b> Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.   |
| HDEFER#     | O<br>GTL+   | <b>Defer:</b> Signals that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.   |



| Signal Name                  | Type        | Description  |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
|------------------------------|-------------|--|---------|------|------|---------------------------|-----------|------------|---------------------------|-----------|------------|---------------------------|-----------|------------|---------------------------|-----------|-----------|
| HDINV[3:0]#                  | I/O<br>GTL+ | <p><b>Dynamic Bus Inversion:</b> Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8.</p> <p><b>HDINV[x]# Data Bits</b></p> <p>HDINV[3]# HD[63:48]#</p> <p>HDINV[2]# HD[47:32]#</p> <p>HDINV[1]# HD[31:16]#</p> <p>HDINV[0]# HD[15:0]#</p>  |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
| HA[35:3]#                    | I/O<br>GTL+ | <p><b>Host Address Bus:</b> HA[35:3]# connect to the processor address bus. During processor cycles, the HA[35:3]# are inputs. The (G)MCH drives HA[35:3]# during snoop cycles on behalf of DMI and PCI Express* Graphics initiators. HA[35:3]# are transferred at 2x rate.</p>  |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
| HADSTB[1:0]#                 | I/O<br>GTL+ | <p><b>Host Address Strobe:</b> The source synchronous strobes used to transfer HA[35:3]# and HREQ[4:0] at the 2x transfer rate.</p>  |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
| HD[63:0]#                    | I/O<br>GTL+ | <p><b>Host Data:</b> These signals are connected to the processor data bus. Data on HD[63:0] is transferred at 4x rate. Note that the data signals may be inverted on the processor bus, depending on the HDINV[3:0]# signals.</p>   |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
| HDSTBP[3:0]#<br>HDSTBN[3:0]# | I/O<br>GTL+ | <p><b>Differential Host Data Strobes:</b> The differential source synchronous strobes used to transfer HD[63:0]# and HDINV[3:0]# at 4x transfer rate.</p> <p>Named this way because they are not level sensitive. Data is captured on the falling edge of both strobes. Hence, they are pseudo-differential, and not true differential.</p> <table border="1"> <thead> <tr> <th>Strobes</th> <th>Bits</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>HDSTBP[3]#,<br/>HDSTBN[3]#</td> <td>HDINV[3]#</td> <td>HD[63:48]#</td> </tr> <tr> <td>HDSTBP[2]#,<br/>HDSTBN[2]#</td> <td>HDINV[2]#</td> <td>HD[47:32]#</td> </tr> <tr> <td>HDSTBP[1]#,<br/>HDSTBN[1]#</td> <td>HDINV[1]#</td> <td>HD[31:16]#</td> </tr> <tr> <td>HDSTBP[0]#,<br/>HDSTBN[0]#</td> <td>HDINV[0]#</td> <td>HD[15:0]#</td> </tr> </tbody> </table> | Strobes | Bits | Data | HDSTBP[3]#,<br>HDSTBN[3]# | HDINV[3]# | HD[63:48]# | HDSTBP[2]#,<br>HDSTBN[2]# | HDINV[2]# | HD[47:32]# | HDSTBP[1]#,<br>HDSTBN[1]# | HDINV[1]# | HD[31:16]# | HDSTBP[0]#,<br>HDSTBN[0]# | HDINV[0]# | HD[15:0]# |
| Strobes                      | Bits        | Data   |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
| HDSTBP[3]#,<br>HDSTBN[3]#    | HDINV[3]#   | HD[63:48]#   |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
| HDSTBP[2]#,<br>HDSTBN[2]#    | HDINV[2]#   | HD[47:32]#   |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
| HDSTBP[1]#,<br>HDSTBN[1]#    | HDINV[1]#   | HD[31:16]#   |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
| HDSTBP[0]#,<br>HDSTBN[0]#    | HDINV[0]#   | HD[15:0]#  |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
| HHIT#                        | I/O<br>GTL+ | <p><b>Hit:</b> Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HHITM# by the target to extend the snoop window.</p>   |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |
| HHITM#                       | I/O<br>GTL+ | <p><b>Hit Modified:</b> Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HHIT# to extend the snoop window.</p>  |         |      |      |                           |           |            |                           |           |            |                           |           |            |                           |           |           |



| Signal Name | Type                               | Description  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
|-------------|------------------------------------|--|----------|---------------|-----|------------|-----|----------------|-----|-------------------|-----|--------------------------------|-----|------------------------------------|-----|------------------|-----|--------------------|-----|----------------------|
| HTRDY#      | O<br>GTL+                          | <b>Host Target Ready:</b> Indicates that the target of the processor transaction is able to enter the data transfer phase.   |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| HRS[2:0]#   | O<br>GTL+                          | <p><b>Response Signals:</b> Indicates type of response according to the table</p> <table border="1"> <thead> <tr> <th>Encoding</th> <th>Response Type</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Idle state</td> </tr> <tr> <td>001</td> <td>Retry response</td> </tr> <tr> <td>010</td> <td>Deferred response</td> </tr> <tr> <td>011</td> <td>Reserved(not driven by (G)MCH)</td> </tr> <tr> <td>100</td> <td>Hard Failure(not driven by (G)MCH)</td> </tr> <tr> <td>101</td> <td>No data response</td> </tr> <tr> <td>110</td> <td>Implicit Writeback</td> </tr> <tr> <td>111</td> <td>Normal data response</td> </tr> </tbody> </table> | Encoding | Response Type | 000 | Idle state | 001 | Retry response | 010 | Deferred response | 011 | Reserved(not driven by (G)MCH) | 100 | Hard Failure(not driven by (G)MCH) | 101 | No data response | 110 | Implicit Writeback | 111 | Normal data response |
| Encoding    | Response Type                      |  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| 000         | Idle state                         |  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| 001         | Retry response                     |  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| 010         | Deferred response                  |  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| 011         | Reserved(not driven by (G)MCH)     |  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| 100         | Hard Failure(not driven by (G)MCH) |  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| 101         | No data response                   |  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| 110         | Implicit Writeback                 |  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| 111         | Normal data response               |  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| BSEL[2:0]   | I<br>CMOS                          | <b>Bus Speed Select:</b> At the de-assertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus.  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| HRCOMP      | I/O<br>CMOS                        | <b>Host RCOMP:</b> Used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (Vtt).   |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| HSCOMP      | I/O<br>CMOS                        | <b>Slew Rate Compensation:</b> Compensation for the Host Interface   |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| HSCOMP#     | I/O<br>A                           | <b>Slew Rate Compensation:</b> Compensation for the Host Interface for falling edges   |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| HSWING      | I<br>A                             | <b>Host Voltage Swing:</b> This signal provides the reference voltage used by FSB RCOMP circuits. HSWING is used for the signals handled by HRCOMP.  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| HDRVREF     | I<br>A                             | <b>Host Reference Voltage:</b> Voltage input for the Data signals of the Host GTL interface.   |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |
| HACCVREF    | I<br>A                             | <b>Host Reference Voltage:</b> Voltage input for the Address signals of the Host GTL interface.  |          |               |     |            |     |                |     |                   |     |                                |     |                                    |     |                  |     |                    |     |                      |



## 2.2 System Memory (DDR2) Interface Signals

### 2.2.1 System Memory Channel A Interface Signals

| Signal Name  | Type            | Description   |
|--------------|-----------------|---|
| SCLK_A[2:0]  | O<br>SSTL-1.8   | <b>SDRAM Differential Clock:</b> (3 per DIMM), SCLK_A and its complement, SCLK_A# make a differential clock pair output. The crossing of the positive edge of SCLK_A and the negative edge of its complement SCLK_A# are used to sample the command and control signals on the SDRAM. |
| SCLK_A[2:0]# | O<br>SSTL-1.8   | <b>SDRAM Complementary Differential Clock:</b> (3 per DIMM) These are the complementary differential DDR2 Clock signals.  |
| SCS_A[1:0]#  | O<br>SSTL-1.8   | <b>Chip Select:</b> (1 per Rank) These signals select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.  |
| SMA_A[14:0]  | O<br>SSTL-1.8   | <b>Memory Address:</b> These signals are used to provide the multiplexed row and column address to the SDRAM.   |
| SBS_A[2:0]   | O<br>SSTL-1.8   | <b>Bank Select:</b> These signals define which banks are selected within each SDRAM rank.<br><br>DDR2: 1-Gb technology uses 8 banks.  |
| SRAS_A#      | O<br>SSTL-1.8   | <b>Row Address Strobe:</b> Used with SCAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.   |
| SCAS_A#      | O<br>SSTL-1.8   | <b>Column Address Strobe:</b> Used with SRAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.  |
| SWE_A#       | O<br>SSTL-1.8   | <b>Write Enable:</b> Used with SCAS_A# and SRAS_A# (along with SCS_A#) to define the SDRAM commands.  |
| SDQ_A[63:0]  | I/O<br>SSTL-1.8 | <b>Data Lines:</b> SDQ_A signals interface to the SDRAM data bus.   |
| SDM_A[7:0]   | O<br>SSTL-1.8   | <b>Data Mask:</b> When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_A bit for every data byte lane.   |
| SDQS_A[7:0]  | I/O<br>SSTL-1.8 | <b>Data Strobes:</b> For DDR2, SDQS_A, and its complement SDQS_A# make up a differential strobe pair. The data is captured at the crossing point of SDQS_A and its complement SDQS_A# during read and write transactions.   |
| SDQS_A[7:0]# | I/O<br>SSTL-1.8 | <b>Data Strobe Complements:</b> These are the complementary DDR2 strobe signals.  |
| SCKE_A[1:0]  | O<br>SSTL-1.8   | <b>Clock Enable:</b> (1 per Rank) SCKE_A is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.  |
| SODT_A[1:0]  | O<br>SSTL-1.8   | <b>On Die Termination:</b> Active On-die Termination Control signals for DDR2 devices.  |



### 2.2.2 System Memory Channel B Interface Signals

| Signal Name  | Type            | Description   |
|--------------|-----------------|---|
| SCLK_B[2:0]  | O<br>SSTL-1.8   | <b>SDRAM Differential Clock:</b> (3 per DIMM) SCLK_B and its complement, SCLK_B#, make a differential clock pair output. The crossing of the positive edge of SCLK_B and the negative edge of its complement SCLK_B# are used to sample the command and control signals on the SDRAM. |
| SCLK_B[2:0]# | O<br>SSTL-1.8   | <b>SDRAM Complementary Differential Clock:</b> (3 per DIMM) These are the complementary differential DDR2 Clock signals.  |
| SCS_B[1:0]#  | O<br>SSTL-1.8   | <b>Chip Select:</b> (1 per Rank) These signals select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank   |
| SMA_B[14:0]  | O<br>SSTL-1.8   | <b>Memory Address:</b> These signals are used to provide the multiplexed row and column address to the SDRAM.   |
| SBS_B[2:0]   | O<br>SSTL-1.8   | <b>Bank Select:</b> These signals define which banks are selected within each SDRAM rank<br><br>DDR2: 1-Gb technology uses 8 banks.   |
| SRAS_B#      | O<br>SSTL-1.8   | <b>Row Address Strobe:</b> Used with SCAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands  |
| SCAS_B#      | O<br>SSTL-1.8   | <b>Column Address Strobe:</b> Used with SRAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.  |
| SWE_B#       | O<br>SSTL-1.8   | <b>Write Enable:</b> Used with SCAS_B# and SRAS_B# (along with SCS_B#) to define the SDRAM commands.  |
| SDQ_B[63:0]  | I/O<br>SSTL-1.8 | <b>Data Lines:</b> SDQ_B signals interface to the SDRAM data bus.   |
| SDM_B[7:0]   | O<br>SSTL-1.8   | <b>Data Mask:</b> When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SBDM for every data byte lane.  |
| SDQS_B[7:0]  | I/O<br>SSTL-1.8 | <b>Data Strobes:</b> For DDR2, SDQS_B, and its complement ,SDQS_B#, make up a differential strobe pair. The data is captured at the crossing point of SDQS_B and its complement SDQS_B# during read and write transactions.   |
| SDQS_B[7:0]# | I/O<br>SSTL-1.8 | <b>Data Strobe Complements:</b> These are the complementary DDR2 strobe signals.  |
| SCKE_B[1:0]  | O<br>SSTL-1.8   | <b>Clock Enable:</b> (1 per Rank) SCKE_B is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.  |
| SODT_B[1:0]  | O<br>SSTL-1.8   | <b>On Die Termination:</b> Active On-die Termination Control signals for DDR2 devices.  |



### 2.2.3 DDR2 DRAM Reference and Compensation Signals

| Signal Name | Type   | Description  |
|-------------|--------|--|
| SRCOMP[3:0] | I<br>A | <b>System Memory RCOMP</b>   |
| SVREF       | I<br>A | <b>SDRAM Reference Voltage:</b> Reference voltage input for DQ, DQS, and DQS# input signals. |
| SMRCOMPVOL  | I<br>A | <b>System Memory RCOMP reference</b>   |
| SMRCOMPVOH  | I<br>A | <b>System Memory RCOMP reference</b>   |

### 2.3 PCI Express\* Interface Signals

| Signal Name                    | Type                 | Description  |
|--------------------------------|----------------------|--|
| EXP_RXN[15:0]<br>EXP_RXP[15:0] | I<br>PCI<br>EXPRESS* | <b>PCI Express* Receive Differential Pair (RX)</b>           |
| EXP_TXN[15:0]<br>EXP_TXP[15:0] | O<br>PCI<br>EXPRESS* | <b>PCI Express* Graphics Transmit Differential Pair (TX)</b> |
| EXP_COMPO                      | I<br>A               | <b>PCI Express* Graphics Output Current Compensation</b>     |
| EXP_COMPI                      | I<br>A               | <b>PCI Express* Graphics Input Current Compensation</b>      |



## 2.4 Analog Display Signals (Intel® 82G31 GMCH Only)

| Signal Name | Type                | Description  |
|-------------|---------------------|--|
| RED         | O<br>A              | <b>RED Analog Video Output:</b> This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 75 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).   |
| RED#        | O<br>A              | <b>RED# Analog Output:</b> This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.  |
| GREEN       | O<br>A              | <b>GREEN Analog Video Output:</b> This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 75 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load). |
| GREEN#      | O<br>A              | <b>GREEN# Analog Output:</b> This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.  |
| BLUE        | O<br>A              | <b>BLUE Analog Video Output:</b> This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 75 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).  |
| BLUE#       | O<br>A              | <b>BLUE# Analog Output:</b> This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.   |
| REFSET      | O<br>A              | <b>Resistor Set:</b> Set point resistor for the internal color palette DAC. A 255 ohm 1% resistor is required between REFSET and motherboard ground.   |
| HSYNC       | O<br>3.3V<br>CMOS   | <b>CRT Horizontal Synchronization:</b> This signal is used as the horizontal sync (polarity is programmable) or "sync interval", 3.3 V output  |
| VSYNC       | O<br>3.3V<br>CMOS   | <b>CRT Vertical Synchronization:</b> This signal is used as the vertical sync (polarity is programmable) 3.3V output.  |
| DDC_CLK     | I/O<br>3.3V<br>CMOS | <b>Monitor Control Clock</b>   |
| DDC_DATA    | I/O<br>3.3V<br>CMOS | <b>Monitor Control Data</b>  |



## 2.5 Clocks, Reset, and Miscellaneous

| Signal Name             | Type        | Description  |
|-------------------------|-------------|--|
| HCLKP<br>HCLKN          | I<br>HCSL   | <b>Differential Host Clock In:</b> These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the (G)MCH logic that is in the Host clock domain. Memory domain clocks are also derived from this source.   |
| GCLKP<br>GCLKN          | I<br>HCSL   | <b>Differential PCI Express* Graphics Clock In:</b> These pins receive a differential 100 MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.  |
| DREFCLKN<br>DREFCLKP    | I<br>HCSL   | <b>Display PLL Differential Clock In</b>   |
| RSTIN#                  | I<br>HVIN   | <b>Reset In:</b> When asserted, this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PCIRST# output of the Intel® ICH7. All PCI Express Graphics Attach output signals will also tri-state compliant to <i>PCI Express* Specification Rev 1.1</i> .<br><br>This input should have a Schmitt trigger to avoid spurious resets.<br><br>This signal is required to be 3.3V tolerant. |
| EXP_SLR                 | I<br>CMOS   | <b>PCI Express* Static Lane Reversal/Form Factor Selection:</b> (G)MCH's PCI Express lane numbers are reversed to differentiate BTX and ATX form factors<br>0 = (G)MCH PCI Express lane numbers are reversed (BTX)<br>1 = Normal operation (ATX)   |
| BSEL2<br>BSEL1<br>BSEL0 | I<br>HCSL   | <b>Bus Speed Select:</b> At the assertion of PWROK, the value sampled on these pins determines the expected frequency of the bus. These pins must also be routed to probe points or to the XDP connector when applicable   |
| EXP_EN                  | I<br>GTL+   | <b>Concurrent PCI Express Port Enable:</b> Concurrent SDVO and PCI Express<br>0 = Only SDVO or PCI Express is operational.<br>1 = Both SDVO and PCI Express are operating simultaneously via the PCI Express port.<br><br><b>NOTE:</b> For the 82P31 MCH, this signal should be connected to ground.   |
| PWROK                   | I/O<br>SSTL | <b>Power OK:</b> When asserted, PWROK is an indication to the (G)MCH that core power has been stable for at least 10 us.   |
| ICH_SYNC#               | O<br>HVCMOS | Maintains synchronization between (G)MCH and ICH   |



| Signal Name          | Type            | Description  |                 |  |
|----------------------|-----------------|--|-----------------|--|
| ALLZTEST/<br>XORTEST | I/O<br><br>GTL+ | <b>XORTEST</b>   | <b>ALLZTEST</b> | <b>Description</b>   |
|                      |                 | 0  | 0               | Intel Reserved   |
|                      |                 | 0  | 1               | XOR Chain. Used for Chipset Bed of Nails testing to execute XOR Chain Test |
|                      |                 | 1  | 0               | All pins tristated. Used for chipset testing                               |
| 1                    | 1               | Normal   |                 |  |
| TEST[2:0]            | I/O<br><br>A    | <b>In Circuit Test:</b> These pins should be connected to test points on the motherboard. They are internally shorted to the package ground and can be used to determine if the corner balls on the (G)MCH are correctly soldered down to the motherboard.<br>These pins should NOT connect to ground on the motherboard. If TEST[2:0] are not going to be used, they should be left as no connects. |                 |  |

## 2.6 Direct Media Interface

| Signal Name                | Type     | Description  |
|----------------------------|----------|--|
| DMI_RXP_3:0<br>DMI_RXN_3:0 | I<br>DMI | <b>Direct Media Interface:</b> Receive differential pair (RX). MCH-ICH serial interface input.   |
| DMI_TXP_3:0<br>DMI_TXN_3:0 | O<br>DMI | <b>Direct Media Interface:</b> Transmit differential pair (TX). MCH-ICH serial interface output. |

## 2.7 Serial DVO Interface (Intel® 82G31 GMCH Only)

All but two of the pins in this section are multiplexed with the PCI Express interface. sDVO is mapped to lanes 0-7 or lanes 15-8 of the PEG port depending on the PCI Express Static Lane Reversal and sDVO/PCI Express Coexistence straps. The lower 8 lanes are used when **both** straps are either asserted or not asserted. Otherwise, the upper 8 lanes are used.

| Signal Name | Type      | Description  |
|-------------|-----------|--|
| SDVOB_CLKN  | O<br>PCIE | <b>Serial Digital Video Channel B Clock Complement</b> |
| SDVOB_CLKP  | O<br>PCIE | <b>Serial Digital Video Channel B Clock</b>            |
| SDVOB_RED#  | O<br>PCIE | <b>Serial Digital Video Channel C Red Complement</b>   |



| Signal Name   | Type      | Description  |
|---------------|-----------|--|
| SDVOB_RED     | O<br>PCIE | <b>Serial Digital Video Channel C Red</b>                          |
| SDVOB_GREEN#  | O<br>PCIE | <b>Serial Digital Video Channel B Green Complement</b>             |
| SDVOB_GREEN   | O<br>PCIE | <b>Serial Digital Video Channel B Green</b>                        |
| SDVOB_BLUE#   | O<br>PCIE | <b>Serial Digital Video Channel B Blue Complement</b>              |
| SDVOB_BLUE    | O<br>PCIE | <b>Serial Digital Video Channel B Blue</b>                         |
| SDVOC_RED#    | O<br>PCIE | <b>Serial Digital Video Channel C Red Complement</b>               |
| SDVOC_RED     | O<br>PCIE | <b>Serial Digital Video Channel C Red Channel B Alpha</b>          |
| SDVOC_GREEN#  | O<br>PCIE | <b>Serial Digital Video Channel C Green Complement</b>             |
| SDVOC_GREEN   | O<br>PCIE | <b>Serial Digital Video Channel C Green</b>                        |
| SDVOC_BLUE#   | O<br>PCIE | <b>Serial Digital Video Channel C Blue Complement</b>              |
| SDVOC_BLUE    | O<br>PCIE | <b>Serial Digital Video Channel C Blue</b>                         |
| SDVOC_CLKN    | O<br>PCIE | <b>Serial Digital Video Channel C Clock Complement</b>             |
| SDVOC_CLKP    | O<br>PCIE | <b>Serial Digital Video Channel C Clock</b>                        |
| SDVO_TVCLKIN# | I<br>PCIE | <b>Serial Digital Video TVOUT Synchronization Clock Complement</b> |
| SDVO_TVCLKIN  | I<br>PCIE | <b>Serial Digital Video TVOUT Synchronization Clock</b>            |
| SDVOB_INT#    | I<br>PCIE | <b>Serial Digital Video Input Interrupt Complement</b>             |
| SDVOB_INT     | I<br>PCIE | <b>Serial Digital Video Input Interrupt</b>                        |



| Signal Name    | Type       | Description                                     |
|----------------|------------|---|
| SDVOC_INT#     | I<br>PCIE  | Serial Digital Video Input Interrupt Complement |
| SDVOC_INT      | I<br>PCIE  | Serial Digital Video Input Interrupt            |
| SDVO_FLDSTALL# | I<br>PCIE  | Serial Digital Video Field Stall Complement.    |
| SDVO_FLDSTALL  | I<br>PCIE  | Serial Digital Video Field Stall                |
| SDVO_CTRLCLK   | I/O<br>COD | Serial Digital Video Device Control Clock       |
| SDVO_CTRLDATA  | I/O<br>COD | Serial Digital Video Device Control Data        |

### 2.7.1 SDVO/PCI Express\* Signal Mapping

| sDVO Signal  | Configuration-wise Mapping |                      |   |   |
|--------------|----------------------------|----------------------|---|---|
|              | sDVO Only – Normal         | sDVO Only – Reversed | Concurrent sDVO and PCI Express* – Normal | Concurrent sDVO and PCI Express* – Reversed |
| SDVOB_RED#   | EXP_TXN0                   | EXP_TXN15            | EXP_TXN15                                 | EXP_TXN0                                    |
| SDVOB_RED    | EXP_TXP0                   | EXP_TXP15            | EXP_TXP15                                 | EXP_TXP0                                    |
| SDVOB_GREEN# | EXP_TXN1                   | EXP_TXN14            | EXP_TXN14                                 | EXP_TXN1                                    |
| SDVOB_GREEN  | EXP_TXP1                   | EXP_TXP14            | EXP_TXP14                                 | EXP_TXP1                                    |
| SDVOB_BLUE#  | EXP_TXN2                   | EXP_TXN13            | EXP_TXN13                                 | EXP_TXN2                                    |
| SDVOB_BLUE   | EXP_TXP2                   | EXP_TXP13            | EXP_TXP13                                 | EXP_TXP2                                    |
| SDVOB_CLKN   | EXP_TXN3                   | EXP_TXN12            | EXP_TXN12                                 | EXP_TXN3                                    |
| SDVOB_CLKP   | EXP_TXP3                   | EXP_TXP12            | EXP_TXP12                                 | EXP_TXP3                                    |
| SDVOC_RED#   | EXP_TXN4                   | EXP_TXN11            | EXP_TXN11                                 | EXP_TXN4                                    |
| SDVOC_RED    | EXP_TXP4                   | EXP_TXP11            | EXP_TXP11                                 | EXP_TXP4                                    |
| SDVOC_GREEN# | EXP_TXN5                   | EXP_TXN10            | EXP_TXN10                                 | EXP_TXN5                                    |
| SDVOC_GREEN  | EXP_TXP5                   | EXP_TXP10            | EXP_TXP10                                 | EXP_TXP5                                    |
| SDVOC_BLUE#  | EXP_TXN6                   | EXP_TXN9             | EXP_TXN9                                  | EXP_TXN6                                    |
| SDVOC_BLUE   | EXP_TXP6                   | EXP_TXP9             | EXP_TXP9                                  | EXP_TXP6                                    |
| SDVOC_CLKN   | EXP_TXN7                   | EXP_TXN8             | EXP_TXN8                                  | EXP_TXN7                                    |
| SDVOC_CLKP   | EXP_TXP7                   | EXP_TXP8             | EXP_TXP8                                  | EXP_TXP7                                    |



| sDVO Signal    | Configuration-wise Mapping |                      |   |   |
|----------------|----------------------------|----------------------|---|---|
|                | sDVO Only – Normal         | sDVO Only – Reversed | Concurrent sDVO and PCI Express* – Normal | Concurrent sDVO and PCI Express* – Reversed |
| SDVO_TVCLKIN#  | EXP_RXN0                   | EXP_RXN15            | EXP_RXN15                                 | EXP_RXN0                                    |
| SDVO_TVCLKIN   | EXP_RXP0                   | EXP_RXP15            | EXP_RXP15                                 | EXP_RXP0                                    |
| SDVOB_INT#     | EXP_RXN1                   | EXP_RXN14            | EXP_RXN14                                 | EXP_RXN1                                    |
| SDVOB_INT      | EXP_RXP1                   | EXP_RXP14            | EXP_RXP14                                 | EXP_RXP1                                    |
| SDVOC_INT#     | EXP_RXN5                   | EXP_RXN10            | EXP_RXN10                                 | EXP_RXN5                                    |
| SDVOC_INT      | EXP_RXP5                   | EXP_RXP10            | EXP_RXP10                                 | EXP_RXP5                                    |
| SDVO_FLDSTALL# | EXP_RXN2                   | EXP_RXN13            | EXP_RXN13                                 | EXP_RXN2                                    |
| SDVO_FLDSTALL  | EXP_RXP2                   | EXP_RXP13            | EXP_RXP13                                 | EXP_RXP2                                    |

## 2.8 Power and Ground

| Name       | Voltage     | Description                    |
|------------|-------------|--------------------------------|
| VCC        | 1.25 V      | Core Power                     |
| VTT        | 1.05V/1.2 V | Processor System Bus Power     |
| VCC_EXP    | 1.25 V      | PCI Express* and DMI Power     |
| VCCSM      | 1.8V        | System Memory Power            |
| VCC_SMCLK  | 1.8V        | System Clock Memory Power      |
| VCC3_3     | 3.3 V       | 3.3 V CMOS Power               |
| VCCA_EXP   | 1.25 V      | PCI Express PLL Analog Power   |
| VCCA_DPLLA | 1.25 V      | Display PLL A Analog Power     |
| VCCA_DPLLB | 1.25 V      | Display PLL B Analog Power     |
| VCCA_HPLL  | 1.25 V      | Host PLL Analog Power          |
| VCCA_MPLL  | 1.25 V      | System Memory PLL Analog Power |
| VCCA_DAC   | 3.3 V       | Display DAC Analog Power       |
| VCCD_CRT   | 1.5/1.8 V   | Display Digital Supply Power   |
| VSS        | 0 V         | Ground                         |





## 3 System Address Map

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The (G)MCH supports 64 GB (36 bit) of host address space and 64 KB+3 of addressable I/O space. There is a programmable memory address space under the 1 MB region which is divided into regions which can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only. Attribute programming is described in the Register Description section. This section focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has simpler mapping and is explained near the end of this section.

**Note:** Address mapping information for the Integrated Graphics Device applies to the 82G31 GMCH only. The 82P31 MCH does not have an IGD.

The (G)MCH supports PEG port upper pre-fetchable base/limit registers. This allows the PEG unit to claim IO accesses above 36 bit, complying with the PCI Express Specification. Addressing of greater than 4 GB is allowed on either the DMI Interface or PCI Express interface. The (G)MCH supports a maximum of 4 GB of DRAM. No DRAM memory will be accessible above 4 GB.

When running in internal graphics mode, writes to GMADR range linear range are supported. Write accesses to linear regions are supported from DMI only. Write accesses to tileX and tileY regions (defined via fence registers) are not supported from DMI or the PEG port. GMADR read accesses are not supported from either DMI or PEG.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI Interface. The exception to this rule is VGA ranges, which may be mapped to PCI-Express, DMI, or to the internal graphics device (IGD). In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI Interface/PCI, while cycle descriptions referencing PCI Express or IGD are related to the PCI Express bus or the internal graphics device respectively. The (G)MCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS. The reclaim base/reclaim limit registers remap logical accesses bound for addresses above 4 GB onto physical addresses that fall within DRAM.



The Address Map includes a number of programmable ranges:

- 1. Device 0
  - PXPEPBAR – Express port registers. Necessary for setting up VC1 as an isochronous channel using time based weighted round robin arbitration. (4 KB window)
  - MCHBAR – Memory mapped range for internal (G)MCH registers. For example, memory buffer register controls. (16 KB window)
  - PCIEXBAR – Flat memory-mapped address spaced to access device configuration registers. This mechanism can be used to access PCI configuration space (0–FFh) and Extended configuration space (100h–FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (64 MB, 128 MB, or 256 MB window).
  - DMIBAR – This window is used to access registers associated with the Direct Media Interface (DMI) register memory range. (4 KB window)
  - GGCGMS (82G31 GMCH only) – GMCH graphics control register, Graphics Mode Select. Used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes. (0-256 MB options).
  - GGCGMS (82G31 GMCH only) – GMCH graphics control register, GTT Graphics Memory Size. GGCGMS is used to select the amount of main memory that is pre-allocated to support the Internal Graphics Translation Table. (0-2 MB options).
- Device 1
  - MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.
  - PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window.
  - PMUBASE/PMULIMIT – PCI Express port upper prefetchable memory access window
  - IOBASE1/IOLIMIT1 – PCI Express port IO access window.
- Device 2, Function 0 (82G31 GMCH only)
  - MMADR – IGD registers and internal graphics instruction port. (512 KB window)
  - IOBAR – IO access window for internal graphics. Though this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed. Note, this allows accessing the same registers as MMADR. In addition, the IOBAR can be used to issue writes to the GTTADR table.
  - GMADR – Internal graphics translation window. (128 MB, 256 MB or 512 MB window).
  - GTTADR – Internal graphics translation table location. (1 MB window). Note that the Base of GTT stolen Memory register (Device 0 A8) indicates the physical address base which is 1 MB aligned.
- Device 2, Function 1 (82G31 GMCH only)
  - MMADR – Function 1 IGD registers and internal graphics instruction port. (512 KB window)

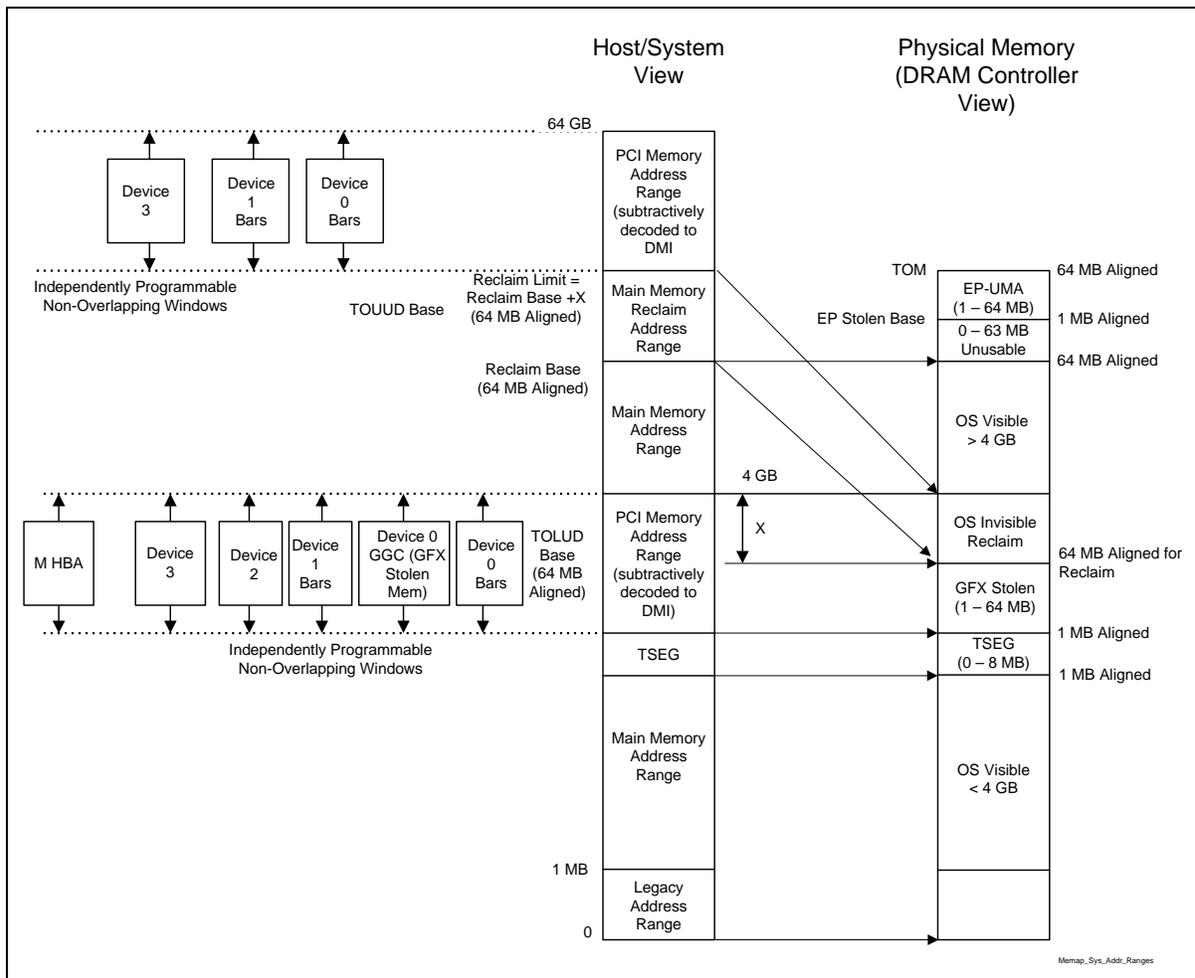


The rules for the above programmable ranges are:

1. ALL of these ranges MUST be unique and NON-OVERLAPPING. It is the BIOS or system designers' responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.
2. There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
3. Accesses to overlapped ranges may produce indeterminate results.
4. The only peer-to-peer cycles allowed below the top of Low Usable memory (register TOLUD) are DMI Interface to PCI Express VGA range writes. Note that peer to peer cycles to the Internal Graphics VGA range are not supported.

Figure 3-1 represents the system memory address map in a simplified form.

Figure 3-1. System Address Ranges



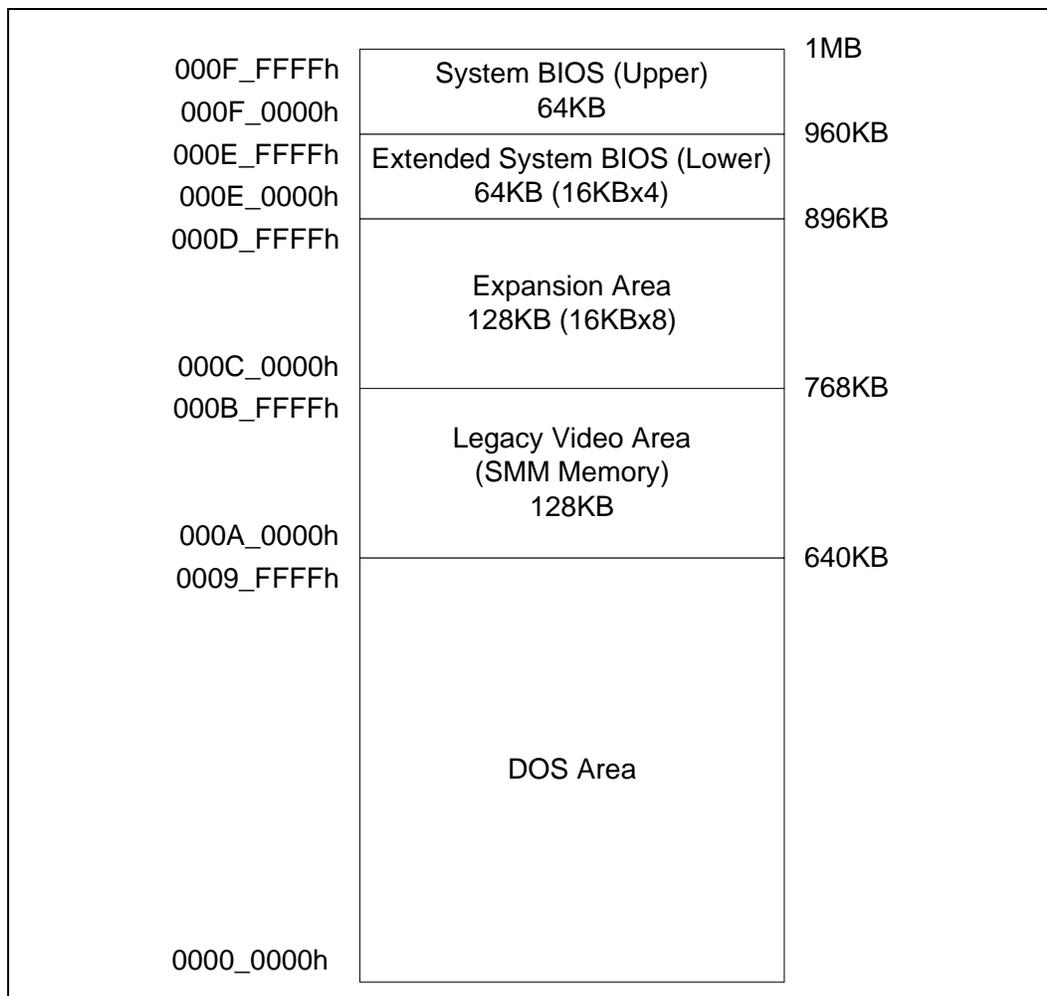


### 3.1 Legacy Address Range

This area is divided into the following address regions:

- 0 – 640 KB – DOS Area
- 640 – 768 KB – Legacy Video Buffer Area
- 768 – 896 KB in 16 KB sections (total of 8 sections) – Expansion Area
- 896 – 960 KB in 16 KB sections (total of 4 sections) – Extended System BIOS Area
- 960 KB – 1 MB Memory – System BIOS Area

Figure 3-2. DOS Legacy Address Range





### 3.1.1 DOS Range (0h – 9\_FFFFh)

The DOS area is 640 KB (0000\_0000h – 0009\_FFFFh) in size and is always mapped to the main memory controlled by the (G)MCH.

### 3.1.2 Legacy Video Area (A\_0000h-B\_FFFFh)

The legacy 128KB VGA memory range, frame buffer, (000A\_0000h – 000B\_FFFFh) can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI Interface. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. Based on the VGA steering bits, priority for VGA mapping is constant. The (G)MCH always decodes internally mapped devices first. Internal to the (G)MCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD (82G31 GMCH only) and PCI-Express. Subsequent decoding of regions mapped to PCI Express or the DMI Interface depends on the Legacy VGA configuration bits (VGA Enable & MDAP). This region is also the default for SMM space.

#### Compatible SMRAM Address Range (A\_0000h-B\_FFFFh)

When compatible SMM space is enabled, SMM-mode processor accesses to this range are routed to physical system DRAM at 000A 0000h – 000B FFFFh. Non-SMM-mode processor accesses to this range are considered to be to the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed and are considered to be to the Video Buffer Area, if IGD on the 82G31 GMCH is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as Peer cycles, and will master abort on PCI if no external VGA device claims them.

#### Monochrome Adapter (MDA) Range (B\_0000h-B\_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, PCI Express, or the DMI Interface (depending on configuration bits). Since the monochrome adapter may be mapped to anyone of these devices, the (G)MCH must decode cycles in the MDA range (000B\_0000h - 000B\_7FFFh) and forward either to IGD, PCI Express, or the DMI Interface. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the (G)MCH decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either IGD, PCI-Express, and/or the DMI Interface.

#### PEG 16-bit VGA Decode

The *PCI to PCI Bridge Architecture Specification Revision 1.2*, it is required that 16-bit VGA decode be a feature.



### 3.1.3 Expansion Area (C\_0000h-D\_FFFFh)

This 128 KB ISA Expansion region (000C\_0000h – 000D\_FFFFh) is divided into eight 16 KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through (G)MCH and are subtractive decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

**Table 3-1. Expansion Area Memory Segments**

| Memory Segments   | Attributes | Comments    |
|-------------------|------------|-------------|
| 0C0000h – 0C3FFFh | WE RE      | Add-on BIOS |
| 0C4000h – 0C7FFFh | WE RE      | Add-on BIOS |
| 0C8000h – 0CBFFFh | WE RE      | Add-on BIOS |
| 0CC000h – 0CFFFFh | WE RE      | Add-on BIOS |
| 0D0000h – 0D3FFFh | WE RE      | Add-on BIOS |
| 0D4000h – 0D7FFFh | WE RE      | Add-on BIOS |
| 0D8000h – 0DBFFFh | WE RE      | Add-on BIOS |
| 0DC000h – 0DFFFFh | WE RE      | Add-on BIOS |



### 3.1.4 Extended System BIOS Area (E\_0000h-E\_FFFFh)

This 64 KB area (000E\_0000h – 000E\_FFFFh) is divided into four 16 KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to DMI Interface. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

**Table 3-2. Extended System BIOS Area Memory Segments**

| Memory Segments   | Attributes | Comments       |
|-------------------|------------|----------------|
| 0E0000h – 0E3FFFh | WE RE      | BIOS Extension |
| 0E4000h – 0E7FFFh | WE RE      | BIOS Extension |
| 0E8000h – 0EBFFFh | WE RE      | BIOS Extension |
| 0EC000h – 0EFFFFh | WE RE      | BIOS Extension |

### 3.1.5 System BIOS Area (F\_0000h-F\_FFFFh)

This area is a single 64 KB segment (000F\_0000h – 000F\_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to DMI Interface. By manipulating the Read/Write attributes, the (G)MCH can “shadow” BIOS into the main DRAM. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

**Table 3-3. System BIOS Area Memory Segments**

| Memory Segments    | Attributes | Comments  |
|--------------------|------------|-----------|
| 0F0000h – 0FFFFFFh | WE RE      | BIOS Area |

### 3.1.6 PAM Memory Area Details

The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM Memory Area.

The (G)MCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there will normally not be IWB cycles targeting DMI. However, DMI becomes the default target for processor and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RD it is possible to get IWB cycles targeting DMI. This may occur for processor originated cycles and for DMI originated cycles to disabled PAM regions.



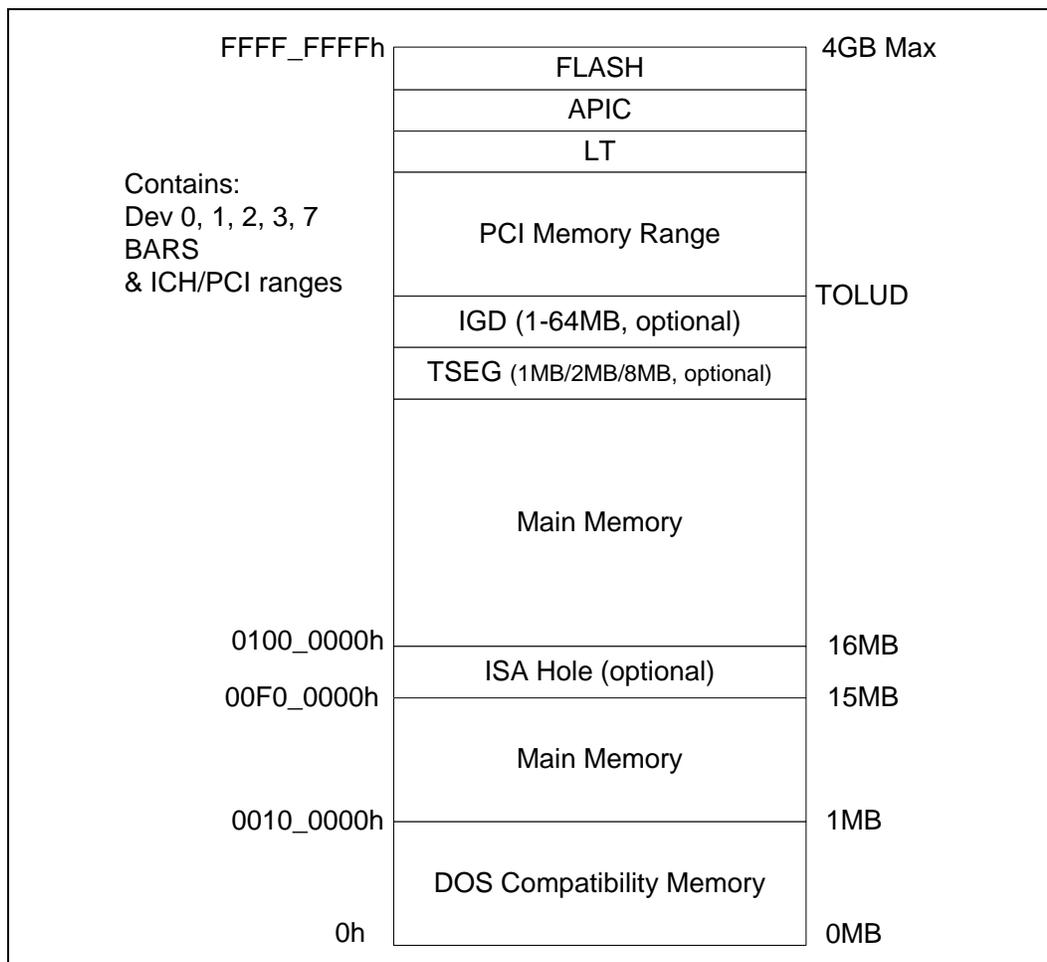
For example, say that a particular PAM region is set for “Read Disabled” and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is “Read Disabled” the default target for the Memory Read becomes DMI. The IWB associated with this cycle will cause the (G)MCH to hang.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

### 3.2 Main Memory Address Range (1MB – TOLUD)

This address range extends from 1 MB to the top of Low Usable physical memory that is permitted to be accessible by the (G)MCH (as programmed in the TOLUD register). All accesses to addresses within this range will be forwarded by the (G)MCH to the DRAM unless it falls into the optional TSEG, optional ISA Hole, or optional IGD stolen VGA memory.

Figure 3-3. Main Memory Address Range





### 3.2.1 ISA Hole (15 MB-16 MB)

A hole can be created at 15 MB–16 MB as controlled by the fixed hole enable in Device 0 space. Accesses within this hole are forwarded to the DMI Interface. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15 MB–16 MB hole is an optionally enabled ISA hole.

Video accelerators originally used this hole. It is also used by validation and customer SV teams for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15 MB–16 MB window.

### 3.2.2 TSEG

TSEG is optionally 1 MB, 2 MB, or 8 MB in size. TSEG is below IGD stolen memory, which is at the top of Low Usable physical memory (TOLUD). SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-processor originated accesses are not allowed to SMM space. PCI Express, DMI, and Internal Graphics originated cycle to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, processor accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses. Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. When SMM is enabled, the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register which is fixed at 1 MB, 2 MB or 8 MB.

### 3.2.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode, legacy VGA graphics compatibility, and graphics GTT stolen memory. **It is the responsibility of BIOS to properly initialize these regions.** Table 3-4 details the location and attributes of the regions. Enabling/Disabling these ranges are described in the (G)MCH Control Register Device 0 (GCC).

**Table 3-4. Pre-allocated Memory Example for 64 MB DRAM, 1 MB VGA, 1 MB GTT stolen and 1 MB TSEG**

| Memory Segments         | Attributes                      | Comments  |
|-------------------------|---------------------------------|---|
| 0000_0000h – 03CF_FFFFh | R/W                             | Available System Memory 61 MB   |
| 03D0_0000h – 03DF_FFFFh | SMM Mode Only - Processor Reads | TSEG Address Range and Pre-allocated Memory   |
| 03E0_0000h – 03EF_FFFFh | R/W                             | Pre-allocated Graphics VGA memory.<br>1MB (or 4/8/16/32/64/128/256 MB) when IGD is enabled. |
| 03F0_0000h – 03FF_FFFFh | R/W                             | Pre-allocated Graphics GTT stolen memory.<br>1 MB (or 2 MB) when IGD is enabled.            |

**NOTES:**

- References to IDG and graphics STOLEN memory is only for the 82G31 GMCH.



### 3.3 PCI Memory Address Range (TOLUD – 4 GB)

This address range, from the top of low usable DRAM (TOLUD) to 4 GB is normally mapped to the DMI Interface.

Device 0 exceptions are:

- Addresses decoded to the Express port registers (PXPEPBAR)
- Addresses decoded to the memory mapped range for internal (G)MCH registers (MCHBAR)
- Addresses decoded to the flat memory-mapped address spaced to access device configuration registers (PCIEXBAR)
- Addresses decoded to the registers associated with the Direct Media Interface (DMI) register memory range. (DMIBAR)

With PCI Express port, there are two exceptions to this rule:

- Addresses decoded to the PCI Express Memory Window defined by the MBASE1, MLIMIT1, registers are mapped to PCI Express.
- Addresses decoded to the PCI Express prefetchable Memory Window defined by the PMBASE1, PMLIMIT1, registers are mapped to PCI Express.

In integrated graphics configurations, there are exceptions to this rule:

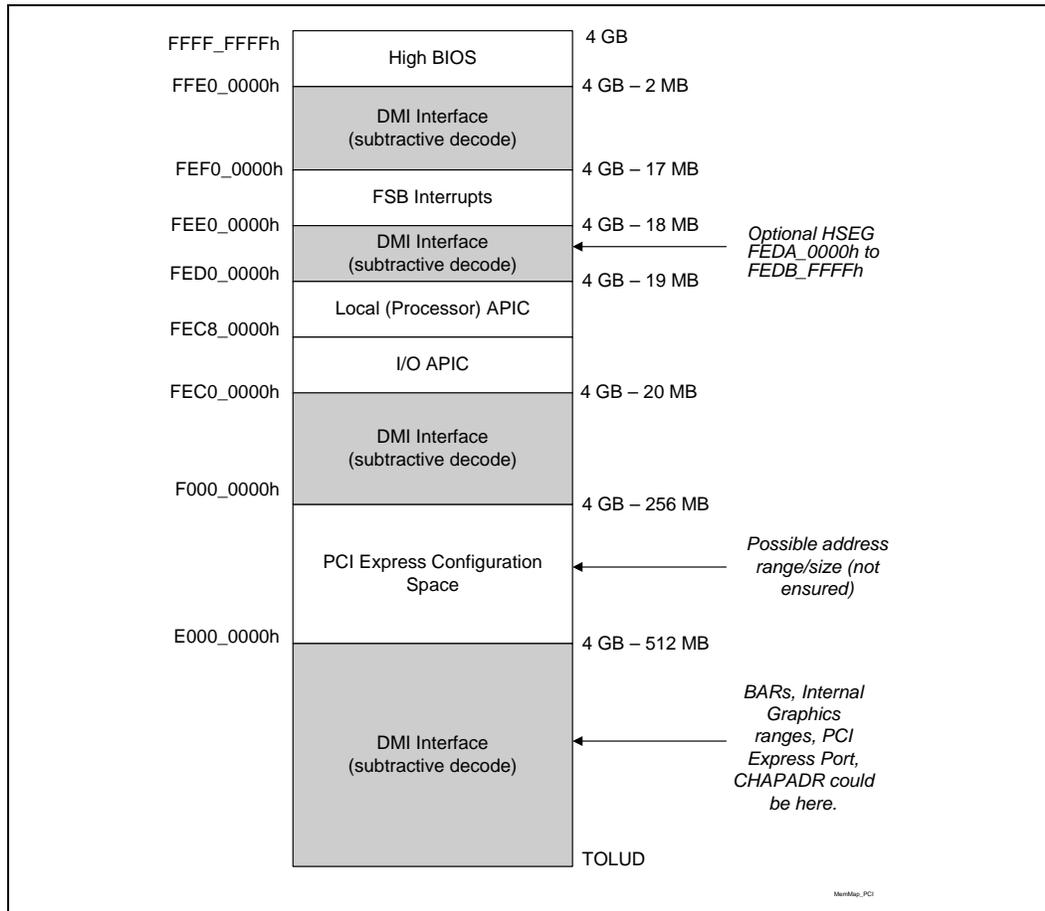
- Addresses decoded to the IGD registers and internal graphics instruction port (Function 0 MMADR, Function 1 MMADR)
- Addresses decode to the internal graphics translation window (GMADR)
- Addresses decode to the Internal graphics translation table (GTTADR)

Some of the MMIO Bars may be mapped to this range or to the range above TOLUD.

There are sub-ranges within the PCI Memory address range defined as APIC Configuration Space, FSB Interrupt Space, and High BIOS Address Range. The exceptions listed above for internal graphics and the PCI Express ports ***MUST NOT overlap with these ranges.***



Figure 3-4. PCI Memory Address Range



### 3.3.1 APIC Configuration Space (FEC0\_0000h–FECF\_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the ICH portion of the chip-set, but may also exist as stand-alone components like PXH.

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the default IOAPIC region (FEC0\_0000h to FEC7\_FFFFh) are always forwarded to DMI.

The (G)MCH optionally supports additional I/O APICs behind the PCI Express “Graphics” port. When enabled via the PCI Express Configuration register (Device 1 Offset 200h), the PCI Express port will positively decode a subset of the APIC configuration space – specifically FEC8\_0000h thru FECF\_FFFFh. Memory request to this range would then be forwarded to the PCI Express port. This mode is intended for the entry Workstation/Server SKU of the (G)MCH, and would be disabled in typical Desktop systems. When disabled, any access within entire APIC Configuration space (FEC0\_0000h to FECF\_FFFFh) is forwarded to DMI.



### 3.3.2 HSEG (FEDA\_0000h–FEDB\_FFFFh)

This optional segment from FEDA\_0000h to FEDB\_FFFFh provides a remapping window to SMM Memory. It is sometimes called the High SMM memory space. SMM-mode processor accesses to the optionally enabled HSEG are remapped to 000A\_0000h – 000B\_FFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode Write Back cycles which are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All cacheline writes with WB attribute or Implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

### 3.3.3 FSB Interrupt Memory Space (FEE0\_0000–FEEF\_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express or DMI may issue a Memory Write to 0FEEh\_xxxxh. The (G)MCH will forward this Memory Write along with the data to the FSB as an Interrupt Message Transaction. The (G)MCH terminates the FSB transaction by providing the response and asserting HTRDYB. This Memory Write cycle does not go to DRAM.

### 3.3.4 High BIOS Area

The top 2 MB (FEE0\_0000h – FFFF\_FFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to DMI Interface so that the upper subset of this region aliases to 16 MB–256 KB range. The actual address space required for the BIOS is less than 2 MB but the minimum processor MTRR range for this region is 2 MB so that full 2 MB must be considered.

## 3.4 Main Memory Address Space (4 GB to TOUUD)

The (G)MCH supports 36 bit addressing. The maximum main memory size supported is 4 GB total DRAM memory. A hole between TOLUD and 4 GB occurs when main memory size approaches 4 GB or larger. As a result, TOM, and TOUUD registers and RECLAIMBASE/RECLAIMLIMIT registers become relevant.

The new reclaim configuration registers exist to reclaim lost main memory space. The greater than 32 bit reclaim handling will be handled similar to other (G)MCHs. Upstream read and write accesses above 36-bit addressing will be treated as invalid cycles by PEG and DMI.

### Top of Memory

The “Top of Memory” (TOM) register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped I/O above TOM).



The Top of Upper Usable Dram (TOUUD) register reflects the total amount of addressable DRAM. If reclaim is enabled, then it will reflect the reclaim limit. TOLUD register is restricted to 4 GB memory (A[31:20]). When reclaim is enabled, TOLUD must be 64 MB aligned, but when reclaim is disabled, TOLUD can be 1 MB aligned.

C1DRB3 cannot be used directly to determine the effective size of memory as the values programmed in the DRBs depend on the memory mode (stacked, interleaved). The Reclaim Base/Limit registers also can not be used because reclaim can be disabled. The CODRB3 register is used for memory channel identification (channel 0 vs. channel 1) in the case of stacked memory.

### 3.4.1 Memory Re-claim Background

The following are examples of Memory Mapped IO devices are typically located below 4 GB:

- High BIOS
- HSEG
- TSEG
- Graphics stolen
- GTT stolen
- XAPIC
- Local APIC
- FSB Interrupts
- Mbase/Mlimit
- Memory Mapped IO space that supports only 32 B addressing

The (G)MCH provides the capability to re-claim the physical memory overlapped by the Memory Mapped IO logical address space. The (G)MCH re-maps physical memory from the Top of Low Memory (TOLUD) boundary up to the 4 GB boundary to an equivalent sized logical address range.

### 3.4.2 Memory Reclaiming

An incoming address (referred to as a logical address) is checked to see if it falls in the memory re-map window. The bottom of the re-map window is defined by the value in the RECLAIMBASE register. The top of the re-map window is defined by the value in the RECLAIMLIMIT register. An address that falls within this window is reclaimed to the physical memory starting at the address defined by the TOLUD register. The TOLUD register must be 64 MB aligned when RECLAIM is enabled, but can be 1 MB aligned when reclaim is disabled.

## 3.5 PCI Express\* Configuration Address Space

There is a device 0 register, PCIEXBAR, which defines the base address for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. The size of this range is programmable because the Intel G31/P31 Express chipset BIOS must assign this address range such that it will not conflict with any other address ranges.

See the configuration portion of this document for more details.



### 3.6 PCI Express\* Graphics Attach (PEG)

The (G)MCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two ranges specified via registers in (G)MCH's Device 1 configuration space.

- The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers.
- The second range is controlled via the Pre-fetchable Memory Base (PMBASE) and Pre-fetchable Memory Limit (PMLIMIT) registers.

Conceptually, address decoding for each range follows the same basic concept. The top 12 bits of the respective Memory Base and Memory Limit registers correspond to address bits A[31:20] of a memory address. For the purpose of address decoding, the (G)MCH assumes that address bits A[19:0] of the memory base are zero and that address bits A[19:0] of the memory limit address are FFFFh. This forces each memory address range to be aligned to 1 MB boundary and to have a size granularity of 1 MB.

The (G)MCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

$$\text{Memory\_Base\_Address} \leq \text{Address} \leq \text{Memory\_Limit\_Address}$$

$$\text{Prefetchable\_Memory\_Base\_Address} \leq \text{Address} \leq \text{Prefetchable\_Memory\_Limit\_Address}$$

The window size is programmed by the plug-and-play configuration software. The window size depends on the size of memory claimed by the PCI Express device. Normally these ranges will reside above the Top-of-Low Usable-DRAM and below High BIOS and APIC address ranges. They MUST reside above the top of low memory (TOLUD) if they reside below 4 GB and MUST reside above top of upper memory (TOUUD) if they reside above 4 GB or they will steal physical DRAM memory space.

It is essential to support a separate Pre-fetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note that the (G)MCH Device 1 memory range registers described above are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the device 1 PCICMD1 register to enable the memory base/limit and pre-fetchable base/limit windows.

For the Intel® G31/P31 Express Chipset, the upper PMUBASE1/PMULIMIT1 registers have been implemented for PCI Express Specification compliance. The G31/P31 Express Chipset locates MMIO space above 4 GB using these registers.



### 3.7 Graphics Memory Address Ranges (Intel® 82G31 GMCH Only)

The (G)MCH can be programmed to direct memory accesses to IGD when addresses are within any of three ranges specified via registers in the (G)MCH's Device 2 configuration space.

- The Memory Map Base Register (MMADR) is used to access graphics control registers.
- The Graphics Memory Aperture Base Register (GMADR) is used to access graphics memory allocated via the graphics translation table.
- The Graphics Translation Table Base Register (GTTADR) is used to access the translation table.

These ranges can reside above the Top-of-Low-DRAM and below High BIOS and APIC address ranges. They MUST reside above the top of memory (TOLUD) and below 4 GB so they do not steal any physical DRAM memory space.

GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

### 3.8 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The (G)MCH supports: Compatible SMRAM (C\_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the operating system so that the processor has immediate access to this memory space upon entry to SMM. (G)MCH provides three SMRAM options:

- Below 1 MB option that supports compatible SMI handlers.
- Above 1 MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. The TSEG area lies below IGD stolen memory.

The above 1 MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

**Note:** DMI Interface and PCI Express masters are not allowed to access the SMM space.



### 3.8.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space is a different address range. Note that the High DRAM space is the same as the Compatible Transaction Address space. Table 3-5 describes three unique address ranges.

Table 3-5. Pre-Allocated Memory Example for 64-MB DRAM, 1-MB VGA and 1-MB TSEG

| SMM Space Enabled | Transaction Address Space           | DRAM Space (DRAM)                   |
|-------------------|-------------------------------------|-------------------------------------|
| Compatible        | 000A_0000h to 000B_FFFFh            | 000A_0000h to 000B_FFFFh            |
| High              | FEDA_0000h to FEDB_FFFFh            | 000A_0000h to 000B_FFFFh            |
| TSEG              | (TOLUD-STOLEN-TSEG) to TOLUD-STOLEN | (TOLUD-STOLEN-TSEG) to TOLUD-STOLEN |

**NOTES:**

1. STOLEN memory is only for the 82G31 GMCH.

### 3.8.2 SMM Space Restrictions

If any of the following conditions are violated the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space **must not** be set-up as cacheable.
- High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any "PCI" devices (including DMI Interface, PCI-Express, and graphics devices). This is a BIOS responsibility.
- Both D\_OPEN and D\_CLOSE **must not** be set to 1 at the same time.
- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
- Any address translated through the GMADR TLB must not target DRAM from A\_0000-F\_FFFFh.



### 3.8.3 SMM Space Combinations

When High SMM is enabled (G\_SMROME=1 and H\_SMRAM\_EN=1) the Compatible SMM space is effectively disabled. Processor originated accesses to the Compatible SMM space are forwarded to PCI Express if VGAEN=1 (also depends on MDAP), otherwise they are forwarded to the DMI Interface. PCI Express and DMI Interface originated accesses are **never** allowed to access SMM space.

Table 3-6. SMM Space Table

| Global Enable<br>G_SMROME | High Enable<br>H_SMRAM_EN | TSEG Enable<br>TSEG_EN | Compatible<br>(C) Range | High (H)<br>Range | TSEG (T)<br>Range |
|---------------------------|---------------------------|------------------------|-------------------------|-------------------|-------------------|
| 0                         | X                         | X                      | Disable                 | Disable           | Disable           |
| 1                         | 0                         | 0                      | Enable                  | Disable           | Disable           |
| 1                         | 0                         | 1                      | Enable                  | Disable           | Enable            |
| 1                         | 1                         | 0                      | Disabled                | Enable            | Disable           |
| 1                         | 1                         | 1                      | Disabled                | Enable            | Enable            |

### 3.8.4 SMM Control Combinations

The G\_SMROME bit provides a global enable for all SMM memory. The D\_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at power-up. The D\_LCK bit limits the SMM range access to only SMM mode accesses. The D\_CLS bit causes SMM (both CSEG and TSEG) data accesses to be forwarded to the DMI Interface or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

### 3.8.5 SMM Space Decode and Transaction Handling

Only the processor is allowed to access SMM space. PCI Express and DMI Interface originated transactions are not allowed to SMM space.

### 3.8.6 Processor WB Transaction to an Enabled SMM Address Space

Processor Writeback transactions (REQa[1]# = 0) to enabled SMM Address Space must be written to the associated SMM DRAM even though D\_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.



### 3.8.7 SMM Access Through GTT TLB (Intel® 82G31 GMCH Only)

Accesses through GTT TLB address translation to enabled SMM DRAM space are not allowed. Writes will be routed to Memory address 000C\_0000h with byte enables de-asserted and reads will be routed to Memory address 000C\_0000h. If a GTT TLB translated address hits enabled SMM DRAM space, an error is recorded.

PCI Express and DMI Interface originated accesses are **never** allowed to access SMM space directly or through the GTT TLB address translation. If a GTT TLB translated address hits enabled SMM DRAM space, an error is recorded.

PCI Express and DMI Interface write accesses through GMADR range will be snooped. Accesses to GMADR linear range (defined via fence registers) are supported. PCI Express and DMI Interface tileY and tileX writes to GMADR are not supported. If, when translated, the resulting physical address is to enabled SMM DRAM space, the request will be remapped to address 000C\_0000h with de-asserted byte enables.

PCI Express and DMI Interface read accesses to the GMADR range are not supported; therefore, there are no address translation concerns. PCI Express and DMI Interface reads to GMADR will be remapped to address 000C\_0000h. The read will complete with UR (unsupported request) completion status.

GTT fetches are always decoded (at fetch time) to ensure not in SMM (actually, anything above base of TSEG or 640 KB – 1 MB). Thus, they will be invalid and go to address 000C\_0000h, but that is not specific to PCI Express or DMI; it applies to processor or internal graphics engines. Also, since the GMADR snoop would not be directly to the SMM space, there would not be a writeback to SMM. In fact, the writeback would also be invalid (because it uses the same translation) and go to address 000C\_0000h.

## 3.9 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into (G)MCH DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as a read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. Processor bus transactions are routed accordingly.



## 3.10 I/O Address Space

The (G)MCH does not support the existence of any other I/O devices beside itself on the processor bus. The (G)MCH generates either DMI Interface or PCI Express bus cycles for all processor I/O accesses that it does not claim. The (G)MCH contains two internal registers in the processor I/O space: Configuration Address Register (CONFIG\_ADDRESS) and the Configuration Data Register (CONFIG\_DATA). These locations are used to implement the configuration space access mechanism.

The processor allows 64 K+3 bytes to be addressed within the I/O space. The (G)MCH propagates the processor I/O address without any translation on to the destination bus and therefore provides addressability for 64K+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when processor bus HA16# address signal is asserted. HA16# is asserted on the processor bus when an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HA16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) are consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics I/O decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI Interface bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are NOT posted. Memory writes to ICH or PCI Express are posted. The PCICMD1 register can disable the routing of I/O cycles to the PCI Express.

The (G)MCH responds to I/O cycles initiated on PCI Express or DMI with an UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to Memory address 000C\_0000h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with an UR completion status.

For Intel processors, I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as 1 transaction. The (G)MCH will break this into 2 separate transactions. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into 2 transactions by the processor.

### 3.10.1 PCI Express\* I/O Address Mapping

The (G)MCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in (G)MCH Device 1 configuration space.

Address decoding for this range is based on the following concept. The top 4 bits of the respective I/O Base and I/O Limit registers correspond to address bits A[15:12] of an I/O address. For the purpose of address decoding, the (G)MCH assumes that lower 12 address bits A[11:0] of the I/O base are zero and that address bits A[11:0] of the I/O limit address are FFFh. This forces the I/O address range alignment to 4 KB boundary and produces a size granularity of 4 KB.



The (G)MCH positively decodes I/O accesses to PCI Express I/O address space as defined by the following equation:

$$\text{I/O\_Base\_Address} \leq \text{CPU I/O Cycle Address} \leq \text{I/O\_Limit\_Address}$$

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the PCI Express device.

The (G)MCH also forwards accesses to the Legacy VGA I/O ranges according to the settings in the Device 1 configuration registers BCTRL (VGA Enable) and PCICMD1 (IOAE1), unless a second adapter (monochrome) is present on the DMI Interface/PCI (or ISA). The presence of a second graphics adapter is determined by the MDAP configuration bit. When MDAP is set, the (G)MCH will decode legacy monochrome I/O ranges and forward them to the DMI Interface. The I/O ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3Bah and 3BFh.

Note that the (G)MCH Device 1 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on PCI Express.

The PCICMD1 register can disable the routing of I/O cycles to PCI Express.

### 3.11 (G)MCH Decode Rules and Cross-Bridge Address Mapping

VGAA = 000A\_0000 – 000A\_FFFF  
MDA = 000B\_0000 – 000B\_7FFF  
VGAB = 000B\_8000 – 000B\_FFFF  
MAINMEM = 0100\_0000 to TOLUD  
HIGHMEM = 4 GB to TOM  
RECLAIMMEM = RECLAIMBASE to RECLAIMLIMIT

#### 3.11.1 Legacy VGA and I/O Range Decode Rules

The legacy 128 KB VGA memory range 000A\_0000h-000B\_FFFFh can be mapped to IGD (Device 2 in 82G31 GMCH), to PCI Express (Device 1), and/or to the DMI Interface depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the (G)MCH always decodes internally mapped devices first. Internal to the (G)MCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI-Express. Subsequent decoding of regions mapped to PCI Express or the DMI Interface depends on the Legacy VGA configurations bits (VGA Enable and MDAP).

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## 4 (G)MCH Register Description

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The (G)MCH contains two sets of software accessible registers, accessed via the Host processor I/O address space: Control registers and internal configuration registers.

- Control registers are I/O mapped into the processor I/O space, which control access to PCI and PCI Express configuration space (see Section 4.5).
- Internal configuration registers residing within the (G)MCH are partitioned into three logical device register sets (“logical” since they reside within a single physical device). The first register set is dedicated to Host Bridge functionality (i.e., DRAM configuration, other chipset operating parameters and optional features). The second register block is dedicated to Host-PCI Express Bridge functions (controls PCI Express interface configurations and operating parameters). For the 82G31 GMCH, another register block is for the internal graphics functions.

The (G)MCH internal registers (I/O Mapped, Configuration and PCI Express Extended Configuration registers) are accessible by the Host processor. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16 bit), or DWord (32 bit) quantities, with the exception of CONFIG\_ADDRESS, which can only be accessed as a DWord. All multi-byte numeric fields use “little-endian” ordering (i.e., lower addresses contain the least significant parts of the field). Registers which reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in DWord (32 bit) quantities.

Some of the (G)MCH registers described in this section contain reserved bits. These bits are labeled “Reserved”. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operation for the Configuration Address Register.

In addition to reserved bits within a register, the (G)MCH contains address locations in the configuration space of the Host Bridge entity that are marked either “Reserved” or “Intel Reserved”. The (G)MCH responds to accesses to “Reserved” address locations by completing the host cycle. When a “Reserved” register location is read, a zero value is returned. (“Reserved” registers can be 8-, 16-, or 32 bits in size). Writes to “Reserved” registers have no effect on the (G)MCH. Registers that are marked as “Intel Reserved” must not be modified by system software. Writes to “Intel Reserved” registers may cause system failure. Reads from “Intel Reserved” registers may return a non-zero value.

Upon a Full Reset, the (G)MCH sets its entire set of internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bringing up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the (G)MCH registers accordingly.



## 4.1 Register Terminology

The following table shows the register-related terminology that is used.

| Item    | Definition  |
|---------|---|
| RO      | Read Only bit(s). Writes to these bits have no effect. This may be a status bit or a static value.  |
| RO/S    | Read Only / Sticky bit(s). Writes to these bits have no effect. These are status bits only. Bits are not returned to their default values by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec).   |
| RS/WC   | Read Set / Write Clear bit(s). The first time the bit is read with an enabled byte, it returns the value 0, but a side-effect of the read is that the value changes to 1. Any subsequent reads with enabled bytes return a 1 until a 1 is written to the bit. When the bit is read, but the byte is not enabled, the state of the bit does not change, and the value returned is irrelevant, but will match the state of the bit.<br><br>When a 0 is written to the bit, there is no effect. When a 1 is written to the bit, its value becomes 0, until the next byte-enabled read. When the bit is written, but the byte is not enabled, there is no effect.       |
| R/W     | Read / Write bit(s). These bits can be read and written by software. Hardware may only change the state of this bit by reset.   |
| R/WC    | Read / Write Clear bit(s). These bits can be read. Internal events may set this bit. A software write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect.  |
| R/WC/L  | Read / Write Clear / Lockable bit(s). These bits can be read. Internal events may set this bit. A software write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).   |
| R/WC/S  | Read / Write Clear / Sticky bit(s). These bits can be read. Internal events may set this bit. A software write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec).  |
| R/W/B   | Read / Write / Blind bit(s). These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit.  |
| R/W/B/L | Read / Write / Blind / Lockable bit(s). These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only). |



| Item     | Definition   |
|----------|--|
| R/W/K    | Read / Write / Key bit(s). These bits can be read and written by software. Additionally this bit, when set, prohibits some other bit field(s) from being writeable (bit fields become Read Only).  |
| R/W/L    | Read / Write / Lockable bit(s). These bits can be read and written by software. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).  |
| R/W/L/K  | Read / Write / Lockable / Key bit(s). These bits can be read and written by software. Additionally this bit is a Key bit that, when set, prohibits this bit field and/or some other specified bit fields from being writeable (bit fields become Read Only).   |
| R/W/S    | Read / Write / Sticky bit(s). These bits can be read and written by software. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec).   |
| R/W/S/B  | Read / Write / Sticky / Blind bit(s). These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec). |
| R/W/SC   | Read / Write / Self Clear bit(s). These bits can be read and written by software. When the bit is '1', hardware may clear the bit to '0' based upon internal events, possibly sooner than any subsequent software read could retrieve a '1'.   |
| R/W/SC/L | Read / Write / Self Clear / Lockable bit(s). These bits can be read and written by software. When the bit is '1', hardware may clear the bit to '0' based upon internal events, possibly sooner than any subsequent software read could retrieve a '1'. Additionally there is a bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).  |
| R/WO     | Write Once bit(s). Once written by software, bits with this attribute become Read Only. These bits can only be cleared by a Reset. If there are multiple R/WO fields within a DWORD, they should be written all at once (atomically) to avoid capturing an incorrect value.  |
| W        | Write Only. These bits may be written by software, but will always return zeros when read. They are used for write side-effects. Any data written to these registers cannot be retrieved.  |



## 4.2 Configuration Process and Registers

### 4.2.1 Platform Configuration Structure

The DMI physically connects the (G)MCH and the Intel ICH7; so, from a configuration standpoint, the DMI is logically PCI bus 0. As a result, all devices internal to the (G)MCH and the Intel ICH7 appear to be on PCI bus 0.

**Note:** The ICH7 internal LAN controller does not appear on bus 0 – it appears on the external PCI bus (whose number is configurable).

The system's primary PCI expansion bus is physically attached to the Intel ICH7 and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. The PCI Express Graphics Attach appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI bus 0.

**Note:** A physical PCI bus 0 does not exist and that DMI and the internal devices in the (G)MCH and Intel ICH7 logically constitute PCI Bus 0 to configuration software.

The (G)MCH contains three PCI devices within a single physical component. The configuration registers for the three devices are mapped as devices residing on PCI bus 0.

- **Device 0: Host Bridge/DRAM Controller.** Logically this appears as a PCI device residing on PCI bus #0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), configuration for the DMI, and other (G)MCH specific registers.
- **Device 1: Host-PCI Express Bridge.** Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI bus #0 and is compliant with PCI Express Specification rev 1.0. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.
- **Device 2: Internal Graphics Control (82G31 GMCH only).** Logically, this appears as a PCI device residing on PCI bus 0. Physically, device 2 contains the configuration registers for 3D, 2D, and display functions.



## 4.3 Configuration Mechanisms

The processor is the originator of configuration cycles so the FSB is the only interface in the platform where these mechanisms are used. Internal to the (G)MCH transactions received through both configuration mechanisms are translated to the same format.

### 4.3.1 Standard PCI Configuration Mechanism

The following is the mechanism for translating processor I/O bus cycles to configuration cycles.

The PCI specification defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the (G)MCH.

The configuration access mechanism makes use of the CONFIG\_ADDRESS Register (at I/O address 0CF8h through 0CFBh) and CONFIG\_DATA Register (at I/O address 0CFCh through 0CFFh). To reference a configuration register a DW I/O write cycle is used to place a value into CONFIG\_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device and a specific configuration register of the device function being accessed. CONFIG\_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG\_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG\_ADDRESS. Any read or write to CONFIG\_DATA will result in the (G)MCH translating the CONFIG\_ADDRESS into the appropriate configuration cycle.

The (G)MCH is responsible for translating and routing the processor's I/O accesses to the CONFIG\_ADDRESS and CONFIG\_DATA registers to internal (G)MCH configuration registers, DMI or PCI Express.

### 4.3.2 PCI Express\* Enhanced Configuration Mechanism

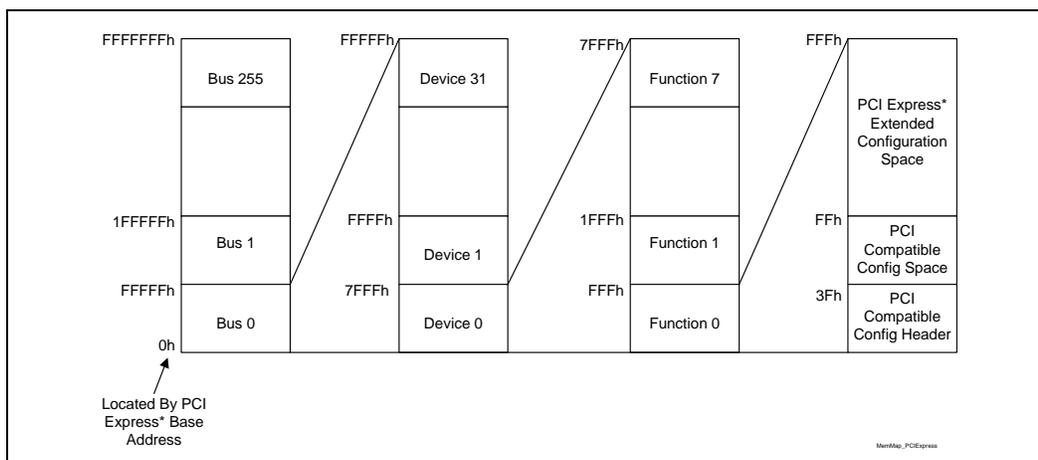
PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by PCI Specification Revision 2.3. PCI Express configuration space is divided into a PCI 2.3 compatible region, which consists of the first 256B of a logical device's configuration space and a PCI Express extended region which consists of the remaining configuration space.

The PCI compatible region can be accessed using either the Standard PCI Configuration Mechanism or using the PCI Express Enhanced Configuration Mechanism described in this section. The extended configuration registers may only be accessed using the PCI Express Enhanced Configuration Mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the DWord to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent.

The PCI Express Enhanced Configuration Mechanism utilizes a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. There is a register, PCIEXBAR, that defines the base address for the block of addresses below 4 GB for the configuration space associated with busses, devices and functions that are potentially a part of the PCI Express root complex hierarchy. In the PCIEXBAR register there exists controls to limit the size of this reserved memory mapped space. 256 MB is the amount of address space required to reserve space for every bus, device, and function that could possibly exist. Options for 128 MB and 64 MB exist in order to free up those addresses for other uses. In these cases the number of busses and all of their associated devices and functions are limited to 128 or 64 busses respectively.

The PCI Express Configuration Transaction Header includes an additional 4 bits (ExtendedRegisterAddress[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all zeros.

Figure 4-1. Memory Map to PCI Express\* Device Configuration Space



Just the same as with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function and extended address numbers) to provide access to the correct register.

To access this space (steps 1, 2, 3 are done only once by BIOS),

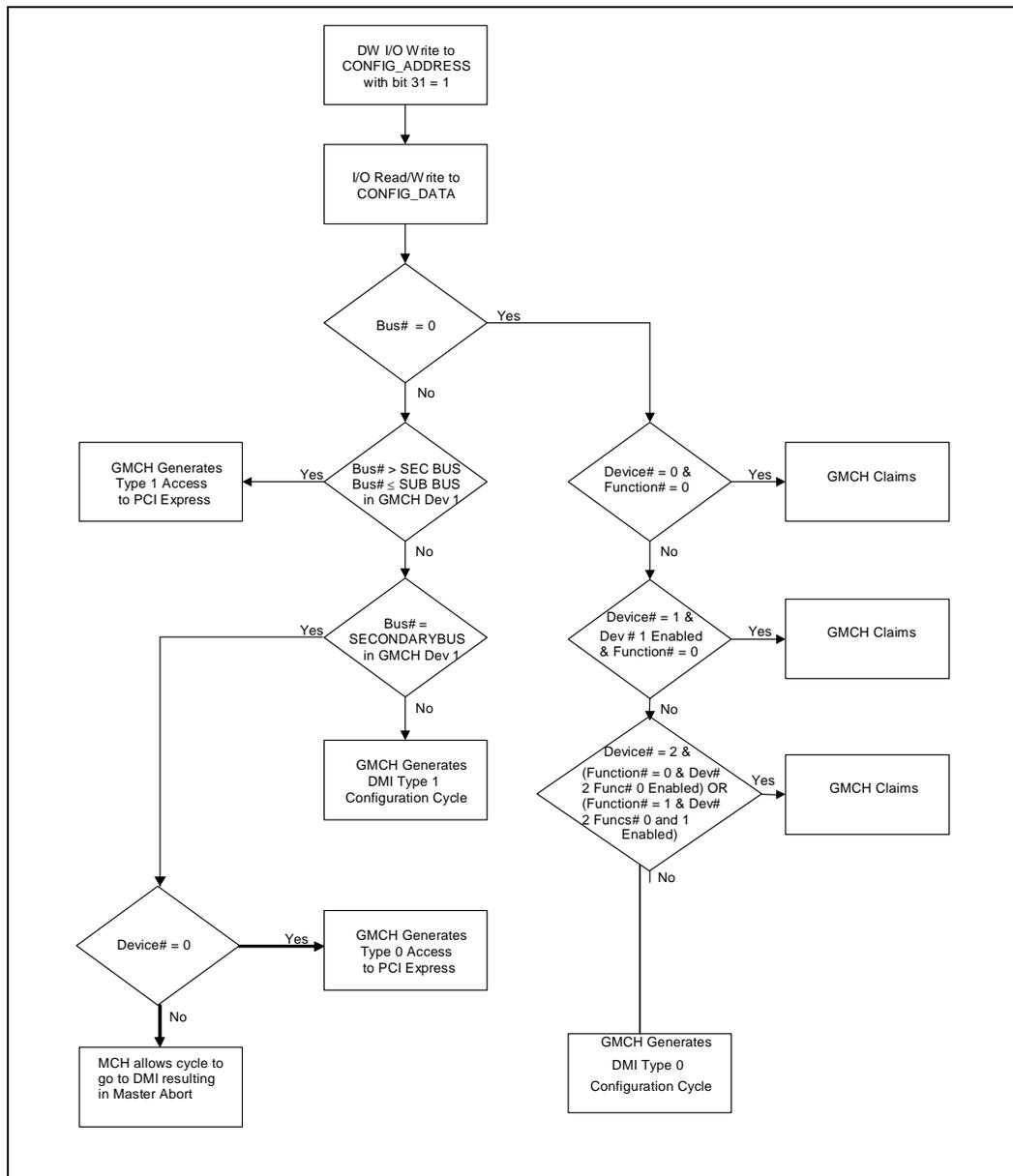
1. use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 0 of the PCIEXBAR register.
2. use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register
3. calculate the host address of the register you wish to set using (PCI Express base + (bus number \* 1 MB) + (device number \* 32KB) + (function number \* 4 KB) + (1 B \* offset within the function) = host address)
4. use a memory write or memory read cycle to the calculated host address to write or read that register.



## 4.4 Routing Configuration Accesses

The (G)MCH supports two PCI related interfaces: DMI and PCI Express. The (G)MCH is responsible for routing PCI and PCI Express configuration cycles to the appropriate device that is an integrated part of the (G)MCH or to one of these two interfaces. Configuration cycles to the ICH7 internal devices and Primary PCI (including downstream devices) are routed to the ICH7 via DMI. Configuration cycles to both the PCI Express Graphics PCI compatibility configuration space and the PCI Express Graphics extended configuration space are routed to the PCI Express Graphics port device or associated link.

Figure 4-2. GMCH Configuration Cycle Flow Chart





## 4.4.1 Internal Device Configuration Accesses

The (G)MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG\_ADDRESS register. If the Bus Number field of CONFIG\_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device.

If the targeted PCI Bus #0 device exists in the (G)MCH and is not disabled, the configuration cycle is claimed by the appropriate device.

## 4.4.2 Bridge Related Configuration Accesses

Configuration accesses on PCI Express or DMI are PCI Express Configuration TLPs.

- Bus Number [7:0] is Header Byte 8 [7:0]
- Device Number [4:0] is Header Byte 9 [7:3]
- Function Number [2:0] is Header Byte 9 [2:0]

And special fields for this type of TLP:

- Extended Register Number [3:0] is Header Byte 10 [3:0]
- Register Number [5:0] is Header Byte 11 [7:2]

See the PCI Express specification for more information on both the PCI 2.3 compatible and PCI Express Enhanced Configuration Mechanism and transaction rules.

### 4.4.2.1 PCI Express\* Configuration Accesses

When the Bus Number of a type 1 Standard PCI Configuration cycle or PCI Express Enhanced Configuration access matches the Device #1 Secondary Bus Number a PCI Express Type 0 Configuration TLP is generated on the PCI Express link targeting the device directly on the opposite side of the link. This should be Device #0 on the bus number assigned to the PCI Express link (likely Bus #1).

The device on other side of link must be Device #0. The (G)MCH will Master Abort any Type 0 Configuration access to a non-zero Device number. If there is to be more than one device on that side of the link there must be a bridge implemented in the downstream device.

When the Bus Number of a type 1 Standard PCI Configuration cycle or PCI Express Enhanced Configuration access is within the claimed range (between the upper bound of the bridge device's Subordinate Bus Number register and the lower bound of the bridge device's Secondary Bus Number register) but doesn't match the Device #1 Secondary Bus Number, a PCI Express Type 1 Configuration TLP is generated on the secondary side of the PCI Express link.

PCI Express Configuration Writes:

- Internally the host interface unit will translate writes to PCI Express extended configuration space to configuration writes on the backbone.
- Writes to extended space are posted on the FSB, but non-posted on the PCI Express or DMI (i.e.. translated to config writes)



#### 4.4.2.2 DMI Configuration Accesses

Accesses to disabled (G)MCH internal devices, bus numbers not claimed by the Host-PCI Express bridge, or PCI Bus #0 devices not part of the (G)MCH will subtractively decode to the ICH7 and consequently be forwarded over the DMI via a PCI Express configuration TLP.

If the Bus Number is zero, the (G)MCH will generate a Type 0 Configuration Cycle TLP on DMI. If the Bus Number is non-zero, and falls outside the range claimed by the Host-PCI Express bridge, the (G)MCH will generate a Type 1 Configuration Cycle TLP on DMI.

The ICH7 routes configurations accesses in a manner similar to the (G)MCH. The ICH7 decodes the configuration TLP and generates a corresponding configuration access. Accesses targeting a device on PCI Bus #0 may be claimed by an internal device. The ICH7 compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its P2P bridges to determine if the configuration access is meant for Primary PCI, or some other downstream PCI bus or PCI Express link.

Configuration accesses that are forwarded to the ICH7, but remain unclaimed by any device or bridge will result in a master abort.

### 4.5 I/O Mapped Registers

The (G)MCH contains two registers that reside in the processor I/O address space – the Configuration Address (CONFIG\_ADDRESS) Register and the Configuration Data (CONFIG\_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

#### 4.5.1 CONFIG\_ADDRESS—Configuration Address Register

|                |                        |
|----------------|------------------------|
| I/O Address:   | 0CF8h Accessed as a DW |
| Default Value: | 00000000h              |
| Access:        | R/W                    |
| Size:          | 32 bits                |

CONFIG\_ADDRESS is a 32-bit register that can be accessed only as a DW. A Byte or Word reference will "pass through" the Configuration Address Register and DMI onto the Primary PCI bus as an I/O cycle. The CONFIG\_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31    | RW<br>0b         | <b>Configuration Enable (CFGE).</b><br>0 = Disable<br>1 = Enable |
| 30:24 |                  | Reserved   |



| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 23:16 | RW<br>00h        | <p><b>Bus Number.</b> If the Bus Number is programmed to 00h the target of the Configuration Cycle is a PCI Bus 0 agent. If this is the case and the (G)MCH is not the target (i.e., the device number is <math>\geq 2</math>), then a DMI Type 0 Configuration Cycle is generated.</p> <p>If the Bus Number is non-zero, and does not fall within the ranges enumerated by device 1's Secondary Bus Number or Subordinate Bus Number Register, then a DMI Type 1 Configuration Cycle is generated.</p> <p>If the Bus Number is non-zero and matches the value programmed into the Secondary Bus Number Register of device 1, a Type 0 PCI configuration cycle will be generated on PCI Express-G.</p> <p>If the Bus Number is non-zero, greater than the value in the Secondary Bus Number register of device 1 and less than or equal to the value programmed into the Subordinate Bus Number Register of device 1 a Type 1 PCI configuration cycle will be generated on PCI Express-G.</p> <p>This field is mapped to byte 8 [7:0] of the request header format during PCI Express Configuration cycles and A[23:16] during the DMI Type 1 configuration cycles.</p> |
| 15:11 | RW<br>00h        | <p><b>Device Number.</b> This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is "00" the (G)MCH decodes the Device Number field. The (G)MCH is always Device Number 0 for the Host bridge entity, Device Number 1 for the Host-PCI Express entity. Therefore, when the Bus Number =0 and the Device Number equals 0, 1, or 2 the internal (G)MCH devices are selected.</p> <p>This field is mapped to byte 6 [7:3] of the request header format during PCI Express Configuration cycles and A [15:11] during the DMI configuration cycles.</p>  |
| 10:8  | RW<br>00b        | <p><b>Function Number.</b> This field allows the configuration registers of a particular function in a multi-function device to be accessed. The (G)MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1.</p> <p>This field is mapped to byte 6 [2:0] of the request header format during PCI Express Configuration cycles and A[10:8] during the DMI configuration cycles.</p>   |
| 7:2   | RW<br>00h        | <p><b>Register Number.</b> This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register.</p> <p>This field is mapped to byte 7 [7:2] of the request header format during PCI Express Configuration cycles and A[7:2] during the DMI Configuration cycles.</p>   |
| 1:0   |                  | Reserved  |



### 4.5.2 CONFIG\_DATA—Configuration Data Register

I/O Address: 0CFCh  
Default Value: 00000000h  
Access: R/W  
Size: 32 bits

CONFIG\_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG\_DATA is determined by the contents of CONFIG\_ADDRESS.

| Bit  | Access & Default   | Description   |
|------|--------------------|---|
| 31:0 | R/W<br>0000 0000 h | <b>Configuration Data Window (CDW)</b><br>If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed. |

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## 5 DRAM Controller Registers (D0:F0)

The DRAM Controller registers are in Device 0 (D0), Function 0 (F0).

### 5.1 DRAM Controller (D0:F0)

**Warning:** Address locations that are not listed are considered Intel Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

All registers that are defined in the PCI 2.3 specification, but are not necessary or implemented in this component are simply not included in this document. The reserved/unimplemented space in the PCI configuration header space is not documented as such in this summary.

**Table 5-1. DRAM Controller Register Address Map (D0:F0)**

| Address Offset | Register Symbol | Register Name                            | Default Value            | Access  |
|----------------|-----------------|--|--------------------------|---------|
| 00–01h         | VID             | Vendor Identification                    | 8086h                    | RO      |
| 02–03h         | DID             | Device Identification                    | 29C0h                    | RO      |
| 04–05h         | PCICMD          | PCI Command                              | 0006h                    | RO, RW  |
| 06–07h         | PCISTS          | PCI Status                               | 0090h                    | RWC, RO |
| 08h            | RID             | Revision Identification                  | See register description | RO      |
| 09–0Bh         | CC              | Class Code                               | 060000h                  | RO      |
| 0Dh            | MLT             | Master Latency Timer                     | 00h                      | RO      |
| 0Eh            | HDR             | Header Type                              | 00h                      | RO      |
| 2C–2Dh         | SVID            | Subsystem Vendor Identification          | 0000h                    | RWO     |
| 2E–2Fh         | SID             | Subsystem Identification                 | 0000h                    | RWO     |
| 34h            | CAPPTR          | Capabilities Pointer                     | E0h                      | RO      |
| 40–47h         | PXPEPBAR        | PCI Express Port Base Address            | 0000000000<br>000000h    | RW, RO  |
| 48–4Fh         | MCHBAR          | (G)MCH Memory Mapped Register Range Base | 0000000000<br>000000h    | RW, RO  |
| 52–53h         | GGC             | GMCH Graphics Control Register           | 0030h                    | RO, RW  |
| 54–57h         | DEVEN           | Device Enable                            | 000003DBh                | RO, RW  |



| Address Offset | Register Symbol | Register Name                            | Default Value          | Access               |
|----------------|-----------------|--|------------------------|----------------------|
| 60–67h         | PCIEXBAR        | PCI Express Register Range Base Address  | 00000000E000000h       | RO, RW/L, RW/L/K     |
| 68–6Fh         | DMIBAR          | Root Complex Register Range Base Address | 000000000000000h       | RO, RW               |
| 90h            | PAM0            | Programmable Attribute Map 0             | 00h                    | RO, RW               |
| 91h            | PAM1            | Programmable Attribute Map 1             | 00h                    | RO, RW               |
| 92h            | PAM2            | Programmable Attribute Map 2             | 00h                    | RO, RW               |
| 93h            | PAM3            | Programmable Attribute Map 3             | 00h                    | RO, RW               |
| 94h            | PAM4            | Programmable Attribute Map 4             | 00h                    | RO, RW               |
| 95h            | PAM5            | Programmable Attribute Map 5             | 00h                    | RO, RW               |
| 96h            | PAM6            | Programmable Attribute Map 6             | 00h                    | RO, RW               |
| 97h            | LAC             | Legacy Access Control                    | 00h                    | RW/L, RO, RW         |
| 98–99h         | REMAPBASE       | Remap Base Address Register              | 03FFh                  | RO, RW               |
| 9A–9Bh         | REMAPLIMIT      | Remap Limit Address Register             | 0000h                  | RO, RW               |
| 9Dh            | SMRAM           | System Management RAM Control            | 02h                    | RO, RW/L, RW, RW/L/K |
| 9Eh            | ESMRAMC         | Extended System Management RAM Control   | 38h                    | RW/L, RWC, RO        |
| A0–A1h         | TOM             | Top of Memory                            | 0001h                  | RO, RW               |
| A2–A3h         | TOUUD           | Top of Upper Usable Dram                 | 0000h                  | RW                   |
| A4–A7h         | GBSM            | Graphics Base of Stolen Memory           | 00000000h              | RW/L, RO             |
| A8–ABh         | BGSM            | Base of GTT stolen Memory                | 00000000h              | RW/L, RO             |
| AC–AFh         | TSEGMB          | TSEG Memory Base                         | 00000000h              | RW/L, RO             |
| B0–B1h         | TOLUD           | Top of Low Usable DRAM                   | 0010h                  | RW/L, RO             |
| C8–C9h         | ERRSTS          | Error Status                             | 0000h                  | RO, RWC/S            |
| CA–CBh         | ERRCMD          | Error Command                            | 0000h                  | RO, RW               |
| CC–CDh         | SMICMD          | SMI Command                              | 0000h                  | RO, RW               |
| DC–DFh         | SKPD            | Scratchpad Data                          | 00000000h              | RW                   |
| E0–EAh         | CAPIDO          | Capability Identifier                    | 0000010000000010B0009h | RO                   |



### 5.1.1 VID—Vendor Identification

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 0–1h  
 Default Value: 8086h  
 Access: RO  
 Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:0 | RO<br>8086h      | <b>Vendor Identification Number (VID):</b> PCI standard identification for Intel. |

### 5.1.2 DID—Device Identification

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 02–03h  
 Default Value: See table below  
 Access: RO  
 Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:0 | RO<br>29C0h      | <b>Device Identification Number (DID):</b><br>29C0h = Intel® 82G31/82P31 (G)MCH |



### 5.1.3 PCI CMD—PCI Command

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 4–5h  
 Default Value: 0006h  
 Access: RO, RW  
 Size: 16 bits

Since (G)MCH Device 0 does not physically reside on PCI\_A many of the bits are not implemented.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>00h        | Reserved  |
| 9     | RO<br>0b         | <b>Fast Back-to-Back Enable (FB2B):</b> This bit controls whether or not the master can do fast back-to-back write. Since device 0 is strictly a target, this bit is not implemented and is hardwired to 0.   |
| 8     | RW<br>0b         | <b>SERR Enable (SERRE):</b> This bit is a global enable bit for Device 0 SERR messaging. The (G)MCH does not have an SERR signal. The (G)MCH communicates the SERR condition by sending an SERR message over DMI to the ICH.<br><br>1 = The (G)MCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD and DMIUEMSK registers. The error status is reported in the ERRSTS, PCISTS, and DMIUEST registers.<br><br>0 = The SERR message is not generated by the (G)MCH for Device 0.<br><br>Note that this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring in that device. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism. |
| 7     | RO<br>0b         | <b>Address/Data Stepping Enable (ADSTEP):</b> Address/data stepping is not implemented in the (G)MCH, and this bit is hardwired to 0.   |
| 6     | RW<br>0b         | <b>Parity Error Enable (PERRE):</b> This bit controls whether or not the Master Data Parity Error bit in the PCI Status register can be set.<br><br>0 = Master Data Parity Error bit in PCI Status register can NOT be set.<br>1 = Master Data Parity Error bit in PCI Status register CAN be set.  |
| 5     | RO<br>0b         | <b>VGA Palette Snoop Enable (VGASNOOP):</b> The (G)MCH does not implement this bit and it is hardwired to a 0.  |
| 4     | RO<br>0b         | <b>Memory Write and Invalidate Enable (MWIE):</b> The (G)MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0.   |
| 3     | RO<br>0b         | <b>Special Cycle Enable (SCE):</b> The (G)MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.   |
| 2     | RO<br>1b         | <b>Bus Master Enable (BME):</b> The (G)MCH is always enabled as a master on the backbone. This bit is hardwired to a 1.   |
| 1     | RO<br>1b         | <b>Memory Access Enable (MAE):</b> The (G)MCH always allows access to main memory. This bit is not implemented and is hardwired to 1.   |
| 0     | RO<br>0b         | <b>I/O Access Enable (IOAE):</b> This bit is not implemented in the (G)MCH and is hardwired to a 0.   |



### 5.1.4 PCISTS—PCI Status

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 6–7h  
 Default Value: 0090h  
 Access: RWC, RO  
 Size: 16 bits

This status register reports the occurrence of error events on Device 0's PCI interface. Since the (G)MCH Device 0 does not physically reside on PCI\_A many of the bits are not implemented.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15   | RWC<br>0b        | <b>Detected Parity Error (DPE):</b><br>1 = Device received a Poisoned TLP.  |
| 14   | RWC<br>0b        | <b>Signaled System Error (SSE):</b> Software clears this bit by writing a 1 to it.<br><br>1 = The (G)MCH Device 0 generated a SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, ERRCMD, and DMIUEMSK registers. Device 0 error flags are read/reset from the PCISTS, ERRSTS, or DMIUEST registers. |
| 13   | RWC<br>0b        | <b>Received Master Abort Status (RMAS):</b> Software clears this bit by writing a 1 to it.<br><br>1 = (G)MCH generated a DMI request that receives an Unsupported Request completion packet.  |
| 12   | RWC<br>0b        | <b>Received Target Abort Status (RTAS):</b> Software clears this bit by writing a 1 to it.<br><br>1 = (G)MCH generated a DMI request that receives a Completer Abort completion packet.   |
| 11   | RO<br>0b         | <b>Signaled Target Abort Status (STAS):</b> The (G)MCH will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the (G)MCH and is hardwired to a 0.  |
| 10:9 | RO<br>00b        | <b>DEVSEL Timing (DEVT):</b> These bits are hardwired to "00". Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the (G)MCH.  |
| 8    | RWC<br>0b        | <b>Master Data Parity Error Detected (DPD):</b><br><br>1 = This bit is set when DMI received a Poisoned completion from the ICH.<br><br><b>NOTE:</b> This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.  |
| 7    | RO<br>1b         | <b>Fast Back-to-Back (FB2B):</b> This bit is hardwired to 1. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the (G)MCH.  |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 6   | RO<br>0b         | Reserved   |
| 5   | RO<br>0b         | <b>66 MHz Capable:</b> Does not apply to PCI Express. Hardwired to 0.  |
| 4   | RO<br>1b         | <b>Capability List (CLIST):</b> This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability Identification register resides. |
| 3:0 | RO<br>0h         | Reserved   |

### 5.1.5 RID—Revision Identification

|                 |                          |
|-----------------|--------------------------|
| B/D/F/Type:     | 0/0/0/PCI                |
| Address Offset: | 8h                       |
| Default Value:  | See register table below |
| Access:         | RO                       |
| Size:           | 8 bits                   |

This register contains the revision number of the (G)MCH Device #0. These bits are read only and writes to this register have no effect.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>00h        | <b>Revision Identification Number (RID):</b> This is an 8-bit value that indicates the revision identification number for the (G)MCH Device 0. Refer to the <i>Intel® G31/P31 Express Chipset Family Specification Update</i> for the value of the Revision ID register. |



### 5.1.6 CC—Class Code

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 09–0Bh  
 Default Value: 060000h  
 Access: RO  
 Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 23:16 | RO<br>06h        | <b>Base Class Code (BCC):</b> This is an 8-bit value that indicates the base class code for the (G)MCH.<br><br>06h = Bridge device.  |
| 15:8  | RO<br>00h        | <b>Sub-Class Code (SUBCC):</b> This is an 8-bit value that indicates the category of Bridge into which the (G)MCH falls.<br><br>00h = Host Bridge.   |
| 7:0   | RO<br>00h        | <b>Programming Interface (PI):</b> This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device. |

### 5.1.7 MLT—Master Latency Timer

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 0Dh  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

Device 0 in the (G)MCH is not a PCI master. Therefore this register is not implemented.

| Bit | Access & Default | Description |
|-----|------------------|-------------|
| 7:0 | RO<br>00h        | Reserved    |



### 5.1.8 HDR—Header Type

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/0/0/PCI |
| Address Offset: | Eh        |
| Default Value:  | 00h       |
| Access:         | RO        |
| Size:           | 8 bits    |

This register identifies the header layout of the configuration space. No physical register exists at this location.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RO<br>00h        | <b>PCI Header (HDR):</b> This field always returns 0 to indicate that the (G)MCH is a single function device with standard header layout. Reads and writes to this location have no effect. |

### 5.1.9 SVID—Subsystem Vendor Identification

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/0/0/PCI |
| Address Offset: | 2C–2Dh    |
| Default Value:  | 0000h     |
| Access:         | RWO       |
| Size:           | 16 bits   |

This value is used to identify the vendor of the subsystem.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:0 | RWO<br>0000h     | <b>Subsystem Vendor ID (SUBVID):</b> This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only. |

### 5.1.10 SID—Subsystem Identification

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/0/0/PCI |
| Address Offset: | 2E–2Fh    |
| Default Value:  | 0000h     |
| Access:         | RWO       |
| Size:           | 16 bits   |

This value is used to identify a particular subsystem.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:0 | RWO<br>0000h     | <b>Subsystem ID (SUBID):</b> This field should be programmed during BIOS initialization. After it has been written once, it becomes read only. |



### 5.1.11 CAPPTR—Capabilities Pointer

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 34h  
 Default Value: E0h  
 Access: RO  
 Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>E0h        | <b>Capabilities Pointer (CAPPTR):</b> Pointer to the offset of the first capability ID register block. In this case the first capability is the product-specific Capability Identifier (CAPID0). |

### 5.1.12 PXPEPBAR—PCI Express\* Egress Port Base Address

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 40–47h  
 Default Value: 0000000000000000h  
 Access: RW, RO  
 Size: 64 bits

This is the base address for the PCI Express Egress Port MMIO Configuration space. There is no physical memory within this 4 KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Egress port MMIO configuration space is disabled and must be enabled by writing a 1 to PXPEPBAREN [Dev 0, offset 40h, bit 0]

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 63:36 | RO<br>0000000h   | Reserved  |
| 35:12 | RW<br>000000h    | <b>PCI Express Egress Port MMIO Base Address (PXPEPBAR):</b> This field corresponds to bits 35:12 of the base address PCI Express Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4 KB block of contiguous memory address space. This register ensures that a naturally aligned 4 KB space is allocated within the first 64 GB of addressable memory space. System Software uses this base address to program the (G)MCH MMIO register set. |
| 11:1  | RO<br>000h       | Reserved  |
| 0     | RW<br>0b         | <b>PXPEPBAR Enable (PXPEPBAREN):</b><br>0 = PXPEPBAR is disabled and does not claim any memory<br>1 = PXPEPBAR memory mapped accesses are claimed and decoded appropriately   |



### 5.1.13 MCHBAR—(G)MCH Memory Mapped Register Range Base

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 48–4Fh  
 Default Value: 0000000000000000h  
 Access: RW, RO  
 Size: 64 bits

This is the base address for the (G)MCH Memory Mapped Configuration space. There is no physical memory within this 16 KB window that can be addressed. The 16 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the (G)MCH MMIO Memory Mapped Configuration space is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset 48h, bit 0]

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 63:36 | RO<br>0000000h   | Reserved  |
| 35:14 | RW<br>000000h    | <b>GMCH Memory Mapped Base Address (MCHBAR):</b> This field corresponds to bits 35:14 of the base address (G)MCH Memory Mapped configuration space. BIOS will program this register resulting in a base address for a 16 KB block of contiguous memory address space. This register ensures that a naturally aligned 16 KB space is allocated. System Software uses this base address to program the (G)MCH Memory Mapped register set. |
| 13:1  | RO<br>0000h      | Reserved  |
| 0     | RW<br>0b         | <b>MCHBAR Enable (MCHBAREN):</b><br>0 = MCHBAR is disabled and does not claim any memory<br>1 = MCHBAR memory mapped accesses are claimed and decoded appropriately   |

### 5.1.14 GGC—GMCH Graphics Control Register (Intel® 82G31 GMCH Only)

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 52–53h  
 Default Value: 0030h  
 Access: RO, RW  
 Size: 16 bits

| Bit   | Access & Default | Description |
|-------|------------------|-------------|
| 15:10 | RO<br>00h        | Reserved    |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 9:8 | RW<br>0h         | <p><b>GTT Graphics Memory Size (GGMS):</b> This field is used to select the amount of main memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>00 = No memory pre-allocated. GTT cycles (Memory and I/O) are not claimed.</p> <p>01 = 1 MB of memory pre-allocated for GTT.</p> <p>10 = Reserved</p> <p>11 = Reserved</p> <p><b>Note:</b> This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.</p>   |
| 7:4 | RW<br>0011b      | <p><b>Graphics Mode Select (GMS):</b> This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>0000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80h.</p> <p>0001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer.</p> <p>0010 = DVMT (UMA) mode, 4 MB of memory pre-allocated for frame buffer.</p> <p>0011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer.</p> <p>0100 = DVMT (UMA) mode, 16 MB of memory pre-allocated for frame buffer.</p> <p>0101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer.</p> <p>0110 = DVMT (UMA) mode, 48 MB of memory pre-allocated for frame buffer.</p> <p>0111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer.</p> <p>1000 = DVMT (UMA) mode, 128 MB of memory pre-allocated for frame buffer.</p> <p>1001 = DVMT (UMA) mode, 256 MB of memory pre-allocated for frame buffer.</p> <p><b>Note:</b> This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.</p> <p><b>BIOS Requirement:</b> BIOS must not set this field to 000 if IVD (bit 1 of this register) is 0.</p> |
| 3:2 | RO<br>00b        | Reserved   |



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 1   | RW<br>0b         | <p><b>IGD VGA Disable (IVD):</b></p> <p>0 = Enable. Device 2 (IGD) claims VGA memory and I/O cycles, the Sub-Class Code within Device 2 Class Code register is 00h.</p> <p>1 = Disable. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80h.</p> <p><b>BIOS Requirement:</b> BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register) pre-allocates no memory. This bit <b>MUST</b> be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[46] = 1) or via a register (DEVEN[3] = 0).</p> |
| 0   | RO<br>0b         | Reserved  |

### 5.1.15 DEVEN—Device Enable

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 54–57h  
 Default Value: 000003DBh  
 Access: RO, RW  
 Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the (G)MCH.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:10 | RO<br>0s         | Reserved   |
| 9:6   | RO<br>1s         | Reserved   |
| 5     | RO<br>0b         | Reserved   |
| 4     | RW<br>1b         | <p><b>82G31 GMCH</b></p> <p><b>Internal Graphics Engine Function 1 (D2F1EN):</b></p> <p>0 = Bus 0, Device 2, Function 1 is disabled and hidden</p> <p>1 = Bus 0, Device 2, Function 1 is enabled and visible</p> <p>If Device 2, Function 0 is disabled and hidden, then Device 2, Function 1 is also disabled and hidden independent of the state of this bit.</p> <p>If this component is not capable of Dual Independent Display (CAPID0[78] = 1), then this bit is hardwired to 0b to hide Device 2, Function 1.</p> <p><b>82P31 MCH</b></p> <p>Reserved</p> |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 3   | RW<br>1b         | <p><b>82G31 GMCH</b></p> <p><b>Internal Graphics Engine Function 0 (D2FOEN):</b></p> <p>0 = Bus 0, Device 2, Function 0 is disabled and hidden</p> <p>1 = Bus 0, Device 2, Function 0 is enabled and visible</p> <p>If this GMCH does not have internal graphics capability (CAPID0[46] = 1), then Device 2, Function 0 is disabled and hidden independent of the state of this bit.</p> <p><b>82P31 MCH</b></p> <p>Reserved</p>   |
| 2   | RO<br>0b         | Reserved   |
| 1   | RW<br>1b         | <p><b>PCI Express Port (D1EN):</b></p> <p>0 = Bus 0, Device 1, Function 0 is disabled and hidden.</p> <p>1 = Bus 0, Device 1, Function 0 is enabled and visible.</p> <p>Default value is determined by the device capabilities (see CAPID0 [44]), SDVO Presence hardware strap and the SDVO/PCIe Concurrent hardware strap. Device 1 is Disabled on Reset if the SDVO Presence strap was sampled high, and the SDVO/PCIe Concurrent strap was sampled low at the last assertion of PWROK, and is enabled by default otherwise.</p> <p>Note: SDVO references are for the 82G31 GMCH only.</p> |
| 0   | RO<br>1b         | <p><b>Host Bridge (DOEN):</b> Bus 0, Device 0, Function 0 may not be disabled and is therefore hardwired to 1.</p>   |



### 5.1.16 PCIEXBAR—PCI Express\* Register Range Base Address

B/D/F/Type: 0/0/0/PCI  
Address Offset: 60–67h  
Default Value: 00000000E0000000h  
Access: RO, RW/L, RW/L/K  
Size: 64 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 KB of configuration space for each PCI Express device that can potentially be part of the PCI Express Hierarchy associated with the (G)MCH. There is not actual physical memory within this window of up to 256 MB that can be addressed. The actual length is determined by a field in this register. Each PCI Express Hierarchy requires a PCI Express BASE register. The (G)MCH supports one PCI Express hierarchy. The region reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. For example, MCHBAR reserves a 16 KB space and PXPEPBAR reserves a 4 KB space both outside of PCIEXBAR space. They cannot be overlaid on the space reserved by PCIEXBAR for devices 0.

On reset, this register is disabled and must be enabled by writing a 1 to the enable field in this register. This base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register), above TOLUD and still within 64 bit addressable memory space. All other bits not decoded are read only 0. The PCI Express Base Address cannot be less than the maximum address written to the Top of physical memory register (TOLUD). Software must ensure that these ranges do not overlap with known ranges located above TOLUD. Software must ensure that the sum of Length of enhanced configuration region + TOLUD + (other known ranges reserved above TOLUD) is not greater than the 36-bit addressable limit of 64 GB. In general system implementation and number of PCI/PCI Express/PCI-X buses supported in the hierarchy will dictate the length of the region.

| Bit   | Access & Default | Description |
|-------|------------------|-------------|
| 63:36 | RO<br>0000000h   | Reserved    |



| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 35:28 | RW/L<br>0Eh      | <p><b>PCI Express Base Address (PCIEXBAR):</b> This field corresponds to bits 35:28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a contiguous memory address space; size is defined by bits 2:1 of this register.</p> <p>This Base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register) above TOLUD and still within 64-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register.</p> <p>The address used to access the PCI Express configuration space for a specific device can be determined as follows:</p> <p>PCI Express Base Address + Bus Number * 1 MB + Device Number * 32 KB + Function Number * 4 KB</p> <p>The address used to access the PCI Express configuration space for Device 1 in this component would be PCI Express Base Address + 0 * 1 MB + 1 * 32 KB + 0 * 4 KB = PCI Express Base Address + 32 KB. Remember that this address is the beginning of the 4 KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.</p> |
| 27    | RW/L<br>0b       | <p><b>128 MB Base Address Mask (128ADMSK):</b> This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.</p>   |
| 26    | RW/L<br>0b       | <p><b>64 MB Base Address Mask (64ADMSK):</b> This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.</p>   |
| 25:3  | RO<br>000000h    | Reserved   |
| 2:1   | RW/L/K<br>00b    | <p><b>Length (LENGTH):</b> This Field describes the length of this region.</p> <p>Enhanced Configuration Space Region/Buses Decoded</p> <p>00 = 256 MB (buses 0–255). Bits 31:28 are decoded in the PCI Express Base Address Field</p> <p>01 = 128 MB (Buses 0–127). Bits 31:27 are decoded in the PCI Express Base Address Field.</p> <p>10 = 64 MB (Buses 0–63). Bits 31:26 are decoded in the PCI Express Base Address Field.</p> <p>11 = Reserved</p>  |
| 0     | RW/L<br>0b       | <p><b>PCIEXBAR Enable (PCIEXBAREN):</b></p> <p>0 = The PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR bits 35:26 are R/W with no functionality behind them.</p> <p>1 = The PCIEXBAR register is enabled. Memory read and write transactions whose address bits 35:26 match PCIEXBAR will be translated to configuration reads and writes within the (G)MCH. These Translated cycles are routed as shown in the table above.</p>   |



### 5.1.17 DMIBAR—Root Complex Register Range Base Address

B/D/F/Type: 0/0/0/PCI  
Address Offset: 68–6Fh  
Default Value: 0000000000000000h  
Access: RO, RW  
Size: 64 bits

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express Hierarchy associated with the (G)MCH. There is no physical memory within this 4 KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Root Complex configuration space is disabled and must be enabled by writing a 1 to DMIBAREN [Dev 0, offset 68h, bit 0].

| Bit   | Access         | Description   |
|-------|----------------|---|
| 63:36 | RO<br>0000000h | Reserved  |
| 35:12 | RW<br>000000h  | <b>DMI Base Address (DMIBAR):</b> This field corresponds to bits 35:12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4 KB block of contiguous memory address space. This register ensures that a naturally aligned 4 KB space is allocated within the first 64 GB of addressable memory space. System Software uses this base address to program the DMI register set. |
| 11:1  | RO<br>000h     | Reserved  |
| 0     | RW<br>0b       | <b>DMIBAR Enable (DMIBAREN):</b><br>0 = DMIBAR is disabled and does not claim any memory<br>1 = DMIBAR memory mapped accesses are claimed and decoded appropriately   |



### 5.1.18 PAM0—Programmable Attribute Map 0

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/0/0/PCI |
| Address Offset: | 90h       |
| Default Value:  | 00h       |
| Access:         | RO, RW    |
| Size:           | 8 bits    |

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h–0FFFFFFh. The (G)MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 768 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

- RE – Read Enable. When RE = 1, the processor read accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI\_A.
- WE – Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI\_A.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only. Each PAM Register controls two regions, typically 16 KB in size.

Note that the (G)MCH may hang if a PCI Express Graphics Attach or DMI originated access to Read Disabled or Write Disabled PAM segments occur (due to a possible IWB to non-DRAM).

For these reasons the following critical restriction is placed on the programming of the PAM regions: At the time that a DMI or PCI Express Graphics Attach accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:6 | RO<br>00b        | Reserved  |
| 5:4 | RW<br>00b        | <b>0F0000h–0FFFFFh Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0F0000h to 0FFFFFh.<br><br>00 = DRAM Disabled: All accesses are directed to DMI.<br><br>01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI.<br><br>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.<br><br>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. |
| 3:0 | RO<br>0h         | Reserved  |



### 5.1.19 PAM1—Programmable Attribute Map 1

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 91h  
 Default Value: 00h  
 Access: RO, RW  
 Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h–0C7FFFh.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:6 | RO<br>00b        | Reserved   |
| 5:4 | RW<br>00b        | <p><b>0C4000h–0C7FFFh Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0C4000 to 0C7FFF.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.</p> <p>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.</p> <p>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.</p> <p>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p>   |
| 3:2 | RO<br>00b        | Reserved   |
| 1:0 | RW<br>00b        | <p><b>0C0000h–0C3FFFh Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.</p> <p>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.</p> <p>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.</p> <p>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> |



### 5.1.20 PAM2—Programmable Attribute Map 2

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 92h  
 Default Value: 00h  
 Access: RO, RW  
 Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h–0CFFFFh.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:6 | RO<br>00b        | Reserved   |
| 5:4 | RW<br>00b        | <b>0CC000h–0CFFFFh Attribute (HIENABLE):</b><br>00 = DRAM Disabled: Accesses are directed to DMI.<br>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.<br>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.<br>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.  |
| 3:2 | RO<br>00b        | Reserved   |
| 1:0 | RW<br>00b        | <b>0C8000h–0CBFFFh Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh.<br>00 = DRAM Disabled: Accesses are directed to DMI.<br>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.<br>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.<br>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.. |



### 5.1.21 PAM3—Programmable Attribute Map 3

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 93h  
 Default Value: 00h  
 Access: RO, RW  
 Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h–0D7FFFh.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:6 | RO<br>00b        | Reserved   |
| 5:4 | RW<br>00b        | <p><b>0D4000h–0D7FFFh Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.</p> <p>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.</p> <p>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.</p> <p>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> |
| 3:2 | RO<br>00b        | Reserved   |
| 1:0 | RW<br>00b        | <p><b>0D0000–0D3FFF Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.</p> <p>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.</p> <p>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.</p> <p>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p>   |



### 5.1.22 PAM4—Programmable Attribute Map 4

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 94h  
 Default Value: 00h  
 Access: RO, RW  
 Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h–0DFFFFh.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:6 | RO<br>00b        | Reserved   |
| 5:4 | RW<br>00b        | <p><b>0DC000h–0DFFFFh Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.</p> <p>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.</p> <p>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.</p> <p>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> |
| 3:2 | RO<br>00b        | Reserved   |
| 1:0 | RW<br>00b        | <p><b>0D8000h–0DBFFFh Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.</p> <p>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.</p> <p>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.</p> <p>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> |



### 5.1.23 PAM5—Programmable Attribute Map 5

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 95h  
 Default Value: 00h  
 Access: RO, RW  
 Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h–0E7FFFh.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:6 | RO<br>00b        | Reserved   |
| 5:4 | RW<br>00b        | <p><b>0E4000h–0E7FFFh Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.</p> <p>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.</p> <p>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.</p> <p>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> |
| 3:2 | RO<br>00b        | Reserved   |
| 1:0 | RW<br>00b        | <p><b>0E0000h–0E3FFFh Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.</p> <p>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.</p> <p>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.</p> <p>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> |



### 5.1.24 PAM6—Programmable Attribute Map 6

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 96h  
 Default Value: 00h  
 Access: RO, RW  
 Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h–0EFFFFh.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:6 | RO<br>00b        | Reserved   |
| 5:4 | RW<br>00b        | <p><b>0EC000h–0EFFFFh Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.</p> <p>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.</p> <p>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.</p> <p>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> |
| 3:2 | RO<br>00b        | Reserved   |
| 1:0 | RW<br>00b        | <p><b>0E8000h–0EBFFFh Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.</p> <p>01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.</p> <p>10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.</p> <p>11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> |



### 5.1.25 LAC—Legacy Access Control

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 97h  
 Default Value: 00h  
 Access: RW, RO, RW  
 Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15–16 MB.

| Bit   | Access & Default | Description  |       |      |             |   |   |   |   |   |                     |   |   |   |   |   |   |
|-------|------------------|--|-------|------|-------------|---|---|---|---|---|---------------------|---|---|---|---|---|---|
| 7     | RW<br>0b         | <p><b>Hole Enable (HEN):</b> This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped.</p> <p>0 = No memory hole.<br/>                     1 = Memory hole from 15 MB to 16 MB..</p>   |       |      |             |   |   |   |   |   |                     |   |   |   |   |   |   |
| 6:1   | RO<br>00000b     | Reserved   |       |      |             |   |   |   |   |   |                     |   |   |   |   |   |   |
| 0     | RW<br>0b         | <p><b>MDA Present (MDAP):</b> This bit works with the VGA Enable bits in the BCTRL register of Device 1 to control the routing of processor initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1's VGA Enable bit is not set.</p> <p>If device 1's VGA enable bit is not set, then accesses to IO address range x3BCh–x3BFh are forwarded to DMI.</p> <p>If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh–x3BFh are forwarded to PCI Express if the address is within the corresponding IOBASE and IOLIMIT, otherwise they are forwarded to DMI.</p> <p>MDA resources are defined as the following:</p> <p>Memory: 0B0000h – 0B7FFFh<br/>                     I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode)</p> <p>Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the DMI even if the reference includes I/O locations not listed above.</p> <p>The following table shows the behavior for all combinations of MDA and VGA:</p> <table border="1"> <thead> <tr> <th>VGAEN</th> <th>MDAP</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>All References to MDA and VGA space are routed to DMI</td> </tr> <tr> <td>0</td> <td>1</td> <td>Invalid combination</td> </tr> <tr> <td>1</td> <td>0</td> <td>All VGA and MDA references are routed to PCI Express Graphics Attach.</td> </tr> <tr> <td>1</td> <td>1</td> <td>All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to DMI.</td> </tr> </tbody> </table> <p>VGA and MDA memory cycles can only be routed across the PEG when MAE (PCICMD1[1]) is set. VGA and MDA I/O cycles can only be routed across the PEG if IOAE (PCICMD1[0]) is set.</p> | VGAEN | MDAP | Description | 0 | 0 | All References to MDA and VGA space are routed to DMI | 0 | 1 | Invalid combination | 1 | 0 | All VGA and MDA references are routed to PCI Express Graphics Attach. | 1 | 1 | All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to DMI. |
| VGAEN | MDAP             | Description  |       |      |             |   |   |   |   |   |                     |   |   |   |   |   |   |
| 0     | 0                | All References to MDA and VGA space are routed to DMI  |       |      |             |   |   |   |   |   |                     |   |   |   |   |   |   |
| 0     | 1                | Invalid combination  |       |      |             |   |   |   |   |   |                     |   |   |   |   |   |   |
| 1     | 0                | All VGA and MDA references are routed to PCI Express Graphics Attach.  |       |      |             |   |   |   |   |   |                     |   |   |   |   |   |   |
| 1     | 1                | All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to DMI.  |       |      |             |   |   |   |   |   |                     |   |   |   |   |   |   |



### 5.1.26 REMAPBASE—Remap Base Address Register

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 98–99h  
 Default Value: 03FFh  
 Access: RO, RW  
 Size: 16 bits

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>000000b    | Reserved  |
| 9:0   | RW<br>3FFh       | <p><b>Remap Base Address [35:26] (REMAPBASE):</b> The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the Remap Base Address are assumed to be 0s. Thus, the bottom of the defined memory range will be aligned to a 64 MB boundary.</p> <p>When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled.</p> |

### 5.1.27 REMAPLIMIT—Remap Limit Address Register

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 9A–9Bh  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>000000b    | Reserved  |
| 9:0   | RW<br>000h       | <p><b>Remap Limit Address [35:26] (REMAPLMT):</b> The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the remap limit address are assumed to be Fhs. Thus the top of the defined range will be one less than a 64 MB boundary.</p> <p>When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled.</p> |



### 5.1.28 SMRAM—System Management RAM Control

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 9Dh  
 Default Value: 02h  
 Access: RO, RW/L, RW, RW/L/K  
 Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G\_SMFRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7   | RO<br>0b         | Reserved  |
| 6   | RW/L<br>0b       | <b>SMM Space Open (D_OPEN):</b> When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.  |
| 5   | RW<br>0b         | <b>SMM Space Closed (D_CLS):</b> When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.  |
| 4   | RW/L/K<br>0b     | <b>SMM Space Locked (D_LCK):</b> When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMFRAME_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function. |
| 3   | RW/L<br>0b       | <b>Global SMRAM Enable (G_SMFRAME):</b> If set to a 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.   |
| 2:0 | RO<br>0b         | <b>Compatible SMM Space Base Segment (C_BASE_SEG):</b> This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the (G)MCH supports only the SMM space between A0000 and BFFFF, this field is hardwired to 010.   |



### 5.1.29 ESMRAMC—Extended System Management RAM Control

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 9Eh  
 Default Value: 38h  
 Access: RW, RWC, RO  
 Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E\_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7   | RW<br>0b         | <b>Enable High SMRAM (H_SMRAME):</b> This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB) When G_SMRAME is 1 and H_SMRAME is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.  |
| 6   | RWC<br>0b        | <b>Invalid SMRAM Access (E_SMERR):</b> This bit is set when processor has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.  |
| 5   | RO<br>1b         | <b>SMRAM Cacheable (SM_CACHE):</b> This bit is forced to 1 by the (G)MCH.   |
| 4   | RO<br>1b         | <b>L1 Cache Enable for SMRAM (SM_L1):</b> This bit is forced to 1 by the (G)MCH.  |
| 3   | RO<br>1b         | <b>L2 Cache Enable for SMRAM (SM_L2):</b> This bit is forced to 1 by the (G)MCH.  |
| 2:1 | RW<br>00b        | <b>TSEG Size (TSEG_SZ):</b> Selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to DMI when the TSEG memory block is enabled.<br><br>00 = 1 MB TSEG. (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size – 1 MB) to (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size).<br><br>01 = 2 MB TSEG. (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size – 2 MB) to (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size).<br><br>10 = 8 MB TSEG. (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size – 8 MB) to (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size).<br><br>11 = Reserved.<br><br>Once D_LCK has been set, these bits becomes read only. |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 0   | RW<br>0b         | <b>TSEG Enable (T_EN)</b> : Enabling of SMRAM memory for Extended SMRAM space only. When G_SMROME = 1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only. |

### 5.1.30 TOM—Top of Memory

B/D/F/Type: 0/0/0/PCI  
 Address Offset: A0–A1h  
 Default Value: 0001h  
 Access: RO, RW  
 Size: 16 bits

This Register contains the size of physical memory. BIOS determines the memory size reported to the OS using this Register.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>00h        | Reserved  |
| 9:0   | RW<br>001h       | <b>Top of Memory (TOM)</b> : This register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped I/O). These bits correspond to address bits 35:26 (64 MB granularity). Bits 25:0 are assumed to be 0. |



### 5.1.31 TOUUD—Top of Upper Usable Dram

B/D/F/Type: 0/0/0/PCI  
Address Offset: A2–A3h  
Default Value: 0000h  
Access: RW  
Size: 16 bits

This 16 bit register defines the Top of Upper Usable DRAM.

Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to (reclaim limit + 1 byte) 64 MB aligned since reclaim limit is 64 MB aligned. Address bits 19:0 are assumed to be 000\_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4 GB.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:0 | RW<br>0000h      | <b>TOUUD (TOUUD):</b> This register contains bits 35:20 of an address one byte above the maximum DRAM memory above 4 GB that is usable by the operating system. Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to (reclaim limit + 1 byte) 64 MB aligned since reclaim limit is 64 MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4 GB. |



### 5.1.32 GBSM—Graphics Base of Stolen Memory

B/D/F/Type: 0/0/0/PCI  
 Address Offset: A4–A7h  
 Default Value: 00000000h  
 Access: RW, RO  
 Size: 32 bits

This register contains the base address of graphics data stolen DRAM memory. BIOS determines the base of graphics data stolen memory by subtracting the graphics data stolen memory size (PCI Device 0 offset 52h bits 7:4) from TOLUD (PCI Device 0, offset B0h, bits 15:4).

**Note:** This register is locked and becomes Read Only when the D\_LCK bit in the SMRAM register is set.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:20 | RW<br>000h       | <b>Graphics Base of Stolen Memory (GBSM):</b> This register contains bits 31:20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0, offset 52h, bits 6:4) from TOLUD (PCI Device 0, offset B0h, bits 15:04).<br><br><b>Note:</b> This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. |
| 19:0  | RO<br>00000h     | Reserved  |



### 5.1.33 BGSM—Base of GTT stolen Memory

B/D/F/Type: 0/0/0/PCI  
 Address Offset: A8–ABh  
 Default Value: 00000000h  
 Access: RW/L, RO  
 Size: 32 bits

This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 9:8) from the graphics stolen memory base (PCI Device 0, offset A4h, bits 31:20).

**Note:** This register is locked and becomes Read Only when the D\_LCK bit in the SMRAM register is set.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:20 | RW/L<br>000h     | <b>Graphics Base of Stolen Memory (GBSM):</b> This register contains bits 31:20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0, offset 52h, bits 9:8) from the graphics stolen memory base (PCI Device 0, offset A4h, bits 31:20).<br><br><b>Note:</b> This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. |
| 19:0  | RO<br>00000h     | Reserved  |

### 5.1.34 TSEGMB—TSEG Memory Base

B/D/F/Type: 0/0/0/PCI  
 Address Offset: AC–AFh  
 Default Value: 00000000h  
 Access: RW/L, RO  
 Size: 32 bits

This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory by subtracting the TSEG size (PCI Device 0, offset 9Eh, bits 2:1) from graphics GTT stolen base (PCI Device 0, offset A8h, bits 31:20).

Once D\_LCK has been set, these bits becomes read only.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:20 | RW/L<br>000h     | <b>TSEG Memory base (TSEGMB):</b> This register contains bits 31:20 of the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory by subtracting the TSEG size (PCI Device 0, offset 9Eh, bits 2:1) from graphics GTT stolen base (PCI Device 0, offset A8h, bits 31:20).<br><br>Once D_LCK has been set, these bits becomes read only. |
| 19:0  | RO<br>00000h     | Reserved   |



### 5.1.35 TOLUD—Top of Low Usable DRAM

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/0/0/PCI |
| Address Offset: | B0–B1h    |
| Default Value:  | 0010h     |
| Access:         | RW, RO    |
| Size:           | 16 bits   |

This 16 bit register defines the Top of Low Usable DRAM. TSEG, GTT Graphics Memory and Graphics Stolen Memory are within the DRAM space defined. From the top, (G)MCH optionally claims 1 to 64 MB of DRAM for internal graphics if enabled 1, 2 MB of DRAM for GTT Graphics Stolen Memory (if enabled) and 1, 2, or 8 MB of DRAM for TSEG, if enabled.

#### Programming Example :

C1DRB3 is set to 4 GB

TSEG is enabled and TSEG size is set to 1 MB

Internal Graphics is enabled and Graphics Mode Select set to 32 MB

GTT Graphics Stolen Memory Size set to 2 MB

BIOS knows the OS requires 1 GB of PCI space.

BIOS also knows the range from FEC0\_0000h to FFFF\_FFFFh is not usable by the system. This 20MB range at the very top of addressable memory space is lost to APIC.

According to the above equation, TOLUD is originally calculated to:

4 GB = 1\_0000\_0000h

The system memory requirements are: 4GB (max addressable space) – 1 GB (PCI space) – 35 MB (lost memory) = 3 GB – 35 MB (minimum granularity) = ECB0\_0000h

Since ECB0\_0000h (PCI and other system requirements) is less than 1\_0000\_0000h, TOLUD should be programmed to ECBh.



| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:4 | RW<br>001h       | <p><b>Top of Low Usable DRAM (TOLUD):</b> This register contains bits 31:20 of an address one byte above the maximum DRAM memory below 4 GB that is usable by the operating system. Address bits 31:20 programmed to 01h implies a minimum memory size of 1 MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register.</p> <p>Note that the Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and TSEG. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by TSEG size to determine base of TSEG.</p> <p>This register must be 64 MB aligned when reclaim is enabled.</p> |
| 3:0  | RO<br>0000b      | Reserved  |

### 5.1.36 ERRSTS—Error Status

B/D/F/Type: 0/0/0/PCI  
 Address Offset: C8–C9h  
 Default Value: 0000h  
 Access: RO, RWC/S  
 Size: 16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. An SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers).

These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 15  | RO<br>0b         | Reserved   |
| 14  | RWC/S<br>0b      | <p><b>Isochronous TBWRR Run Behind FIFO Full (ITCV):</b></p> <p>If set, this bit indicates a VC1 TBWRR is running behind, resulting in the slot timer to stop until the request is able to complete.</p> <p>If this bit is already set, then an interrupt message will not be sent on a new error event.</p> |



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 13  | RWC/S<br>0b      | <p><b>Isochronous TBWRR Run behind FIFO Put (ITSTV):</b></p> <p>If set, this bit indicates a VC1 TBWRR request was put into the run behind. This will likely result in a resulting in a contract violation due to the (G)MCH Express port taking too long to service the isochronous request.</p> <p>If this bit is already set, then an interrupt message will not be sent on a new error event.</p>   |
| 12  | RWC/S<br>0b      | <p><b>(G)MCH Software Generated Event for SMI (GSGESMI):</b> This indicates the source of the SMI was a Device 2 Software Event.</p>  |
| 11  | RWC/S<br>0b      | <p><b>(G)MCH Thermal Sensor Event for SMI/SCI/SERR (GTSE):</b> This bit indicates that a (G)MCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is invalid). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event.</p> |
| 10  | RO<br>0b         | Reserved  |
| 9   | RWC/S<br>0b      | <p><b>LOCK to non-DRAM Memory Flag (LCKF):</b></p> <p>1 = (G)MCH has detected a lock operation to memory space that did not map into DRAM.</p>  |
| 8   | RO<br>0b         | Reserved  |
| 7   | RWC/S<br>0b      | <p><b>DRAM Throttle Flag (DTF):</b></p> <p>1 = DRAM Throttling condition occurred.</p> <p>0 = Software has cleared this flag since the most recent throttling event.</p>  |
| 6:0 | RO<br>0s         | Reserved  |



### 5.1.37 ERRCMD—Error Command

B/D/F/Type: 0/0/0/PCI  
 Address Offset: CA–CBh  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

This register controls the (G)MCH responses to various system errors. Since the (G)MCH does not have an SERR# signal, SERR messages are passed from the (G)MCH to the ICH over DMI.

When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:12 | RO<br>0h         | Reserved  |
| 11    | RW<br>0b         | <b>SERR on (G)MCH Thermal Sensor Event (TSESERR):</b><br>1 = The (G)MCH generates a DMI SERR special cycle when bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event.<br>0 = Reporting of this condition via SERR messaging is disabled. |
| 10    | RO<br>0b         | Reserved  |
| 9     | RW<br>0b         | <b>SERR on LOCK to non-DRAM Memory (LCKERR):</b><br>1 = The (G)MCH will generate a DMI SERR special cycle whenever a processor lock cycle is detected that does not hit DRAM.<br>0 = Reporting of this condition via SERR messaging is disabled.  |
| 8:7   | RW<br>00b        | Reserved  |
| 6:0   | RO<br>0s         | Reserved  |



### 5.1.38 SMICMD—SMI Command

B/D/F/Type: 0/0/0/PCI  
 Address Offset: CC-CDh  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:12 | RO<br>0h         | Reserved  |
| 11    | RW<br>0b         | <b>SMI on (G)MCH Thermal Sensor Trip (TSTSMI):</b><br><br>1 = A SMI DMI special cycle is generated by (G)MCH when the thermal sensor trip requires an SMI. A thermal sensor trip point cannot generate more than one special cycle.<br><br>0 = Reporting of this condition via SMI messaging is disabled. |
| 10:0  | RO<br>0s         | Reserved  |

### 5.1.39 SKPD—Scratchpad Data

B/D/F/Type: 0/0/0/PCI  
 Address Offset: DC-DFh  
 Default Value: 00000000h  
 Access: RW  
 Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 31:0 | RW<br>00000000h  | <b>Scratchpad Data (SKPD):</b> 1 DWord of data storage. |



### 5.1.40 CAPID0—Capability Identifier

B/D/F/Type: 0/0/0/PCI  
 Address Offset: E0–EAh  
 Default Value: 000001000000000010B0009h  
 Access: RO  
 Size: 88 bits

Control of bits in this register are only required for customer visible SKU differentiation.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 87:79 | RO<br>0s         | Reserved   |
| 78    | RO<br>0b         | <p><b>82G31 GMCH</b></p> <p><b>Dual Independent Display Disable (DIDD):</b> This bit determines whether the component is capable of Dual Independent Display functionality. This functionality requires both functions (0 and 1) to be visible in the Internal Graphics Device 2. This capability is only meaningful if the component is capable of Internal Graphics.</p> <p>Definitions:</p> <ul style="list-style-type: none"> <li>• Clone mode – Same Image. Different display timing on each pipe.</li> <li>• Twin mode – Same Image. Same exact display timings.</li> <li>• Extended Desktop mode – Unique images. Different display timings on each pipe.</li> </ul> <p>When Device 2 Function 1 is hidden, the second controller and its associated frame buffer are no longer visible to the Operating System. The OS thinks our device has only one display controller and stops supporting Extended Desktop mode.</p> <p>0 = Capable of Dual Independent Display (independent frame buffers), Extended Desktop mode is supported.</p> <p>1 = Not capable of Dual Independent Display. Hardwires bit 4 of the Device Enable (DEVEN) register (Device 0 Offset 54h) to '0'. Clone mode and twin mode are still supported (single frame buffer).</p> <p><b>82P31 MCH</b></p> <p>Reserved</p> |
| 77    | RO<br>0b         | <p><b>Dual Channel Disable (DCD):</b></p> <p>0 = Dual channel operation allowed</p> <p>1 = Only single channel operation allowed</p>   |
| 76    | RO<br>1b         | <p><b>2 DIMMS per Channel Disable (2DPCD):</b> This bit is 1 indicating support for 1 DIMM per channel.</p>  |
| 75:71 | RO<br>0000b      | Reserved   |



| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 70    | RO<br>0b         | <p><b>Multiprocessor Disable (MD):</b></p> <p>0 = (G)MCH capable of Multiple Processors</p> <p>1 = (G)MCH capable of uni-processor only.</p>   |
| 69    | RO<br>0b         | <p><b>FAN Speed Control Disable (FSCD):</b> Not supported.</p>   |
| 68:52 | RO<br>0s         | Reserved   |
| 51    | RO<br>0b         | <p><b>VLD and IDCT Disable (VLDIDCTD):</b></p> <p>0 = Enable VLD and IDCT</p> <p>1 = Disable VLD and IDCT</p>  |
| 50:48 | RO<br>0s         | Reserved   |
| 47    | RO<br>0b         | <p><b>82G31 GMCH</b></p> <p><b>3D Integrated graphics Disable (3DIGD):</b></p> <p>0 = 3D Internal Graphics are enabled</p> <p>1 = 3D Internal Graphics are disabled. VGA still supported</p> <p><b>82P31 MCH</b></p> <p>Reserved</p>   |
| 46    | RO<br>0b         | <p><b>82G31 GMCH</b></p> <p><b>Internal Graphics Disable (IGD):</b></p> <p>0 = There is a graphics engine within this GMCH. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the GMCH. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control register in Device 1 (If PCI Express graphics attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GMCH Control Register). Graphics Memory is pre-allocated above TSEG Memory.</p> <p>1 = There is no graphics engine within this GMCH. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Device 1. DEVEN [4:3] (Device 0, offset 54h) have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.</p> <p><b>82P31 MCH</b></p> <p>Reserved</p> |



| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 45    | RO<br>0b         | <p><b>PEG Port x16 Disable (PEGX16D):</b></p> <p>0 = Capable of x16 PEG Port.</p> <p>1 = Not Capable of x16 PEG port, instead PEG limited to x8 and below. Causes PEG port to enable and train logical lanes 7:0 only. Logical lanes 15:8 are powered down, and the Max Link Width field of the Link Capability register reports x8 instead of x16. (in the case of lane reversal, lanes 15:8 are active and lanes 7:0 are powered down)</p>   |
| 44    | RO<br>0b         | <p><b>PCI Express Port Disable (PEGPD):</b></p> <p>0 = There is a PCI Express Port on this (G)MCH. Device 1 and associated memory spaces are accessible. All non-SIMM memory and I/O accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Device 1 and VGA settings controlling internal graphics VGA if internal graphics is enabled.</p> <p>1 = There is no PCI Express Port on this (G)MCH. Device 1 and associated memory and IO spaces are disabled by hardwiring the D1EN field bit 1 of the Device Enable register (DEVEN Dev 0 Offset 54h). In addition, Next_Pointer = 00h, VGA memory and I/O cannot decode to the PCI Express interface. From a Physical Layer perspective, all 16 lanes are powered down and the link does not attempt to train.</p> |
| 43:34 | RO<br>0s         | Reserved   |
| 33:31 | RO<br>000b       | <p><b>DDR Frequency Capability (DDRFC):</b> This field controls which values may be written to the Memory Frequency Select field 6:4 of the Clocking Configuration registers (MCHBAR Offset C00h). Any attempt to write an unsupported value will be ignored.</p> <p>000 = (G)MCH capable of "All" memory frequencies<br/>           001 = Reserved<br/>           010 = Reserved<br/>           011 = Reserved<br/>           100 = (G)MCH capable of up to DDR2 1067<br/>           101 = (G)MCH capable of up to DDR2 800<br/>           110 = (G)MCH capable of up to DDR2 667</p>   |



| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 30:28 | RO<br>000b       | <p><b>FSB Frequency Capability (FSBFC):</b> This field controls which values are allowed in the FSB Frequency Select Field 2:0 of the Clocking Configuration Register. These values are determined by the BSEL[2:0] frequency straps. Any unsupported strap values will render the (G)MCH System Memory Interface inoperable.</p> <p>000 = (G)MCH capable of "All" Memory Frequencies<br/>                     001 = Reserved<br/>                     010 = Reserved<br/>                     011 = Reserved<br/>                     100 = (G)MCH capable of up to FSB 1067<br/>                     101 = (G)MCH capable of up to FSB 800<br/>                     110 = (G)MCH capable of up to FSB 667</p> |
| 27:24 | RO<br>1h         | <p><b>CAPID Version (CAPIDV):</b> This field has the value 0001b to identify the first revision of the CAPID register definition.</p>   |
| 23:16 | RO<br>0bh        | <p><b>CAPID Length (CAPIDL):</b> This field has the value 0bh to indicate the structure length (11 bytes).</p>  |
| 15:8  | RO<br>00h        | <p><b>Next Capability Pointer (NCP):</b> This field is hardwired to 00h indicating the end of the capabilities linked list.</p>   |
| 7:0   | RO<br>09h        | <p><b>Capability Identifier (CAP_ID):</b> This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.</p>   |



## 5.2 MCHBAR

The MCHBAR registers are offset from the MCHBAR base address. Table 5-2 provides an address map of the registers listed by address offset in ascending order. Detailed register bit descriptions follow the table.

**Table 5-2. MCHBAR Register Address Map**

| Address Offset | Register Symbol | Register Name                          | Default Value  | Access     |
|----------------|-----------------|--|----------------|------------|
| 111h           | CHDECMISC       | Channel Decode Miscellaneous           | 00h            | RW         |
| 200–01h        | C0DRB0          | Channel 0 DRAM Rank Boundary Address 0 | 0000h          | RO, RW     |
| 250–251h       | C0CYCTRKPCHG    | Channel 0 CYCTRK PCHG                  | 0000h          | RW, RO     |
| 252–255h       | C0CYCTRKACT     | Channel 0 CYCTRK ACT                   | 00000000h      | RW, RO     |
| 256–257h       | C0CYCTRKWR      | Channel 0 CYCTRK WR                    | 0000h          | RW         |
| 258–25Ah       | C0CYCTRKRCD     | Channel 0 CYCTRK READ                  | 000000h        | RW, RO     |
| 25B–25Ch       | C0CYCTRKREFR    | Channel 0 CYCTRK REFR                  | 0000h          | RO, RW     |
| 260–263h       | C0CKECTRL       | Channel 0 CKE Control                  | 00000800h      | RO, RW, RW |
| 269–26Eh       | C0REFRCTRL      | Channel 0 DRAM Refresh Control         | 021830000 C30h | RW, RO     |
| 29C–29Fh       | C0ODTCTRL       | Channel 0 ODT Control                  | 00000000h      | RO, RW     |
| 600–601h       | C1DRB0          | Channel 1 DRAM Rank Boundary Address 0 | 0000h          | RW, RO     |
| 602–603h       | C1DRB1          | Channel 1 DRAM Rank Boundary Address 1 | 0000h          | RW, RO     |
| 604–605h       | C1DRB2          | Channel 1 DRAM Rank Boundary Address 2 | 0000h          | RW, RO     |
| 606–607h       | C1DRB3          | Channel 1 DRAM Rank Boundary Address 3 | 0000h          | RW, RO     |
| 608–609h       | C1DRA01         | Channel 1 DRAM Rank 0,1 Attributes     | 0000h          | RW,        |
| 60A–60Bh       | C1DRA23         | Channel 1 DRAM Rank 2,3 Attributes     | 0000h          | RW         |
| 650–651h       | C1CYCTRKPCHG    | Channel 1 CYCTRK PCHG                  | 0000h          | RO, RW     |
| 652–655h       | C1CYCTRKACT     | Channel 1 CYCTRK ACT                   | 00000000h      | RO, RW     |
| 656–657h       | C1CYCTRKWR      | Channel 1 CYCTRK WR                    | 0000h          | RW,        |
| 658–65Ah       | C1CYCTRKRCD     | Channel 1 CYCTRK READ                  | 000000h        | RO, RW     |
| 660–663h       | C1CKECTRL       | Channel 1 CKE Control                  | 00000800h      | RW, RW, RO |
| 669–66Eh       | C1REFRCTRL      | Channel 1 DRAM Refresh Control         | 021830000 C30h | RW, RO     |
| 69C–69Fh       | C1ODTCTRL       | Channel 1 ODT Control                  | 00000000h      | RO, RW     |



| Address Offset | Register Symbol | Register Name                             | Default Value | Access           |
|----------------|-----------------|---|---------------|------------------|
| A00– A01h      | EPCODRB0        | EP Channel 0 DRAM Rank Boundary Address 0 | 0000h         | RW, RO           |
| A02– A03h      | EPCODRB1        | EP Channel 0 DRAM Rank Boundary Address 1 | 0000h         | RO, RW           |
| A04– A05h      | EPCODRB2        | EP Channel 0 DRAM Rank Boundary Address 2 | 0000h         | RO, RW           |
| A06– A07h      | EPCODRB3        | EP Channel 0 DRAM Rank Boundary Address 3 | 0000h         | RW, RO           |
| A08– A09h      | EPCODRA01       | EP Channel 0 DRAM Rank 0,1 Attribute      | 0000h         | RW               |
| A0A– A0Bh      | EPCODRA23       | EP Channel 0 DRAM Rank 2,3 Attribute      | 0000h         | RW               |
| A19– A1Ah      | EPDCYCTRKWRTPRE | EPD CYCTRK WRT PRE                        | 0000h         | RW, RO           |
| A1C– A1Fh      | EPDCYCTRKWRTACT | EPD CYCTRK WRT ACT                        | 00000000h     | RO, RW           |
| A20– A21h      | EPDCYCTRKWRTWR  | EPD CYCTRK WRT WR                         | 0000h         | RW, RO           |
| A22– A23h      | EPDCYCTRKWRTREF | EPD CYCTRK WRT REF                        | 0000h         | RO, RW           |
| A24– A26h      | EPDCYCTRKWRTRD  | EPD CYCTRK WRT READ                       | 000000h       | RW               |
| A28– A33h      | EPDCKECONFIGREG | EPD CKE related configuration registers   | 00E0000000h   | RW               |
| A30–A33h       | EPDREFCONFIG    | EP DRAM Refresh Configuration             | 40000C30h     | RO, RW           |
| CD8h           | TSC1            | Thermal Sensor Control 1                  | 00h           | RW/L, RW, RS/WC  |
| CD9h           | TSC2            | Thermal Sensor Control 2                  | 00h           | RW/L, RO         |
| CDAh           | TSS             | Thermal Sensor Status                     | 00h           | RO               |
| CDC–CDFh       | TSTTP           | Thermal Sensor Temperature Trip Point     | 00000000h     | RO, RW, RW/L     |
| CE2h           | TCO             | Thermal Calibration Offset                | 00h           | RW/L/K, RW/L     |
| CE4h           | THERM1          | Hardware Throttle Control                 | 00h           | RW/L, RO, RW/L/K |
| CEA–CEBh       | TIS             | Thermal Interrupt Status                  | 0000h         | RO, RWC          |
| CF1h           | TSMICMD         | Thermal SMI Command                       | 00h           | RO, RW           |
| F14–F17h       | PMSTS           | Power Management Status                   | 00000000h     | RWC/S, RO        |



### 5.2.1 CHDECMISC—Channel Decode Miscellaneous

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 111h  
 Default Value: 00h  
 Access: RW  
 Size: 8 bits

This register has Miscellaneous CHDEC/MAGEN configuration bits.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7   | RW<br>0b         | Reserved   |
| 6:5 | RW<br>00b        | <b>Enhanced Mode Select (ENHMODESEL):</b><br>00 = Swap Enabled for Bank Selects and Rank Selects<br>01 = XOR Enabled for Bank Selects and Rank Selects<br>10 = Swap Enabled for Bank Selects only<br>11 = XOR Enabled for Bank Select only |
| 4   | RW<br>0b         | <b>Ch2 Enhanced Mode (CH2_ENHMODE):</b> This bit enables Enhanced addressing mode of operation is enabled for Ch 2.<br>0 = Disable<br>1 = Enable   |
| 3   | RW<br>0b         | <b>Ch1 Enhanced Mode (CH1_ENHMODE):</b> This bit enables Enhanced addressing mode of operation is enabled for Ch 1.<br>0 = Disable<br>1 = Enable   |
| 2   | RW<br>0b         | <b>Ch0 Enhanced Mode (CH0_ENHMODE):</b> This bit enables Enhanced addressing mode of operation is enabled for Ch 0.<br>0 = Disable<br>1 = Enable   |
| 1   | RW<br>0b         | Reserved   |
| 0   | RW<br>0b         | <b>EP Present (EPPRSNT):</b> This bit indicates whether EP UMA is present in the system or not.<br>0 = Not Present<br>1 = Present  |



### 5.2.2 CODRB0—Channel 0 DRAM Rank Boundary Address 0

|                 |              |
|-----------------|--------------|
| B/D/F/Type:     | 0/0/0/MCHBAR |
| Address Offset: | 200–201h     |
| Default Value:  | 0000h        |
| Access:         | RW, RO       |
| Size:           | 16 bits      |

The DRAM Rank Boundary Registers define the upper boundary address of each DRAM rank with a granularity of 64 MB. Each rank has its own single-word DRB register. These registers are used to determine which chip select will be active for a given address. Channel and rank map:

- Ch 0, Rank 0 = 200h
- Ch 0, Rank 1 = 202h
- Ch 1, Rank 0 = 600h
- Ch 1, Rank 1 = 602h

#### Programming Guide

##### Non-Stacked Mode

If Channel 0 is empty, all of the C0DRBs are programmed with 00h.

- C0DRB0 = Total memory in Ch 0, Rank 0 (in 64 MB increments)
- C0DRB1 = Total memory in Ch 0, Rank 0 + Ch 0, Rank 1 (in 64 MB increments)
- ...

If Channel 1 is empty, all of the C1DRBs are programmed with 00h

- C1DRB0= Total memory in Ch 1, Rank 0 (in 64 MB increments)
- C1DRB1= Total memory in Ch 1, Rank 0 + Ch 1, Rank 1 (in 64 MB increments)
- ...

##### Stacked Mode

CODRBs:

Similar to Non-stacked mode.

C1DRB0, C1DRB1 and C1DRB2:

They are also programmed similar to non-stacked mode. Only exception is, the DRBs corresponding to the topmost populated rank and the (unpopulated) higher ranks in Channel 1 must be programmed with the value of the total Channel 1 population plus the value of total Channel 0 population (C0DRB3).

Example: If only ranks 0 and 1 are populated in Ch1 in stacked mode, then

- C1DRB0 = Total memory in ch1 rank0 (in 64MB increments)
- C1DRB1 = C0DRB3 + Total memory in ch1 rank0 + ch1 rank1 (in 64 MB increments)  
(rank 1 is the topmost populated rank)
- C1DRB2 = C1DRB1



C1DRB3 = C1DRB1

C1DRB3:

C1DRB3 = C0DRB3 + Total memory in Channel 1.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>000000b    | Reserved  |
| 9:0   | RW<br>000h       | <p><b>Channel 0 Dram Rank Boundary Address 0 (C0DRBA0):</b> This register defines the DRAM rank boundary for rank0 of Channel 0 (64 MB granularity)</p> <p>= R0</p> <p>R0 = Total Rank 0 memory size is 64 MB</p> <p>R1 = Total Rank 1 memory size is 64 MB</p> |

### 5.2.3 COCYTRKPCHG—Channel 0 CYCTRK PCHG

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 250–251h  
 Default Value: 0000h  
 Access: RW, RO  
 Size: 16 bits

This register provides Channel 0 CYCTRK Precharge.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:11 | RO<br>00000b     | Reserved  |
| 10:6  | RW<br>00000b     | <p><b>Write To PRE Delayed (C0sd_cr_wr_pchg):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank. This field corresponds to <math>t_{WR}</math> in the DDR Specification.</p> |
| 5:2   | RW<br>0000b      | <p><b>READ To PRE Delayed (C0sd_cr_rd_pchg):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank.</p>   |
| 1:0   | RW<br>00b        | <p><b>PRE To PRE Delayed (C0sd_cr_pchg_pchg):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two PRE commands to the same rank.</p>  |



### 5.2.4 COCYTRKACT—Channel 0 CYCTRK ACT

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 252–255h  
 Default Value: 00000000h  
 Access: RW, RO  
 Size: 32 bits

This register provides Channel 0 CYCTRK Activate.

| Bit   | Access & Default     | Description  |
|-------|----------------------|--|
| 31:28 | RO<br>0h             | Reserved   |
| 27:22 | RW<br>000000b        | <b>ACT Window Count (C0sd_cr_act_windowcnt):</b> This field indicates the window duration (in DRAM clocks) during which the controller counts the # of activate commands which are launched to a particular rank. If the number of activate commands launched within this window is greater than 4, then a check is implemented to block launch of further activates to this rank for the rest of the duration of this window. |
| 21    | RW<br>0b             | <b>Max ACT Check Disable (C0sd_cr_maxact_dischk):</b> This field disenables the check which ensures that there are no more than four activates to a particular rank in a given window.   |
| 20:17 | RW<br>0000b          | <b>ACT to ACT Delayed (C0sd_cr_act_act[]):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank. This field corresponds to $t_{RRD}$ in the DDR Specification.  |
| 16:13 | RW<br>0000b          | <b>PRE to ACT Delayed (C0sd_cr_pre_act):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank. This field corresponds to $t_{RP}$ in the DDR Specification.  |
| 12:9  | RW<br>0h             | <b>ALLPRE to ACT Delay (C0sd0_cr_preall_act):</b> From the launch of a prechargeall command wait for these many # of memory clocks before launching a activate command. This field corresponds to $t_{PALL\_RP}$ .   |
| 8:0   | RW<br>00000000<br>0b | <b>REF to ACT Delayed (C0sd_cr_rfsh_act):</b> This configuration register indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank. This field corresponds to $t_{RFC}$ in the DDR Specification.  |



### 5.2.5 COCYCTRKWR—Channel 0 CYCTRK WR

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: 256–257h  
Default Value: 0000h  
Access: RW  
Size: 16 bits

This register provides Channel 0 CYCTRK WR.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:12 | RW<br>0h         | <b>ACT To Write Delay (C0sd_cr_act_wr):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank. This field corresponds to $t_{RCD\_wr}$ in the DDR Specification.       |
| 11:8  | RW<br>0h         | <b>Same Rank Write To Write Delay (C0sd_cr_wrsr_wr):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.   |
| 7:4   | RW<br>0h         | <b>Different Rank Write to Write Delay (C0sd_cr_wrdr_wr):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to different ranks. This field corresponds to $t_{WR\_WR}$ in the DDR Specification. |
| 3:0   | RW<br>0h         | <b>READ To WRTE Delay (C0sd_cr_rd_wr):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands. This field corresponds to $t_{RD\_WR}$ .  |



### 5.2.6 COCYCTRKRD—Channel 0 CYCTRK READ

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 258–25Ah  
 Default Value: 000000h  
 Access: RW, RO  
 Size: 24 bits

This register provides Channel 0 CYCTRK RD.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 23:21 | RO<br>000b       | Reserved   |
| 20:17 | RW<br>0h         | <b>Min ACT To READ Delay (C0sd_cr_act_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank. This field corresponds to $t_{RCD\_rd}$ in the DDR Specification.              |
| 16:12 | RW<br>00000b     | <b>Same Rank Write To READ Delay (C0sd_cr_wrsr_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank. This field corresponds to $t_{WTR}$ in the DDR Specification.            |
| 11:8  | RW<br>0000b      | <b>Different Ranks Write To READ Delay (C0sd_cr_wrdr_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to different ranks. This field corresponds to $t_{WR\_RD}$ in the DDR Specification. |
| 7:4   | RW<br>0000b      | <b>Same Rank Read To Read Delay (C0sd_cr_rdsr_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.   |
| 3:0   | RW<br>0000b      | <b>Different Ranks Read To Read Delay (C0sd_cr_rddr_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to different ranks. This field corresponds to $t_{RD\_RD}$ .                                    |

### 5.2.7 COCYCTRKREFR—Channel 0 CYCTRK REFR

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 25B–25Ch  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

This register provides Channel 0 CYCTRK Refresh.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:13 | RO<br>000b       | Reserved  |
| 12:9  | RW<br>0000b      | <b>Same Rank PALL to REF Delay (C0sd_cr_pchgall_rfsh):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and REF commands to the same rank. |
| 8:0   | RW<br>000000000b | <b>Same Rank REF to REF Delay (C0sd_cr_rfsh_rfsh):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two REF commands to <b>same</b> ranks.             |



### 5.2.8 COCKECTRL—Channel 0 CKE Control

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 260–263h  
 Default Value: 00000800h  
 Access: RO, RW, RW/L  
 Size: 32 bits

This register provides CKE controls for Channel 0

| Bit   | Access & Default     | Description  |
|-------|----------------------|--|
| 31:28 | RO<br>0000b          | Reserved   |
| 27    | RW<br>0b             | <b>start the self-refresh exit sequence (sd0_cr_srcstart):</b> This field indicates the request to start the self-refresh exit sequence.   |
| 26:24 | RW<br>000b           | <b>CKE pulse width requirement in high phase (sd0_cr_cke_pw_hl_safe):</b> This field indicates CKE pulse width requirement in high phase. This field corresponds to $t_{CKE} (high)$ in the DDR Specification.   |
| 23:22 | RW/L<br>0b           | Reserved   |
| 21    | RW/L<br>0b           | <b>Rank 1 Population (sd0_cr_rankpop1):</b><br>1 = Rank 1 populated<br>0 = Rank 1 not populated  |
| 20    | RW/L<br>0b           | <b>Rank 0 Population (sd0_cr_rankpop0):</b><br>1 = Rank 0 populated<br>0 = Rank 0 not populated  |
| 19:17 | RW<br>000b           | <b>CKE pulse width requirement in low phase (sd0_cr_cke_pw_lh_safe):</b> This field indicates CKE pulse width requirement in low phase. This field corresponds to $t_{CKE} (low)$ in the DDR Specification.  |
| 16    | RW<br>0b             | <b>Enable CKE toggle for PDN entry/exit (sd0_cr_pdn_enable):</b><br>This bit indicates that the toggling of CKEs (for PDN entry/exit) is enabled.  |
| 15:14 | RO<br>00b            | Reserved   |
| 13:10 | RW<br>0010b          | <b>Minimum Powerdown exit to Non-Read command spacing (sd0_cr_txp):</b> This field indicates the minimum number of clocks to wait following assertion of CKE before issuing a non-read command.<br>0000–0001 = Reserved<br>0010–1001 = 2–9clocks<br>1010–1111 = Reserved |
| 9:1   | RW<br>00000000<br>0b | <b>Self refresh exit count (sd0_cr_slfrsh_exit_cnt):</b> This field indicates the Self refresh exit count. (Program to 255). This field corresponds to $t_{XSNR}/t_{XSRD}$ in the DDR Specification.   |
| 0     | RW<br>0b             | <b>Indicates only 1 DIMM populated (sd0_cr_singledimmpop):</b> This bit, when set, indicates that only 1 DIMM is populated.  |



### 5.2.9 COREFRCTRL—Channel 0 DRAM Refresh Control

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 269–26Eh  
 Default Value: 021830000C30h  
 Access: RW, RO  
 Size: 48 bits

This register provides settings to configure the DRAM refresh controller.

| Bit            | Access & Default   | Description  |                |             |     |                        |     |  |     |                       |
|----------------|--|--|----------------|-------------|-----|------------------------|-----|--|-----|-----------------------|
| 47:42          | RO<br>00h  | Reserved   |                |             |     |                        |     |  |     |                       |
| 41:37          | RW<br>10000b   | <b>Direct Rcomp Quiet Window (DIRQUIET):</b> This field indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.   |                |             |     |                        |     |  |     |                       |
| 36:32          | RW<br>11000b   | <b>Indirect Rcomp Quiet Window (INDIRQUIET):</b> This field indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.   |                |             |     |                        |     |  |     |                       |
| 31:27          | RW<br>00110b   | <b>Rcomp Wait (RCOMPWAIT):</b> This field indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.   |                |             |     |                        |     |  |     |                       |
| 26             | RW<br>0b   | Reserved   |                |             |     |                        |     |  |     |                       |
| 25             | RW<br>0b   | <p><b>Refresh Counter Enable (REFCNTEN):</b> This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch.</p> <p>This bit has no effect when Refresh is enabled (i.e., there is no mode where Refresh is enabled but the counter does not run). Thus, in conjunction with bit 23 REFEN, the modes are:</p> <table border="1"> <thead> <tr> <th>REFEN:REFCNTEN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0:0</td> <td>Normal refresh disable</td> </tr> <tr> <td>0:1</td> <td>Refresh disabled, but counter is accumulating refreshes.</td> </tr> <tr> <td>1:X</td> <td>Normal refresh enable</td> </tr> </tbody> </table> | REFEN:REFCNTEN | Description | 0:0 | Normal refresh disable | 0:1 | Refresh disabled, but counter is accumulating refreshes. | 1:X | Normal refresh enable |
| REFEN:REFCNTEN | Description  |  |                |             |     |                        |     |  |     |                       |
| 0:0            | Normal refresh disable                                   |  |                |             |     |                        |     |  |     |                       |
| 0:1            | Refresh disabled, but counter is accumulating refreshes. |  |                |             |     |                        |     |  |     |                       |
| 1:X            | Normal refresh enable                                    |  |                |             |     |                        |     |  |     |                       |
| 24             | RW<br>0b   | <b>All Rank Refresh (ALLRKREF):</b> This configuration bit enables (by default) that all the ranks are refreshed in a staggered/atomic fashion. If set, the ranks are refreshed in an independent fashion.   |                |             |     |                        |     |  |     |                       |
| 23             | RW<br>0b   | <p><b>Refresh Enable (REFEN):</b></p> <p>0 = Disabled<br/>                     1 = Enabled</p>   |                |             |     |                        |     |  |     |                       |
| 22             | RW<br>0b   | <p><b>DDR Initialization Done (INITDONE):</b> Indicates that DDR initialization is complete.</p> <p>0 = Not Done<br/>                     1 = Done</p>   |                |             |     |                        |     |  |     |                       |



| Bit   | Access & Default          | Description  |
|-------|---------------------------|--|
| 21:20 | RW<br>00b                 | Reserved   |
| 19:18 | RW<br>00b                 | <b>DRAM Refresh Panic Watermark (REFPANICWM):</b> When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_panic flag is set.<br><br>00 = 5<br>01 = 6<br>10 = 7<br>11 = 8                          |
| 17:16 | RW<br>00b                 | <b>DRAM Refresh High Watermark (REFHIGHWM):</b> When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set.<br><br>00 = 3<br>01 = 4<br>10 = 5<br>11 = 6                             |
| 15:14 | RW<br>00b                 | <b>DRAM Refresh Low Watermark (REFLOWWM):</b> When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set.<br><br>00 = 1<br>01 = 2<br>10 = 3<br>11 = 4                                |
| 13:0  | RW<br>001100001<br>10000b | <b>Refresh Counter Time Out Value (REFTIMEOUT):</b> Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies this results in the following values:<br><br>667 MHz -> 1450 hex |

### 5.2.10 COODTCTRL—Channel 0 ODT Control

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 29C–29Fh  
 Default Value: 00000000h  
 Access: RO, RW  
 Size: 32 bits

This register provides ODT controls.

| Bit   | Access & Default | Description |
|-------|------------------|-------------|
| 31:12 | RO<br>00000h     | Reserved    |
| 11:0  | RW<br>0s         | Reserved    |



### 5.2.11 C1DRB0—Channel 1 DRAM Rank Boundary Address 0

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 600–601h  
 Default Value: 0000h  
 Access: RW, RO  
 Size: 16 bits

The operation of this register is detailed in the description for register C0DRB0.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>000000b    | Reserved  |
| 9:0   | RW<br>000h       | <b>Channel 1 DRAM Rank Boundary Address 0 (C1DRBA0):</b> See C0DRB0 register. In stacked mode, if this is the topmost populated rank in Channel 1, program this value to be cumulative of Ch0 DRB3. |

### 5.2.12 C1DRB1—Channel 1 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 602–603h  
 Default Value: 0000h  
 Access: RW, RO  
 Size: 16 bits

The operation of this register is detailed in the description for register C0DRB0.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>000000b    | Reserved  |
| 9:0   | RW<br>000h       | <b>Channel 1 DRAM Rank Boundary Address 1 (C1DRBA1):</b> See C0DRB1 register. In stacked mode, if this is the topmost populated rank in Channel 1, program this value to be cumulative of Ch0 DRB3. |



### 5.2.13 C1DRB2—Channel 1 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: 604–605h  
Default Value: 0000h  
Access: RW, RO  
Size: 16 bits

The operation of this register is detailed in the description for register C0DRB0.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>000000b    | Reserved  |
| 9:0   | RW<br>000h       | <b>Channel 1 DRAM Rank Boundary Address 2 (C1DRBA2):</b> See C0DRB2 register. In stacked mode, if this is the topmost populated rank in Channel 1, program this value to be cumulative of Ch0 DRB3. |

### 5.2.14 C1DRB3—Channel 1 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: 606–607h  
Default Value: 0000h  
Access: RW, RO  
Size: 16 bits

The operation of this register is detailed in the description for register C0DRB0.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>000000b    | Reserved  |
| 9:0   | RW<br>000h       | <b>Channel 1 DRAM Rank Boundary Address 3 (C1DRBA3):</b> See C0DRB3 register. In stacked mode, this will be cumulative of Ch0 DRB3. |



### 5.2.15 C1DRA01—Channel 1 DRAM Rank 0,1 Attributes

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 608–609h  
 Default Value: 0000h  
 Access: RW  
 Size: 16 bits

The operation of this register is detailed in the description for register CODRA01.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:8 | RW<br>00h        | <b>Channel 1 DRAM Rank-1 Attributes (C1DRA1):</b> See CODRA1 register. |
| 7:0  | RW<br>00h        | <b>Channel 1 DRAM Rank-0 Attributes (C1DRA0):</b> See CODRA0 register. |

### 5.2.16 C1DRA23—Channel 1 DRAM Rank 2,3 Attributes

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 60A–60Bh  
 Default Value: 0000h  
 Access: RW  
 Size: 16 bits

The operation of this register is detailed in the description for register CODRA01.

| Bit  | Access & Default | Description |
|------|------------------|-------------|
| 15:8 | RW<br>00h        | Reserved    |
| 7:0  | RW<br>00h        | Reserved    |



### 5.2.17 C1CYCTRKPCHG—Channel 1 CYCTRK PCHG

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: 650–651h  
Default Value: 0000h  
Access: RO, RW  
Size: 16 bits

This register provides Channel 1 CYCTRK Precharge.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:11 | RO<br>00000b     | Reserved  |
| 10:6  | RW<br>00000b     | <b>Write To PRE Delayed (C1sd_cr_wr_pchg):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank. This field corresponds to $t_{WR}$ in the DDR Specification. |
| 5:2   | RW<br>0000b      | <b>READ To PRE Delayed (C1sd_cr_rd_pchg):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank   |
| 1:0   | RW<br>00b        | <b>PRE To PRE Delayed (C1sd_cr_pchg_pchg):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two PRE commands to the same rank.   |



### 5.2.18 C1CYCTRKACT—Channel 1 CYCTRK ACT

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 652–655h  
 Default Value: 00000000h  
 Access: RO, RW  
 Size: 32 bits

This register provides Channel 1 CYCTRK ACT.

| Bit   | Access & Default     | Description  |
|-------|----------------------|--|
| 31:28 | RO<br>0h             | Reserved   |
| 27:22 | RW<br>000000b        | <b>ACT Window Count (C1sd_cr_act_windowcnt):</b> This field indicates the window duration (in DRAM clocks) during which the controller counts the # of activate commands which are launched to a particular rank. If the number of activate commands launched within this window is greater than 4, then a check is implemented to block launch of further activates to this rank for the rest of the duration of this window.         |
| 21    | RW<br>0b             | <b>Max ACT Check Disable (C1sd_cr_maxact_dischk):</b> This field disenables the check which ensures that there are no more than four activates to a particular rank in a given window.   |
| 20:17 | RW<br>0000b          | <b>ACT to ACT Delayed (C1sd_cr_act_act[]):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank. This field corresponds to $t_{RRD}$ in the DDR Specification.  |
| 16:13 | RW<br>0000b          | <b>PRE to ACT Delayed (C1sd_cr_pre_act):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank: 12:9R/W0000bPRE-ALL to ACT Delayed (C1sd_cr_preall_act): This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and ACT commands to the same rank. This field corresponds to $t_{RP}$ in the DDR Specification. |
| 12:9  | RW<br>0h             | <b>ALLPRE to ACT Delay (C1sd_cr_preall_act):</b> From the launch of a Prechargeall command wait for these many # of memory clocks before launching a activate command. This field corresponds to $t_{PALL\_RP}$ .  |
| 8:0   | RW<br>00000000<br>0b | <b>REF to ACT Delayed (C1sd_cr_rfsh_act):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank. This field corresponds to $t_{RFC}$ in the DDR Specification.   |



### 5.2.19 C1CYCTRKWR—Channel 1 CYCTRK WR

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 656–657h  
 Default Value: 0000h  
 Access: RW  
 Size: 16 bits

This register provides Channel 1 CYCTRK WR.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:12 | RW<br>0h         | <b>ACT To Write Delay (C1sd_cr_act_wr):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank. This field corresponds to $t_{RCD\_wr}$ in the DDR Specification.       |
| 11:8  | RW<br>0h         | <b>Same Rank Write To Write Delayed (C1sd_cr_wrsr_wr):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.   |
| 7:4   | RW<br>0h         | <b>Different Rank Write to Write Delay (C1sd_cr_wrdr_wr):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to different ranks. This field corresponds to $t_{WR\_WR}$ in the DDR Specification. |
| 3:0   | RW<br>0h         | <b>READ To WRTE Delay (C1sd_cr_rd_wr):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands. This field corresponds to $t_{RD\_WR}$ .  |



### 5.2.20 C1CYCTRKR—Channel 1 CYCTRK READ

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 658–65Ah  
 Default Value: 000000h  
 Access: RO, RW  
 Size: 24 bits

This is the Channel 1 CYCTRK READ register.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 23:21 | RO<br>0h         | Reserved   |
| 20:17 | RW<br>0h         | <b>Min ACT To READ Delayed (C1sd_cr_act_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank. This field corresponds to $t_{RCD\_rd}$ in the DDR Specification.              |
| 16:12 | RW<br>00000b     | <b>Same Rank Write To READ Delayed (C1sd_cr_wrsr_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank. This field corresponds to $t_{WTR}$ in the DDR Specification.            |
| 11:8  | RW<br>0000b      | <b>Different Ranks Write To READ Delayed (C1sd_cr_wrdr_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to different ranks. This field corresponds to $t_{WR\_RD}$ in the DDR Specification. |
| 7:4   | RW<br>0000b      | <b>Same Rank Read To Read Delayed (C1sd_cr_rdsr_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.   |
| 3:0   | RW<br>0000b      | <b>Different Ranks Read To Read Delayed (C1sd_cr_rddr_rd):</b> This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to different ranks. This field corresponds to $t_{RD\_RD}$ .                   |



### 5.2.21 C1CKECTRL—Channel 1 CKE Control

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 660–663h  
 Default Value: 00000800h  
 Access: RW/L, RW, RO  
 Size: 32 bits

This register provides Channel 1 CKE Controls.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:28 | RO<br>0h         | Reserved   |
| 27    | RW<br>0b         | <b>start the self-refresh exit sequence (sd1_cr_srcstart):</b> This field indicates the request to start the self-refresh exit sequence.   |
| 26:24 | RW<br>000b       | <b>CKE pulse width requirement in high phase (sd1_cr_cke_pw_hl_safe):</b> This field indicates CKE pulse width requirement in high phase. This field corresponds to $t_{CKE}$ (high) in the DDR Specification.               |
| 23:22 | RW/L<br>00b      | Reserved   |
| 21    | RW/L<br>0b       | <b>Rank 1 Population (sd1_cr_rankpop1):</b><br>1 = Rank 1 populated<br>0 = Rank 1 not populated.   |
| 20    | RW/L<br>0b       | <b>Rank 0 Population (sd1_cr_rankpop0):</b><br>1 = Rank 0 populated<br>0 = Rank 0 not populated  |
| 19:17 | RW<br>000b       | <b>CKE pulse width requirement in low phase (sd1_cr_cke_pw_lh_safe):</b> This configuration register indicates CKE pulse width requirement in low phase. This field corresponds to $t_{CKE}$ (low) in the DDR Specification. |
| 16    | RW<br>0b         | <b>Enable CKE toggle for PDN entry/exit (sd1_cr_pdn_enable):</b> This configuration bit indicates that the toggling of CKEs (for PDN entry/exit) is enabled.   |
| 15:14 | RO<br>00b        | Reserved   |



| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 13:10 | RW<br>0010b      | <b>Minimum Powerdown Exit to Non-Read command spacing (sd1_cr_txp):</b> This configuration register indicates the minimum number of clocks to wait following assertion of CKE before issuing a non-read command.<br><br>1010–1111 = Reserved.<br>0010–1001 = 2–9 clocks<br>0000–0001 = Reserved. |
| 9:1   | RW<br>000000000b | <b>Self refresh exit count (sd1_cr_slrfsh_exit_cnt):</b> This configuration register indicates the Self refresh exit count. (Program to 255). This field corresponds to $t_{XSNR}/t_{XSRD}$ in the DDR Specification.  |
| 0     | RW<br>0b         | <b>Indicates only 1 DIMM pPopulated (sd1_cr_singledimmpop):</b> This bit indicates that only 1 DIMM is populated.  |

### 5.2.22 C1REFRCTRL—Channel 1 DRAM Refresh Control

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 669–66Eh  
 Default Value: 021830000C30h  
 Access: RW, RO  
 Size: 48 bits

This register provides settings to configure the DRAM refresh controller.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 47:42 | RO<br>00h        | Reserved   |
| 41:37 | RW<br>10000b     | <b>Direct Rcomp Quiet Window (DIRQUIET):</b> This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.     |
| 36:32 | RW<br>11000b     | <b>Indirect Rcomp Quiet Window (INDIRQUIET):</b> This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh. |
| 31:27 | RW<br>00110b     | <b>Rcomp Wait (RCOMPWAIT):</b> This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.                   |
| 26    | RW<br>0b         | <b>ZQCAL Enable (ZQCALEN):</b> This bit enables the DRAM controller to issue ZQCAL S command periodically.<br><br>0 = Disable<br>1 = Enable  |



| Bit            | Access & Default   | Description  |                |             |     |                        |     |  |     |                       |
|----------------|--|--|----------------|-------------|-----|------------------------|-----|--|-----|-----------------------|
| 25             | RW<br>0b   | <p><b>Refresh Counter Enable (REFCNTEN):</b> This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch.</p> <p>This bit has no effect when Refresh is enabled (i.e., there is no mode where Refresh is enabled but the counter does not run). Thus, in conjunction with bit 23 REFEN, the modes are:</p> <table border="1"> <thead> <tr> <th>REFEN:REFCNTEN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0:0</td> <td>Normal refresh disable</td> </tr> <tr> <td>0:1</td> <td>Refresh disabled, but counter is accumulating refreshes.</td> </tr> <tr> <td>1:X</td> <td>Normal refresh enable</td> </tr> </tbody> </table> | REFEN:REFCNTEN | Description | 0:0 | Normal refresh disable | 0:1 | Refresh disabled, but counter is accumulating refreshes. | 1:X | Normal refresh enable |
| REFEN:REFCNTEN | Description  |  |                |             |     |                        |     |  |     |                       |
| 0:0            | Normal refresh disable                                   |  |                |             |     |                        |     |  |     |                       |
| 0:1            | Refresh disabled, but counter is accumulating refreshes. |  |                |             |     |                        |     |  |     |                       |
| 1:X            | Normal refresh enable                                    |  |                |             |     |                        |     |  |     |                       |
| 24             | RW<br>0b   | <p><b>All Rank Refresh (ALLRKREF):</b> This configuration bit enables (by default) that all the ranks are refreshed in a staggered/atomic fashion. If set, the ranks are refreshed in an independent fashion.</p>  |                |             |     |                        |     |  |     |                       |
| 23             | RW<br>0b   | <p><b>Refresh Enable (REFEN):</b> Refresh is enabled.</p> <p>0 = Disabled<br/>1 = Enabled</p>  |                |             |     |                        |     |  |     |                       |
| 22             | RW<br>0b   | <p><b>DDR Initialization Done (INITDONE):</b> Indicates that DDR initialization is complete.</p> <p>0 = Not Done<br/>1 = Done</p>  |                |             |     |                        |     |  |     |                       |
| 21:20          | RW<br>00b  | <p><b>DRAM Refresh Hysteresis (REFHYSTERISIS):</b> Hysteresis level - Useful for dref_high watermark cases. The dref_high flag is set when the dref_high watermark level is exceeded, and is cleared when the refresh count is less than the hysteresis level. This field should be set to a value less than the high watermark level.</p> <p>00 = 3<br/>01 = 4<br/>10 = 5<br/>11 = 6</p>  |                |             |     |                        |     |  |     |                       |
| 19:18          | RW<br>00b  | <p><b>DRAM Refresh Panic Watermark (REFPANICWWM):</b> When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_panic flag is set.</p> <p>00 = 5<br/>01 = 6<br/>10 = 7<br/>11 = 8</p>   |                |             |     |                        |     |  |     |                       |
| 17:16          | RW<br>00b  | <p><b>DRAM Refresh High Watermark (REFHIGHWM):</b> When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set.</p> <p>00 = 3<br/>01 = 4<br/>10 = 5<br/>11 = 6</p>   |                |             |     |                        |     |  |     |                       |



| Bit   | Access & Default          | Description   |
|-------|---------------------------|---|
| 15:14 | RW<br>00b                 | <b>DRAM Refresh Low Watermark (REFLOWWM):</b> When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set.<br><br>00 = 1<br>01 = 2<br>10 = 3<br>11 = 4   |
| 13:0  | RW<br>00110000<br>110000b | <b>Refresh Counter Time Out Value (REFTIMEOUT):</b> Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies this results in the following values:<br><br>266 MHz -> 820 hex<br>333 MHz -> A28 hex<br>400 MHz -> C30 hex<br>533 MHz -> 104B hex<br>666 MHz -> 1450 hex |

### 5.2.23 C1ODTCTRL—Channel 1 ODT Control

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 69C–69Fh  
 Default Value: 00000000h  
 Access: RO, RW  
 Size: 32 bits

This register provides ODT controls.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:12 | RO<br>00000h     | Reserved  |
| 11:8  | RW<br>0h         | <b>DRAM ODT for Read Commands (sd1_cr_odt_duration_rd):</b> Specifies the duration in MDCLKs to assert DRAM ODT for Read Commands. The Async value should be used when the Dynamic Powerdown bit is set. Else use the Sync value.   |
| 7:4   | RW<br>0h         | <b>DRAM ODT for Write Commands (sd1_cr_odt_duration_wr):</b> Specifies the duration in MDCLKs to assert DRAM ODT for Write Commands. The Async value should be used when the Dynamic Powerdown bit is set. Else use the Sync value. |
| 3:0   | RW<br>0h         | <b>MCH ODT for Read Commands (sd1_cr_mchodt_duration):</b> Specifies the duration in MDCLKs to assert (G)MCH ODT for Read Commands  |



### 5.2.24 EPCODRB1—EP Channel 0 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: A02–A03h  
Default Value: 0000h  
Access: RO, RW  
Size: 16 bits

See C0DRB0 register.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15:10 | RO<br>000000b    | Reserved   |
| 9:0   | RW<br>000h       | <b>Channel 0 Dram Rank Boundary Address 1 (C0DRBA1):</b> |

### 5.2.25 EPCODRB2—EP Channel 0 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: A04–A05h  
Default Value: 0000h  
Access: RO, RW  
Size: 16 bits

See C0DRB0 register.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15:10 | RO<br>000000b    | Reserved   |
| 9:0   | RW<br>000h       | <b>Channel 0 DRAM Rank Boundary Address 2 (C0DRBA2):</b> |

### 5.2.26 EPCODRB3—EP Channel 0 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: A06–A07h  
Default Value: 0000h  
Access: RW, RO  
Size: 16 bits

See C0DRB0 register.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15:10 | RO<br>000000b    | Reserved   |
| 9:0   | RW<br>000h       | <b>Channel 0 DRAM Rank Boundary Address 3 (C0DRBA3):</b> |



### 5.2.27 EPCODRA01—EP Channel 0 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: A08–A09h  
 Default Value: 0000h  
 Access: RW  
 Size: 16 bits

The DRAM Rank Attribute Registers define the page sizes/number of banks to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks. Channel and rank map:

Ch0 Rank0, 1: 108h – 109h  
 Ch1 Rank0, 1: 188h – 189h

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:8 | RW<br>00h        | <b>Channel 0 DRAM Rank-1 Attributes (CODRA1):</b> This field defines DRAM pagesize/number-of-banks for rank1 for given channel. |
| 7:0  | RW<br>00h        | <b>Channel 0 DRAM Rank-0 Attributes (CODRA0):</b> This field defines DRAM pagesize/number-of-banks for rank0 for given channel. |

### 5.2.28 EPCODRA23—EP Channel 0 DRAM Rank 2,3 Attribute

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: A0A–A0Bh  
 Default Value: 0000h  
 Access: RW  
 Size: 16 bits

See CODRA01 register.

| Bit  | Access & Default | Description |
|------|------------------|-------------|
| 15:0 | RW<br>00h        | Reserved    |



### 5.2.29 EPDCYCTRKWRTPRE—EPD CYCTRK WRT PRE

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: A19–A1Ah  
 Default Value: 0000h  
 Access: RW, RO  
 Size: 16 bits

This register provides EPD CYCTRK WRT PRE Status.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15:11 | RW<br>00000b     | <b>ACT to PRE Delayed (C0sd_cr_act_pchg)</b> : This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and PRE commands to the same rank-bank    |
| 10:6  | RW<br>00000b     | <b>Write To PRE Delayed (C0sd_cr_wr_pchg)</b> : This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank |
| 5:2   | RW<br>0000b      | <b>READ To PRE Delayed (C0sd_cr_rd_pchg)</b> : This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank   |
| 1:0   | RO<br>00b        | Reserved   |

### 5.2.30 EPDCYCTRKWRTACT—EPD CYCTRK WRT ACT

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: A1C–A1Fh  
 Default Value: 00000000h  
 Access: RO, RW  
 Size: 32 bits

This register provides EPD CYCTRK WRT ACT Status.

| Bit   | Access & Default     | Description  |
|-------|----------------------|--|
| 31:21 | RO<br>000h           | Reserved   |
| 20:17 | RW<br>0000b          | <b>ACT to ACT Delayed (C0sd_cr_act_act[])</b> : This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank.   |
| 16:13 | RW<br>0000b          | <b>PRE to ACT Delayed (C0sd_cr_pre_act)</b> : This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank: 12:9R/W0000bPRE-ALL to ACT Delayed (C0sd_cr_preall_act):<br>This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and ACT commands to the same rank. |
| 12:9  | RO<br>0h             | Reserved   |
| 8:0   | RW<br>00000000<br>0b | <b>REF to ACT Delayed (C0sd_cr_rfsh_act)</b> : This field indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank.  |



### 5.2.31 EPDCYCTRKWRTWR—EPD CYCTRK WRT WR

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: A20–A21h  
 Default Value: 0000h  
 Access: RW, RO  
 Size: 16 bits

This register provides EPD CYCTRK WRT WR Status.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:12 | RW<br>0h         | <b>ACT To Write Delay (C0sd_cr_act_wr):</b> This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank.      |
| 11:8  | RW<br>0h         | <b>Same Rank Write To Write Delayed (C0sd_cr_wrsr_wr):</b> This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.    |
| 7:4   | RO<br>0h         | Reserved  |
| 3:0   | RW<br>0h         | <b>Same Rank WRITE to READ Delay (C0sd_cr_rd_wr):</b> This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank |



### 5.2.32 EPDCYCTRKWRTRD—EPD CYCTRK WRT READ

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: A24–A26h  
 Default Value: 000000h  
 Access: RW  
 Size: 24 bits  
 BIOS Optimal Default: 000h

This register provides EPD CYCTRK WRT RD Status.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 23:23 | RO<br>0h         | Reserved  |
| 22:20 | RW<br>000b       | <b>EPDunit DQS Slave DLL Enable to Read Safe (EPDSDLL2RD):</b> This field provides the setting for Read command safe from the point of enabling the slave DLLs.             |
| 19:18 | RO<br>0h         | Reserved  |
| 17:14 | RW<br>0h         | <b>Min ACT To READ Delayed (C0sd_cr_act_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank. |
| 13:9  | RW<br>00000b     | <b>Same Rank READ to WRITE Delayed (C0sd_cr_wrsr_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands.            |
| 8:6   | RO<br>0h         | Reserved  |
| 5:3   | RW<br>000b       | <b>Same Rank Read To Read Delayed (C0sd_cr_rdsr_rd):</b> This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.      |
| 2:0   | RO<br>0h         | Reserved  |



### 5.2.33 EPDCKECONFIGREG—EPD CKE Related Configuration Register

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: A28–A2Ch  
 Default Value: 00E0000000h  
 Access: RW  
 Size: 40 bits  
 BIOS Optimal Default 0h

This register provides CKE related configuration for EPD.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 39:35 | RW<br>00000b     | <b>EPDunit TXPDLL Count (EPDTPDLL)</b> : This field specifies the delay from precharge power down exit to a command that requires the DRAM DLL to be operational. The commands are read/write.  |
| 34:32 | RW<br>000b       | <b>EPDunit TXP count (EPDCKETXP)</b> : This field specifies the timing requirement for Active power down exit or fast exit pre-charge power down exit to any command or slow exit pre-charge power down to Non-DLL (rd/wr/odt) command. |
| 31:29 | RW<br>111b       | <b>Mode Select (sd0_cr_sms)</b> : This field indicates the mode in which the controller is operating in.<br><br>111 = indicates normal mode of operation, else special mode of operation.   |
| 28:27 | RW<br>00b        | <b>EPDunit EMRS command select. (EPDEMRSEL)</b> : EMRS mode to select BANK address.<br><br>01 = EMRS<br>10 = EMRS2<br>11 = EMRS3  |
| 26:24 | RW<br>000b       | <b>CKE pulse width requirement in high phase (sd0_cr_cke_pw_hl_safe)</b> : This field indicates CKE pulse width requirement in high phase.  |
| 23:20 | RW<br>0h         | <b>one-hot active rank population (ep_scr_actrank)</b> : This field indicates the active rank in a one hot manner   |
| 19:17 | RW<br>000b       | <b>CKE pulse width requirement in low phase (sd0_cr_cke_pw_lh_safe)</b> : This field indicates CKE pulse width requirement in low phase.  |
| 16:15 | RO<br>0h         | Reserved  |
| 14    | RW<br>0b         | <b>EPDunit MPR mode (EPDMPR)</b> : MPR Read Mode<br><br>1 = MPR mode<br>0 = Normal mode<br><br>In MPR mode, only read cycles must be issued by Firmware. Page Results are ignored by DCS and just issues the read chip select.          |



| Bit   | Access & Default     | Description   |
|-------|----------------------|---|
| 13    | RW<br>0b             | <b>EPDunit Power Down enable for ODT Rank (EPDOAPDEN):</b><br>Configuration to enable the ODT ranks to dynamically enter power down.<br><br>1 = Enable active power down.<br>0 = Disable active power down.   |
| 12    | RW<br>0b             | <b>EPDunit Power Down enable for Active Rank (EPDAAPDEN):</b><br>Configuration to enable the active rank to dynamically enter power down.<br><br>1 = Enable active power down.<br>0 = Disable active power down.  |
| 11:10 | RO<br>0h             | Reserved  |
| 9:1   | RW<br>00000000<br>0b | <b>Self refresh exit count (sd0_cr_slfrsh_exit_cnt):</b> This field indicates the Self refresh exit count. (Program to 255)   |
| 0     | RW<br>0b             | <b>indicates only 1 rank enabled (sd0_cr_singledimmpop):</b> This field indicates that only 1 rank is enabled. This bit needs to be set if there is one active rank and no odt ranks, or if there is one active rank and one odt rank and they are the same rank. |



### 5.2.34 EPDREFCONFIG—EP DRAM Refresh Configuration

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: A30–A33h  
 Default Value: 40000C30h  
 Access: RO, RW  
 Size: 32 bits

This register provides settings to configure the EPD refresh controller.

| Bit            | Access & Default   | Description   |                |             |     |                        |     |  |     |                       |
|----------------|--|---|----------------|-------------|-----|------------------------|-----|--|-----|-----------------------|
| 31             | RO<br>0b   | Reserved  |                |             |     |                        |     |  |     |                       |
| 30:29          | RW<br>10b  | <p><b>EPDunit refresh count addition for self refresh exit. (EPDREF4SR):</b> Configuration indicating the number of additional refreshes that needs to be added to the refresh request count after exiting self refresh.</p> <p>Typical value is to add 2 refreshes.</p> <p>00 = Add 0 Refreshes<br/>                     01 = Add 1 Refreshes<br/>                     10 = Add 2 Refreshes<br/>                     11 = Add 3 Refreshes</p> <p>Signal name used: ep_scr_refreq_aftersr[1:0]</p>  |                |             |     |                        |     |  |     |                       |
| 28             | RW<br>0b   | <p><b>Refresh Counter Enable (REFCNTEN):</b> This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch.</p> <p>This bit has no effect when Refresh is enabled (i.e. there is no mode where Refresh is enabled but the counter does not run). Thus, in conjunction with bit 23 REFEN, the modes are:</p> <table border="1"> <thead> <tr> <th>REFEN:REFCNTEN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0:0</td> <td>Normal refresh disable</td> </tr> <tr> <td>0:1</td> <td>Refresh disabled, but counter is accumulating refreshes.</td> </tr> <tr> <td>1:X</td> <td>Normal refresh enable</td> </tr> </tbody> </table> | REFEN:REFCNTEN | Description | 0:0 | Normal refresh disable | 0:1 | Refresh disabled, but counter is accumulating refreshes. | 1:X | Normal refresh enable |
| REFEN:REFCNTEN | Description  |   |                |             |     |                        |     |  |     |                       |
| 0:0            | Normal refresh disable                                   |   |                |             |     |                        |     |  |     |                       |
| 0:1            | Refresh disabled, but counter is accumulating refreshes. |   |                |             |     |                        |     |  |     |                       |
| 1:X            | Normal refresh enable                                    |   |                |             |     |                        |     |  |     |                       |
| 27             | RW<br>0b   | <p><b>Refresh Enable (REFEN):</b></p> <p>0 = Disabled<br/>                     1 = Enabled</p>  |                |             |     |                        |     |  |     |                       |
| 26             | RW<br>0b   | <p><b>DDR Initialization Done (INITDONE):</b> Indicates that DDR initialization is complete.</p> <p>0 = Not Done<br/>                     1 = Done</p>  |                |             |     |                        |     |  |     |                       |



| Bit   | Access & Default          | Description  |
|-------|---------------------------|--|
| 25:22 | RW<br>0000b               | <p><b>DRAM Refresh Hysterisis (REFHYSTERISIS):</b> Hysterisis level - Useful for dref_high watermark cases. The dref_high flag is set when the dref_high watermark level is exceeded, and is cleared when the refresh count is less than the hysterisis level. This bit should be set to a value less than the high watermark level.</p> <p>0000 = 0<br/>0001 = 1<br/>.....<br/>1000 = 8</p> |
| 21:18 | RW<br>0000b               | <p><b>DRAM Refresh High Watermark (REFHIGHWM):</b> When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set.</p> <p>0000 = 0<br/>0001 = 1<br/>.....<br/>1000 = 8</p>  |
| 17:14 | RW<br>0000b               | <p><b>DRAM Refresh Low Watermark (REFLOWWM):</b> When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set.</p> <p>0000 = 0<br/>0001 = 1<br/>.....<br/>1000 = 8</p>   |
| 13:0  | RW<br>001100001<br>10000b | <p><b>Refresh Counter Time Out Value (REFTIMEOUT):</b> Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies this results in the following values:</p> <p>266 MHz -&gt; 820 hex<br/>333 MHz -&gt; A28 hex<br/>400 MHz -&gt; C30 hex<br/>533 MHz -&gt; 104B hex<br/>666 MHz -&gt; 1450 hex</p>                          |



### 5.2.35 TSC1—Thermal Sensor Control 1

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: CD8h  
 Default Value: 00h  
 Access: RW/L, RW, RS/WC  
 Size: 8 bits

This register controls the operation of the thermal sensor. Bit 0 is reset to its default by PLTRST#.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7   | RW/L<br>0b       | <b>Thermal Sensor Enable (TSE):</b> This bit enables power to the thermal sensor. Lockable via TCO bit 7.<br><br>0 = Disabled<br>1 = Enabled   |
| 6   | RW<br>0b         | <b>Analog Hysteresis Control (AHC):</b> This bit enables the analog hysteresis control to the thermal sensor. When enabled, about 1 degree of hysteresis is applied. This bit should normally be off in thermometer mode since the thermometer mode of the thermal sensor defeats the usefulness of analog hysteresis.<br><br>0 = hysteresis disabled<br>1 = analog hysteresis enabled.  |
| 5:2 | RW<br>0000b      | <b>Digital Hysteresis Amount (DHA):</b> This bit determines whether no offset, 1 LSB, 2... 15 is used for hysteresis for the trip points.<br><br>0000 = digital hysteresis disabled, no offset added to trip temperature<br><br>0001 = offset is 1 LSB added to each trip temperature when tripped<br><br>...<br><br>0110 = ~3.0 °C (Recommended setting)<br><br>...<br><br>1110 = added to each trip temperature when tripped<br>1111 = added to each trip temperature when tripped |
| 1   | RW/L<br>0b       | <b>Thermal Sensor Comparator Select (TSCS):</b> This bit multiplexes between the two analog comparator outputs. Normally Catastrophic is used. Lockable via TCO bit 7.<br><br>0 = Catastrophic<br>1 = Hot  |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 0   | RS/WC<br>0b      | <p><b>In Use (IU):</b> Software semaphore bit.</p> <p>After a full (G)MCH RESET, a read to this bit returns a 0.</p> <p>After the first read, subsequent reads will return a 1.</p> <p>A write of a 1 to this bit will reset the next read value to 0.</p> <p>Writing a 0 to this bit has no effect.</p> <p>Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor.</p> <p>This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the thermal sensor.</p> <p>Software that reads this register but does not intend to claim exclusive access of the thermal sensor must write a one to this bit if it reads a 0, in order to allow other software threads to claim it.</p> <p>See also THERM3 bit 7 and IUB, which are independent additional semaphore bits.</p> |

### 5.2.36 TSC2—Thermal Sensor Control 2

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: CD9h  
 Default Value: 00h  
 Access: RW/L, RO  
 Size: 8 bits

This register controls the operation of the thermal sensor.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:4 | RO<br>0h         | Reserved  |
| 3:0 | RW/L<br>0h       | <p><b>Thermometer Mode Enable and Rate (TE):</b> If analog thermal sensor mode is not enabled by setting these bits to 0000b, these bits enable the thermometer mode functions and set the Thermometer controller rate.</p> <p>When the Thermometer mode is disabled and TSC1[TSE] =enabled, the analog sensor mode should be fully functional. In the analog sensor mode, the Catastrophic trip is functional, and the Hot trip is functional at the offset below the catastrophic programmed into TSC2[CHO]. The other trip points are not functional in this mode.</p> <p>When Thermometer mode is enabled, all the trip points (Catastrophic, Hot, Aux0) will all operate using the programmed trip points and Thermometer mode rate.</p> <p><b>Note:</b> When disabling the Thermometer mode while thermometer running, the Thermometer mode controller will finish the current cycle.</p> <p><b>Note:</b> During boot, all other thermometer mode registers (except</p> |



| Bit | Access & Default | Description   |
|-----|------------------|---|
|     |                  | <p>lock bits) should be programmed appropriately before enabling the Thermometer Mode.</p> <p>Clock used is the memory command clock (i.e., ep_mcclk).</p> <p><b>Note:</b> The same legacy thermal sensor design in prior (G)MCHs has been used in this design. However, the thermal sensor logic runs in a memory command clock domain that is ½ the frequency of the memory clock used in prior designs. Hence the period counted for the thermal sensor settling time has doubled for the same settings, compared to prior (G)MCHs. Thus the thermal sensor programming should be updated to maintain the same thermometer rate count as in prior (G)MCHs.</p> <p>Lockable via TCO bit 7.</p> <p>0000 = Thermometer mode disabled (i.e., analog sensor mode)</p> <p>0001 = enabled, 512 clock mode</p> <p>0010 = enabled, 1024 clock mode<br/>(normal Thermometer mode operation, for DDR 667/800)<br/>provides ~6.14 us settling time @ 167 MHz ep_mcclk (DDR 667)<br/>provides ~5.12 us settling time @ 200 MHz ep_mcclk (DDR 800)</p> <p>0011 = enabled, 1536 clock mode<br/>(normal Thermometer mode operation, for DDR 1066)<br/>provides ~9.22 us settling time @ 167 MHz ep_mcclk (DDR 667)<br/>provides ~7.68 us settling time @ 200 MHz ep_mcclk (DDR 800)</p> <p>0100 = enabled, 2048 clock mode<br/>(normal Thermometer mode operation, for DDR 1333)<br/>provides ~15.36 us settling time @ 133 MHz ep_mcclk (DDR 533)<br/>provides ~12.29 us settling time @ 167 MHz ep_mcclk (DDR 667)<br/>provides ~10.24 us settling time @ 200 MHz ep_mcclk (DDR 800)</p> <p>0101 = enabled, 3072 clock mode</p> <p>0110 = enabled, 4096 clock mode</p> <p>0111 = enabled, 6144 clock mode</p> <p>all other permutations are reserved</p> <p>1111 = enabled, 4 clock mode (for testing digital logic)</p> <p><b>NOTE:</b> The settling time for DAC and Thermal Diode is between 2 and 5 us. To meet this requirement the SE value must be programmed to be 5 us or more. Recommendation is to use: "0010" setting for DDR 667/800.</p> |



### 5.2.37 TSS—Thermal Sensor Status

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: CDAh  
Default Value: 00h  
Access: RO  
Size: 8 bits

This read only register provides trip point and other status of the thermal sensor.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7   | RO<br>0b         | <b>Catastrophic Trip Indicator (CTI):</b><br>1 = Internal thermal sensor temperature is above the catastrophic setting.   |
| 6   | RO<br>0b         | <b>Hot Trip Indicator (HTI):</b><br>1 = Internal thermal sensor temperature is above the Hot setting.   |
| 5   | RO<br>0b         | <b>Aux0 Trip Indicator (AOTI):</b><br>1 = Internal thermal sensor temperature is above the Aux0 setting.  |
| 4   | RO<br>0b         | <b>Thermometer Mode Output Valid (TOV):</b><br>1 = Thermometer mode is able to converge to a temperature and that the TR register is reporting a reasonable estimate of the thermal sensor temperature.<br>0 = Thermometer mode is off, or that temperature is out of range, or that the TR register is being looked at before a temperature conversion has had time to complete. |
| 3:2 | RO<br>00b        | Reserved  |
| 1   | RO<br>0b         | <b>Direct Catastrophic Comparator Read (DCCR):</b> This bit reads the output of the Catastrophic comparator directly, without latching via the Thermometer mode circuit. Used for testing.  |
| 0   | RO<br>0b         | <b>Direct Hot Comparator Read (DHCR):</b> This bit reads the output of the Hot comparator directly, without latching via the Thermometer mode circuit. Used for testing.  |



### 5.2.38 TSTTP—Thermal Sensor Temperature Trip Point

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: CDC–CDFh  
 Default Value: 00000000h  
 Access: RO, RW, RW/L  
 Size: 32 bits

This register :

- Sets the target values for the trip points in thermometer mode. See also TST[Direct DAC Connect Test Enable].
- Reports the relative thermal sensor temperature

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:24 | RO<br>00h        | <b>Relative Temperature (RELT):</b> In Thermometer mode, the RELT field of this register report the relative temperature of the thermal sensor. Provides a two's complement value of the thermal sensor relative to the Hot Trip Point. Temperature above the Hot Trip Point will be positive.<br><br>TR and HTPS can both vary between 0 and 255. But RELT will be clipped between ±127 to keep it an 8 bit number.<br><br>See also TSS[Thermometer mode Output Valid]<br><br>In the Analog mode, the RELT field reports HTPS value. |
| 23:16 | RW<br>00h        | <b>Aux0 Trip point setting (A0TPS):</b> Sets the target for the Aux0 trip point.  |
| 15:8  | RW/L<br>00h      | <b>Hot Trip Point Setting (HTPS):</b> Sets the target value for the Hot trip point.<br><br>Lockable via TCO bit 7.  |
| 7:0   | RW/L<br>00h      | <b>Catastrophic Trip Point Setting (CTPS):</b> Sets the target for the Catastrophic trip point. See also TST[Direct DAC Connect Test Enable].<br><br>Lockable via TCO bit 7.  |



### 5.2.39 TCO—Thermal Calibration Offset

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: CE2h  
 Default Value: 00h  
 Access: RW/L/K, RW/L  
 Size: 8 bits

Bit 7: reset to its default by PLTRST#.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7   | RW/L/K<br>0b     | <b>Lock Bit for Catastrophic (LBC):</b> This bit, when written to a 1, locks the Catastrophic programming interface, including bits 7:0 of this register and bits 15:0 of TSTTP, bits 1,7 of TSC 1, bits 3:0 of TSC 2, bits 4:0 of TSC 3, and bits 0,7 of TST. This bit may only be set to a 0 by a hardware reset (PLTRST#). Writing a 0 to this bit has no effect.   |
| 6:0 | RW/L<br>00h      | <b>Calibration Offset (CO):</b> This field contains the current calibration offset for the Thermal Sensor DAC inputs. The calibration offset is a twos complement signed number which is added to the temperature counter value to help generate the final value going to the thermal sensor DAC.<br><br>This field is Read/Write and can be modified by Software unless locked by setting bit 7 of this register.<br><br>The fuses cannot be programmed via this register.<br><br>Once this register has been overwritten by software, the values of the TCO fuses can be read using the Therm3 register.<br><br>Note for TCO operation:<br><br>While this is a seven-bit field, the 7th bit is sign extended to 9 bits for TCO operation. The range of 00h to 3Fh corresponds to 0 0000 0000 to 0 0011 1111. The range of 41h to 7Fh corresponds to 1 1100 001 (i.e., negative 3Fh) to 1 1111 1111 (i.e., negative 1), respectively. |



### 5.2.40 THERM1—Hardware Throttle Control

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: CE4h  
 Default Value: 00h  
 Access: RW/L, RO, RW/L/K  
 Size: 8 bits

All bits in this register are reset to their defaults by PLTRST#.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7   | RW/L<br>00h      | <b>Internal Thermal Hardware Throttling Enable (ITHTE):</b> This bit is a master enable for internal thermal sensor-based hardware throttling.<br>0 = Disable. Hardware actions via the internal thermal sensor are disabled.<br>1 = Enable. Hardware actions via the internal thermal sensor are enabled.  |
| 6   | RW/L<br>00h      | <b>Internal Thermal Hardware Throttling Type (ITHTT):</b> This policy bit determines what type of hardware throttling will be enacted by the internal thermal sensor when enabled by ITHTE.<br>0 = (G)MCH throttling<br>1 = DRAM throttling   |
| 5   | RO<br>00h        | Reserved  |
| 4   | RW/L<br>00h      | <b>Throttling Temperature Range Selection (TTRS):</b> This bit determines what temperature ranges will enable throttling. Lockable by bit 0 of this register. See also the throttling registers in MCHBAR configuration space C0GTC and C1GTC [(G)MCH Thermal Sensor Trip Enable] and PEFC [Thermal Sensor Trip Enable] which are used to enable or disable throttling.<br>0 = Catastrophic only. The Catastrophic thermal temperature range will enable main memory thermal throttling.<br>1 = Hot and Catastrophic. |
| 3   | RW/L<br>00h      | <b>Halt on Catastrophic (HOC):</b><br>0 = Continue to toggle clocks when the catastrophic sensor trips.<br>1 = All clocks are disabled when the catastrophic sensor trips. A system reset is required to bring the system out of a halt from the thermal sensor.  |
| 2:1 | RO<br>00b        | Reserved  |
| 0   | RW/L/K<br>00h    | <b>Hardware Throttling Lock Bit (HTL):</b> This bit locks bits 7:0 of this register.<br>0 = The register bits are unlocked.<br>1 = The register bits are locked. It may only be set to a 0 by a hardware reset.<br>Writing a 0 to this bit has no effect.   |



### 5.2.41 TIS—Thermal Interrupt Status

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: CEA–CEBh  
 Default Value: 0000h  
 Access: RO, RWC  
 Size: 16 bits

This register is used to report which specific error condition resulted in the dev. 0 fn. 0 ERRSTS[Thermal Sensor event for SMI/SCI/SERR] or memory mapped IIR Thermal Event. Software can examine the current state of the thermal zones by examining the TSS. Software can distinguish internal or external Trip Event by examining EXTTSCS.

Software must write a 1 to clear the status bits in this register.

Following scenario is possible. An interrupt is initiated on a rising temperature trip, the appropriate DMI cycles are generated, and eventually the software services the interrupt and sees a rising temperature trip as the cause in the status bits for the interrupts. Assume that the software then goes and clears the local interrupt status bit in the TIS register for that trip event. It is possible at this point that a falling temperature trip event occurs before the software has had the time to clear the global interrupts status bit. But since software has already looked at the status register before this event happened, software may not clear the local status flag for this event. Therefore, after the global interrupt is cleared by software, software must look at the instantaneous status in the TSS register.

All bits in this register are reset to their defaults by PLTRST#.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>00h        | Reserved  |
| 9     | RWC<br>0b        | <b>Was Catastrophic Thermal Sensor Interrupt Event (WCTSIE):</b><br>1 = Indicates that a Catastrophic Thermal Sensor trip based on a higher to lower temperature transition thru the trip point<br>0 = No trip for this event                                     |
| 8     | RWC<br>0b        | <b>Was Hot Thermal Sensor Interrupt Event (WHTSIE):</b><br>1 = Indicates that a Hot Thermal Sensor trip based on a higher to lower temperature transition thru the trip point<br>0 = No trip for this event   |
| 7     | RWC<br>0b        | <b>Was Aux0 Thermal Sensor Interrupt Event (WAOTSIE):</b><br>1 = Indicates that an Aux0 Thermal Sensor trip based on a higher to lower temperature transition thru the trip point<br>0 = No trip for this event Software must write a 1 to clear this status bit. |
| 6:5   | RO<br>00b        | Reserved  |



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 4   | RWC<br>0b        | <p><b>Catastrophic Thermal Sensor Interrupt Event (CTSIE):</b></p> <p>1 = Indicates that a Catastrophic Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point.</p> <p>0 = No trip for this event Software must write a 1 to clear this status bit.</p> |
| 3   | RWC<br>0b        | <p><b>Hot Thermal Sensor Interrupt Event (HTSIE):</b></p> <p>1 = Indicates that a Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point.</p> <p>0 = No trip for this event Software must write a 1 to clear this status bit.</p>                   |
| 2   | RWC<br>0b        | <p><b>Aux0 Thermal Sensor Interrupt Event (A0TSIE):</b></p> <p>1 = Indicates that an Aux0 Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point.</p> <p>0 = No trip for this event Software must write a 1 to clear this status bit.</p>               |
| 1:0 | RO<br>00b        | Reserved  |



### 5.2.42 TSMICMD—Thermal SMI Command

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: CF1h  
Default Value: 00h  
Access: RO, RW  
Size: 8 bits

This register selects specific errors to generate a SMI DMI special cycle, as enabled by the Device 0 SMI Error Command Register [SMI on (G)MCH Thermal Sensor Trip]. The SMI must not be enabled at the same time as the SERR/SCI for the thermal sensor event.

All bits in this register are reset to their defaults by PLTRST#.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:3 | RO<br>00h        | Reserved  |
| 2   | RW<br>0b         | <b>SMI on (G)MCH Catastrophic Thermal Sensor Trip (SMGCTST):</b><br>1 = Does not mask the generation of an SMI DMI special cycle on a catastrophic thermal sensor trip.<br>0 = Disable reporting of this condition via SMI messaging. |
| 1   | RW<br>0b         | <b>SMI on (G)MCH Hot Thermal Sensor Trip (SMGHTST):</b><br>1 = Does not mask the generation of an SMI DMI special cycle on a Hot thermal sensor trip.<br>0 = Disable reporting of this condition via SMI messaging.                   |
| 0   | RW<br>0b         | <b>SMI on (G)MCH Aux Thermal Sensor Trip (SMGATST):</b><br>1 = Does not mask the generation of an SMI DMI special cycle on an Auxiliary thermal sensor trip.<br>0 = Disable reporting of this condition via SMI messaging.            |



### 5.2.43 PMSTS—Power Management Status

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: F14–F17h  
 Default Value: 00000000h  
 Access: RWC/S, RO  
 Size: 32 bits

This register is Reset by PWROK only.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 31:9 | RO<br>000000h    | Reserved  |
| 8    | RWC/S<br>0b      | <p><b>Warm Reset Occurred (WRO):</b> Set by the PMunit whenever a Warm Reset is received, and cleared by PWROK=0.</p> <p>0 = No Warm Reset occurred.<br/>                     1 = Warm Reset occurred.</p> <p><b>BIOS Requirement:</b> BIOS can check and clear this bit whenever executing POST code. This way BIOS knows that if the bit is set, then the PMSTS bits [1:0] must also be set, and if not BIOS needs to power-cycle the platform.</p>   |
| 7:2  | RO<br>00h        | Reserved  |
| 1    | RWC/S<br>0b      | <p><b>Channel 1 in Self-Refresh (C1SR):</b> Set by power management hardware after Channel 1 is placed in self refresh as a result of a Power State or a Reset Warn sequence.</p> <p>Cleared by Power management hardware before starting Channel 1 self refresh exit sequence initiated by a power management exit.</p> <p>Cleared by the BIOS by writing a 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence.</p> <p>0 = Channel 1 not ensured to be in self refresh.<br/>                     1 = Channel 1 in Self Refresh.</p> |
| 0    | RWC/S<br>0b      | <p><b>Channel 0 in Self-Refresh (COSR):</b> Set by power management hardware after Channel 0 is placed in self refresh as a result of a Power State or a Reset Warn sequence.</p> <p>Cleared by Power management hardware before starting Channel 0 self refresh exit sequence initiated by a power management exit.</p> <p>Cleared by the BIOS by writing a 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence.</p> <p>0 = Channel 0 not ensured to be in self refresh.<br/>                     1 = Channel 0 in Self Refresh.</p> |



## 5.3 EPBAR

Table 5-3. EPBAR Register Address Map

| Address Offset | Symbol | Register Name               | Default Value        | Access  |
|----------------|--------|-----------------------------|----------------------|---------|
| 44–47h         | EPESD  | EP Element Self Description | 00000201h            | RO, RWO |
| 50–53h         | EPLE1D | EP Link Entry 1 Description | 01000000h            | RO, RWO |
| 58–5Fh         | EPLE1A | EP Link Entry 1 Address     | 000000000<br>000000h | RO, RWO |
| 60–63h         | EPLE2D | EP Link Entry 2 Description | 02000002h            | RO, RWO |
| 68–6Fh         | EPLE2A | EP Link Entry 2 Address     | 000000000<br>008000h | RO      |

### 5.3.1 EPESD—EP Element Self Description

B/D/F/Type: 0/0/0/PXPEPBAR  
 Address Offset: 44–47h  
 Default Value: 00000201h  
 Access: RO, RWO  
 Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:24 | RO<br>00h        | <b>Port Number (PN):</b> This field specifies the port number associated with this element with respect to the component that contains this element. A value of 00h indicates to configuration software that this is the default Express port.   |
| 23:16 | RWO<br>00h       | <b>Component ID (CID):</b> This field indicates identifies the physical component that contains this Root Complex Element.<br><b>BIOS Requirement:</b> Must be initialized according to guidelines in the <i>PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> . |
| 15:8  | RO<br>0sh        | <b>Number of Link Entries (NLE):</b> This field indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PEG and DMI).  |
| 7:4   | RO<br>0h         | Reserved   |
| 3:0   | RO<br>1h         | <b>Element Type (ET):</b> This field indicates the type of the Root Complex Element. Value of 1 h represents a port to system memory.  |



### 5.3.2 EPLE1D—EP Link Entry 1 Description

B/D/F/Type: 0/0/0/PXPEPBAR  
 Address Offset: 50–53h  
 Default Value: 01000000h  
 Access: RO, RWO  
 Size: 32 bits

This register provides the first part of a Link Entry which declares an internal link to another Root Complex Element.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:24 | RO<br>01h        | <b>Target Port Number (TPN):</b> Specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.  |
| 23:16 | RWO<br>00h       | <b>Target Component ID (TCID):</b> This field indicates the physical or logical component that is targeted by this link entry.<br><b>BIOS Requirement:</b> Must be initialized according to guidelines in the <i>PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> . |
| 15:2  | RO<br>0000h      | Reserved   |
| 1     | RO<br>0b         | <b>Link Type (LTYP):</b> This field indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.   |
| 0     | RWO<br>0b        | <b>Link Valid (LV):</b><br>0 = Link Entry is not valid and will be ignored.<br>1 = Link Entry specifies a valid link.  |

### 5.3.3 EPLE1A—EP Link Entry 1 Address

B/D/F/Type: 0/0/0/PXPEPBAR  
 Address Offset: 58–5Fh  
 Default Value: 0000000000000000h  
 Access: RO, RWO  
 Size: 64 bits

This register provides the second part of a Link Entry which declares an internal link to another Root Complex Element.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 63:36 | RO<br>0s         | Reserved   |
| 35:12 | RWO<br>0s        | <b>Link Address (LA):</b> This field contains the memory mapped base address of the RCRB that is the target element (DMI) for this link entry. |
| 11:0  | RO<br>0s         | Reserved   |



### 5.3.4 EPLE2D—EP Link Entry 2 Description

|                 |                |
|-----------------|----------------|
| B/D/F/Type:     | 0/0/0/PXPEPBAR |
| Address Offset: | 60–63h         |
| Default Value:  | 02000002h      |
| Access:         | RO, RWO        |
| Size:           | 32 bits        |

This register provides the first part of a Link Entry which declares an internal link to another Root Complex Element.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:24 | RO<br>02h        | <b>Target Port Number (TPN):</b> This field specifies the port number associated with the element targeted by this link entry (PEG). The target port number is with respect to the component that contains this element as specified by the target component ID.  |
| 23:16 | RWO<br>00h       | <b>Target Component ID (TCID):</b> This field indicates the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component.<br><b>BIOS Requirement:</b> Must be initialized according to guidelines in the <i>PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> . |
| 15:2  | RO<br>0s         | Reserved  |
| 1     | RO<br>1b         | <b>Link Type (LTYP):</b> This field indicates that the link points to configuration space of the integrated device which controls the x16 root port.<br><br>The link address specifies the configuration address (segment, bus, device, function) of the target root port.  |
| 0     | RWO<br>0b        | <b>Link Valid (LV):</b><br>0 = Link Entry is not valid and will be ignored.<br>1 = Link Entry specifies a valid link.   |



### 5.3.5 EPLE2A—EP Link Entry 2 Address

B/D/F/Type: 0/0/0/PXPEPBAR  
 Address Offset: 68–6Fh  
 Default Value: 0000000000008000h  
 Access: RO  
 Size: 64 bits

This register provides the second part of a Link Entry which declares an internal link to another Root Complex Element.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 63:28 | RO<br>0s         | <b>Reserved for Configuration Space Base Address (C)</b> : Not required if root complex has only one configuration space. |
| 27:20 | RO<br>0s         | <b>Bus Number (BUSN)</b> :  |
| 19:15 | RO<br>00001b     | <b>Device Number (DEVN)</b> : Target for this link is PCI Express x16 port (Device 1).                                    |
| 14:12 | RO<br>000b       | <b>Function Number (FUNN)</b> :   |
| 11:0  | RO<br>0s         | Reserved  |

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## 6 PCI Express\* Registers (D1:F0)

Device 1 contains the controls associated with the PCI Express x16 root port that is the intended to attach as the point for external graphics. It also functions as the virtual PCI-to-PCI bridge.

**Warning:** When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The *PCI Express\* Specification* defines two types of reserved bits.

Reserved and Preserved:

1. Reserved for future RW implementations; software must preserve value read for writes to bits.
2. Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as reserved are part of the Reserved and Preserved type, which have historically been the typical definition for Reserved.

**Note:** Most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first Disable the link, then program the registers, and then re-enable the link (which will cause a full-retrain with the new settings).

**Table 6-1. PCI Express\* Register Address Map (Device 1, Function 0)**

| Address Offset | Register Symbol | Register Name           | Default Value            | Access  |
|----------------|-----------------|-------------------------|--------------------------|---------|
| 00–01h         | VID1            | Vendor Identification   | 8086h                    | RO      |
| 02–03h         | DID1            | Device Identification   | 29C1h                    | RO      |
| 04–05h         | PCICMD1         | PCI Command             | 0000h                    | RO, RW  |
| 06–07h         | PCISTS1         | PCI Status              | 0010h                    | RO, RWC |
| 08h            | RID1            | Revision Identification | See register description | RO      |
| 09–0Bh         | CC1             | Class Code              | 060400h                  | RO      |
| 0Ch            | CL1             | Cache Line Size         | 00h                      | RW      |
| 0Eh            | HDR1            | Header Type             | 01h                      | RO      |
| 18h            | PBUSN1          | Primary Bus Number      | 00h                      | RO      |
| 19h            | SBUSN1          | Secondary Bus Number    | 00h                      | RW      |
| 1Ah            | SUBUSN1         | Subordinate Bus Number  | 00h                      | RW      |



| Address Offset | Register Symbol | Register Name                             | Default Value | Access             |
|----------------|-----------------|---|---------------|--------------------|
| 1Ch            | IOBASE1         | I/O Base Address                          | F0h           | RW, RO             |
| 1D             | IOLIMIT1        | I/O Limit Address                         | 00h           | RW, RO             |
| 1E–1Fh         | SSTS1           | Secondary Status                          | 0000h         | RWC, RO            |
| 20–21h         | MBASE1          | Memory Base Address                       | FFF0h         | RW, RO             |
| 22–23h         | MLIMIT1         | Memory Limit Address                      | 0000h         | RW, RO             |
| 24–25h         | PMBASE1         | Prefetchable Memory Base Address          | FFF1h         | RW, RO             |
| 26–27h         | PMLIMIT1        | Prefetchable Memory Limit Address         | 0001h         | RW, RO             |
| 28–2Bh         | PMBASEU1        | Prefetchable Memory Base Address          | 00000000h     | RW,                |
| 2C–2Fh         | PMLIMITU1       | Prefetchable Memory Limit Address         | 00000000h     | RW                 |
| 34h            | CAPPTR1         | Capabilities Pointer                      | 88h           | RO                 |
| 3Ch            | INTRLINE1       | Interrupt Line                            | 00h           | RW                 |
| 3Dh            | INTRPIN1        | Interrupt Pin                             | 01h           | RO                 |
| 3E–3Fh         | BCTRL1          | Bridge Control                            | 0000h         | RO, RW             |
| 80–83h         | PM_CAPID1       | Power Management Capabilities             | C8039001h     | RO                 |
| 84–87h         | PM_CS1          | Power Management Control/Status           | 00000000h     | RO,<br>RW/S,<br>RW |
| 88–8Bh         | SS_CAPID        | Subsystem ID and Vendor ID Capabilities   | 0000800Dh     | RO                 |
| 8C–8Fh         | SS              | Subsystem ID and Subsystem Vendor ID      | 00008086h     | RWO                |
| 90–91h         | MSI_CAPID       | Message Signaled Interrupts Capability ID | A005h         | RO                 |
| 92–93h         | MC              | Message Control                           | 0000h         | RW, RO             |
| 94–97h         | MA              | Message Address                           | 00000000h     | RW, RO             |
| 98–99h         | MD              | Message Data                              | 0000h         | RW                 |
| A0–A1h         | PEG_CAPL        | PCI Express-G Capability List             | 0010h         | RO                 |
| A2–A3h         | PEG_CAP         | PCI Express-G Capabilities                | 0141h         | RO, RWO            |
| A4–A7h         | DCAP            | Device Capabilities                       | 00008000h     | RO                 |
| A8–A9h         | DCTL            | Device Control                            | 0000h         | RO, RW             |
| AA–ABh         | DSTS            | Device Status                             | 0000h         | RO, RWC            |
| AC–AFh         | LCAP            | Link Capabilities                         | 02014D01h     | RO, RWO            |
| B0–B1h         | LCTL            | Link Control                              | 0000h         | RO, RW,<br>RW/SC   |
| B2–B3h         | LSTS            | Link Status                               | 1001h         | RO                 |
| B4–B7h         | SLOTCAP         | Slot Capabilities                         | 00040000h     | RWO, RO            |



| Address Offset | Register Symbol | Register Name                              | Default Value         | Access  |
|----------------|-----------------|--|-----------------------|---------|
| B8–B9h         | SLOTCTL         | Slot Control                               | 01C0h                 | RO, RW  |
| BA–BBh         | SLOTSTS         | Slot Status                                | 0000h                 | RO, RWC |
| BC–BDh         | RCTL            | Root Control                               | 0000h                 | RO, RW  |
| C0– C3h        | RSTS            | Root Status                                | 00000000h             | RO, RWC |
| EC– EFh        | PEGLC           | PCI Express-G Legacy Control               | 00000000h             | RW, RO  |
| 100–103h       | VCECH           | Virtual Channel Enhanced Capability Header | 14010002h             | RO      |
| 104–107h       | PVCCAP1         | Port VC Capability Register 1              | 00000000h             | RO      |
| 108–10Bh       | PVCCAP2         | Port VC Capability Register 2              | 00000000h             | RO      |
| 10C–10Dh       | PVCCTL          | Port VC Control                            | 0000h                 | RO, RW  |
| 110–113h       | VCORCAP         | VC0 Resource Capability                    | 00000000h             | RO      |
| 114–117h       | VCORCTL         | VC0 Resource Control                       | 800000FFh             | RO, RW  |
| 11A–11Bh       | VCORSTS         | VC0 Resource Status                        | 0002h                 | RO      |
| 140–143h       | RCLDECH         | Root Complex Link Declaration Enhanced     | 00010005h             | RO      |
| 144–147h       | ESD             | Element Self Description                   | 02000100h             | RO, RWO |
| 150–153h       | LE1D            | Link Entry 1 Description                   | 00000000h             | RO, RWO |
| 158–15Fh       | LE1A            | Link Entry 1 Address                       | 0000000000<br>000000h | RO, RWO |
| 218–21Fh       | PEGSSTS         | PCI Express-G Sequence Status              | 0000000000<br>000FFFh | RO      |



## 6.1 PCI Express\* Configuration Register Details (D1:F0)

### 6.1.1 VID1—Vendor Identification

B/D/F/Type: 0/1/0/PCI  
Address Offset: 00–01h  
Default Value: 8086h  
Access: RO  
Size: 16 bits

This register combined with the Device Identification register uniquely identify any PCI device.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:0 | RO<br>8086h      | <b>Vendor Identification (VID1):</b> PCI standard identification for Intel. |

### 6.1.2 DID1—Device Identification

B/D/F/Type: 0/1/0/PCI  
Address Offset: 02–03h  
Default Value: 29C1h  
Access: RO  
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:8 | RO<br>29h        | <b>Device Identification Number (DID1(UB)):</b> Identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express Graphics port). |
| 7:4  | RO<br>7h         | <b>Device Identification Number (DID1(HW)):</b> Identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express Graphics port)  |
| 3:0  | RO<br>1h         | <b>Device Identification Number (DID1(LB)):</b> Identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express Graphics port). |



### 6.1.3 PCI\_CMD1—PCI Command

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 04–05h  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15:11 | RO<br>00h        | Reserved   |
| 10    | RW<br>0b         | <p><b>INTA Assertion Disable (INTAAD):</b> This bit Only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA–INTD assert and de-assert messages.</p> <p>0 = This device is permitted to generate INTA interrupt messages.</p> <p>1 = This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be de-asserted when this bit is set.</p>   |
| 9     | RO<br>0b         | <b>Fast Back-to-Back Enable (FB2B):</b> Not Applicable or Implemented. Hardwired to 0.   |
| 8     | RW<br>0b         | <p><b>SERR# Message Enable (SERRE1):</b> Controls Device 1 SERR# messaging. The (G)MCH communicates the SERR# condition by sending an SERR message to the ICH. This bit, when set, enables reporting of non-fatal and fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI Express specific bits in the Device Control Register.</p> <p>0 = The SERR message is generated by the (G)MCH for Device #1 only under conditions enabled individually through the Device Control Register.</p> <p>1 = The (G)MCH is enabled to generate SERR messages which will be sent to the ICH for specific Device 1 error conditions generated/detected on the primary side of the virtual PCI to PCI bridge (not those received by the secondary side). The status of SERRs generated is reported in the PCISTS1 register.</p> |
| 7     | RO<br>0b         | Reserved: Not Applicable or Implemented. Hardwired to 0.   |
| 6     | RW<br>0b         | <p><b>Parity Error Response Enable (PERRE):</b> This bit controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set.</p> <p>0 = Master Data Parity Error bit in PCI Status register can NOT be set.</p> <p>1 = Master Data Parity Error bit in PCI Status register CAN be set.</p>  |
| 5     | RO<br>0b         | <b>VGA Palette Snoop (VGAPS):</b> Not Applicable or Implemented. Hardwired to 0.   |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 4   | RO<br>0b         | <b>Memory Write and Invalidate Enable (MWIE):</b> Not Applicable or Implemented. Hardwired to 0.   |
| 3   | RO<br>0b         | <b>Special Cycle Enable (SCE):</b> Not Applicable or Implemented. Hardwired to 0.  |
| 2   | RW<br>0b         | <p><b>Bus Master Enable (BME):</b> This bit controls the ability of the PEG port to forward Memory and IO Read/Write Requests in the upstream direction. This bit does not affect forwarding of Completions from the primary interface to the secondary interface.</p> <p>0 = This device is prevented from making memory or IO requests to its primary bus. Note that according to PCI Specification, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, IO writes/reads, peer writes/reads, and MSIs will all be treated as invalid cycles. Writes are forwarded to memory address <b>000C_0000h</b> with byte enables de-asserted. Reads will be forwarded to memory address <b>000C_0000h</b> and will return Unsupported Request status (or Master abort) in its completion packet.</p> <p>1 = This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available.</p> |
| 1   | RW<br>0b         | <p><b>Memory Access Enable (MAE):</b></p> <p>0 = All of device 1's memory space is disabled.</p> <p>1 = Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.</p>   |
| 0   | RW<br>0b         | <p><b>IO Access Enable (IOAE):</b></p> <p>0 = All of device 1's I/O space is disabled.</p> <p>1 = Enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.</p>   |



### 6.1.4 PCISTS1—PCI Status

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 06–07h  
 Default Value: 0010h  
 Access: RO, RWC  
 Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express bridge embedded within the (G)MCH.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15   | RO<br>0b         | <b>Detected Parity Error (DPE):</b> Not Applicable or Implemented. Hardwired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device (error forwarding is not done).  |
| 14   | RWC<br>0b        | <b>Signaled System Error (SSE):</b> This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is 1. Both received (if enabled by BCTRL1[1]) and internally detected error messages affect this field.  |
| 13   | RO<br>0b         | <b>Received Master Abort Status (RMAS):</b> Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.   |
| 12   | RO<br>0b         | <b>Received Target Abort Status (RTAS):</b> Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.   |
| 11   | RO<br>0b         | <b>Signaled Target Abort Status (STAS):</b> Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.   |
| 10:9 | RO               | <b>DEVSELB Timing (DEVT):</b> This device is not the subtractively decoded device on bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.   |
| 8    | RO<br>0b         | <b>Master Data Parity Error (PMDPE):</b> Because the primary side of the PEG's virtual PCI-to-PCI bridge is integrated with the (G)MCH functionality there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The PCI specification defines it as a RWC, but for this implementation an RO definition behaves the same way and will meet all Microsoft testing requirements.<br><br>This bit can only be set when the Parity Error Enable bit in the PCI Command register is set. |
| 7    | RO<br>0b         | <b>Fast Back-to-Back (FB2B):</b> Not Applicable or Implemented. Hardwired to 0.   |
| 6    | RO<br>0b         | Reserved  |
| 5    | RO<br>0b         | <b>66/60MHz capability (CAP66):</b> Not Applicable or Implemented. Hardwired to 0.  |



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 4   | RO<br>1b         | <b>Capabilities List (CAPL):</b> Indicates that a capabilities list is present. Hardwired to 1.   |
| 3   | RO<br>0b         | <b>INTA Status (INTAS):</b> Indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and de-assert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit. |
| 2:0 | RO<br>000b       | Reserved  |

### 6.1.5 RID1—Revision Identification

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 08h  
 Default Value: See register table below  
 Access: RO  
 Size: 8 bits

This register contains the revision number of the (G)MCH device 1. These bits are read only and writes to this register have no effect.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RO<br>00h        | <b>Revision Identification Number (RID1):</b> This is an 8-bit value that indicates the revision identification number for the (G)MCH Device 0. Refer to the <i>Intel® G31/P31 Express Chipset Family Specification Update</i> for the value of the Revision ID register. |

### 6.1.6 CC1—Class Code

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 09–0Bh  
 Default Value: 060400h  
 Access: RO  
 Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register- specific programming interface.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 23:16 | RO<br>06h        | <b>Base Class Code (BCC):</b> This field indicates the base class code for this device. This code has the value 06h, indicating a Bridge device.  |
| 15:8  | RO<br>04h        | <b>Sub-Class Code (SUBCC):</b> This field indicates the sub-class code for this device. The code is 04h indicating a PCI to PCI Bridge.   |
| 7:0   | RO<br>00h        | <b>Programming Interface (PI):</b> This field indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device. |



### 6.1.7 CL1—Cache Line Size

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 0Ch  
 Default Value: 00h  
 Access: RW  
 Size: 8 bits

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RW<br>00h        | <b>Cache Line Size (Scratch pad):</b> Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality. |

### 6.1.8 HDR1—Header Type

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 0Eh  
 Default Value: 01h  
 Access: RO  
 Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>01h        | <b>Header Type Register (HDR):</b> Returns 01 to indicate that this is a single function device with bridge header layout. |

### 6.1.9 PBUSN1—Primary Bus Number

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 18h  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

This register identifies that this "virtual" Host-PCI Express bridge is connected to PCI bus #0.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RO<br>00h        | <b>Primary Bus Number (BUSN):</b> Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0. |



### 6.1.10 SBUSN1—Secondary Bus Number

B/D/F/Type: 0/1/0/PCI  
Address Offset: 19h  
Default Value: 00h  
Access: RW  
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" bridge (i.e., to PCI Express-G). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RW<br>00h        | <b>Secondary Bus Number (BUSN):</b> This field is programmed by configuration software with the bus number assigned to PCI Express. |

### 6.1.11 SUBUSN1—Subordinate Bus Number

B/D/F/Type: 0/1/0/PCI  
Address Offset: 1Ah  
Default Value: 00h  
Access: RW  
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express-G. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RW<br>00h        | <b>Subordinate Bus Number (BUSN):</b> This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device #1 bridge. When only a single PCI device resides on the PCI Express segment, this register will contain the same value as the SBUSN1 register. |



### 6.1.12 IOBASE1—I/O Base Address

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 1Ch  
 Default Value: F0h  
 Access: RW, RO  
 Size: 8 bits

This register controls the processor to PCI Express-G I/O access routing based on the following formula:

$$IO\_BASE \leq \text{address} \leq IO\_LIMIT$$

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4 KB boundary.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:4 | RW<br>Fh         | <b>I/O Address Base (IOBASE):</b> This field corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express. |
| 3:0 | RO<br>0h         | Reserved   |

### 6.1.13 IOLIMIT1—I/O Limit Address

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 1Dh  
 Default Value: 00h  
 Access: RW, RO  
 Size: 8 bits

This register controls the processor to PCI Express-G I/O access routing based on the following formula:

$$IO\_BASE \leq \text{address} \leq IO\_LIMIT$$

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4 KB aligned address block.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:4 | RW<br>0h         | <b>I/O Address Limit (IOLIMIT):</b> This field corresponds to A[15:12] of the I/O address limit of device 1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express hierarchy associated with this device. |
| 3:0 | RO<br>0h         | Reserved   |



### 6.1.14 SSTS1—Secondary Status

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 1E–1Fh  
 Default Value: 0000h  
 Access: RWC, RO  
 Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., PCI Express side) of the "virtual" PCI-PCI bridge embedded within (G)MCH.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15   | RWC<br>0b        | <b>Detected Parity Error (DPE):</b> This bit is set by the Secondary Side for a Type 1 Configuration Space header device whenever it receives a Poisoned TLP, regardless of the state of the Parity Error Response Enable bit in the Bridge Control Register.          |
| 14   | RWC<br>0b        | <b>Received System Error (RSE):</b> This bit is set when the Secondary Side for a Type 1 configuration space header device receives an ERR_FATAL or ERR_NONFATAL.  |
| 13   | RWC<br>0b        | <b>Received Master Abort (RMA):</b> This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Unsupported Request Completion Status.                 |
| 12   | RWC<br>0b        | <b>Received Target Abort (RTA):</b> This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Completer Abort Completion Status.                     |
| 11   | RO<br>0b         | <b>Signaled Target Abort (STA):</b> Not Applicable or Implemented. Hardwired to 0. The (G)MCH does not generate Target Aborts (the (G)MCH will never complete a request using the Completer Abort Completion status).  |
| 10:9 | RO<br>00b        | <b>DEVSELB Timing (DEVT):</b> Not Applicable or Implemented. Hardwired to 0.   |
| 8    | RWC<br>0b        | <b>Master Data Parity Error (SMDPE):</b> When set, this bit indicates that the (G)MCH received across the link (upstream) a Read Data Completion Poisoned TLP (EP=1). This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set. |
| 7    | RO<br>0b         | <b>Fast Back-to-Back (FB2B):</b> Not Applicable or Implemented. Hardwired to 0.  |
| 6    | RO<br>0b         | Reserved   |
| 5    | RO<br>0b         | <b>66/60 MHz capability (CAP66):</b> Not Applicable or Implemented. Hardwired to 0.  |
| 4:0  | RO<br>00h        | Reserved   |



### 6.1.15 MBASE1—Memory Base Address

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 20–21h  
 Default Value: FFF0h  
 Access: RW, RO  
 Size: 16 bits

This register controls the processor-to-PCI Express non-prefetchable memory access routing based on the following formula:

$$\text{MEMORY\_BASE} \leq \text{address} \leq \text{MEMORY\_LIMIT}$$

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:4 | RW<br>FFFh       | <b>Memory Address Base (MBASE):</b> This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express. |
| 3:0  | RO<br>0h         | Reserved  |



### 6.1.16 MLIMIT1—Memory Limit Address

B/D/F/Type: 0/1/0/PCI  
Address Offset: 22–23h  
Default Value: 0000h  
Access: RW, RO  
Size: 16 bits

This register controls the processor to PCI Express-G non-prefetchable memory access routing based on the following formula:

$$\text{MEMORY\_BASE} \leq \text{address} \leq \text{MEMORY\_LIMIT}$$

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block. NOTE: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved processor - PCI Express memory access performance.

Note also that configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges i.e. prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the (G)MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not ensured.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:4 | RW<br>000h       | <b>Memory Address Limit (MLIMIT):</b> This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express. |
| 3:0  | RO<br>0h         | Reserved  |



### 6.1.17 PMBASE1—Prefetchable Memory Base Address

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 24–25h  
 Default Value: FFF1h  
 Access: RW, RO  
 Size: 16 bits

This register in conjunction with the corresponding Upper Base Address register controls the processor-to-PCI Express prefetchable memory access routing based on the following formula:

$$\text{PREFETCHABLE\_MEMORY\_BASE} \leq \text{address} \leq \text{PREFETCHABLE\_MEMORY\_LIMIT}$$

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:4 | RW<br>FFFh       | <b>Prefetchable Memory Base Address (MBASE):</b> This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express.   |
| 3:0  | RO<br>1h         | <b>64-bit Address Support:</b> This field indicates that the upper 32 bits of the prefetchable memory region base address are contained in the Prefetchable Memory base Upper Address register at 28h. |



### 6.1.18 PMLIMIT1—Prefetchable Memory Limit Address

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/1/0/PCI |
| Address Offset: | 26–27h    |
| Default Value:  | 0001h     |
| Access:         | RW, RO    |
| Size:           | 16 bits   |

This register in conjunction with the corresponding Upper Limit Address register controls the processor-to-PCI Express prefetchable memory access routing based on the following formula:

$$\text{PREFETCHABLE\_MEMORY\_BASE} \leq \text{address} \leq \text{PREFETCHABLE\_MEMORY\_LIMIT}$$

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e. prefetchable) from the processor perspective.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:4 | RW<br>000h       | <b>Prefetchable Memory Address Limit (PMLIMIT):</b> This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express.  |
| 3:0  | RO<br>1h         | <b>64-bit Address Support:</b> This field indicates that the upper 32 bits of the prefetchable memory region limit address are contained in the Prefetchable Memory Base Limit Address register at 2Ch |



### 6.1.19 PMBASEU1—Prefetchable Memory Base Address

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 28–2Bh  
 Default Value: 00000000h  
 Access: RW  
 Size: 32 bits

The functionality associated with this register is present in the PEG design implementation.

This register in conjunction with the corresponding Upper Base Address register controls the processor-to-PCI Express prefetchable memory access routing based on the following formula:

$$\text{PREFETCHABLE\_MEMORY\_BASE} \leq \text{address} \leq \text{PREFETCHABLE\_MEMORY\_LIMIT}$$

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 31:0 | RW<br>00000000h  | <b>Prefetchable Memory Base Address (MBaseU)</b> : This field corresponds to A[63:32] of the lower limit of the prefetchable memory range that will be passed to PCI Express. |



### 6.1.20 PMLIMITU1—Prefetchable Memory Limit Address

B/D/F/Type: 0/1/0/PCI  
Address Offset: 2C–2Fh  
Default Value: 00000000h  
Access: RW  
Size: 32 bits

The functionality associated with this register is present in the PEG design implementation.

This register in conjunction with the corresponding Upper Limit Address register controls the processor-to-PCI Express prefetchable memory access routing based on the following formula:

$$\text{PREFETCHABLE\_MEMORY\_BASE} \leq \text{address} \leq \text{PREFETCHABLE\_MEMORY\_LIMIT}$$

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block.

Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e. prefetchable) from the processor perspective.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 31:0 | RW<br>00000000h  | <b>Prefetchable Memory Address Limit (MLIMITU):</b> This field corresponds to A[63:32] of the upper limit of the prefetchable Memory range that will be passed to PCI Express. |



### 6.1.21 CAPPTR1—Capabilities Pointer

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 34h  
 Default Value: 88h  
 Access: RO  
 Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RO<br>88h        | <b>First Capability (CAPPTR1):</b> The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability. |

### 6.1.22 INTRLIN1—Interrupt Line

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 3Ch  
 Default Value: 00h  
 Access: RW  
 Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RW<br>00h        | <b>Interrupt Connection (INTCON):</b> Used to communicate interrupt line routing information. |

### 6.1.23 INTRPIN1—Interrupt Pin

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 3Dh  
 Default Value: 01h  
 Access: RO  
 Size: 8 bits

This register specifies which interrupt pin this device uses.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>01h        | <b>Interrupt Pin (INTRPIN):</b> As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h=INTA. |



### 6.1.24 BCTRL1—Bridge Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 3E–3Fh  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-to-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., PCI Express) as well as some bits that affect the overall behavior of the "virtual" Host-PCI Express bridge in the (G)MCH (e.g., VGA compatible address ranges mapping).

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:12 | RO<br>0h         | Reserved  |
| 11    | RO<br>0b         | <b>Discard Timer SERR# Enable (DTSERRE)</b> : Not Applicable or Implemented. Hardwired to 0.  |
| 10    | RO<br>0b         | <b>Discard Timer Status (DTSTS)</b> : Not Applicable or Implemented. Hardwired to 0.  |
| 9     | RO<br>0b         | <b>Secondary Discard Timer (SDT)</b> : Not Applicable or Implemented. Hardwired to 0.   |
| 8     | RO<br>0b         | <b>Primary Discard Timer (PDT)</b> : Not Applicable or Implemented. Hardwired to 0.   |
| 7     | RO<br>0b         | <b>Fast Back-to-Back Enable (FB2BEN)</b> : Not Applicable or Implemented. Hardwired to 0.   |
| 6     | RW<br>0b         | <b>Secondary Bus Reset (SRESET)</b> : Setting this bit triggers a hot reset on the corresponding PCI Express Port. This will force the LTSSM to transition to the Hot Reset state (via Recovery) from L0, L0s, or L1 states.  |
| 5     | RO<br>0b         | <b>Master Abort Mode (MAMODE)</b> : Does not apply to PCI Express. Hardwired to 0.  |
| 4     | RW<br>0b         | <b>VGA 16-bit Decode (VGA16D)</b> : Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge.<br><br>0 = Execute 10-bit address decodes on VGA I/O accesses.<br>1 = Execute 16-bit address decodes on VGA I/O accesses. |
| 3     | RW<br>0b         | <b>VGA Enable (VGAEN)</b> : This bit controls the routing of processor initiated transactions targeting VGA compatible I/O and memory address ranges.   |



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 2   | RW<br>0b         | <p><b>ISA Enable (ISAEN):</b> Needed to exclude legacy resource decode to route ISA resources to legacy decode path. This bit modifies the response by the (G)MCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers.</p> <p>0 = All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to PCI Express.</p> <p>1 = (G)MCH will not forward to PCI Express any I/O transactions addressing the last 768 bytes in each 1 KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers.</p> |
| 1   | RW<br>0b         | <p><b>SERR Enable (SERREN):</b></p> <p>0 = No forwarding of error messages from secondary side to primary side that could result in an SERR.</p> <p>1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.</p>  |
| 0   | RW<br>0b         | <p><b>Parity Error Response Enable (PEREN):</b> This bit controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the (G)MCH receives across the link (upstream) a Read Data Completion Poisoned TLP.</p> <p>0 = Master Data Parity Error bit in Secondary Status register can NOT be set.</p> <p>1 = Master Data Parity Error bit in Secondary Status register CAN be set.</p>  |



### 6.1.25 PM\_CAPID1—Power Management Capabilities

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 80–83h  
 Default Value: C8039001h  
 Access: RO  
 Size: 32 bits

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:27 | RO<br>19h        | <b>PME Support (PMES):</b> This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot & D3cold. This device is not required to do anything to support D3hot & D3cold, it simply must report that those states are supported. Refer to the PCI Power Management 1.1 specification for encoding explanation and other power management details. |
| 26    | RO<br>0b         | <b>D2 Power State Support (D2PSS):</b> Hardwired to 0 to indicate that the D2 power management state is NOT supported.   |
| 25    | RO<br>0b         | <b>D1 Power State Support (D1PSS):</b> Hardwired to 0 to indicate that the D1 power management state is NOT supported.   |
| 24:22 | RO<br>000b       | <b>Auxiliary Current (AUXC):</b> Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.  |
| 21    | RO<br>0b         | <b>Device Specific Initialization (DSI):</b> Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.  |
| 20    | RO<br>0b         | <b>Auxiliary Power Source (APS):</b> Hardwired to 0.   |
| 19    | RO<br>0b         | <b>PME Clock (PMECLK):</b> Hardwired to 0 to indicate this device does NOT support PMEB generation.  |
| 18:16 | RO<br>011b       | <b>PCI PM CAP Version (PCIPMCV):</b> A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.  |
| 15:8  | RO<br>90h        | <b>Pointer to Next Capability (PNC):</b> This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h  |
| 7:0   | RO<br>01h        | <b>Capability ID (CID):</b> Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.  |



### 6.1.26 PM\_CS1—Power Management Control/Status

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 84–87h  
 Default Value: 00000000h  
 Access: RO, RW/S, RW  
 Size: 32 bits

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:16 | RO<br>0000h      | Reserved: Not Applicable or Implemented. Hardwired to 0.  |
| 15    | RO<br>0b         | <b>PME Status (PMESTS):</b> This bit indicates that this device does not support PME# generation from D3cold.   |
| 14:13 | RO<br>00b        | <b>Data Scale (DSCALE):</b> This field indicates that this device does not support the power management data register.  |
| 12:9  | RO<br>0h         | <b>Data Select (DSEL):</b> This field indicates that this device does not support the power management data register.   |
| 8     | RW/S<br>0b       | <b>PME Enable (PMEE):</b> This bit indicates that this device does not generate PMEB assertion from any D-state.<br>0 = PMEB generation not possible from any D State<br>1 = PMEB generation enabled from any D State<br>The setting of this bit has no effect on hardware.<br>See PM_CAP[15:11]  |
| 7:2   | RO<br>00h        | Reserved  |
| 1:0   | RW<br>00b        | <b>Power State (PS):</b> This field indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs.<br>00 = D0<br>01 = D1 (Not supported in this device.)<br>10 = D2 (Not supported in this device.)<br>11 = D3<br>Support of D3cold does not require any special action.<br>While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state to be fully-functional.<br>When the Power State is other than D0, the bridge will Master Abort (i.e., not claim) any downstream cycles (with exception of type 0 configuration cycles). Consequently, these unclaimed cycles will go down DMI and come back up as Unsupported Requests, which the (G)MCH logs as Master Aborts in Device 0 PCISTS[13]<br>There is no additional hardware functionality required to support these Power States. |



### 6.1.27 SS\_CAPID—Subsystem ID and Vendor ID Capabilities

B/D/F/Type: 0/1/0/PCI  
Address Offset: 88–8Bh  
Default Value: 0000800Dh  
Access: RO  
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:16 | RO<br>0000h      | Reserved   |
| 15:8  | RO<br>80h        | <b>Pointer to Next Capability (PNC):</b> This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.   |
| 7:0   | RO<br>0Dh        | <b>Capability ID (CID):</b> Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge. |

### 6.1.28 SS—Subsystem ID and Subsystem Vendor ID

B/D/F/Type: 0/1/0/PCI  
Address Offset: 8C–8Fh  
Default Value: 00008086h  
Access: RWO  
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and a hardware reset.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:16 | RWO<br>0000h     | <b>Subsystem ID (SSID):</b> This field identifies the particular subsystem and is assigned by the vendor.   |
| 15:0  | RWO<br>8086h     | <b>Subsystem Vendor ID (SSVID):</b> This field identifies the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group. |



### 6.1.29 MSI\_CAPID—Message Signaled Interrupts Capability ID

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 90–91h  
 Default Value: A005h  
 Access: RO  
 Size: 16 bits

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:8 | RO<br>A0h        | <b>Pointer to Next Capability (PNC):</b> This field contains a pointer to the next item in the capabilities list which is the PCI Express capability. |
| 7:0  | RO<br>05h        | <b>Capability ID (CID):</b> A value of 05h identifies this linked list item (capability structure) as being for MSI registers.                        |

### 6.1.30 MC—Message Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 92–93h  
 Default Value: 0000h  
 Access: RW, RO  
 Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is ensured to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:8 | RO<br>00h        | Reserved   |
| 7    | RO<br>0b         | <b>64-bit Address Capable (64AC):</b> Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address.  |
| 6:4  | RW<br>000b       | <b>Multiple Message Enable (MME):</b> System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested.<br><br>The encoding is the same as for the MMC field below. |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 3:1 | RO<br>000b       | <b>Multiple Message Capable (MMC):</b> System software reads this field to determine the number of messages being requested by this device.<br><br>000 = 1 message requested<br><br>All other encodings are reserved.  |
| 0   | RW<br>0b         | <b>MSI Enable (MSIEN):</b> This bit controls the ability of this device to generate MSIs.<br><br>0 = MSI will not be generated.<br><br>1 = MSI will be generated when we receive PME or HotPlug messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set. |

### 6.1.31 MA—Message Address

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 94–97h  
 Default Value: 00000000h  
 Access: RW, RO  
 Size: 32 bits

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 31:2 | RW<br>00000000h  | <b>Message Address (MA):</b> Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address. |
| 1:0  | RO<br>00b        | <b>Force DWord Align (FDWA):</b> Hardwired to 0 so that addresses assigned by system software are always aligned on a DWord address boundary.   |

### 6.1.32 MD—Message Data

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 98–99h  
 Default Value: 0000h  
 Access: RW  
 Size: 16 bits

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:0 | RW<br>0000h      | <b>Message Data (MD):</b> Base message data pattern assigned by system software and used to handle an MSI from the device.<br><br>When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register. |



### 6.1.33 PEG\_CAPL—PCI Express\*-G Capability List

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/1/0/PCI |
| Address Offset: | A0–A1h    |
| Default Value:  | 0010h     |
| Access:         | RO        |
| Size:           | 16 bits   |

This register enumerates the PCI Express capability structure.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:8 | RO<br>00h        | <b>Pointer to Next Capability (PNC):</b> This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express Extended Configuration Space. |
| 7:0  | RO<br>10h        | <b>Capability ID (CID):</b> This field identifies this linked list item (capability structure) as being for PCI Express registers.  |

### 6.1.34 PEG\_CAP—PCI Express\*-G Capabilities

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/1/0/PCI |
| Address Offset: | A2–A3h    |
| Default Value:  | 0141h     |
| Access:         | RO, RWO   |
| Size:           | 16 bits   |

This register indicates PCI Express device capabilities.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:14 | RO<br>00b        | Reserved  |
| 13:9  | RO<br>00h        | <b>Interrupt Message Number (IMN):</b> Not Applicable or Implemented. Hardwired to 0.   |
| 8     | RWO<br>1b        | <b>Slot Implemented (SI):</b><br>0 = The PCI Express Link associated with this port is connected to an integrated component or is disabled.<br>1 = The PCI Express Link associated with this port is connected to a slot. |
| 7:4   | RO<br>4h         | <b>Device/Port Type (DPT):</b> Hardwired to 4h to indicate root port of PCI Express Root Complex.   |
| 3:0   | RO<br>1h         | <b>PCI Express Capability Version (PCI EXPRESS*CV):</b> Hardwired to 1 as it is the first version.  |



### 6.1.35 DCAP—Device Capabilities

B/D/F/Type: 0/1/0/PCI  
Address Offset: A4–A7h  
Default Value: 00008000h  
Access: RO  
Size: 32 bits

This register indicates PCI Express device capabilities.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:16 | RO<br>0000h      | Reserved: Not Applicable or Implemented. Hardwired to 0.   |
| 15    | RO<br>1b         | <b>Role Based Error Reporting (RBER)</b> : This bit indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 specification. |
| 14:6  | RO<br>000h       | Reserved: Not Applicable or Implemented. Hardwired to 0.   |
| 5     | RO<br>0b         | <b>Extended Tag Field Supported (ETFS)</b> : Hardwired to indicate support for 5-bit Tags as a Requestor.  |
| 4:3   | RO<br>00b        | <b>Phantom Functions Supported (PFS)</b> : Not Applicable or Implemented. Hardwired to 0.  |
| 2:0   | RO<br>000b       | <b>Max Payload Size (MPS)</b> : Hardwired to indicate 128B max supported payload for Transaction Layer Packets (TLP).  |



### 6.1.36 DCTL—Device Control

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/1/0/PCI |
| Address Offset: | A8–A9h    |
| Default Value:  | 0000h     |
| Access:         | RO, RW    |
| Size:           | 16 bits   |

This register provides control for PCI Express device specific capabilities.

The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR\_CORR, ERR\_NONFATAL, ERR\_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:8 | RO<br>000h       | Reserved   |
| 7:5  | RW<br>000b       | <p><b>Max Payload Size (MPS):</b></p> <p>000 = 128B max supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value.</p> <p>All other encodings are reserved.</p> <p>Hardware will actually ignore this field. It is writeable only to support compliance testing.</p>  |
| 4    | RO<br>0b         | Reserved: For Enable Relaxed Ordering  |
| 3    | RW<br>0b         | <p><b>Unsupported Request Reporting Enable (URRE):</b> When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_CORR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_CORR is signaled when an unmasked Advisory Non-Fatal UR is received. An ERR_FATAL or ERR_NONFATAL is sent to the Root Control register when an uncorrectable non-Advisory UR is received with the severity bit set in the Uncorrectable Error Severity register.</p> |
| 2    | RW<br>0b         | <p><b>Fatal Error Reporting Enable (FERE):</b> When set, enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.</p>  |
| 1    | RW<br>0b         | <p><b>Non-Fatal Error Reporting Enable (NERE):</b> When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.</p>   |
| 0    | RW<br>0b         | <p><b>Correctable Error Reporting Enable (CERE):</b> When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.</p>   |



### 6.1.37 DSTS—Device Status

B/D/F/Type: 0/1/0/PCI  
 Address Offset: AA–ABh  
 Default Value: 0000h  
 Access: RO, RWC  
 Size: 16 bits

This register reflects status corresponding to controls in the Device Control register. The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:6 | RO<br>000h       | Reserved and Zero: For future R/WC/S implementations; software must use 0 for writes to bits.  |
| 5    | RO<br>0b         | <b>Transactions Pending (TP):</b><br>0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed.<br>1 = Device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).  |
| 4    | RO<br>0b         | Reserved   |
| 3    | RWC<br>0b        | <b>Unsupported Request Detected (URD):</b><br>0 = Unsupported request <b>Not</b> detected.<br>1 = Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.<br><br>Additionally, the Non-Fatal Error Detected bit or the Fatal Error Detected bit is set according to the setting of the Unsupported Request Error Severity bit. In production systems setting the Fatal Error Detected bit is not an option as support for AER will not be reported. |
| 2    | RWC<br>0b        | <b>Fatal Error Detected (FED):</b><br>0 = Fatal error <b>Not</b> detected.<br>1 = Fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.  |
| 1    | RWC<br>0b        | <b>Non-Fatal Error Detected (NFED):</b><br>0 = Non-Fatal error <b>Not</b> detected.<br>1 = Non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.<br><br>When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.  |



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 0   | RWC<br>0b        | <p><b>Correctable Error Detected (CED):</b></p> <p>0 = Correctable error <b>Not</b> detected.</p> <p>1 = Correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.</p> <p>When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the correctable error mask register.</p> |

### 6.1.38 LCAP—Link Capabilities

B/D/F/Type: 0/1/0/PCI  
 Address Offset: AC–AFh  
 Default Value: 02014D01h  
 Access: RO, RWO  
 Size: 32 bits

This register indicates PCI Express device specific capabilities.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:24 | RO<br>02h        | <p><b>Port Number (PN):</b> This field indicates the PCI Express port number for the given PCI Express link. Matches the value in Element Self Description[31:24].</p>  |
| 23:21 | RO<br>000b       | Reserved  |
| 20    | RO<br>0b         | <p><b>Data Link Layer Link Active Reporting Capable (DLLARC):</b> For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable field of the Slot Capabilities register), this bit must be set to 1b.</p> <p>For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.</p> |
| 19    | RO<br>0b         | <p><b>Surprise Down Error Reporting Capable (SDERC):</b> For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of detecting and reporting a Surprise Down error condition.</p> <p>For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.</p>   |



| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 18    | RO<br>0b         | <p><b>Clock Power Management (CPM):</b> A value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) when the link is in the L1 and L2/3 Ready link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these link states.</p> <p>This capability is applicable only in form factors that support “clock request” (CLKREQ#) capability.</p> <p>For a multi-function device, each function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the multifunction device indicate a 1b in this bit.</p> |
| 17:15 | RWO<br>010b      | <p><b>L1 Exit Latency (L1ELAT):</b> This field indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010b indicates the range of 2 us to less than 4 us.</p> <p>Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.</p>   |
| 14:12 | RO<br>100b       | <p><b>L0s Exit Latency (LOSELAT):</b> Indicates the length of time this Port requires to complete the transition from L0s to L0.</p> <p>000 = Less than 64 ns<br/>           001 = 64ns to less than 128ns<br/>           010 = 128ns to less than 256 ns<br/>           011 = 256ns to less than 512 ns<br/>           100 = 512ns to less than 1 us<br/>           101 = 1 us to less than 2 us<br/>           110 = 2 us – 4 us<br/>           111 = More than 4 us</p> <p>The actual value of this field depends on the common Clock Configuration bit (LCTL[6]) and the Common and Non-Common clock L0s Exit Latency values in PEGLOSLAT (Offset 22Ch)</p>   |
| 11:10 | RWO<br>11b       | <p><b>Active State Link PM Support (ASLPMS):</b></p> <p>00 = Reserved<br/>           01 = L0s is supported<br/>           10 = Reserved<br/>           11 = L1 and L0s are supported</p> <p><b>BIOS Requirement:</b> Desktop chipsets do not support ASPM L1, so BIOS should program this field to 01.</p>  |
| 9:4   | RO<br>10h        | <p><b>Max Link Width (MLW):</b> This field indicates the maximum number of lanes supported for this link.</p>   |
| 3:0   | RO<br>1h         | <p><b>Max Link Speed (MLS):</b> Hardwired to indicate 2.5 Gb/s.</p>   |



### 6.1.39 LCTL—Link Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: B0–B1h  
 Default Value: 0000h  
 Access: RO, RW, RW/SC  
 Size: 16 bits  
 BIOS Optimal Default: 0h

This register allows control of PCI Express link.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:9 | RO<br>0000000b   | Reserved   |
| 8    | RO<br>0b         | <p><b>Enable Clock Power Management (ECPM):</b> Applicable only for form factors that support a “Clock Request” (CLKREQ#) mechanism, this enable functions as follows</p> <p>0 = Disable. Clock power management is disabled and device must hold CLKREQ# signal low (Default)</p> <p>1 = Enable. Device is permitted to use CLKREQ# signal to power manage link clock according to protocol defined in appropriate form factor specification.</p> <p>Components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities Register) must hardwire this bit to 0b.</p> |
| 7    | RW<br>0b         | <p><b>Extended Synch (ES):</b></p> <p>0 = Standard Fast Training Sequence (FTS).</p> <p>1 = Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state.</p> <p>This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication.</p> <p>This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.</p>  |
| 6    | RW<br>0b         | <p><b>Common Clock Configuration (CCC):</b> The state of this bit affects the L0s Exit Latency reported in LCAP[14:12] and the N_FTS value advertised during link training. See PEGLOSLAT at offset 22Ch.</p> <p>0 = This component and the component at the opposite end of this Link are operating with asynchronous reference clock.</p> <p>1 = This component and the component at the opposite end of this Link are operating with a distributed common reference clock.</p>  |
| 5    | RW/SC<br>0b      | <p><b>Retrain Link (RL):</b> This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).</p> <p>0 = Normal operation.</p> <p>1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state.</p>  |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 4   | RW<br>0b         | <b>Link Disable (LD):</b> Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.<br>0 = Normal operation<br>1 = Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0, L0s, or L1 states. Link retraining happens automatically on 0 to 1 transition, just like when coming out of reset. |
| 3   | RO<br>0b         | <b>Read Completion Boundary (RCB):</b> Hardwired to 0 to indicate 64 byte.   |
| 2   | RW<br>0b         | <b>Far-End Digital Loopback (FEDLB):</b>   |
| 1:0 | RW<br>00b        | <b>Active State PM (ASPM):</b> This field controls the level of active state power management supported on the given link.<br>00 = Disabled<br>01 = L0s Entry Supported<br>10 = Reserved<br>11 = L0s and L1 Entry Supported  |



### 6.1.40 LSTS—Link Status

B/D/F/Type: 0/1/0/PCI  
 Address Offset: B2–B3h  
 Default Value: 1001h  
 Access: RO  
 Size: 16 bits

This register indicates PCI Express link status.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15:14 | RO<br>00b        | Reserved and Zero: For future R/WC/S implementations; software must use 0 for writes to bits.  |
| 13    | RO<br>0b         | <b>Data Link Layer Link Active (Optional) (DLLLA):</b> This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise.<br><br>This bit must be implemented if the corresponding Data Link Layer Active Capability bit is implemented. Otherwise, this bit must be hardwired to 0b. |
| 12    | RO<br>1b         | <b>Slot Clock Configuration (SCC):</b><br><br>0 = The device uses an independent clock irrespective of the presence of a reference on the connector.<br><br>1 = The device uses the same physical reference clock that the platform provides on the connector.   |
| 11    | RO<br>0b         | <b>Link Training (LTRN):</b> This bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.  |
| 10    | RO<br>0b         | <b>Undefined:</b> The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.   |
| 9:4   | RO<br>00h        | <b>Negotiated Width (NW):</b> Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed).<br><br>00h = Reserved<br>01h = X1<br>02h = Reserved<br>04h = Reserved<br>08h = Reserved<br>10h = X16<br><br>All other encodings are reserved.                          |
| 3:0   | RO<br>1h         | <b>Negotiated Speed (NS):</b> Indicates negotiated link speed.<br><br>1h = 2.5 Gb/s<br><br>All other encodings are reserved.   |



### 6.1.41 SLOTCAP—Slot Capabilities

B/D/F/Type: 0/1/0/PCI  
 Address Offset: B4–B7h  
 Default Value: 00040000h  
 Access: RWO, RO  
 Size: 32 bits

PCI Express Slot related registers allow for the support of Hot Plug.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:19 | RWO<br>0000h     | <b>Physical Slot Number (PSN):</b> Indicates the physical slot number attached to this Port.   |
| 18    | RWO<br>1b        | <b>No Command Completed Support (NCCS):</b><br>1 = This slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set to 1b if the hotplug capable port is able to accept writes to all fields of the Slot Control register without delay between successive writes.       |
| 17    | RO<br>0b         | Reserved for Electromechanical Interlock Present (EIP):  |
| 16:15 | RWO<br>00b       | <b>Slot Power Limit Scale (SPLS):</b> This field specifies the scale used for the Slot Power Limit Value.<br><br>00 = 1.0x<br>01 = 0.1x<br>10 = 0.01x<br>11 = 0.001x<br><br>If this field is written, the link sends a Set_Slot_Power_Limit message.   |
| 14:7  | RWO<br>00h       | <b>Slot Power Limit Value (SPLV):</b> In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field.<br><br>If this field is written, the link sends a Set_Slot_Power_Limit message. |
| 6     | RO<br>0b         | <b>Hot-plug Capable (HPC):</b><br>0 = Not Hot-plug capable<br>1 = Slot is capable of supporting hot-lug operations.  |
| 5     | RO<br>0b         | <b>Hot-plug Surprise (HPS):</b><br>0 = No Hot-plug surprise<br>1 = An adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation.                     |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 4   | RO<br>0b         | <b>Power Indicator Present (PIP):</b><br>0 = No power indicator<br>1 = A Power Indicator is electrically controlled by the chassis for this slot.                                  |
| 3   | RO<br>0b         | <b>Attention Indicator Present (AIP):</b><br>0 = No Attention indicator<br>1 = An Attention Indicator is electrically controlled by the chassis.                                   |
| 2   | RO<br>0b         | <b>MRL Sensor Present (MSP):</b><br>0 = No MRL sensor<br>1 = MRL Sensor is implemented on the chassis for this slot.   |
| 1   | RO<br>0b         | <b>Power Controller Present (PCP):</b><br>0 = No power controller<br>1 = A software programmable Power Controller is implemented for this slot/adaptor (depending on form factor). |
| 0   | RO<br>0b         | <b>Attention Button Present (ABP):</b><br>0 = No attention button<br>1 = An Attention Button for this slot is electrically controlled by the chassis.                              |

### 6.1.42 SLOTCTL—Slot Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: B8–B9h  
 Default Value: 01C0h  
 Access: RO, RW  
 Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:13 | RO<br>000b       | Reserved  |
| 12    | RO<br>0b         | <b>Data Link Layer State Changed Enable (DLLSCE):</b> If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed.                                     |
| 11    | RO<br>0b         | <b>Electromechanical Interlock Control (EIC):</b> If an Electromechanical Interlock is implemented, a write of 1b to this field causes the state of the interlock to toggle. A write of 0b to this field has no effect. A read to this register always returns a 0. |



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 10  | RO<br>0b         | <p><b>Power Controller Control (PCC):</b> If a Power Controller is implemented, this field when written sets the power state of the slot per the defined encodings. Reads of this field must reflect the value from the latest write, even if the corresponding hotplug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined.</p> <p>Depending on the form factor, the power is turned on/off either to the slot or within the adapter. Note that in some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting.</p> <p>The defined encodings are:</p> <p>0 = Power On<br/>1 = Power Off</p> <p>If the Power Controller Implemented field in the Slot Capabilities register is set to 0b, then writes to this field have no effect and the read value of this field is undefined.</p> |
| 9:8 | RO<br>01b        | <p><b>Power Indicator Control (PIC):</b> If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined.</p> <p>00 = Reserved<br/>01 = On<br/>10 = Blink<br/>11 = Off</p>  |
| 7:6 | RO<br>11b        | <p><b>Attention Indicator Control (AIC):</b> If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state.</p> <p>Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. If the indicator is electrically controlled by chassis, the indicator is controlled directly by the downstream port through implementation specific mechanisms.</p> <p>00 = Reserved<br/>01 = On<br/>10 = Blink<br/>11 = Off</p>  |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 5   | RO<br>0b         | <b>Hot-plug Interrupt Enable (HPIE):</b><br>0 = Disable<br>1 = Enables generation of an interrupt on enabled hot-plug events<br>Default value of this field is 0b. If the Hot Plug Capable field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b.   |
| 4   | RO<br>0b         | <b>Command Completed Interrupt Enable (CCI):</b> If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), when set to 1b, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller.<br><br>If Command Completed notification is not supported, this bit must be hardwired to 0b. |
| 3   | RW<br>0b         | <b>Presence Detect Changed Enable (PDCE):</b><br>0 = Disable<br>1 = Enables software notification on a presence detect changed event.  |
| 2   | RO<br>0b         | <b>MRL Sensor Changed Enable (MSCE):</b> If the MRL Sensor Present field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b.<br><br>0 = Disable (default)<br>1 = Enables software notification on a MRL sensor changed event.  |
| 1   | RO<br>0b         | <b>Power Fault Detected Enable (PFDE):</b> If Power Fault detection is not supported, this bit is permitted to be read-only with a value of 0b.<br><br>0 = Disable (default)<br>1 = Enables software notification on a power fault event.  |
| 0   | RO<br>0b         | <b>Attention Button Pressed Enable (ABPE):</b><br>0 = Disable (default)<br>1 = Enables software notification on an attention button pressed event.   |



### 6.1.43 SLOTSTS—Slot Status

B/D/F/Type: 0/1/0/PCI  
 Address Offset: BA–BBh  
 Default Value: 0000h  
 Access: RO, RWC  
 Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:7 | RO<br>0000000b   | Reserved and Zero: For future R/WC/S implementations; software must use 0 for writes to bits.  |
| 6    | RO<br>0b         | <p><b>Presence Detect State (PDS):</b> This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism.</p> <p>0 = Slot Empty<br/>           1 = Card Present in slot</p> <p>This register must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities Register is 0b), this bit must return 1b.</p> |
| 5    | RO<br>0b         | Reserved   |
| 4    | RO<br>0b         | <p><b>Command Completed (CC):</b> If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no assurance that the action corresponding to the command is complete.</p> <p>If Command Completed notification is not supported, this bit must be hardwired to 0b.</p>  |
| 3    | RWC<br>0b        | <b>Detect Changed (PDC):</b> This bit is set when the value reported in Presence Detect State is changed.  |
| 2    | RO<br>0b         | <b>MRL Sensor Changed (MSC):</b> If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set.   |



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 1   | RO<br>0b         | <b>Power Fault Detected (PFD):</b> If a Power Controller that supports power fault detection is implemented, this bit is set when the Power Controller detects a power fault at this slot. Note that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set. |
| 0   | RO<br>0b         | <b>Attention Button Pressed (ABP):</b> If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set.  |

### 6.1.44 RCTL—Root Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: BC–BDh  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

This register allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:4 | RO<br>000h       | Reserved   |
| 3    | RW<br>0b         | <b>PME Interrupt Enable (PMEIE):</b><br>0 = No interrupts are generated as a result of receiving PME messages.<br>1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state. |
| 2    | RW<br>0b         | <b>System Error on Fatal Error Enable (SEFEE):</b> This bit controls the Root Complex's response to fatal errors.<br>0 = No SERR generated on receipt of fatal error.<br>1 = SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.  |



| Bit | Access & Default | Description  |
|-----|------------------|--|
| 1   | RW<br>0b         | <p><b>System Error on Non-Fatal Uncorrectable Error Enable (SENFUEE):</b> This bit controls the Root Complex's response to non-fatal errors.</p> <p>0 = No SERR generated on receipt of non-fatal error.</p> <p>1 = SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.</p> |
| 0   | RW<br>0b         | <p><b>System Error on Correctable Error Enable (SECEE):</b> This bit controls the Root Complex's response to correctable errors.</p> <p>0 = No SERR generated on receipt of correctable error.</p> <p>1 = SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.</p>         |

### 6.1.45 RSTS—Root Status

B/D/F/Type: 0/1/0/PCI  
 Address Offset: C0–C3h  
 Default Value: 00000000h  
 Access: RO, RWC  
 Size: 32 bits

This register provides information about PCI Express Root Complex specific parameters.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:18 | RO<br>0000h      | Reserved  |
| 17    | RO<br>0b         | <p><b>PME Pending (PMEP):</b></p> <p>1 = Another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.</p> |
| 16    | RWC<br>0b        | <p><b>PME Status (PMES):</b></p> <p>1 = PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.</p>   |
| 15:0  | RO<br>0000h      | <p><b>PME Requestor ID (PMERID):</b> This field indicates the PCI requestor ID of the last PME requestor.</p>   |



### 6.1.46 PEGLC—PCI Express\*-G Legacy Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: EC–EFh  
 Default Value: 00000000h  
 Access: RW, RO  
 Size: 32 bits

This register controls functionality that is needed by Legacy (non-PCI Express aware) operating systems during run time.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 31:3 | RO<br>00000000h  | Reserved   |
| 2    | RW<br>Ob         | <b>PME GPE Enable (PMEGPE):</b><br>0 = Do not generate GPE PME message when PME is received.<br>1 = Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the (G)MCH to support PMEs on the PEG port under legacy operating systems.   |
| 1    | RW<br>Ob         | <b>Hot-Plug GPE Enable (HPGPE):</b><br>0 = Do not generate GPE Hot-Plug message when Hot-Plug event is received.<br>1 = Generate a GPE Hot-Plug message when Hot-Plug Event is received (Assert_HPGPE and Deassert_HPGPE messages on DMI). This enables the (G)MCH to support Hot-Plug on the PEG port under legacy operating systems.   |
| 0    | RW<br>Ob         | <b>General Message GPE Enable (GENGPE):</b><br>0 = Do not forward received GPE assert/de-assert messages.<br>1 = Forward received GPE assert/de-assert messages. These general GPE message can be received via the PEG port from an external Intel device (i.e., PxH) and will be subsequently forwarded to the ICH (via Assert_GPE and Deassert_GPE messages on DMI). For example, PxH might send this message if a PCI Express device is hot plugged into a PxH downstream port. |



### 6.1.47 VCECH—Virtual Channel Enhanced Capability Header

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/1/0/MMR |
| Address Offset: | 100–103h  |
| Default Value:  | 14010002h |
| Access:         | RO        |
| Size:           | 32 bits   |

This register indicates PCI Express device Virtual Channel capabilities. Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:20 | RO<br>140h       | <b>Pointer to Next Capability (PNC):</b> The Link Declaration Capability is the next in the PCI Express extended capabilities list.                                     |
| 19:16 | RO<br>1h         | <b>PCI Express Virtual Channel Capability Version (PCI EXPRESS*VCCV):</b> Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. |
| 15:0  | RO<br>0002h      | <b>Extended Capability ID (ECID):</b> Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.       |

### 6.1.48 PVCCAP1—Port VC Capability Register 1

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/1/0/MMR |
| Address Offset: | 104–107h  |
| Default Value:  | 00000000h |
| Access:         | RO        |
| Size:           | 32 bits   |

This register describes the configuration of PCI Express Virtual Channels associated with this port.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 31:7 | RO<br>0000000h   | Reserved   |
| 6:4  | RO<br>000b       | <b>Low Priority Extended VC Count (LPEVCC):</b> This field indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration.<br>The value of 0 in this field implies strict VC arbitration. |
| 3    | RO<br>0b         | Reserved   |
| 2:0  | RO<br>000b       | <b>Extended VC Count (EVCC):</b> This field indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.   |



### 6.1.49 PVCCAP2—Port VC Capability Register 2

B/D/F/Type: 0/1/0/MMR  
 Address Offset: 108–10Bh  
 Default Value: 00000000h  
 Access: RO  
 Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:24 | RO<br>00h        | <b>VC Arbitration Table Offset (VCATO):</b> This field indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority). |
| 23:0  | RO<br>0s         | Reserved  |

### 6.1.50 PVCCTL—Port VC Control

B/D/F/Type: 0/1/0/MMR  
 Address Offset: 10C–10Dh  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:4 | RO<br>000h       | Reserved  |
| 3:1  | RW<br>000b       | <b>VC Arbitration Select (VCAS):</b> This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. Since there is no other VC supported than the default, this field is reserved. |
| 0    | RO<br>0b         | Reserved  |



### 6.1.51 VCORCAP—VC0 Resource Capability

B/D/F/Type: 0/1/0/MMR  
Address Offset: 110–113h  
Default Value: 00000000h  
Access: RO  
Size: 32 bits

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:16 | RO<br>0000h      | Reserved   |
| 15    | RO<br>0b         | <b>Reject Snoop Transactions (RSNPT):</b><br>0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC.<br>1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request. |
| 14:0  | RO<br>0000h      | Reserved   |



### 6.1.52 VCORCTL—VCO Resource Control

B/D/F/Type: 0/1/0/MMR  
 Address Offset: 114–117h  
 Default Value: 80000FFh  
 Access: RO, RW  
 Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31    | RO<br>1b         | <b>VCO Enable (VCOE)</b> : For VCO, this is hardwired to 1 and read only as VCO can never be disabled.   |
| 30:27 | RO<br>0h         | Reserved   |
| 26:24 | RO<br>000b       | <b>VCO ID (VCOID)</b> : Assigns a VC ID to the VC resource. For VCO, this is hardwired to 0 and read only.   |
| 23:8  | RO<br>0000h      | Reserved   |
| 7:1   | RW<br>7Fh        | <b>TC/VCO Map (TCVCOM)</b> : This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. |
| 0     | RO<br>1b         | <b>TC0/VCO Map (TC0VCOM)</b> : Traffic Class 0 is always routed to VCO.  |



### 6.1.53 VCORSTS—VCO Resource Status

B/D/F/Type: 0/1/0/MMR  
Address Offset: 11A–11Bh  
Default Value: 0002h  
Access: RO  
Size: 16 bits

This register reports the Virtual Channel specific status.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:2 | RO<br>0000h      | Reserved   |
| 1    | RO<br>1b         | <b>VCO Negotiation Pending (VCONP):</b><br>0 = The VC negotiation is complete.<br>1 = The VC resource is still in the process of negotiation (initialization or disabling).<br><br>This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state.<br><br>Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link. |
| 0    | RO<br>0b         | Reserved   |



### 6.1.54 RCLDECH—Root Complex Link Declaration Enhanced

B/D/F/Type: 0/1/0/MMR  
 Address Offset: 140–143h  
 Default Value: 00010005h  
 Access: RO  
 Size: 32 bits

This capability declares links from this element (PEG) to other elements of the root complex component to which it belongs. See PCI Express specification for link/topology declaration requirements.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:20 | RO<br>000h       | <b>Pointer to Next Capability (PNC):</b> This is the last capability in the PCI Express extended capabilities list   |
| 19:16 | RO<br>1h         | <b>Link Declaration Capability Version (LDCV):</b> Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification.                   |
| 15:0  | RO<br>0005h      | <b>Extended Capability ID (ECID):</b> Value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability. |

### 6.1.55 ESD—Element Self Description

B/D/F/Type: 0/1/0/MMR  
 Address Offset: 144–147h  
 Default Value: 02000100h  
 Access: RO, RWO  
 Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:24 | RO<br>02h        | <b>Port Number (PN):</b> This field specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the Express port of the component to provide arbitration to this Root Complex Element. |
| 23:16 | RWO<br>00h       | <b>Component ID (CID):</b> This field identifies the physical component that contains this Root Complex Element.  |
| 15:8  | RO<br>01h        | <b>Number of Link Entries (NLE):</b> This field indicates the number of link entries following the Element Self Description. This field reports 1 (to Express port only as we don't report any peer-to-peer capabilities in our topology).  |
| 7:4   | RO<br>0h         | Reserved  |
| 3:0   | RO<br>0h         | <b>Element Type (ET):</b> This field indicates the type of the Root Complex Element. Value of 0h represents a root port.  |



### 6.1.56 LE1D—Link Entry 1 Description

|                 |           |
|-----------------|-----------|
| B/D/F/Type:     | 0/1/0/MMR |
| Address Offset: | 150–153h  |
| Default Value:  | 00000000h |
| Access:         | RO, RWO   |
| Size:           | 32 bits   |

This register provides the first part of a Link Entry which declares an internal link to another Root Complex Element.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:24 | RO<br>00h        | <b>Target Port Number (TPN):</b> This field specifies the port number associated with the element targeted by this link entry (Express Port). The target port number is with respect to the component that contains this element as specified by the target component ID. |
| 23:16 | RWO<br>00h       | <b>Target Component ID (TCID):</b> This field identifies the physical or logical component that is targeted by this link entry.   |
| 15:2  | RO<br>0000h      | Reserved  |
| 1     | RO<br>0b         | <b>Link Type (LTYP):</b> This field indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.  |
| 0     | RWO<br>0b        | <b>Link Valid (LV):</b><br>0 = Link Entry is not valid and will be ignored.<br>1 = Link Entry specifies a valid link.   |

### 6.1.57 LE1A—Link Entry 1 Address

|                 |                   |
|-----------------|-------------------|
| B/D/F/Type:     | 0/1/0/MMR         |
| Address Offset: | 158–15Fh          |
| Default Value:  | 0000000000000000h |
| Access:         | RO, RWO           |
| Size:           | 64 bits           |

This register provides the second part of a Link Entry which declares an internal link to another Root Complex Element.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 63:32 | RO<br>00000000h  | Reserved  |
| 31:12 | RWO<br>0000h     | <b>Link Address (LA):</b> This field contains the memory-mapped base address of the RCRB that is the target element (Express Port) for this link entry. |
| 11:0  | RO<br>00h        | Reserved  |



### 6.1.58 PEGSSTS—PCI Express\* -G Sequence Status

B/D/F/Type: 0/1/0/MMR  
 Address Offset: 218–21Fh  
 Default Value: 0000000000000FFFh  
 Access: RO  
 Size: 64 bits

This register provides PCI Express status reporting that is required by the PCI Express specification.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 63:60 | RO<br>0h         | Reserved   |
| 59:48 | RO<br>000h       | <b>Next Transmit Sequence Number (NTSN):</b> This field indicates the value of the NXT_TRANS_SEQ counter. This counter represents the transmit Sequence number to be applied to the next TLP to be transmitted onto the Link for the first time. |
| 47:44 | RO<br>0h         | Reserved   |
| 43:32 | RO<br>000h       | <b>Next Packet Sequence Number (NPSN):</b> This field indicates the packet sequence number to be applied to the next TLP to be transmitted or re-transmitted onto the Link.  |
| 31:28 | RO<br>0h         | Reserved   |
| 27:16 | RO<br>000h       | <b>Next Receive Sequence Number (NRSN):</b> This field is the sequence number associated with the TLP that is expected to be received next.  |
| 15:12 | RO<br>0h         | Reserved   |
| 11:0  | RO<br>FFFh       | <b>Last Acknowledged Sequence Number (LASN):</b> This field is the sequence number associated with the last acknowledged TLP.  |

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## 7 Direct Memory Interface (DMI) Registers

This Root Complex Register Block (RCRB) controls the (G)MCH-ICH9 serial interconnect. The base address of this space is programmed in DMIBAR in D0:F0 configuration space. Table 7-1 provides an address map of the DMI registers listed by address offset in ascending order. Section 7.1 provides register bit descriptions.

**Table 7-1. DMI Register Address Map**

| Address Offset | Register Symbol | Register Name                           | Default Value | Access  |
|----------------|-----------------|---|---------------|---------|
| 00–03h         | DMIVCECH        | DMI Virtual Channel Enhanced Capability | 04010002h     | RO      |
| 04–07h         | DMIPVCCAP1      | DMI Port VC Capability Register 1       | 00000001h     | RWO, RO |
| 08–0Bh         | DMIPVCCAP2      | DMI Port VC Capability Register 2       | 00000000h     | RO      |
| 0C–0Dh         | DMIPVCCTL       | DMI Port VC Control                     | 0000h         | RO, RW  |
| 10–13h         | DMIVCORCAP      | DMI VC0 Resource Capability             | 00000001h     | RO      |
| 14–17h         | DMIVCORCTL0     | DMI VC0 Resource Control                | 800000FFh     | RO, RW  |
| 1A–1Bh         | DMIVCORSTS      | DMI VC0 Resource Status                 | 0002h         | RO      |
| 1C–1Fh         | DMIVC1RCAP      | DMI VC1 Resource Capability             | 00008001h     | RO      |
| 20–23h         | DMIVC1RCTL1     | DMI VC1 Resource Control                | 01000000h     | RW, RO  |
| 26–27h         | DMIVC1RSTS      | DMI VC1 Resource Status                 | 0002h         | RO      |
| 84–87h         | DMILCAP         | DMI Link Capabilities                   | 00012C41h     | RO, RWO |
| 88–89h         | DMILCTL         | DMI Link Control                        | 0000h         | RW, RO  |
| 8A–8Bh         | DMILSTS         | DMI Link Status                         | 0001h         | RO      |



## 7.1 Direct Memory Interface (DMI) Configuration Register Details

### 7.1.1 DMIVCECH—DMI Virtual Channel Enhanced Capability

B/D/F/Type: 0/0/0/DMIBAR  
Address Offset: 00–03h  
Default Value: 04010002h  
Access: RO  
Size: 32 bits

This register indicates DMI Virtual Channel capabilities.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:20 | RO<br>040h       | <b>Pointer to Next Capability (PNC):</b> This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability). |
| 19:16 | RO<br>1h         | <b>PCI Express* Virtual Channel Capability Version (PCI EXPRESS*VCCV):</b> Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification.               |
| 15:0  | RO<br>0002h      | <b>Extended Capability ID (ECID):</b> Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.                       |



### 7.1.2 DMIPVCCAP1—DMI Port VC Capability Register 1

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 04–07h  
 Default Value: 00000001h  
 Access: RWO, RO  
 Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 31:7 | RO<br>0000000h   | Reserved   |
| 6:4  | RO<br>000b       | <b>Low Priority Extended VC Count (LPEVCC):</b> This field indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration.<br><br>The value of 0 in this field implies strict VC arbitration. |
| 3    | RO<br>0b         | Reserved   |
| 2:0  | RWO<br>001b      | <b>Extended VC Count (EVCC):</b> This field indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.<br><br>The Private Virtual Channel is not included in this count.   |

### 7.1.3 DMIPVCCAP2—DMI Port VC Capability Register 2

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 08–0Bh  
 Default Value: 00000000h  
 Access: RO  
 Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

| Bit  | Access & Default | Description |
|------|------------------|-------------|
| 31:0 | RO<br>00000000h  | Reserved    |



### 7.1.4 DMIPVCCTL—DMI Port VC Control

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 0C–0Dh  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:4 | RO<br>000h       | Reserved  |
| 3:1  | RW<br>000b       | <b>VC Arbitration Select (VCAS):</b> This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field.<br><br>See the PCI express specification for more details. |
| 0    | RO<br>0b         | Reserved  |

### 7.1.5 DMIVCORCAP—DMI VC0 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 10–13h  
 Default Value: 00000001h  
 Access: RO  
 Size: 32 bits

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:16 | RO<br>00000h     | Reserved   |
| 15    | RO<br>0b         | <b>Reject Snoop Transactions (REJSNPT):</b><br>0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC.<br>1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request. |
| 14:8  | RO<br>00h        | Reserved   |
| 7:0   | RO<br>01h        | <b>Port Arbitration Capability (PAC):</b> Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.   |



### 7.1.6 DMIVCORCTLO—DMI VCO Resource Control

|                 |              |
|-----------------|--------------|
| B/D/F/Type:     | 0/0/0/DMIBAR |
| Address Offset: | 14–17h       |
| Default Value:  | 800000FFh    |
| Access:         | RO, RW       |
| Size:           | 32 bits      |

This register controls the resources associated with PCI Express Virtual Channel 0.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31    | RO<br>1b         | <b>Virtual Channel 0 Enable (VCOE)</b> : For VCO this is hardwired to 1 and read only as VCO can never be disabled.   |
| 30:27 | RO<br>0h         | Reserved  |
| 26:24 | RO<br>000b       | <b>Virtual Channel 0 ID (VCOID)</b> : Assigns a VC ID to the VC resource. For VCO this is hardwired to 0 and read only.   |
| 23:20 | RO<br>0h         | Reserved  |
| 19:17 | RW<br>000b       | <b>Port Arbitration Select (PAS)</b> : This field configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource. Because only bit 0 of that field is asserted.<br><br>This field will always be programmed to 1.  |
| 16:8  | RO<br>000h       | Reserved  |
| 7:1   | RW<br>7Fh        | <b>Traffic Class / Virtual Channel 0 Map (TCVCOM)</b> : This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values.<br><br>For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. To remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. |
| 0     | RO<br>1b         | <b>Traffic Class 0 / Virtual Channel 0 Map (TCOVCOM)</b> : Traffic Class 0 is always routed to VCO.   |



### 7.1.7 DMIVCORSTS—DMI VCO Resource Status

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 1A–1Bh  
 Default Value: 0002h  
 Access: RO  
 Size: 16 bits

This register reports the Virtual Channel specific status.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:2 | RO<br>0000h      | Reserved.   |
| 1    | RO<br>1b         | <p><b>Virtual Channel 0 Negotiation Pending (VCONP):</b> This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state.</p> <p>0 = The VC negotiation is complete.<br/>           1 = The VC resource is still in the process of negotiation (initialization or disabling).</p> <p><b>BIOS Requirement:</b> Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.</p> |
| 0    | RO<br>0b         | Reserved  |

### 7.1.8 DMIVC1RCAP—DMI VC1 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 1C–1Fh  
 Default Value: 00008001h  
 Access: RO  
 Size: 32 bits

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:16 | RO<br>00000h     | Reserved  |
| 15    | RO<br>1b         | <p><b>Reject Snoop Transactions (REJSNPT):</b></p> <p>0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC.<br/>           1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.</p> |
| 14:8  | RO<br>00h        | Reserved  |
| 7:0   | RO<br>01h        | <p><b>Port Arbitration Capability (PAC):</b> Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.</p>   |



### 7.1.9 DMIVC1RCTL1—DMI VC1 Resource Control

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 20–23h  
 Default Value: 01000000h  
 Access: RW, RO  
 Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 1.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31    | RW<br>0b         | <b>Virtual Channel 1 Enable (VC1E):</b><br>0 = Virtual Channel is disabled.<br>1 = Virtual Channel is enabled.  |
| 30:27 | RO<br>0h         | Reserved  |
| 26:24 | RW<br>001b       | <b>Virtual Channel 1 ID (VC1ID):</b> This field assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.   |
| 23:20 | RO<br>0h         | Reserved  |
| 19:17 | RW<br>000b       | <b>Port Arbitration Select (PAS):</b> This field configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.   |
| 16:8  | RO<br>000h       | Reserved  |
| 7:1   | RW<br>00h        | <b>Traffic Class / Virtual Channel 1 Map (TCVC1M):</b> This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values.<br><br>For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. |
| 0     | RO<br>0b         | <b>Traffic Class 0 / Virtual Channel 1 Map (TC0VC1M):</b> Traffic Class 0 is always routed to VC0.  |



### 7.1.10 DMIVC1RSTS—DMI VC1 Resource Status

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 26–27h  
 Default Value: 0002h  
 Access: RO  
 Size: 16 bits

This register reports the Virtual Channel specific status.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:2 | RO<br>0000h      | Reserved  |
| 1    | RO<br>1b         | <b>Virtual Channel 1 Negotiation Pending (VC1NP):</b><br>0 = The VC negotiation is complete.<br>1 = The VC resource is still in the process of negotiation (initialization or disabling). |
| 0    | RO<br>0b         | Reserved  |

### 7.1.11 DMILCAP—DMI Link Capabilities

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 84–87h  
 Default Value: 00012C41h  
 Access: RO, RWO  
 Size: 32 bits

This register indicates DMI specific capabilities.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:18 | RO<br>0000h      | Reserved   |
| 17:15 | RWO<br>010b      | <b>L1 Exit Latency (L1SELAT):</b> This field indicates the length of time this Port requires to complete the transition from L1 to L0.<br>010b = 2 us to less than 4 us.     |
| 14:12 | RWO<br>010b      | <b>LOs Exit Latency (LOSELAT):</b> This field indicates the length of time this Port requires to complete the transition from LOs to L0.<br>010 = 128 ns to less than 256 ns |
| 11:10 | RO<br>11b        | <b>Active State Link PM Support (ASLPMS):</b> L0s & L1 entry supported.  |
| 9:4   | RO<br>04h        | <b>Max Link Width (MLW):</b> This field indicates the maximum number of lanes supported for this link.   |
| 3:0   | RO<br>1h         | <b>Max Link Speed (MLS):</b> Hardwired to indicate 2.5 Gb/s.   |



### 7.1.12 DMILCTL—DMI Link Control

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 88–89h  
 Default Value: 0000h  
 Access: RW, RO  
 Size: 16 bits

This register allows control of DMI.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:8 | RO<br>00h        | Reserved   |
| 7    | RW<br>0b         | <b>Extended Synch (EXTSYNC):</b><br>0 = Standard Fast Training Sequence (FTS).<br>1 = Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state.  |
| 6:3  | RO<br>0h         | Reserved   |
| 2    | RW<br>0b         | <b>Far-End Digital Loopback (FEDLB):</b>   |
| 1:0  | RW<br>00b        | <b>Active State Power Management Support (ASPMS):</b> This field controls the level of active state power management supported on the given link.<br>00 = Disabled<br>01 = L0s Entry Supported<br>10 = Reserved<br>11 = L0s and L1 Entry Supported |



### 7.1.13 DMILSTS—DMI Link Status

B/D/F/Type: 0/0/0/DMIBAR  
Address Offset: 8A–8Bh  
Default Value: 0001h  
Access: RO  
Size: 16 bits

This register indicates DMI status.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:10 | RO<br>00h        | Reserved and Zero for future R/WC/S implementations. Software must use 0 for writes to these bits.  |
| 9:4   | RO<br>00h        | <b>Negotiated Width (NWID):</b> This field indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed).<br>04h = X4<br>All other encodings are reserved. |
| 3:0   | RO<br>1h         | <b>Negotiated Speed (NSPD):</b> This field indicates negotiated link speed.<br>1h = 2.5 Gb/s<br>All other encodings are reserved.   |



## 8 Integrated Graphics Registers (D2:F0,F1) (Intel® 82G31 GMCH Only)

The Integrated Graphics Device (IGD) registers are located in Device 2 (D0), Function 0 (F0) and Function 1 (F1). This chapter provides the descriptions for these registers. Section 8.1 provides the register descriptions for Device 2, Function 0. Section 8.2 provides the register descriptions for Device 2, Function 1.

### 8.1 Integrated Graphics Register Details (D2:F0)

Device 2, Function 0 contains registers for the internal graphics functions. Table 8-1 lists the PCI configuration registers in order of ascending offset address.

Function 0 can be VGA compatible or not, this is selected through bit 1 of GGC register (Device 0, offset 52h).

**Note:** The following sections describe Device 2 PCI configuration registers only.

**Table 8-1. Integrated Graphics Device Register Address Map (Device 2, Function 0)**

| Address Offset | Register Symbol | Register Name                   | Default Value            | Access |
|----------------|-----------------|---------------------------------|--------------------------|--------|
| 00–01h         | VID2            | Vendor Identification           | 8086h                    | RO     |
| 02–03h         | DID             | Device Identification           | 29C2h                    | RO     |
| 04–05h         | PCICMD2         | PCI Command                     | 0000h                    | RO, RW |
| 06–07h         | PCISTS2         | PCI Status                      | 0090h                    | RO     |
| 08h            | RID2            | Revision Identification         | See register description | RO     |
| 09–0Bh         | CC              | Class Code                      | 030000h                  | RO     |
| 0Ch            | CLS             | Cache Line Size                 | 00h                      | RO     |
| 0Dh            | MLT2            | Master Latency Timer            | 00h                      | RO     |
| 0Eh            | HDR2            | Header Type                     | 80h                      | RO     |
| 10–13h         | MMADR           | Memory Mapped Range Address     | 00000000h                | RO, RW |
| 2C–2Dh         | SVID2           | Subsystem Vendor Identification | 0000h                    | RWO    |
| 2E–2Fh         | SID2            | Subsystem Identification        | 0000h                    | RWO    |
| 30–33h         | ROMADR          | Video BIOS ROM Base Address     | 00000000h                | RO     |



| Address Offset | Register Symbol | Register Name                    | Default Value                                | Access   |
|----------------|-----------------|----------------------------------|--|----------|
| 34h            | CAPPOINT        | Capabilities Pointer             | 90h  | RO       |
| 3Eh            | MINGNT          | Minimum Grant                    | 00h  | RO       |
| 3Fh            | MAXLAT          | Maximum Latency                  | 00h  | RO       |
| 40–50h         | CAPID0          | Capability Identifier            | 00000000<br>00000001<br>00000000<br>10B0009h | RO       |
| 52–53h         | MGGC            | GMCH Graphics Control Register   | 0030h  | RO       |
| 54–57h         | DEVEN           | Device Enable                    | 00003DBh                                     | RO       |
| 58–5Bh         | SSRW            | Software Scratch Read Write      | 00000000h                                    | RW       |
| 5C–5Fh         | BSM             | Base of Stolen Memory            | 07800000h                                    | RO       |
| 60–61h         | HSRW            | Hardware Scratch Read Write      | 0000h  | RW       |
| C0h            | GDRST           | Graphics Debug Reset             | 00h  | RO, RW/L |
| D0–D1h         | PMCAPID         | Power Management Capabilities ID | 0001h  | RWO, RO  |
| D2–D3h         | PMCAP           | Power Management Capabilities    | 0022h  | RO       |
| D4–D5h         | PMCS            | Power Management Control/Status  | 0000h  | RO, RW   |
| E0–E1h         | SWSMI           | Software SMI                     | 0000h  | RW       |
| E4–E7h         | ASLE            | System Display Event Register    | 00000000h                                    | RW       |
| FC–FFh         | ASLS            | ASL Storage                      | 00000000h                                    | RW       |

### 8.1.1 VID2—Vendor Identification

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 00–01h  
 Default Value: 8086h  
 Access: RO  
 Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:0 | RO<br>8086h      | <b>Vendor Identification Number (VID):</b> PCI standard identification for Intel. |



### 8.1.2 DID—Device Identification

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 02–03h  
 Default Value: 29C2h  
 Access: RO  
 Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:0 | RO<br>29C2h      | <b>Device Identification Number (DID):</b> This is a 16 bit value assigned to the GMCH Graphic device. |

### 8.1.3 PCICMD2—PCI Command

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 04–05h  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:11 | RO<br>00h        | Reserved  |
| 10    | RW<br>0b         | <b>Interrupt Disable (INTDIS):</b> This bit disables the device from asserting INTx#.<br>0 = Enable the assertion of this device's INTx# signal.<br>1 = Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.                              |
| 9     | RO<br>0b         | <b>Fast Back-to-Back (FB2B):</b> Not Implemented. Hardwired to 0.   |
| 8     | RO<br>0b         | <b>SERR Enable (SERRE):</b> Not Implemented. Hardwired to 0.  |
| 7     | RO<br>0b         | <b>Address/Data Stepping Enable (ADSTEP):</b> Not Implemented. Hardwired to 0.  |
| 6     | RO<br>0b         | <b>Parity Error Enable (PERRE):</b> Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation. |



*Integrated Graphics Registers (D2:F0,F1) (Intel® 82G31 GMCH Only)*

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 5   | RO<br>0b         | <b>Video Palette Snooping (VPS):</b> This bit is hardwired to 0 to disable snooping.  |
| 4   | RO<br>0b         | <b>Memory Write and Invalidate Enable (MWIE):</b> Hardwired to 0. The IGD does not support memory write and invalidate commands.  |
| 3   | RO<br>0b         | <b>Special Cycle Enable (SCE):</b> This bit is hardwired to 0. The IGD ignores Special cycles.  |
| 2   | RW<br>0b         | <b>Bus Master Enable (BME):</b> This bit controls the IGD's response to bus master accesses.<br><br>0 = Disable IGD bus mastering.<br><br>1 = Enable the IGD to function as a PCI compliant master. |
| 1   | RW<br>0b         | <b>Memory Access Enable (MAE):</b> This bit controls the IGD's response to memory space accesses.<br><br>0 = Disable.<br><br>1 = Enable.  |
| 0   | RW<br>0b         | <b>I/O Access Enable (IOAE):</b> This bit controls the IGD's response to I/O space accesses.<br><br>0 = Disable.<br><br>1 = Enable.   |



### 8.1.4 PCISTS2—PCI Status

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 06–07h  
 Default Value: 0090h  
 Access: RO  
 Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15   | RO<br>0b         | <b>Detected Parity Error (DPE):</b> Since the IGD does not detect parity, this bit is always hardwired to 0.  |
| 14   | RO<br>0b         | <b>Signaled System Error (SSE):</b> The IGD never asserts SERR#, therefore this bit is hardwired to 0.  |
| 13   | RO<br>0b         | <b>Received Master Abort Status (RMAS):</b> The IGD never gets a Master Abort, therefore this bit is hardwired to 0.  |
| 12   | RO<br>0b         | <b>Received Target Abort Status (RTAS):</b> The IGD never gets a Target Abort, therefore this bit is hardwired to 0.  |
| 11   | RO<br>0b         | <b>Signaled Target Abort Status (STAS):</b> Hardwired to 0. The IGD does not use target abort semantics.  |
| 10:9 | RO<br>00b        | <b>DEVSEL Timing (DEVT):</b> N/A. These bits are hardwired to "00".   |
| 8    | RO<br>0b         | <b>Master Data Parity Error Detected (DPD):</b> Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.  |
| 7    | RO<br>1b         | <b>Fast Back-to-Back (FB2B):</b> Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.   |
| 6    | RO<br>0b         | <b>User Defined Format (UDF):</b> Hardwired to 0.   |
| 5    | RO<br>0b         | <b>66 MHz PCI Capable (66C):</b> Hardwired to 0.  |
| 4    | RO<br>1b         | <b>Capability List (CLIST):</b> This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.                      |
| 3    | RO<br>0b         | <b>Interrupt Status (INTSTS):</b> This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted. |
| 2:0  | RO<br>000b       | Reserved  |



### 8.1.5 RID2—Revision Identification

B/D/F/Type: 0/2/0/PCI  
Address Offset: 08h  
Default Value: See register table below  
Access: RO  
Size: 8 bits

This register contains the revision number for Device #2 Functions 0 and 1.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>00h        | <b>Revision Identification Number (RID):</b> This is an 8-bit value that indicates the revision identification number for the GMCH Device 2. Refer to the <i>Intel® G31/P31 Express Chipset Family Specification Update</i> for the value of the Revision ID register. |

### 8.1.6 CC—Class Code

B/D/F/Type: 0/2/0/PCI  
Address Offset: 09–0Bh  
Default Value: 030000h  
Access: RO  
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 23:16 | RO<br>03h        | <b>Base Class Code (BCC):</b> This is an 8-bit value that indicates the base class code for the GMCH. This code has the value 03h, indicating a Display Controller.                  |
| 15:8  | RO<br>00h        | <b>Sub-Class Code (SUBCC):</b> Value will be determined based on Device 0 GGC register, GMS and IVD fields.<br><br>00h = VGA compatible<br>80h = Non VGA (GMS = "0000" or IVD = "1") |
| 7:0   | RO<br>00h        | <b>Programming Interface (PI):</b><br>00h = Hardwired as a Display controller.   |



### 8.1.7 CLS—Cache Line Size

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 0Ch  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

The IGD does not support this register as a PCI slave.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>00h        | <b>Cache Line Size (CLS):</b> This field is hardwired to 0s. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size. |

### 8.1.8 MLT2—Master Latency Timer

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 0Dh  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RO<br>00h        | <b>Master Latency Timer Count Value (MLTCV):</b> Hardwired to 0s. |



### 8.1.9 HDR2—Header Type

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 0Eh  
 Default Value: 80h  
 Access: RO  
 Size: 8 bits

This register contains the Header Type of the IGD.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7   | RO<br>1b         | <b>Multi Function Status (MFUNC)</b> : Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device #0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the MFUNC bit is also set. |
| 6:0 | RO<br>00h        | <b>Header Code (H)</b> : This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.   |

### 8.1.10 GMADR—Graphics Memory Range Address

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 18–1Bh  
 Default Value: 00000008h  
 Access: RW, RO, RW/L  
 Size: 32 bits

IGD graphics memory base address is specified in this register.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:29 | RW<br>000b       | <b>Memory Base Address (MBA)</b> : Set by the OS, these bits correspond to address signals 31:29.   |
| 28    | RW/L<br>0b       | <b>512MB Address Mask (512ADMSK)</b> : This Bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (D2:F0, offset 62h) for details.  |
| 27    | RW/L<br>0b       | <b>256 MB Address Mask (256ADMSK)</b> : This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (D2:F0, offset 62h) for details. |
| 26:4  | RO<br>000000h    | <b>Address Mask (ADM)</b> : Hardwired to 0s to indicate at least 128 MB address range.  |
| 3     | RO<br>1b         | <b>Prefetchable Memory (PREFMEM)</b> : Hardwired to 1 to enable prefetching.  |
| 2:1   | RO<br>00b        | <b>Memory Type (MEMTYP)</b> : Hardwired to 0 to indicate 32-bit address.  |
| 0     | RO<br>0b         | <b>Memory/IO Space (MIOS)</b> : Hardwired to 0 to indicate memory space.  |



### 8.1.11 IOBAR—I/O Base Address

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 14–17h  
 Default Value: 0000001h  
 Access: RO, RW  
 Size: 32 bits

This register provides the Base offset of the I/O registers within Device 2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16 bit I/O Address Space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of I/O space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1–D3 or if I/O Enable is clear or if Device 2 is turned off or if Internal graphics is disabled thru the fuse or fuse override mechanisms.

Note that access to this IO BAR is independent of VGA functionality within Device 2. Also note that this mechanism is available only through function 0 of Device 2 and is not duplicated in function 1.

If accesses to this IO bar is allowed then the GMCH claims all 8, 16 or 32 bit I/O cycles from the processor that falls within the 8B claimed.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:16 | RO<br>0000h      | Reserved   |
| 15:3  | RW<br>0000h      | <b>IO Base Address (IOBASE):</b> Set by the OS, these bits correspond to address signals 15:3. |
| 2:1   | RO<br>00b        | <b>Memory Type (MEMTYPE):</b> Hardwired to 0s to indicate 32-bit address.                      |
| 0     | RO<br>1b         | <b>Memory/I/O Space (MIOS):</b> Hardwired to 1 to indicate I/O space.                          |

### 8.1.12 SVID2—Subsystem Vendor Identification

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 2C–2Dh  
 Default Value: 0000h  
 Access: RWO  
 Size: 16 bits

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:0 | RWO<br>0000h     | <b>Subsystem Vendor ID (SUBVID):</b> This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset. |



### 8.1.13 SID2—Subsystem Identification

B/D/F/Type: 0/2/0/PCI  
Address Offset: 2E–2Fh  
Default Value: 0000h  
Access: RWO  
Size: 16 bits

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:0 | RWO<br>0000h     | <b>Subsystem Identification (SUBID):</b> This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset. |

### 8.1.14 ROMADR—Video BIOS ROM Base Address

B/D/F/Type: 0/2/0/PCI  
Address Offset: 30–33h  
Default Value: 00000000h  
Access: RO  
Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:18 | RO<br>0000h      | <b>ROM Base Address (RBA):</b> Hardwired to 0s.                                |
| 17:11 | RO<br>00h        | <b>Address Mask (ADMSK):</b> Hardwired to 0s to indicate 256 KB address range. |
| 10:1  | RO<br>000h       | Reserved. Hardwired to 0s.   |
| 0     | RO<br>0b         | <b>ROM BIOS Enable (RBE):</b><br>0 = ROM not accessible.                       |



### 8.1.15 CAPPOINT—Capabilities Pointer

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 34h  
 Default Value: 90h  
 Access: RO  
 Size: 8 bits

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RO<br>90h        | <b>Capabilities Pointer Value (CPV):</b> This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the MSI Capabilities ID registers at address 90h or the Power Management capability at D0h.<br><br>This value is determined by the configuration in CAPL[0]. |

### 8.1.16 INTRLIN—Interrupt Line

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 3Ch  
 Default Value: 00h  
 Access: RW  
 Size: 8 bits

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RW<br>00h        | <b>Interrupt Connection (INTCON):</b> This field is used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected. |

### 8.1.17 INTRPIN—Interrupt Pin

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 3Dh  
 Default Value: 01h  
 Access: RO  
 Size: 8 bits

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>01h        | <b>Interrupt Pin (INTRPIN):</b> As a single function device, the IGD specifies INTA# as its interrupt pin.<br><br>01h = INTA#. |



### 8.1.18 MINGNT—Minimum Grant

B/D/F/Type: 0/2/0/PCI  
Address Offset: 3Eh  
Default Value: 00h  
Access: RO  
Size: 8 bits

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RO<br>00h        | <b>Minimum Grant Value (MGV):</b> The IGD does not burst as a PCI compliant master. |

### 8.1.19 MAXLAT—Maximum Latency

B/D/F/Type: 0/2/0/PCI  
Address Offset: 3Fh  
Default Value: 00h  
Access: RO  
Size: 8 bits

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>00h        | <b>Maximum Latency Value (MLV):</b> The IGD has no specific requirements for how often it needs to access the PCI bus. |



### 8.1.20 CAPID0—Capability Identifier

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 40–50h  
 Default Value: 0000000000000000010000000010B0009h  
 Access: RO  
 Size: 136 bits  
 BIOS Optimal Default 000000000000h

This register control of bits in this register are only required for customer visible SKU differentiation.

| Bit    | Access & Default | Description  |
|--------|------------------|--|
| 135:28 | RO<br>0s         | Reserved   |
| 27:24  | RO<br>1h         | <b>CAPID Version (CAPIDV):</b> This field has the value 0001b to identify the first revision of the CAPID register definition.                                 |
| 23:16  | RO<br>0Bh        | <b>CAPID Length (CAPIDL):</b> This field has the value 0bh to indicate the structure length (11 bytes).  |
| 15:8   | RO<br>00h        | <b>Next Capability Pointer (NCP):</b> This field is hardwired to 00h indicating the end of the capabilities linked list.                                       |
| 7:0    | RO<br>09h        | <b>Capability Identifier (CAP_ID):</b> This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers. |



### 8.1.21 MGGC—GMCH Graphics Control Register

B/D/F/Type: 0/2/0/PCI  
Address Offset: 52–53h  
Default Value: 0030h  
Access: RO  
Size: 16 bits

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15:10 | RO<br>00h        | Reserved   |
| 9:8   | RO<br>0h         | <p><b>GTT Graphics Memory Size (GGMS):</b> This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>00 = No memory pre-allocated. GTT cycles (Memory and I/O) are not claimed.</p> <p>01 = No VT mode, 1 MB of memory pre-allocated for GTT.</p> <p>10 = VT mode, 2 MB of memory pre-allocated for GTT.</p> <p>11 = Reserved</p> <p><b>Note:</b> This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.</p> |



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:4 | RO<br>0011b      | <p><b>Graphics Mode Select (GMS):</b> This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>0000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80.</p> <p>0001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer.</p> <p>0010 = DVMT (UMA) mode, 4 MB of memory pre-allocated for frame buffer.</p> <p>0011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer.</p> <p>0100 = DVMT (UMA) mode, 16 MB of memory pre-allocated for frame buffer.</p> <p>0101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer.</p> <p>0110 = DVMT (UMA) mode, 48 MB of memory pre-allocated for frame buffer.</p> <p>0111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer.</p> <p>1000 = DVMT (UMA) mode, 128 MB of memory pre-allocated for frame buffer.</p> <p>1001 = DVMT (UMA) mode, 256 MB of memory pre-allocated for frame buffer.</p> <p><b>Note:</b> This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.</p> <p><b>BIOS Requirement:</b> BIOS must not set this field to 000 if IVD (bit 1 of this register) is 0.</p> |
| 3:0 | RO<br>0000b      | Reserved  |



### 8.1.22 DEVEN—Device Enable

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 54–57h  
 Default Value: 000003DBh  
 Access: RO  
 Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the GMCH. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:10 | RO<br>0s         | Reserved   |
| 9:6   | RO<br>1111b      | Reserved   |
| 5     | RO<br>0b         | Reserved   |
| 4     | RO<br>1b         | <p><b>Internal Graphics Engine Function 1 (D2F1EN):</b><br/>           0 = Bus 0, Device 2, Function 1 is disabled and hidden<br/>           1 = Bus 0, Device 2, Function 1 is enabled and visible<br/>           If Device 2, Function 0 is disabled and hidden, then Device 2, Function 1 is also disabled and hidden independent of the state of this bit.<br/>           If this component is not capable of Dual Independent Display (CAPID0[78] = 1), then this bit is hardwired to 0b to hide Device 2, Function 1.</p>                            |
| 3     | RO<br>1b         | <p><b>Internal Graphics Engine Function 0 (D2FOEN):</b><br/>           0 = Bus 0, Device 2, Function 0 is disabled and hidden<br/>           1 = Bus 0, Device 2, Function 0 is enabled and visible<br/>           If this GMCH does not have internal graphics capability (CAPID0[46] = 1), then Device 2, Function 0 is disabled and hidden independent of the state of this bit.</p>  |
| 2     | RO<br>0b         | Reserved   |
| 1     | RO<br>1b         | <p><b>PCI Express Port (D1EN):</b><br/>           0 = Bus 0, Device 1, Function 0 is disabled and hidden.<br/>           1 = Bus 0, Device 1, Function 0 is enabled and visible.<br/>           Default value is determined by the device capabilities (see CAPID0 [44]), SDVO Presence hardware strap and the SDVO/PCIe Concurrent hardware strap. Device 1 is Disabled on Reset if the SDVO Presence strap was sampled high, and the SDVO/PCIe Concurrent strap was sampled low at the last assertion of PWROK, and is enabled by default otherwise.</p> |
| 0     | RO<br>1b         | <p><b>Host Bridge (DOEN):</b> Bus 0, Device 0, Function 0 may not be disabled and is therefore hardwired to 1.</p>   |



### 8.1.23 SSRW—Software Scratch Read Write

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 58–5Bh  
 Default Value: 00000000h  
 Access: RW  
 Size: 32 bits

| Bit  | Access & Default | Description |
|------|------------------|-------------|
| 31:0 | RW<br>00000000h  | Reserved    |

### 8.1.24 BSM—Base of Stolen Memory

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 5C–5Fh  
 Default Value: 07800000h  
 Access: RO  
 Size: 32 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, GMCH claims 1 to 64 MBs of DRAM for internal graphics if enabled.

The base of stolen memory will always be below 4 GB. This is required to prevent aliasing between stolen range and the reclaim region.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:20 | RO<br>078h       | <b>Base of Stolen Memory (BSM):</b> This field contains bits 31:20 of the base address of stolen DRAM memory. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation. |
| 19:0  | RO<br>00000h     | Reserved   |

### 8.1.25 HSRW—Hardware Scratch Read Write

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 60–61h  
 Default Value: 0000h  
 Access: RW  
 Size: 16 bits

| Bit  | Access & Default | Description |
|------|------------------|-------------|
| 15:0 | RW<br>0000h      | Reserved    |



### 8.1.26 MC—Message Control

B/D/F/Type: 0/2/0/PCI  
Address Offset: 92–93h  
Default Value: 0000h  
Access: RO, RW  
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is ensured to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:8 | RO<br>00h        | Reserved   |
| 7    | RO<br>0b         | <b>64 Bit Capable (64BCAP):</b> Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32b / 4 GB limit. |
| 6:4  | RW<br>000b       | <b>Multiple Message Enable (MME):</b> System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field (Bits 3:1).   |
| 3:1  | RO<br>000b       | <b>Multiple Message Capable (MMC):</b> System Software reads this field to determine the number of messages being requested by this device.<br>000 = 1<br>All of the following are reserved in this implementation<br>001 = 2<br>010 = 4<br>011 = 8<br>100 = 16<br>101 = 32<br>110 = Reserved<br>111 = Reserved          |
| 0    | RW<br>0b         | <b>MSI Enable (MSIEN):</b> This bit controls the ability of this device to generate MSIs.  |



### 8.1.27 MA—Message Address

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 94–97h  
 Default Value: 00000000h  
 Access: RW, RO  
 Size: 32 bits

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 31:2 | RW<br>00000000h  | <b>Message Address (MESSADD):</b> Used by system software to assign an MSI address to the device.<br><br>The device handles an MSI by writing the padded contents of the MD register to this address. |
| 1:0  | RO<br>00b        | <b>Force DWord Align (FDWORD):</b> Hardwired to 0 so that addresses assigned by system software are always aligned on a DWord address boundary.   |

### 8.1.28 MD—Message Data

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 98–99h  
 Default Value: 0000h  
 Access: RW  
 Size: 16 bits

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:0 | RW<br>0000h      | <b>Message Data (MESSDATA):</b> Base message data pattern assigned by system software and used to handle an MSI from the device.<br><br>When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register. |



### 8.1.29 GDRST—Graphics Debug Reset

B/D/F/Type: 0/2/0/PCI  
 Address Offset: C0h  
 Default Value: 00h  
 Access: RO, RW  
 Size: 8 bits

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:4 | RO<br>0h         | Reserved  |
| 3:2 | RW<br>00b        | <p><b>Graphics Reset Domain (GRDOM):</b></p> <p>00 = Full Graphics Reset will be performed (both render and display clock domain resets asserted)</p> <p>01 = Reserved (Invalid Programming)</p> <p>10 = Reserved (Invalid Programming)</p> <p>11 = Reserved (Invalid Programming)</p>  |
| 1   | RO<br>0b         | Reserved  |
| 0   | RW<br>0b         | <p><b>Graphics Reset Enable (GR):</b> Setting this bit asserts graphics-only reset. The clock domains to be reset are determined by GRDOM. Hardware resets this bit when the reset is complete. Setting this bit without waiting for it to clear, is undefined behavior. Once this bit is set to a 1, all graphics core MMIO registers are returned to power on default state. All Ring buffer pointers are reset, command stream fetches are dropped and ongoing render pipeline processing is halted, state machines and State Variables returned to power on default state. If the Display is reset, all display engines are halted (garbage on screen). VGA memory is not available, Store DWords and interrupts are not assured to be completed. Device 2 I/O registers are not available.</p> <p>When issuing the graphics reset, disable the cursor, display, and overlay engines using the MMIO registers. Wait 1 us. Issue the graphics reset by setting this bit to 1.</p> <p>Device 2 Configuration registers continue to be available while graphics reset is asserted.</p> <p>This bit is hardware auto-clear.</p> |



### 8.1.30 PMCAPID—Power Management Capabilities ID

B/D/F/Type: 0/2/0/PCI  
 Address Offset: D0–D1h  
 Default Value: 0001h  
 Access: RWO, RO  
 Size: 16 bits

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:8 | RWO<br>00h       | <b>Next Capability Pointer (NEXT_PTR):</b> This field contains a pointer to the next item in the capabilities list. BIOS is responsible for writing this to the FLR Capability when applicable. |
| 7:0  | RO<br>01h        | <b>Capability Identifier (CAP_ID):</b> SIG defines this ID is 01h for power management.   |

### 8.1.31 PMCAP—Power Management Capabilities

B/D/F/Type: 0/2/0/PCI  
 Address Offset: D2–D3h  
 Default Value: 0022h  
 Access: RO  
 Size: 16 bits

This register is a Mirror of Function 0 with the same read/write attributes. The hardware implements a single physical register common to both functions 0 and 1.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:11 | RO<br>00h        | <b>PME Support (PMES):</b> This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.   |
| 10    | RO<br>0b         | <b>D2 Support (D2):</b> The D2 power management state is not supported. This bit is hardwired to 0.   |
| 9     | RO<br>0b         | <b>D1 Support (D1):</b> Hardwired to 0 to indicate that the D1 power management state is not supported.   |
| 8:6   | RO<br>000b       | Reserved  |
| 5     | RO<br>1b         | <b>Device Specific Initialization (DSI):</b> Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.   |
| 4     | RO<br>0b         | Reserved  |
| 3     | RO<br>0b         | <b>PME Clock (PMECLK):</b> Hardwired to 0 to indicate IGD does not support PME# generation.   |
| 2:0   | RO<br>010b       | <b>Version (VER):</b> Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification. |



### 8.1.32 PMCS—Power Management Control/Status

B/D/F/Type: 0/2/0/PCI  
Address Offset: D4–D5h  
Default Value: 0000h  
Access: RO, RW  
Size: 16 bits

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15    | RO<br>0b         | <b>PME Status (PMESTS):</b> This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).  |
| 14:13 | RO<br>00b        | <b>Data Scale (DSCALE):</b> The IGD does not support data register. This bit always returns 00 when read, write operations have no effect.   |
| 12:9  | RO<br>0h         | <b>Data Select (DSEL):</b> The IGD does not support data register. This bit always returns 0h when read, write operations have no effect.  |
| 8     | RO<br>0b         | <b>PME Enable (PME_EN):</b> This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.  |
| 7:2   | RO<br>00h        | Reserved   |
| 1:0   | RW<br>00b        | <b>Power State (PWRSTAT):</b> This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values.<br><br>00 = D0 (Default)<br>01 = D1 (Not Supported)<br>10 = D2 (Not Supported)<br>11 = D3 |



### 8.1.33 SWSMI—Software SMI

B/D/F/Type: 0/2/0/PCI  
 Address Offset: E0–E1h  
 Default Value: 0000h  
 Access: RW  
 Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, D2, F0 address E0h–E1h must be reserved for this register.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:8 | RW<br>00h        | <b>Software Scratch Bits (SWSB):</b>  |
| 7:1  | RW<br>00h        | <b>Software Flag (SWF):</b> This field is used to indicate caller and SMI function desired, as well as return result.         |
| 0    | RW<br>0b         | <b>GMCH Software SMI Event (GSSMIE):</b> When Set, this bit will trigger an SMI. Software must write a "0" to clear this bit. |



## 8.2 IGD Configuration Register Details (D2:F1)

The Integrated Graphics Device registers are located in Device 2 (D2), Function 0 (F0) and Function 1 (F1). This section provides the descriptions for the D2:F1 registers. Table 8-2 provides an address map of the D2:F1 registers listed in ascending order by address offset. Detailed bit descriptions follow the table.

**Table 8-2. Integrated Graphics Device Register Address Map (D2:F1)**

| Address Offset | Register Symbol | Register Name                                    | Default Value                                   | Access |
|----------------|-----------------|--|---|--------|
| 00–01h         | VID2            | Vendor Identification                            | 8086h   | RO     |
| 02–03h         | DID2            | Device Identification                            | 29C3h   | RO     |
| 04–05h         | PCICMD2         | PCI Command                                      | 0000h   | RO, RW |
| 06–07h         | PCISTS2         | PCI Status                                       | 0090h   | RO     |
| 08h            | RID2            | Revision Identification                          | See register description                        | RO     |
| 09–0Bh         | CC              | Class Code Register                              | 038000h   | RO     |
| 0Ch            | CLS             | Cache Line Size                                  | 00h   | RO     |
| 0Dh            | MLT2            | Master Latency Timer                             | 00h   | RO     |
| 0Eh            | HDR2            | Header Type                                      | 80h   | RO     |
| 10–13h         | MMADR           | Memory Mapped Range Address                      | 00000000h                                       | RW, RO |
| 2C–2Dh         | SVID2           | Subsystem Vendor Identification                  | 0000h   | RO     |
| 2E–2Fh         | SID2            | Subsystem Identification                         | 0000h   | RO     |
| 30–33h         | ROMADR          | Video BIOS ROM Base Address                      | 00000000h                                       | RO     |
| 34h            | CAPPOINT        | Capabilities Pointer                             | D0h   | RO     |
| 3Eh            | MINGNT          | Minimum Grant                                    | 00h   | RO     |
| 3Fh            | MAXLAT          | Maximum Latency                                  | 00h   | RO     |
| 40–50h         | CAPID0          | Mirror of Dev0 Capability Identifier             | 0000000000<br>0000000100<br>000000010<br>B0009h | RO     |
| 52–53h         | MGGC            | Mirror of Dev 0 GMCH Graphics Control Register   | 0030h   | RO     |
| 54–57h         | DEVEN           | Device Enable                                    | 000003DBh                                       | RO     |
| 58–5Bh         | SSRW            | Mirror of Fun 0 Software Scratch Read Write      | 00000000h                                       | RO     |
| 5C–5Fh         | BSM             | Mirror of Func0 Base of Stolen Memory            | 07800000h                                       | RO     |
| 60–61h         | HSRW            | Mirror of Dev2 Func0 Hardware Scratch Read Write | 0000h   | RO     |



| Address Offset | Register Symbol | Register Name   | Default Value | Access   |
|----------------|-----------------|---|---------------|----------|
| 62h            | MSAC            | Mirror of Dev2 Func0 Multi Size Aperture Control                      | 02h           | RO       |
| C0h            | GDRST           | Mirror of Dev2 Func0 Graphics Reset                                   | 00h           | RO       |
| C1–C3h         | MI_GFX_CG_DIS   | Mirror of Fun 0 MI Graphics Unit Level Clock Ungating                 | 000000h       | RO       |
| C4–C7h         | RSVD            | Reserved  | 00000000h     | RO       |
| C8h            | RSVD            | Reserved  | 00h           | RO       |
| CA–CBh         | RSVD            | Reserved  | 0000h         | RO       |
| CC–CDh         | GCDGMBUS        | Mirror of Dev2 Func0 Graphics Clock Frequency Register for GMBUS unit | 0000h         | RO       |
| D0–D1h         | PMCAPID         | Mirror of Fun 0 Power Management Capabilities ID                      | 0001h         | RO       |
| D2–D3h         | PMCAP           | Mirror of Fun 0 Power Management Capabilities                         | 0022h         | RO       |
| D4–D5h         | PMCS            | Power Management Control/Status                                       | 0000h         | RO, RW   |
| D8–DBh         | RSVD            | Reserved  | 00000000h     | RO       |
| E0–E1h         | SWSMI           | Mirror of Func0 Software SMI  | 0000h         | RO       |
| E4–E7h         | ASLE            | Mirror of Dev2 Func0 System Display Event Register                    | 00000000h     | RO       |
| F0–F3h         | GCFG            | Mirror of Dev2 Func0 Graphics Clock Frequency and Gating Control      | 00000000h     | RO/P, RO |
| F4–F7h         | RSVD            | Mirror of Fun 0 Reserved for LBB-Legacy Backlight Brightness          | 00000000h     | RO       |
| FC–FFh         | ASLS            | ASL Storage   | 00000000h     | RW       |



### 8.2.1 VID2—Vendor Identification

B/D/F/Type: 0/2/1/PCI  
Address Offset: 00–01h  
Default Value: 8086h  
Access: RO  
Size: 16 bits

This register, combined with the Device Identification register, uniquely identifies any PCI device.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:0 | RO<br>8086h      | <b>Vendor Identification Number (VID):</b> PCI standard identification for Intel. |

### 8.2.2 DID2—Device Identification

B/D/F/Type: 0/2/1/PCI  
Address Offset: 02–03h  
Default Value: 29C3h  
Access: RO  
Size: 16 bits

This register is unique in Function 1 (the Function 0 DID is separate). This difference in Device ID is necessary for allowing distinct Plug and Play enumeration of function 1 when both function 0 and function 1 have the same class code.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:0 | RO<br>29C3h      | <b>Device Identification Number (DID):</b> This is a 16 bit value assigned to the GMCH Graphic device Function 1 |



### 8.2.3 PCICMD2—PCI Command

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 04–05h  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15:10 | RO<br>0s         | Reserved   |
| 9     | RO<br>0b         | <b>Fast Back-to-Back (FB2B)</b> : Not Implemented. Hardwired to 0.   |
| 8     | RO<br>0b         | <b>SERR Enable (SERRE)</b> : Not Implemented. Hardwired to 0.  |
| 7     | RO<br>0b         | <b>Address/Data Stepping Enable (ADSTEP)</b> : Not Implemented. Hardwired to 0.  |
| 6     | RO<br>0b         | <b>Parity Error Enable (PERRE)</b> : Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation. |
| 5     | RO<br>0b         | <b>VGA Palette Snoop Enable (VGASNOOP)</b> : This bit is hardwired to 0 to disable snooping.   |
| 4     | RO<br>0b         | <b>Memory Write and Invalidate Enable (MWIE)</b> : Hardwired to 0. The IGD does not support memory write and invalidate commands.  |
| 3     | RO<br>0b         | <b>Special Cycle Enable (SCE)</b> : This bit is hardwired to 0. The IGD ignores Special cycles.  |
| 2     | RW<br>0b         | <b>Bus Master Enable (BME)</b> :<br>0 = Disable IGD bus mastering.<br>1 = Enable the IGD to function as a PCI compliant master.  |
| 1     | RW<br>0b         | <b>Memory Access Enable (MAE)</b> : This bit controls the IGD's response to memory space accesses.<br>0 = Disable.<br>1 = Enable.  |
| 0     | RW<br>0b         | <b>I/O Access Enable (IOAE)</b> : This bit controls the IGD's response to I/O space accesses.<br>0 = Disable.<br>1 = Enable.   |



### 8.2.4 PCISTS2—PCI Status

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 06–07h  
 Default Value: 0090h  
 Access: RO  
 Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15   | RO<br>0b         | <b>Detected Parity Error (DPE):</b> Since the IGD does not detect parity, this bit is always hardwired to 0.   |
| 14   | RO<br>0b         | <b>Signaled System Error (SSE):</b> The IGD never asserts SERR#, therefore this bit is hardwired to 0.   |
| 13   | RO<br>0b         | <b>Received Master Abort Status (RMAS):</b> The IGD never gets a Master Abort, therefore this bit is hardwired to 0.   |
| 12   | RO<br>0b         | <b>Received Target Abort Status (RTAS):</b> The IGD never gets a Target Abort, therefore this bit is hardwired to 0.   |
| 11   | RO<br>0b         | <b>Signaled Target Abort Status (STAS):</b> Hardwired to 0. The IGD does not use target abort semantics.   |
| 10:9 | RO<br>00b        | <b>DEVSEL Timing (DEVT):</b> N/A. These bits are hardwired to "00".  |
| 8    | RO<br>0b         | <b>Master Data Parity Error Detected (DPD):</b> Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.   |
| 7    | RO<br>1b         | <b>Fast Back-to-Back (FB2B):</b> Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.  |
| 6    | RO<br>0b         | <b>User Defined Format (UDF):</b> Hardwired to 0.  |
| 5    | RO<br>0b         | <b>66 MHz PCI Capable (66C):</b> N/A - Hardwired to 0.   |
| 4    | RO<br>1b         | <b>Capability List (CLIST):</b> This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list. |
| 3    | RO<br>0b         | <b>Interrupt Status (INTSTS):</b> Hardwired to 0.  |
| 2:0  | RO<br>000b       | Reserved   |



### 8.2.5 RID2—Revision Identification

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 08h  
 Default Value: See register table below  
 Access: RO  
 Size: 8 bits

This register contains the revision number for Device 2 Functions 0 and 1.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>00h        | <b>Revision Identification Number (RID):</b> This is an 8-bit value that indicates the revision identification number for the GMCH Device 2. Refer to the <i>Intel® G31/P31 Express Chipset Family Specification Update</i> for the value of the Revision ID register. |

### 8.2.6 CC—Class Code Register

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 09–0Bh  
 Default Value: 038000h  
 Access: RO  
 Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 23:16 | RO<br>03h        | <b>Base Class Code (BCC):</b> This is an 8-bit value that indicates the base class code for the GMCH. This code has the value 03h, indicating a Display Controller. |
| 15:8  | RO<br>80h        | <b>Sub-Class Code (SUBCC):</b><br>80h = Non VGA   |
| 7:0   | RO<br>00h        | <b>Programming Interface (PI):</b><br>00h = Hardwired as a Display controller.  |



### 8.2.7 CLS—Cache Line Size

B/D/F/Type: 0/2/1/PCI  
Address Offset: 0Ch  
Default Value: 00h  
Access: RO  
Size: 8 bits

The IGD does not support this register as a PCI slave.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>00h        | <b>Cache Line Size (CLS):</b> This field is hardwired to 0s. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size. |

### 8.2.8 MLT2—Master Latency Timer

B/D/F/Type: 0/2/1/PCI  
Address Offset: Dh  
Default Value: 00h  
Access: RO  
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RO<br>00h        | <b>Master Latency Timer Count Value (MLTCV):</b> Hardwired to 0s. |



### 8.2.9 HDR2—Header Type

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 0Eh  
 Default Value: 80h  
 Access: RO  
 Size: 8 bits

This register contains the Header Type of the IGD.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7   | RO<br>1b         | <b>Multi Function Status (MFUNC):</b> Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the MFUNC bit is also set. |
| 6:0 | RO<br>00h        | <b>Header Code (H):</b> This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.  |

### 8.2.10 MMADR—Memory Mapped Range Address

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 10–13h  
 Default Value: 00000000h  
 Access: RW, RO  
 Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits 31:19.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:19 | RW<br>0000h      | <b>Memory Base Address (MBA):</b> Set by the OS, these bits correspond to address signals 31:19. |
| 18:4  | RO<br>0000h      | <b>Address Mask (ADMSK):</b> Hardwired to 0s to indicate 512 KB address range.                   |
| 3     | RO<br>0b         | <b>Prefetchable Memory (PREFMEM):</b> Hardwired to 0 to prevent prefetching.                     |
| 2:1   | RO<br>00b        | <b>Memory Type (MEMTYP):</b> Hardwired to 0s to indicate 32-bit address.                         |
| 0     | RO<br>0b         | <b>Memory / IO Space (MIOS):</b> Hardwired to 0 to indicate memory space.                        |



### 8.2.11 SVID2—Subsystem Vendor Identification

B/D/F/Type: 0/2/1/PCI  
Address Offset: 2C–2Dh  
Default Value: 0000h  
Access: RO  
Size: 16 bits

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:0 | RO<br>0000h      | <b>Subsystem Vendor ID (SUBVID):</b> This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset. |

### 8.2.12 SID2—Subsystem Identification

B/D/F/Type: 0/2/1/PCI  
Address Offset: 2E–2Fh  
Default Value: 0000h  
Access: RO  
Size: 16 bits

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:0 | RO<br>0000h      | <b>Subsystem Identification (SUBID):</b> This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset. |



### 8.2.13 ROMADR—Video BIOS ROM Base Address

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 30–33h  
 Default Value: 00000000h  
 Access: RO  
 Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 31:18 | RO<br>0000h      | <b>ROM Base Address (RBA):</b> Hardwired to 0s.                                |
| 17:11 | RO<br>00h        | <b>Address Mask (ADMSK):</b> Hardwired to 0s to indicate 256 KB address range. |
| 10:1  | RO<br>000h       | Reserved. Hardwired to 0s.   |
| 0     | RO<br>0b         | <b>ROM BIOS Enable (RBE):</b><br>0 = ROM not accessible.                       |

### 8.2.14 CAPPOINT—Capabilities Pointer

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 34h  
 Default Value: D0h  
 Access: RO  
 Size: 8 bits

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RO<br>D0h        | <b>Capabilities Pointer Value (CPV):</b> This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the MSI Capabilities ID registers at the Power Management capability at D0h. |



### 8.2.15 MINGNT—Minimum Grant

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 3Eh  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:0 | RO<br>00h        | <b>Minimum Grant Value (MGV):</b> The IGD does not burst as a PCI compliant master. |

### 8.2.16 MAXLAT—Maximum Latency

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 3Fh  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>00h        | <b>Maximum Latency Value (MLV):</b> The IGD has no specific requirements for how often it needs to access the PCI bus. |

### 8.2.17 CAPID0—Mirror of Dev0 Capability Identifier

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 40–50h  
 Default Value: 0000000000000000100000000010B0009h  
 Access: RO  
 Size: 136 bits  
 BIOS Optimal Default: 000000000000h

Control of bits in this register are only required for customer visible component differentiation.

| Bit | Access & Default | Description  |
|-----|------------------|--|
| 7:0 | RO<br>09h        | <b>Capability Identifier (CAP_ID):</b> This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers. |



### 8.2.18 MGGC—Mirror of Dev 0 GMCH Graphics Control Register

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 52–53h  
 Default Value: 0030h  
 Access: RO  
 Size: 16 bits

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15:10 | RO<br>00h        | Reserved   |
| 9:8   | RO<br>0h         | <p><b>GTT Graphics Memory Size (GGMS):</b> This field is used to select the amount of main memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>00 = No memory pre-allocated. GTT cycles (Memory and I/O) are not claimed.</p> <p>01 = No VT mode, 1 MB of memory pre-allocated for GTT.</p> <p>10 = VT mode, 2 MB of memory pre-allocated for GTT.</p> <p>11 = reserved</p> <p><b>Note:</b> This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.</p> |



*Integrated Graphics Registers (D2:F0,F1) (Intel® 82G31 GMCH Only)*

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:4 | RO<br>0011b      | <p><b>Graphics Mode Select (GMS)</b> This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>0000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80h.</p> <p>0001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer.</p> <p>0010 = DVMT (UMA) mode, 4 MB of memory pre-allocated for frame buffer.</p> <p>0011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer.</p> <p>0100 = DVMT (UMA) mode, 16 MB of memory pre-allocated for frame buffer.</p> <p>0101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer.</p> <p>0110 = DVMT (UMA) mode, 48 MB of memory pre-allocated for frame buffer.</p> <p>0111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer.</p> <p>1000 = DVMT (UMA) mode, 128 MB of memory pre-allocated for frame buffer.</p> <p>1001 = DVMT (UMA) mode, 256 MB of memory pre-allocated for frame buffer.</p> <p><b>Note:</b> This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.</p> <p><b>BIOS Requirement:</b> BIOS must not set this field to 000 if IVD (bit 1 of this register) is 0.</p> |
| 3:2 | RO<br>00b        | Reserved  |
| 1   | RO<br>0b         | <p><b>IGD VGA Disable (IVD):</b></p> <p>0 = Enable. Device 2 (IGD) claims VGA memory and I/O cycles, the Sub-Class Code within Device 2 Class Code register is 00.</p> <p>1 = Disable. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub- Class Code field within Device 2, function 0 Class Code register is 80h.</p> <p><b>BIOS Requirement:</b> BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register) pre-allocates no memory.</p> <p>This bit <b>MUST</b> be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPIDO[38] = 1) or via a register (DEVEN[3] = 0).</p>   |
| 0   | RO<br>0b         | Reserved  |



### 8.2.19 DEVEN—Device Enable

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 54–57h  
 Default Value: 000003DBh  
 Access: RO  
 Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the GMCH. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 31:5 | RO<br>0s         | Reserved   |
| 4    | RO<br>1b         | <p><b>Internal Graphics Engine Function 1 (D2F1EN):</b></p> <p>0 = Bus 0:Device2:Function1 is disabled and hidden<br/>                     1 = Bus0:Device2:Function1 is enabled and visible</p> <p>If Device2:Function0 is disabled and hidden, then Device2:Function1 is also disabled and hidden independent of the state of this bit.</p> <p>If this component is not capable of Dual Independent Display (CAPID0[78] = 1), then this bit is hardwired to 0b to hide Device2:Function1.</p>  |
| 3    | RO<br>1b         | <p><b>Internal Graphics Engine Function 0 (D2F0EN):</b></p> <p>0 = Bus0:Device2:Function0 is disabled and hidden<br/>                     1 = Bus0:Device2:Function0 is enabled and visible</p> <p>If this GMCH does not have internal graphics capability (CAPID0[46] = 1), then Device2:Function0 is disabled and hidden independent of the state of this bit.</p>   |
| 2    | RO<br>0b         | Reserved   |
| 1    | RO<br>1b         | <p><b>PCI Express Port (D1EN):</b></p> <p>0 = Bus0:Device1:Function0 is disabled and hidden.<br/>                     1 = Bus0:Device1:Function0 is enabled and visible.</p> <p>Default value is determined by the device capabilities (see CAPID0 [44]), SDVO Presence hardware strap and the SDVO/PCIe Concurrent hardware strap. Device 1 is Disabled on Reset if the SDVO Presence strap was sampled high, and the SDVO/PCIe Concurrent strap was sampled low at the last assertion of PWROK, and is enabled by default otherwise.</p> |
| 0    | RO<br>1b         | <p><b>Host Bridge (D0EN):</b> Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.</p>   |



### 8.2.20 SSRW—Mirror of Fun 0 Software Scratch Read Write

B/D/F/Type: 0/2/1/PCI  
Address Offset: 58–5Bh  
Default Value: 00000000h  
Access: RO  
Size: 32 bits

| Bit  | Access & Default | Description |
|------|------------------|-------------|
| 31:0 | RO<br>00000000h  | Reserved    |

### 8.2.21 BSM—Mirror of Func0 Base of Stolen Memory

B/D/F/Type: 0/2/1/PCI  
Address Offset: 5C–5Fh  
Default Value: 07800000h  
Access: RO  
Size: 32 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, GMCH claims 1 to 64 MBs of DRAM for internal graphics if enabled.

The base of stolen memory will always be below 4 GB. This is required to prevent aliasing between stolen range and the reclaim region.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 31:20 | RO<br>078h       | <b>Base of Stolen Memory (BSM):</b> This register contains bits 31:20 of the base address of stolen DRAM memory. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation. |
| 19:0  | RO<br>00000h     | Reserved  |



### 8.2.22 HSRW—Mirror of Dev2 Func0 Hardware Scratch Read Write

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 60–61h  
 Default Value: 0000h  
 Access: RO  
 Size: 16 bits

| Bit  | Access & Default | Description |
|------|------------------|-------------|
| 15:0 | RO<br>0000h      | Reserved    |

### 8.2.23 GDRST—Mirror of Dev2 Func0 Graphics Reset

B/D/F/Type: 0/2/1/PCI  
 Address Offset: C0h  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

This register is a mirror of the Graphics Reset Register in Device 2.

| Bit | Access & Default | Description   |
|-----|------------------|---|
| 7:4 | RO<br>0h         | Reserved  |
| 3:2 | RO<br>00b        | <b>Graphics Reset Domain (GRDOM):</b><br>00 = Full Graphics Reset will be performed (both render and display clock domain resets asserted)<br>01 = Reserved (Invalid Programming)<br>10 = Reserved (Invalid Programming)<br>11 = Reserved (Invalid Programming) |
| 1   | RO<br>0b         | Reserved  |



| Bit | Access & Default | Description   |
|-----|------------------|---|
| 0   | RO<br>0b         | <p><b>Graphics Reset (GDR):</b> Setting this bit asserts graphics-only reset. The clock domains to be reset are determined by GRDOM. Hardware resets this bit when the reset is complete. Setting this bit without waiting for it to clear, is undefined behavior.</p> <p>Once this bit is set to a 1, all graphics core MMIO registers are returned to power on default state. All Ring buffer pointers are reset, command stream fetches are dropped and ongoing render pipeline processing is halted, state machines and State Variables returned to power on default state. If the Display is reset, all display engines are halted (garbage on screen). VGA memory is not available; Store DWords and interrupts are not ensured to be completed. Device 2 I/O registers are not available.</p> <p>Device 2 Configuration registers continue to be available while Graphics reset is asserted.</p> <p>This bit is hardware auto-clear.</p> |

### 8.2.24 PMCAPID—Mirror of Fun 0 Power Management Capabilities ID

B/D/F/Type: 0/2/1/PCI  
 Address Offset: D0–D1h  
 Default Value: 0001h  
 Access: RO  
 Size: 16 bits

This register is a mirror of function 0 with the same R/W attributes. The hardware implements a single physical register common to both functions 0 and 1.

| Bit  | Access & Default | Description  |
|------|------------------|--|
| 15:8 | RO<br>00h        | <b>Next Capability Pointer (NEXT_PTR):</b> This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h. |
| 7:0  | RO<br>01h        | <b>Capability Identifier (CAP_ID):</b> SIG defines this ID is 01h for power management.  |



### 8.2.25 PMCAP—Mirror of Fun 0 Power Management Capabilities

B/D/F/Type: 0/2/1/PCI  
 Address Offset: D2–D3h  
 Default Value: 0022h  
 Access: RO  
 Size: 16 bits

This register is a Mirror of Function 0 with the same read/write attributes. The hardware implements a single physical register common to both functions 0 and 1.

| Bit   | Access & Default | Description   |
|-------|------------------|---|
| 15:11 | RO<br>00h        | <b>PME Support (PMES):</b> This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.   |
| 10    | RO<br>0b         | <b>D2 Support (D2):</b> The D2 power management state is not supported. This bit is hardwired to 0.   |
| 9     | RO<br>0b         | <b>D1 Support (D1):</b> Hardwired to 0 to indicate that the D1 power management state is not supported.   |
| 8:6   | RO<br>000b       | Reserved  |
| 5     | RO<br>1b         | <b>Device Specific Initialization (DSI):</b> Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.   |
| 4     | RO<br>0b         | Reserved  |
| 3     | RO<br>0b         | <b>PME Clock (PMECLK):</b> Hardwired to 0 to indicate IGD does not support PME# generation.   |
| 2:0   | RO<br>010b       | <b>Version (VER):</b> Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification. |



### 8.2.26 PMCS—Power Management Control/Status

B/D/F/Type: 0/2/1/PCI  
 Address Offset: D4–D5h  
 Default Value: 0000h  
 Access: RO, RW  
 Size: 16 bits

| Bit   | Access & Default | Description  |
|-------|------------------|--|
| 15    | RO<br>0b         | <b>PME Status (PMESTS):</b> This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).  |
| 14:13 | RO<br>00b        | <b>Data Scale (DSCALE):</b> The IGD does not support data register. This bit always returns 0 when read, write operations have no effect.  |
| 12:9  | RO<br>0h         | <b>Data Select (DATASEL):</b> The IGD does not support data register. This bit always returns 0 when read, write operations have no effect.  |
| 8     | RO<br>0b         | <b>PME Enable (PME_EN):</b> This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.  |
| 7:2   | RO<br>00h        | Reserved   |
| 1:0   | RW<br>00b        | <b>Power State (PWRSTAT):</b> This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values.<br><br>00 = D0 (Default)<br>01 = D1 (Not Supported)<br>10 = D2 (Not Supported)<br>11 = D3 |



### 8.2.27 SWSMI—Mirror of Func0 Software SMI

B/D/F/Type: 0/2/1/PCI  
 Address Offset: E0–E1h  
 Default Value: 0000h  
 Access: RO  
 Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, D2:F0 address E0h–E1h must be reserved for this register.

| Bit  | Access & Default | Description   |
|------|------------------|---|
| 15:8 | RO<br>00h        | <b>Software Scratch Bits (SWSB):</b>  |
| 7:1  | RO<br>00h        | <b>Software Flag (SWF):</b> This field is used to indicate caller and SMI function desired, as well as return result.       |
| 0    | RO<br>0b         | <b>GMCH Software SMI Event (GSSMIE):</b> When Set, this bit will trigger an SMI. Software must write a 0 to clear this bit. |

§



*Integrated Graphics Registers (D2:F0,F1) (Intel® 82G31 GMCH Only)*



## 9 Functional Description

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### 9.1 Host Interface

The (G)MCH supports the Intel® Core 2 Duo processor. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped and a new address can be generated every other bus clock. At 200/267 MHz bus clock the address signals run at 667 MT/s. The data is quad pumped and an entire 64B cache line can be transferred in two bus clocks. At 200/266 MHz bus clock, the data signals run at 800/1066 MT/s for a maximum bandwidth of 6.4/8.5 GB/s.

#### 9.1.1 FSB IOQ Depth

The Scalable Bus supports up to 12 simultaneous outstanding transactions.

#### 9.1.2 FSB OoQ Depth

The (G)MCH supports only one outstanding deferred transaction on the FSB.

#### 9.1.3 FSB GTL+ Termination

The (G)MCH integrates GTL+ termination resistors on die.

#### 9.1.4 FSB Dynamic Bus Inversion

The (G)MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the (G)MCH. HDINV[3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

| HDINV[3:0]# | Data Bits  |
|-------------|------------|
| HDINV0#     | HD[15:0]#  |
| HDINV1#     | HD[31:16]# |
| HDINV2#     | HD[47:32]# |
| HDINV3#     | HD[63:48]# |

Whenever the processor or the (G)MCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the



corresponding HDINV# signal will be asserted, and the data will be inverted prior to being driven on the bus. Whenever the processor or the (G)MCH receives data, it monitors HDINV[3:0]# to determine if the corresponding data segment should be inverted.

### 9.1.5 APIC Cluster Mode Support

APIC Cluster mode support is required for backwards compatibility with existing software, including various operating systems. As one example, beginning with Microsoft Windows 2000, there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.

- The (G)MCH supports three types of interrupt re-direction:
  - Physical
  - Flat-Logical
  - Clustered-Logical

## 9.2 System Memory Controller

The system memory controller supports DDR2 protocols with two independent 64 bit wide channels each accessing one DIMM. It supports a maximum of one un-buffered non-ECC DDR2 DIMM per channel.

### 9.2.1 System Memory Organization Modes

The system memory controller supports three memory organization modes, Single Channel, Dual Channel Symmetric, and Dual Channel Asymmetric.

#### 9.2.1.1 Single Channel Mode

In this mode, all memory cycles are directed to a single channel.

Single channel mode is used when either Channel A or Channel B DIMMs are populated in any order, but not both.

#### 9.2.1.2 Dual Channel Symmetric Mode

This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels after each cache line (64 byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels.

Dual channel symmetric mode is used when both Channel A and Channel B DIMMs are populated in any order with the total amount of memory in each channel being the same, but the DRAM device technology and width may vary from one channel to the other.



Table 9-1 is a sample dual channel symmetric memory configuration showing the rank organization:

**Table 9-1. Sample System Memory Dual Channel Symmetric Organization Mode with Intel® Flex Memory Mode Enabled**

|        | Channel 0 population | Cumulative top address in Channel 0 | Channel 1 population | Cumulative top address in Channel 1 |
|--------|----------------------|-------------------------------------|----------------------|-------------------------------------|
| Rank 1 | 512 MB               | 2048 MB                             | 512 MB               | 2048 MB                             |
| Rank 0 | 512 MB               | 1024 MB                             | 512 MB               | 1024 MB                             |

### 9.2.1.3 Dual Channel Asymmetric Mode with Intel® Flex Memory Mode Enabled

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start in channel 0 and stay there until the end of the highest rank in channel 0, and then addresses continue from the bottom of channel 1 to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth will be limited to that of a single channel.

Dual channel asymmetric mode is used when both Channel A and Channel B DIMMs are populated in any order with the total amount of memory in each channel being different.

Table 9-2 is a sample dual channel asymmetric memory configuration showing the rank organization.

**Table 9-2. Sample System Memory Dual Channel Asymmetric Organization Mode with Intel® Flex Memory Mode Disabled**

|        | Channel 0 population | Cumulative top address in Channel 0 | Channel 1 population | Cumulative top address in Channel 1 |
|--------|----------------------|-------------------------------------|----------------------|-------------------------------------|
| Rank 1 | 512 MB               | 1024 MB                             | 512 MB               | 2304 MB                             |
| Rank 0 | 512 MB               | 512 MB                              | 512 MB               | 1792 MB                             |



## 9.2.2 System Memory Technology Supported

The (G)MCH supports the following DDR2 Data Transfer Rates, DIMM Modules, and DRAM Device Technologies:

- DDR2 Data Transfer Rates: 667 (PC2-5300) , 800 (PC2-6400)
- DDR2 DIMM Modules:
  - Raw Card C - Single Sided x16 un-buffered non-ECC
  - Raw Card D - Single Sided x8 un-buffered non-ECC
  - Raw Card E - Double Sided x8 un-buffered non-ECC
- DDR2 and DRAM Device Technology: 512 MB and 1 GB

**Table 9-3. Supported DIMM Module Configurations**

| Mem. Type              | Raw Card Ver. | DIMM Cap. | DRAM Device Tech. | DRAM Org. | # of DRAM Devices | # of Physical Device Ranks | # of Row/Col Address Bits | # of Banks Inside DRAM | Page Size |
|------------------------|---------------|-----------|-------------------|-----------|-------------------|----------------------------|---------------------------|------------------------|-----------|
| DDR2<br>667 and<br>800 | C             | 256 MB    | 512 Mb            | 32M X 16  | 4                 | 1                          | 13/10                     | 4                      | 8K        |
|                        |               | 512 MB    | 1 Gb              | 64M X 16  | 4                 | 1                          | 13/10                     | 8                      | 8K        |
|                        | D             | 512 MB    | 512 Mb            | 64M X 8   | 8                 | 1                          | 14/10                     | 4                      | 8K        |
|                        |               | 1 GB      | 1 Gb              | 128M X 8  | 8                 | 1                          | 14/10                     | 8                      | 8K        |
|                        | E             | 1 GB      | 512 Mb            | 64M X 8   | 16                | 2                          | 14/10                     | 4                      | 8K        |
|                        |               | 2 GB      | 1 Gb              | 128M X 8  | 16                | 2                          | 14/10                     | 8                      | 8K        |



## 9.3 PCI Express\*

See Section 1.3 for a list of PCI Express features, and the PCI Express specification for further details.

This (G)MCH is part of a PCI Express root complex. This means it connects a host processor/memory subsystem to a PCI Express hierarchy. The control registers for this functionality are located in device #1 configuration space and two Root Complex Register Blocks (RCRBs). The DMI RCRB contains registers for control of the Intel ICH7 attach ports.

### PCI Express\* Architecture

The PCI Express architecture is specified in layers. Compatibility with the PCI addressing model (a load-store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial speed of 1.25 GHz (250 MHz internally) results in 2.5 GB/s/direction which provides a 250 MB/s communications channel in each direction (500 MB/s total) that is close to twice the data rate of classic PCI per lane.

### Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

### Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

### Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.



### 9.3.1 Intel® Serial Digital Video Output (sDVO) (Intel® 82G31 GMCH Only)

The sDVO description is located here because it is multiplexed onto the PCI Express x16 port pins. The Intel® sDVO Port is the second generation of digital video output from compliant Intel® GMCHs. The electrical interface is based on the PCI Express interface, though the protocol and timings are completely unique. Whereas PCI Express runs at a fixed frequency, the frequency of the sDVO interface is dependant upon the active display resolution and timing. The port can be dynamically configured in several modes to support display configurations.

Essentially, an sDVO port will transmit display data in a high speed, serial format across differential AC coupled signals. An sDVO port consists of a sideband differential clock pair and a number of differential data pairs.

#### 9.3.1.1 Intel® sDVO Capabilities

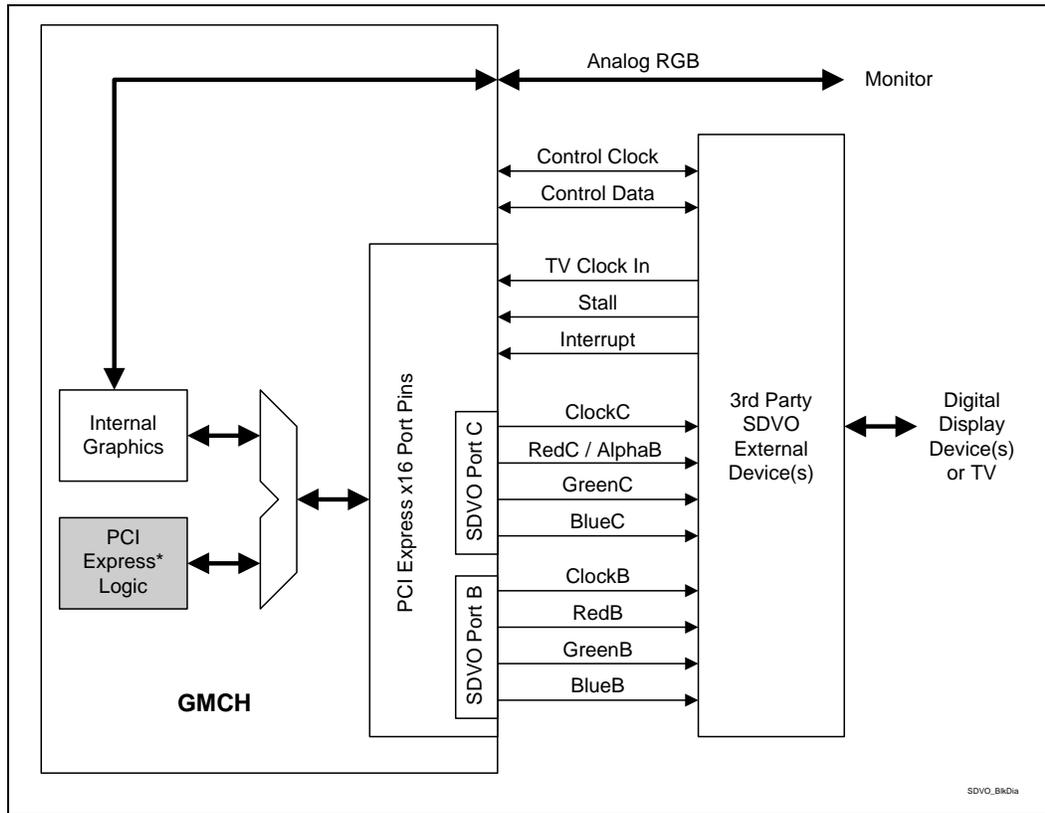
sDVO ports can support a variety of display types including LVDS, DVI, Analog CRT, TV-Out and external CE type devices. The GMCH uses an external sDVO device to translate from sDVO protocol and timings to the desired display format and timings.

The Internal Graphics Controller can have one or two sDVO ports multiplexed on the x16 PCI Express interface. When an external x16 PCI Express graphics accelerator is not in use, an ADD2 card may be plugged into the x16 connector or if a x16 slot is not present, the sDVO(s) may be located 'down' on the motherboard to access the multiplexed sDVO ports and provide a variety of digital display options.

The ADD2/Media Expansion card is designed to fit in a x16 PCI Express connector. The ADD2/Media Expansion card can support one or two devices. If a single channel sDVO device is utilized, it should be attached to the channel B sDVO pins. The ADD2 card can support two separate sDVO devices when the interface is in Dual Independent or Dual Simultaneous Standard modes. The Media Expansion card adds Video in capabilities.

The sDVO port defines a two-wire point-to-point communication path between the sDVO device and GMCH. The sDVO Control Clock and Data provide similar functionality to I<sup>2</sup>C. However unlike I<sup>2</sup>C, this interface is intended to be point-to-point (from the GMCH to the sDVO device) and will require the sDVO device to act as a switch and direct traffic from the sDVO Control bus to the appropriate receiver. Additionally, this Control bus will be able to run at faster speeds (up to 1 MHz) than a traditional I<sup>2</sup>C interface would.

Figure 9-1. sDVO Conceptual Block Diagram



### 9.3.1.2 Intel® sDVO Modes

The port can be dynamically configured in several modes:

- **Standard.** This mode provides baseline SDVO functionality. It supports Pixel Rates between 25 MP/s and 225 MP/s. It uses three data pairs to transfer RGB data.
- **Dual Standard.** This mode uses Standard data streams across both SDVOB and SDVOC. Both channels can only run in Standard mode (3 data pairs) and each channel supports Pixel Rates between 25 MP/s and 225 MP/s.
  - **Dual Independent Standard.** In Dual Independent Standard mode, each SDVO channel sees a different pixel stream. The data stream across SDVOB is not the same as the data stream across SDVOC.
  - **Dual Simultaneous Standard.** In Dual Simultaneous Standard mode, both SDVO channels see the same pixel stream. The data stream across SDVOB is the same as the data stream across SDVOC. The display timings will be identical, but the transfer timings may not be (i.e., SDVOB clocks and data may not be perfectly aligned with SDVOC clock and data as seen at the SDVO device(s)). Since this mode uses just a single data stream, it uses a single pixel pipeline within the GMCH.



### 9.3.1.3 PCI Express\* and Internal Graphics Simultaneous Operation

#### 9.3.1.3.1 Standard PCI Express\* Cards and Internal Graphics

BIOS control of simultaneous operation is needed to ensure the PCI Express is configured appropriately.

#### 9.3.1.3.2 Media Expansion Cards (Concurrent sDVO and PCI Express\*)

sDVO lane reversal is supported in the 82G31 GMCH. This functionality allows current sDVO ADD2 cards to work in current ATX and BTX systems instead of requiring a separate card. The GMCH allows sDVO and PCI Express to operate concurrently on the PCI Express Port. The card that plugs into the x16 connector in this case is called a Media Expansion card. It uses 4 or 8 lanes for sDVO and up to 8 lanes of standard PCI Express.

The GMCH only supports PCI Express width when sDVO is present is x1.

This concurrency is supported in reversed and non-reversed configurations. Mirroring / Reversing is always about the axis.

**Table 9-4. Concurrent sDVO / PCI Express\* Configuration Strap Controls**

| Configuration # | Description  | Slot Reversed Strap | sDVO Present Strap | sDVO/PCI Express* Concurrent Strap |
|-----------------|--|---------------------|--------------------|------------------------------------|
| 1               | PCI Express* not reversed                          | —                   | —                  | —                                  |
| 2               | PCI Express* Reversed                              | Yes                 | —                  | —                                  |
| 3               | sDVO (ADD2) not reversed                           | —                   | Yes                | —                                  |
| 4               | sDVO (ADD2) Reversed                               | Yes                 | Yes                | —                                  |
| 5               | sDVO & PCI Express* (MEDIA EXPANSION) not reversed | —                   | Yes                | Yes                                |
| 6               | sDVO & PCI Express* (MEDIA EXPANSION) Reversed     | Yes                 | Yes                | Yes                                |

Notes:

1. The Configuration #s refer to the following figures (no intentional relation to validation configs).
2. Configuration 4, 5, and 6 (required addition of sDVO/PCI Express\* Concurrent Strap).



Figure 9-2. Concurrent sDVO / PCI Express\* Non-Reversed Configurations

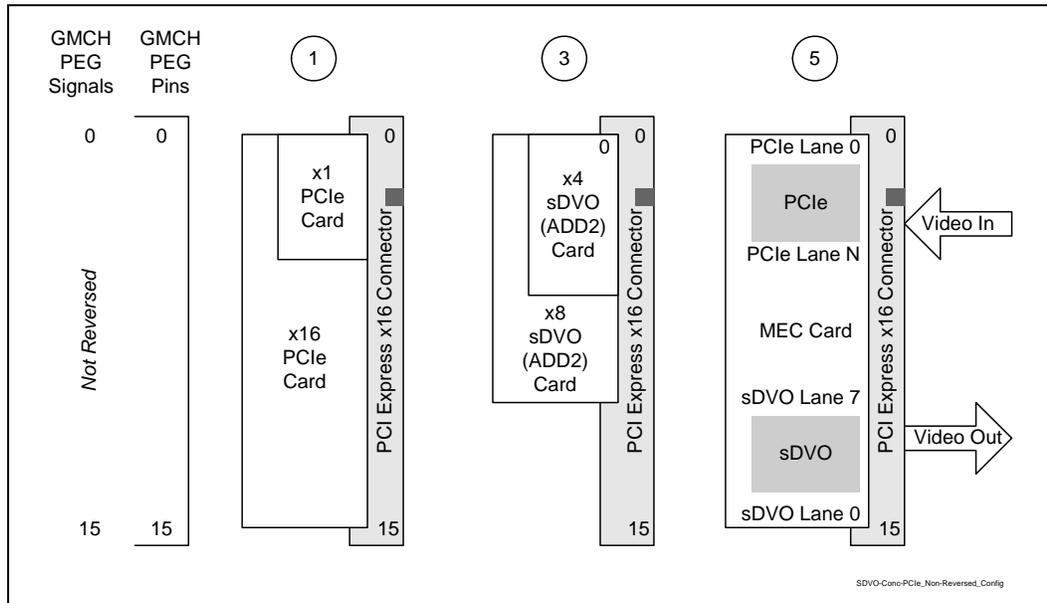
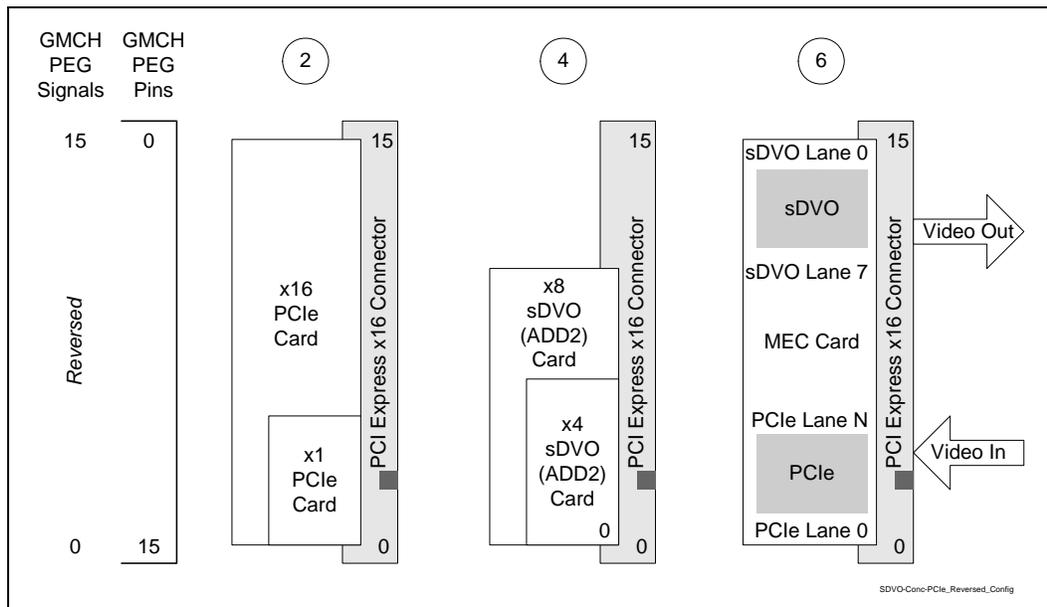


Figure 9-3. Concurrent sDVO / PCI Express\* Reversed Configurations





## 9.4 Integrated Graphics Controller (Intel® 82G31 GMCH Only)

The major components in the Integrated Graphics Device (IGD) are the engines, planes, pipes and ports. The GMCH has a 3D/2D instruction processing unit to control the 3D and 2D engines. The IGD's 3D and 2D engines are fed with data through the memory controller. The output of the engines are surfaces sent to memory that are then retrieved and processed by the GMCH planes.

The GMCH contains a variety of planes, such as display, overlay, cursor and VGA. A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces that are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

A pipe consists of a set of combined planes and a timing generator. The GMCH has two independent display pipes, allowing for support of two independent display streams. A port is the destination for the result of the pipe. The GMCH contains three display ports; 1 analog (DAC) and two digital (sDVO ports B and C). The ports will be explained in more detail later in this section.

The entire IGD is fed with data from its memory controller. The GMCH's graphics performance is directly related to the amount of bandwidth available. If the engines are not receiving data fast enough from the memory controller, the rest of the IGD will also be affected.

The rest of this section will focus on explaining the IGD components, their limitations, and dependencies.

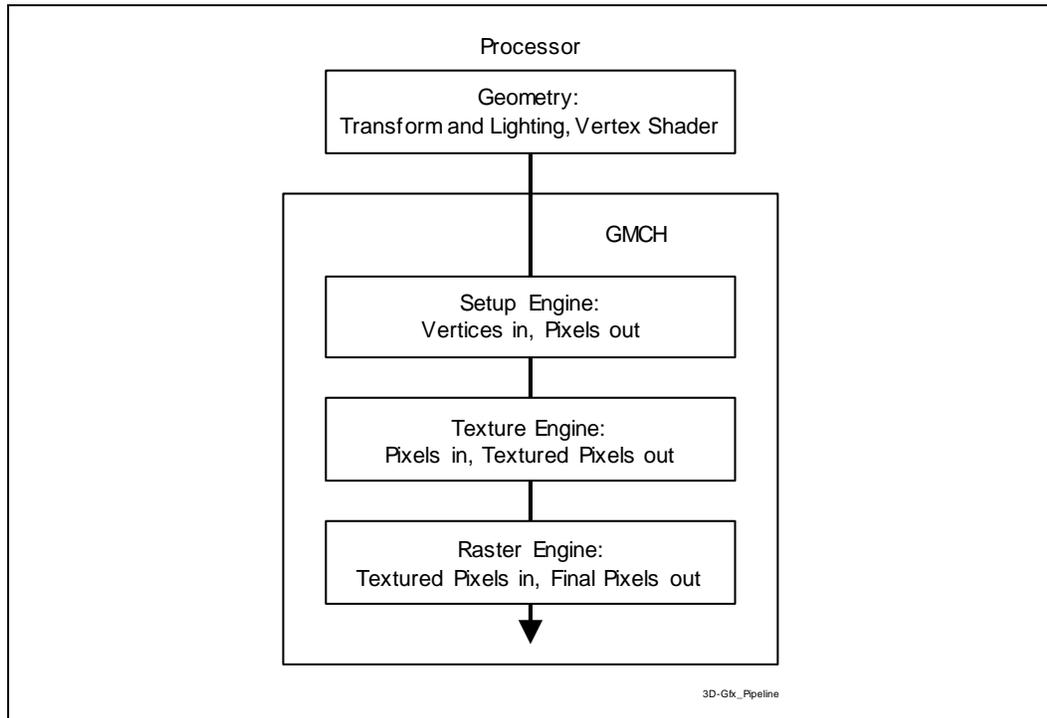
### 9.4.1 3D Graphics Pipeline

The 82G31 GMCH graphics is the next step in the evolution of integrated graphics. In addition to running the graphics engine at 400 MHz, the GMCH graphics has two pixel pipelines that provide a 1.3 GB/s fill rate that enables an excellent consumer gaming experience.

The 3D graphics pipeline for the GMCH has a deep pipelined architecture in which each stage can simultaneously operate on different primitives or on different portions of the same primitive. The 3D graphics pipeline is divided into four major stages: geometry processing, setup (vertex processing), texture application, and rasterization.

The GMCH graphics is optimized for use with current and future Intel® processors for advance software based transform and lighting techniques (geometry processing) as defined by the Microsoft DirectX\* API. The other three stages of 3D processing are handled on the integrated graphics device. The setup stage is responsible for vertex processing; converting vertices to pixels. The texture application stage applies textures to pixels. The rasterization engine takes textured pixels and applies lighting and other environmental affects to produce the final pixel value. From the rasterization stage, the final pixel value is written to the frame buffer in memory so it can be displayed.

Figure 9-4. Integrated 3D Graphics Pipeline



### 9.4.1.1 3D Engine

The 3D engine on the GMCH has been designed with a deep pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive. The GMCH supports Perspective-Correct Texture Mapping, Multitextures, Bump-Mapping, Cubic Environment Maps, Bilinear, Trilinear and Anisotropic MIP mapped filtering, Gouraud shading, Alpha-blending, Vertex and Per Pixel Fog and Z/W Buffering.

The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the setup engine, scan converter, texture pipeline, and raster pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rendering instructions containing 3D primitive vertex data.

The engines' performance is dependent on the memory bandwidth available. Systems that have more bandwidth available will outperform systems with less bandwidth. The engines' performance is also dependent on the core clock frequency. The higher the frequency, the more data is processed.

### 9.4.1.2 Texture Engine

The GMCH allows an image, pattern, or video to be placed on the surface of a 3D polygon. The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the scan converter. The texture processor performs texture color or ChromaKey matching, texture filtering (anisotropic, trilinear, and bilinear interpolation), and YUV-to-RGB conversions.



### 9.4.1.3 Raster Engine

The raster engine is where the color data (such as, fogging, specular RGB, texture map blending, etc.) is processed. The final color of the pixel is calculated and the RGBA value combined with the corresponding components resulting from the texture engine. These textured pixels are modified by the specular and fog parameters. These specular highlighted, fogged, textured pixels are color blended with the existing values in the frame buffer. In parallel, stencil, alpha, and depth buffer tests are conducted that determine whether the frame and depth buffers will be updated with the new pixel values.

## 9.5 Display Interfaces (Intel® 82G31 GMCH Only)

The GMCH has three display ports, one analog and two digital. Each port can transmit data according to one or more protocols. The digital ports are connected to an external device that converts one protocol to another. Examples of these are TV encoders, external DACs, LVDS transmitters, HDMI transmitters and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device.

The GMCH has one dedicated display port, the analog port. sDVO ports B and C are multiplexed with the PCI Express Graphics (PEG) interface and are not available if an external PEG device is in use. When a system utilizes a PEG connector, sDVO ports B and C can be utilized via an ADD2 (Advanced Digital Display 2) or MEC (Media Expansion Card).

- The GMCH's analog port utilizes an integrated 350 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 75 Hz.
- The GMCH's sDVO ports are each capable of driving a 225 MP pixel rate. Each port is capable of driving a digital display up to 1920x1200 @ 60Hz.

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT).

The GMCH is compliant with HDMI Specification 1.1. When combined with a HDMI compliant external device and connector, the external HDMI device can supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.



## 9.5.1 Analog Display Port Characteristics

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality added to the signals to enhance that capability.

**Table 9-1. Analog Port Characteristics**

| Signal | Port Characteristic     | Support                   |
|--------|-------------------------|---------------------------|
| RGB    | Voltage Range           | 0.7 V p-p only            |
|        | Monitor Sense           | Analog Compare            |
|        | Analog Copy Protection  | No                        |
|        | Sync on Green           | No                        |
|        | Voltage                 | 2.5 V                     |
| HSYNC  | Enable/Disable          | Port control              |
|        | Polarity adjust         | VGA or port control       |
| VSYNC  | Composite Sync Support  | No                        |
|        | Special Flat Panel Sync | No                        |
|        | Stereo Sync             | No                        |
| DDC    | Voltage                 | Externally buffered to 5V |
|        | Control                 | Through GPIO interface    |

### 9.5.1.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. GMCH's integrated 350 MHz RAMDAC supports resolutions up to 2048 x 1536 @ 75 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.

### 9.5.1.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support will be included.



### 9.5.1.3 VESA/VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

### 9.5.1.4 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug- and-play systems to be realized. Support for DDC 1 and 2 is implemented. The GMCH uses the DDC\_CLK and DDC\_DATA signals to communicate with the analog monitor. The GMCH generates these signals at 2.5 V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The GMCH implements a hardware GMBus controller that can be used to control these signals allowing for transactions speeds up to 400 kHz.

## 9.5.2 Digital Display Interface

The GMCH has several options for driving digital displays. The GMCH contains two sDVO ports that are multiplexed on the PEG interface. When an external PEG graphics accelerator is not present, the GMCH can use the multiplexed sDVO ports to provide extra digital display options. These additional digital display capabilities may be provided through an ADD2/MEDIA EXPANSION CARD, which is designed to plug in to a PCI Express connector.

### 9.5.2.1 Multiplexed Digital Display Channels – Intel® sDVOB and Intel® sDVOC

The GMCH has the capability to support digital display devices through two sDVO ports multiplexed with the PEG signals. When an external graphics accelerator is used via the PEG port, these sDVO ports are not available.

The shared sDVO ports each support a pixel clock up to 225 MHz and can support a variety of transmission devices.

SDVOCTRLDATA is an open-drain signal that will act as a strap during reset to tell the GMCH whether the interface is a PCI Express interface or an sDVO interface. When implementing sDVO, either via ADD2 cards or with a down device, a pull-up is placed on this line to signal to the GMCH to run in sDVO mode and for proper GMBus operation.

#### 9.5.2.1.1 ADD2/MEDIA EXPANSION CARD(MEC)

When a G31 Express Chipset platform uses a PEG connector, the multiplexed sDVO ports may be used via an ADD2 or MEC card. The ADD2 card will be designed to fit a standard PCI Express (x16) connector. Please refer to the latest ADD2/MEC EDS and ADD2 or MEC card design kits for more details on ADD2/MEC.



### 9.5.2.2 TMDs Capabilities

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT). The GMCH can drive a flat panel up to 1920x1200 or a dCRT/HDTV up to 1400x1050. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities. The GMCH will however, provide unscaled mode where the display is centered on the panel.

#### 9.5.2.2.1 HDMI Capabilities

The GMCH is compliant with HDMI Specification 1.1. When combined with a HDMI compliant external device and connector, the external HDMI device can supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. The GMCH has a high speed interface to a digital display (e.g., flat panel or digital TV). The GMCH can drive a digital TV up to 1600x1200.

#### 9.5.2.2.2 LVDS Capabilities

The GMCH may use the multiplexed sDVO ports to drive an LVDS transmitter. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities. The GMCH will however, provide unscaled mode where the display is centered on the panel. The GMCH supports scaling in the LVDS transmitter through the sDVO stall input pair.

#### 9.5.2.2.3 TV-IN Capabilities

The GMCH in conjunction with ADD2/MEDIA EXPANSION CARD can function as a TV-Tuner card capable of taking in both analog or HD signals

#### 9.5.2.2.4 TV-Out Capabilities

Although traditional TVs are not digital displays, the GMCH uses a digital display channel to communicate with a TV-Out transmitter. For that reason, the GMCH considers a TV-Output to be a digital display. The GMCH supports NTSC/PAL/SECAM standard definition formats. The GMCH will generate the proper timing for the external encoder. The external encoder is responsible for generation of the proper format signal. Since the multiplexed sDVO interface is a NTSC/PAL/SECAM display on the TV-out port can be configured to be the boot device. It is necessary to ensure that appropriate BIOS support is provided.

The TV-out interface on GMCH allows an external TV encoder device to drive a pixel clock signal on SDVO\_TVClk[+/-] that the GMCH uses as a reference frequency. The frequency of this clock is dependent on the output resolution required.



### Flicker Filter and Overscan Compensation

The overscan compensation scaling and the flicker filter is done in the external TV encoder chip. Care must be taken to allow for support of TV sets with high performance de-interlacers and progressive scan displays connected to by way of a non-interlaced signal. Timing will be generated with pixel granularity to allow more overscan ratios to be supported.

### Analog Content Protection

Analog content protection will be provided through the external encoder using Macrovision 7.01. DVD software must verify the presence of a Macrovision TV encoder before playback continues. Simple attempts to disable the Macrovision operation must be detected.

### Connectors

Target TV connectors support includes the CVBS, S-Video, Component, HDMI and SCART connectors. The external TV encoder in use will determine the method of support.

#### 9.5.2.2.5 Control Bus

Communication to SDVO registers and if utilized, ADD2/MEC PROMs and monitor DDCs, are accomplished by using the SDVOCTRLDATA and SDVOCTRLCLK signals through the SDVO device. These signals run up to 1 MHz and connect directly to the SDVO device. The SDVO device is then responsible for routing the DDC and PROM data streams to the appropriate location. Consult SDVO device data sheets for level shifting requirements of these signals.

#### 9.5.2.2.6 Intel® sDVO Modes

The port can be dynamically configured in several modes:

- **Standard.** This mode provides baseline SDVO functionality. It supports pixel rates between 25 MP/s and 225 MP/s. It uses three data pairs to transfer RGB data.
- **Dual Standard.** This mode provides Standard data streams across both SDVOB and SDVOC. Both channels can only run in Standard mode (3 data pairs) and each channel supports Pixel Rates between 25 MP/s and 225 MP/s.
  - **Dual Independent Standard.** In Dual Independent Standard mode, each SDVO channel will transmit a different pixel stream. The data stream across SDVOB will not be the same as the data stream across SDVOC.
  - **Dual Simultaneous Standard.** In Dual Simultaneous Standard mode, both SDVO channels will transmit the same pixel stream. The data stream across SDVOB will be the same as the data stream across SDVOC. The display timings will be identical, but the transfer timings may not be (i.e., SDVOB clocks and data may not be perfectly aligned with SDVOC clock and data as seen at the SDVO device(s)). Since this uses just a single data stream, it uses a single pixel pipeline within the GMCH.



### 9.5.3 Multiple Display Configurations

Microsoft Windows\* 2000, Windows XP and Windows Vista\* operating systems supports for multi-monitor display. Since the GMCH has several display ports available for its two pipes, it can support up to two different images on different display devices. Timings and resolutions for these two images may be different. The GMCH supports Dual Display Clone, Dual Display Twin, and Extended Desktop.

Dual Display Clone uses both display pipes to drive the same content, at the same resolution and color depth to two different displays. This configuration allows for different refresh rates on each display.

Dual Display Twin uses one of the display pipes to drive the same content, at the same resolution, color depth, and refresh rates to two different displays.

Extended Desktop uses both display pipes to drive different content, at potentially different resolutions, refresh rates, and color depths to two different displays. This configuration allows for a larger Windows Desktop by utilizing both displays as a work surface.

**Note:** The (G)MCH is also incapable of operating in parallel with an external PCI Express graphics device. The (G)MCH can, however, work in conjunction with a PCI graphics adapter.

## 9.6 Power Management

Power Management Feature List:

- ACPI 1.0b support
- ACPI S0, S1, S3 (both Cold and chipset Hot), S5, C0, C1, and C2 states
- Enhanced power management state transitions for increasing time processor spends in low power states
- Internal Graphics Display Device Control D0, D1, D2, D3
- Graphics Adapter States: D0, D3
- PCI Express Link States: L0, L0s, L2/L3 Ready, L3



## 9.7 Thermal Sensor

There are several registers that need to be configured to support the (G)MCH thermal sensor functionality and SMI# generation. Customers must enable the Catastrophic Trip Point at 115 °C as protection for the (G)MCH. If the Catastrophic Trip Point is crossed, then the (G)MCH will instantly turn off all clocks inside the device. Customers may optionally enable the Hot Trip Point between 85 °C and 105 °C to generate SMI#. Customers will be required to then write their own SMI# handler in BIOS that will speed up the (G)MCH (or system) fan to cool the part.

### 9.7.1 PCI Device 0, Function 0

The SMICMD register requires that a bit be set to generate an SMI# when the Hot trip point is crossed. The ERRSTS register can be inspected for the SMI alert.

| Address Offset | Symbol | Register Name | Default Value | Access    |
|----------------|--------|---------------|---------------|-----------|
| C8–C9h         | ERRSTS | Error Status  | 0000h         | RO, RWC/S |
| CC–CDh         | SMICMD | SMI Command   | 0000h         | RO, RW    |

### 9.7.2 MCHBAR Thermal Sensor Registers

The Digital Thermometer Configuration Registers reside in the MCHBAR configuration space.

| Address Offset | Symbol  | Register Name                         | Default Value | Access              |
|----------------|---------|---------------------------------------|---------------|---------------------|
| CD8h           | TSC1    | Thermal Sensor Control 1              | 00h           | RW/L, RW<br>RS/WC,  |
| CD9h           | TSC2    | Thermal Sensor Control 2              | 00h           | RW/L, RO            |
| CDAh           | TSS     | Thermal Sensor Status                 | 00h           | RO                  |
| CDC–CDFh       | TSTTP   | Thermal Sensor Temperature Trip Point | 00000000h     | RO, RW,<br>RW/L     |
| CE2h           | TCO     | Thermal Calibration Offset            | 00h           | RW/L/K,<br>RW/L     |
| CE4h           | THERM1  | Hardware Protection                   | 00h           | RW/L, RO,<br>RW/L/K |
| CE6h           | THERM3  | TCO Fuses                             | 00h           | RS/WC,<br>RO        |
| CEA–CEBh       | TIS     | Thermal Interrupt Status              | 0000h         | RO, RWC,            |
| CF1h           | TSMICMD | Thermal SMI Command                   | 00h           | RO, RW              |

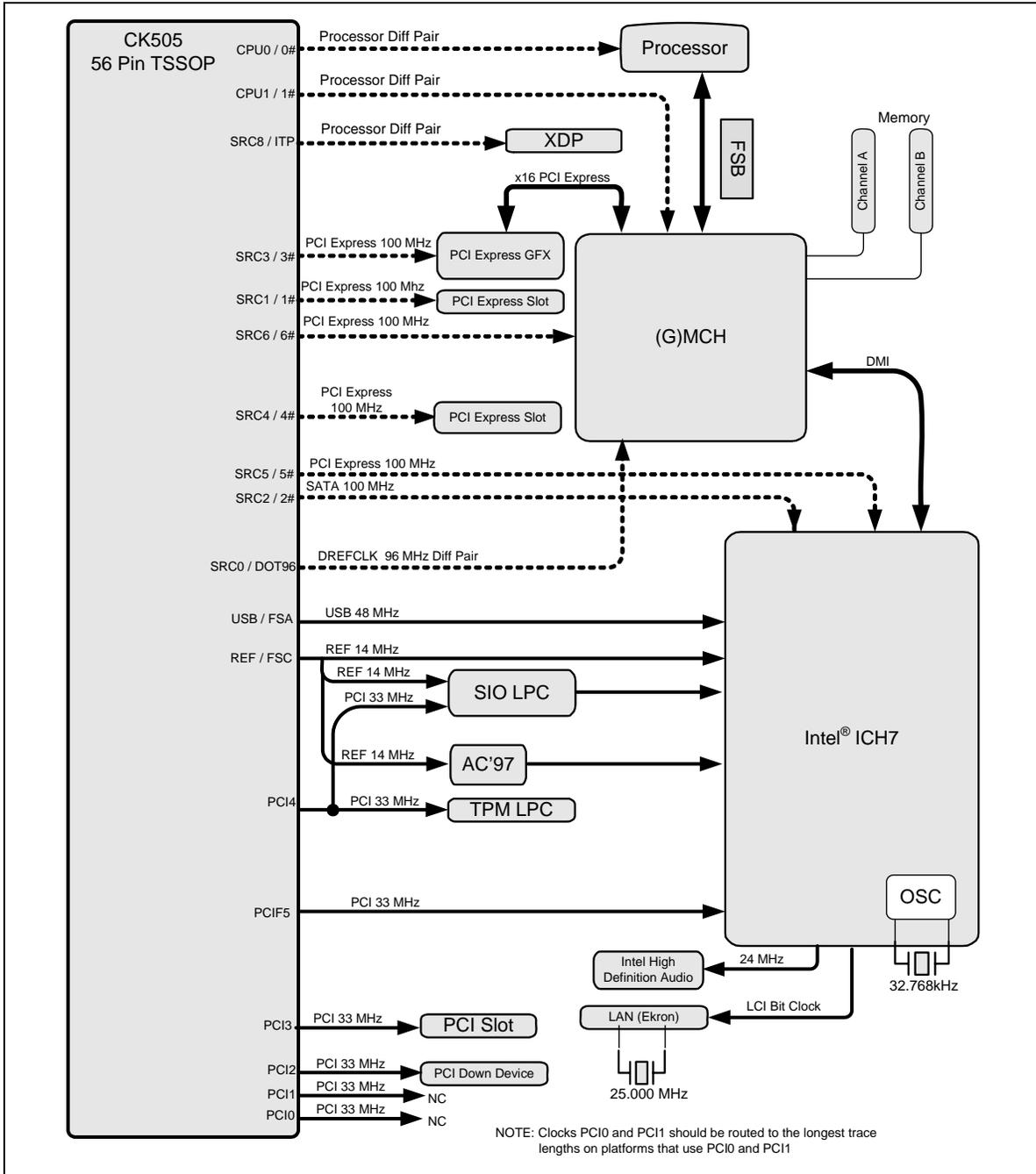


## 9.8 Clocking

The (G)MCH has a total of 5 PLLs providing many times that many internal clocks. The PLLs are:

- Host PLL – Generates the main core clocks in the host clock domain. Can also be used to generate memory and internal graphics core clocks. Uses the Host clock (H\_CLKIN) as a reference.
- Memory I/O PLL - Optionally generates low jitter clocks for memory I/O interface, as opposed to from Host PLL. Uses the Host FSB differential clock (HPL\_CLKINP/HPL\_CLKINN) as a reference. Low jitter clock source from Memory I/O PLL is required for DDR667 and higher frequencies.
- PCI Express PLL – Generates all PCI Express related clocks, including the Direct Media Interface that connects to the ICH. This PLL uses the 100 MHz clock (G\_CLKIN) as a reference.
- Display PLL A – Generates the internal clocks for Display A. Uses D\_REFCLKIN as a reference.
- Display PLL B – Generates the internal clocks for Display B. Also uses D\_REFCLKIN as a reference.
- CK505 is the Clocking chip is required for the Intel® G31/P31 Express Chipset platform

Figure 9-5. Intel® G31/P31 Express Chipset System Clock Diagram





# 10 Electrical Characteristics

This chapter provides the DC characteristics for the 82G31 GMCH and 82P31 MCH.

**Note:** References to the internal graphics device or associated ports (e.g., SDVO port, analog port) apply to the 82G31 GMCH.

## 10.1 Absolute Minimum and Maximum Ratings

Table 10-1 specifies the (G)MCH absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time its reliability will be severely degraded or not function when returned to conditions within the functional operating condition limits.

Although the (G)MCH contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

**Table 10-1. Absolute Minimum and Maximum Ratings**

| Symbol  | Parameter   | Min  | Max   | Unit | Notes |
|---|---|------|-------|------|-------|
| T <sub>storage</sub>                              | Storage Temperature   | -55  | 150   | °C   | 1     |
| <b>(G)MCH Core</b>                                |   |      |       |      |       |
| VCC   | 1.25 V Core Supply Voltage with respect to VSS              | -0.3 | 1.375 | V    |       |
| <b>Host Interface (800/1066 MHz)</b>              |   |      |       |      |       |
| VTT   | System Bus Input Voltage with respect to VSS                | -0.3 | 1.32  | V    |       |
| VCCA_HPLL   | 1.25 V Host PLL Analog Supply Voltage with respect to VSS   | -0.3 | 1.375 | V    |       |
| <b>System Memory Interface (DDR2 667/800 MHz)</b> |   |      |       |      |       |
| VCCSM   | 1.8 V DDR2 System Memory Supply Voltage with respect to VSS | -0.3 | 4.0   | V    |       |



| Symbol   | Parameter  | Min  | Max   | Unit | Notes |
|--|--|------|-------|------|-------|
| VCC_SMCLK  | 1.8 V DDR2 Clock System Memory Supply Voltage with respect to VSS  | -0.3 | 4.0   | V    |       |
| VCCA_MPLL  | 1.25 V System Memory PLL Analog Supply Voltage with respect to VSS | -0.3 | 1.375 | V    |       |
| <b>PCI Express* / Intel® sDVO / DMI Interface</b>  |  |      |       |      |       |
| VCC_EXP  | 1.25 V PCI Express* and DMI Supply Voltage with respect to VSS     | -0.3 | 1.375 | V    |       |
| VCCA_EXP   | 3.3 V PCI Express* Analog Supply Voltage with respect to VSS       | -0.3 | 3.63  | V    |       |
| VCCA_EXPPLL  | 1.25 V PCI Express* PLL Analog Supply Voltage with respect to VSS  | -0.3 | 1.375 | V    |       |
| <b>R, G, B / CRT DAC Display Interface (8 bit)</b> |  |      |       |      |       |
| VCCA_DAC   | 3.3 V Display DAC Analog Supply Voltage with respect to VSS        | -0.3 | 3.63  | V    |       |
| VCCD_CRT   | 1.5 V Display DAC Digital Supply Voltage with respect to VSS       | -0.3 | 1.98  | V    |       |
| VCCDQ_CRT  | 1.5 V Display DAC Quiet Digital Supply Voltage with respect to VSS | -0.3 | 1.98  | V    |       |
| VCCA_DPLLA   | 1.25 V Display PLL A Analog Supply Voltage with respect to VSS     | -0.3 | 1.375 | V    |       |
| VCCA_DPLLB   | 1.25 V Display PLL B Analog Supply Voltage with respect to VSS     | -0.3 | 1.375 | V    |       |
| <b>Controller Link Interface</b>                   |  |      |       |      |       |
| VCC_CL   | 1.25 V Supply Voltage with respect to VSS                          | -0.3 | 1.375 | V    |       |
| <b>CMOS Interface</b>                              |  |      |       |      |       |
| VCC3_3   | 3.3 V CMOS Supply Voltage with respect to VSS                      | -0.3 | 3.63  | V    |       |

**NOTE:**

1. Possible damage to the (G)MCH may occur if the (G)MCH temperature exceeds 150 °C. Intel does not ensure functionality for parts that have exceeded temperatures above 150 °C due to spec violation.



## 10.1.1 Current Consumption

Table 10-2 shows the current consumption for the (G)MCH in the Advanced Configuration and Power Interface (ACPI) S0 state. I<sub>cc</sub> max values are determined on a per-interface basis, at the highest frequencies for each interface. Sustained current values or Max current values cannot occur simultaneously on all interfaces. Sustained Values are *measured* sustained RMS maximum current consumption and includes leakage estimates. The measurements are made with fast silicon at 96° C T<sub>case</sub> temperature, at the Max voltage listed in Table 10-4. The Max values are maximum theoretical pre-silicon calculated values. In some cases, the Sustained measured values have exceeded the Max theoretical values.

**Table 10-2. Current Consumption in S0**

| Symbol                  | Parameter  | Signal Names               | Sustained | Max  | Unit | Notes   |
|-------------------------|--|----------------------------|-----------|------|------|---------|
| I <sub>VCC</sub>        | 1.25 V Core Supply Current<br>(Using Integrated Graphics)                                  | VCC<br>(int. graphics)     | 5.27      | 7.00 | A    | 1, 2    |
|                         | 1.25 V Core Supply Current<br>(Using External Graphics)                                    | VCC<br>(ext. graphics)     | 2.34      | 3.18 |      |         |
| I <sub>VCCSM</sub>      | DDR2 System Memory Interface<br>(1.8 V) Supply Current                                     | VCCSM                      | 2.62      | 3.71 | A    | 1, 2, 3 |
| I <sub>VCC_SMCLK</sub>  | DDR2 System Memory Clock<br>Interface (1.8 V) Supply Current                               | VCC_SMCLK                  | 180       | 220  | mA   |         |
| I <sub>VCC_EXP</sub>    | 1.25 V PCI Express* / Intel®<br>SDVO and DMI Supply Current<br>(Using Integrated Graphics) | VCC_EXP<br>(int. graphics) | 0.46      | 1.00 | A    | 2       |
|                         | 1.25 V PCI Express* / Intel®<br>SDVO and DMI Supply Current<br>(Using External Graphics)   | VCC_EXP<br>(ext. graphics) | 1.43      | 2.45 |      |         |
| I <sub>VCC_CL</sub>     | 1.25 V Controller Supply Current   | VCC_CL                     | 2.45      | 3.88 | A    | 2       |
| I <sub>VTT</sub>        | System Bus Supply Current  | VTT                        | 0.52      | 1    | A    | 1       |
| I <sub>VCCA_EXP</sub>   | 3.3 V PCI Express* / Intel®<br>SDVO and DMI Analog Supply<br>Current                       | VCCA_EXP                   | 39        | 72   | mA   |         |
| I <sub>VCCA_DAC</sub>   | 3.3 V Display DAC Analog Supply<br>Current   | VCCA_DAC                   | 74        | 78   | mA   |         |
| I <sub>VCC3_3</sub>     | 3.3 V CMOS Supply Current  | VCC3_3                     | 0.5       | 16   | mA   |         |
| I <sub>VCCD_CRT</sub>   | 1.5 V Display Digital Supply Current   | VCCD_CRT                   | 20        | 30   | mA   | 3       |
| I <sub>VCCDQ_CRT</sub>  | 1.5 V Display Quiet Digital Supply<br>Current  | VCCDQ_CRT                  | 9         | 11   | mA   |         |
| I <sub>VCCA_EXPLL</sub> | 1.25 V PCI Express* / Intel® SDVO<br>and DMI PLL Analog Supply Current                     | VCCA_EXPLL                 | 39        | 72   | mA   |         |
| I <sub>VCCA_HPLL</sub>  | 1.25 V Host PLL Supply Current   | VCCA_HPLL                  | 20        | 30   | mA   |         |



| Symbol                  | Parameter                                      | Signal Names | Sustained | Max | Unit | Notes |
|-------------------------|--|--------------|-----------|-----|------|-------|
| I <sub>VCCA_DPLLA</sub> | 1.25 V Display PLL A and PLL B Supply Current  | VCCA_DPLLA   | 49        | 73  | mA   |       |
| I <sub>VCCA_DPLLB</sub> | 1.25 V Display PLL A and PLL B Supply Current  | VCCA_DPLLB   | 42        | 70  | mA   |       |
| I <sub>VCCA_MPLL</sub>  | 1.25 V System Memory PLL Analog Supply Current | VCCA_MPLL    | 115       | 173 | mA   |       |

**NOTES:**

1. Measurements are for current coming through chipset's supply pins.
2. Rail includes DLLs (and FSB sense amps on VCC).
3. Sustained Measurements are combined because one voltage regulator on the platform supplies both rails on the (G)MCH.



## 10.2 Signal Groups

The signal description includes the type of buffer used for the particular signal:

|                            |  |
|----------------------------|--|
| PCI Express* / Intel® sDVO | PCI Express interface signals. These signals are compatible with PCI Express 1.1 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = $( D+ - D- ) * 2 = 1.2V_{max}$ . Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.   |
| DMI                        | Direct Media Interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = $( D+ - D- ) * 2 = 1.2V_{max}$ . Single-ended maximum = 1.25 V. Single-ended minimum = 0 V. |
| GTL+                       | Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details.  |
| HCSL                       | Host Clock Signal Level buffers. Current mode differential pair. Differential typical swing = $( D+ - D- ) * 2 = 1.4V$ . Single ended input tolerant from -0.35V to 1.2V. Typical crossing voltage 0.35V.  |
| SSTL-1.8                   | Stub Series Termination Logic. These are 1.8 V output capable buffers. 1.8 V tolerant.   |
| SSTL-1.5                   | Stub Series Termination Logic. These are 1.5 V output capable buffers. 1.5 V tolerant.   |
| CMOS                       | CMOS buffers   |
| Analog                     | Analog reference or output. May be used as a threshold voltage or for buffer compensation.   |

**Table 10-3. Signal Groups**

| Signal Type                         | Signals   | Notes |
|-------------------------------------|---|-------|
| <b>Host Interface Signal Groups</b> |   |       |
| GTL+ Input/Outputs                  | HADS#, HBNR#, HBREQ0#, HDBSY#, HDRDY#, HDINV[3:0]#, HA[35:3]#, HADSTB[1:0]#, HD[63:0]#, HDSTBP[3:0]#, HDSTBN[3:0]#, HHIT#, HHITM#, HREQ[4:0]#, HLOCK# |       |
| GTL+ Common Clock Outputs           | HBPRI#, HCPURST#, HDEFER#, HTRDY#, HRS[2:0]#  |       |
| Analog Host I/F Ref & Comp. Signals | HDVREF, HACCVREF, HSWING, HRCOMP, HSCOMP, HSCOMP#   |       |
| GTL+ Input                          | BSEL[2:0]   |       |



| Signal Type  | Signals   | Notes |
|--|---|-------|
| <b>PCI Express* Graphics and Intel® sDVO Interface Signal Groups</b> |   |       |
| PCI Express* / Intel® sDVO Input                                     | <b>PCI Express* Interface:</b> EXP_RXN[15:0], EXP_RXP[15:0],<br><b>Intel® sDVO Interface:</b> SDVO_TVCLKIN+, SDVO_TVCLKIN-, SDVOB_INT+, SDVOB_INT-, SDVO_STALL+, SDVO_STALL-, SDVOC_INT+, SDVOC_INT-  | 1     |
| PCI Express* / Intel® sDVO Output                                    | <b>PCI Express* Interface:</b> EXP_TXN[15:0], EXP_TXP[15:0]<br><b>Intel® sDVO Interface:</b> SDVOB_RED+, SDVOB_RED-, SDVOB_GREEN+, SDVOB_GREEN-, SDVOB_BLUE+, SDVOB_BLUE-, SDVOB_CLK+, SDVOB_CLK-, SDVOC_RED+/SDVOB_ALPHA+, SDVOC_RED-/SDVOB_ALPHA-, SDVOC_GREEN+, SDVOC_GREEN-, SDVOC_BLUE+, SDVOC_BLUE-, SDVOC_CLK+, SDVOC_CLK- | 1     |
| CMOS I/O OD  | SDVO_CTRLCLK, SDVO_CTRLDATA   |       |
| Analog PCI Express* / Intel® sDVO I/F Compensation Signals           | EXP_COMPO, EXP_COMPI  |       |
| <b>Direct Media Interface Signal Groups</b>                          |   |       |
| DMI Input  | DMI_RXN[3:0], DMI_RXP[3:0]  |       |
| DMI Output   | DMI_TXN[3:0], DMI_TXP[3:0]  |       |
| <b>System Memory Interface Signal Groups</b>                         |   |       |
| SSTL-1.8 / SSTL-1.5 Input/Output                                     | SDQ_A[63:0], SDQ_B[63:0], SDQS_A[7:0], SDQS_A[7:0]#, SDQS_B[7:0], SDQS_B[7:0]#  |       |
| SSTL-1.8 / SSTL-1.5 Output   | SDM_A[7:0], SDM_B[7:0], SMA_A[14:0], SMA_B[14:0], SBS_A[2:0], SBS_B[2:0], SRAS_A#, SRAS_B#, SCAS_A#, SCAS_B#, SWE_A#, SWE_B#, SODT_A[3:0], SODT_B[3:0], SCKE_A[3:0], SCKE_B[3:0], SCS_A[3:0]#, SCS_B[3:0]#, SCLK_A[5:0], SCLK_A[5:0]#, SCLK_B[5:0], SCLK_B[5:0]#  |       |
| CMOS Input   | N/A   |       |
| Reference and Comp. Voltages   | SRCOMP[3:0], SMVREF, SRCOMP_VOL, SRCOMP_VOH   |       |
| <b>Controller Link Signal Groups</b>                                 |   |       |
| CMOS I/O OD  | CL_DATA, CL_CLK   |       |
| CMOS Input   | CL_RST#, CL_PWROK   |       |
| Analog Controller Link Reference Voltage                             | CL_VREF   |       |



| Signal Type  | Signals  | Notes |
|--|--|-------|
| <b>R, G, B / CRT DAC Display Signal Groups</b>         |  |       |
| Analog Current Outputs                                 | RED, RED#, GREEN, GREEN#, BLUE, BLUE#                    |       |
| Analog/Ref DAC Miscellaneous                           | REFSET   | 2     |
| CMOS I/O OD  | DDC_CLK, DDC_DATA  |       |
| HVCMOS Output  | HSYNC, VSYNC   |       |
| <b>Clocks</b>  |  |       |
| HCSL   | HCLKN, HCLKP, DREFCLKP, DREFCLKN, GCLKP, GCLKN           |       |
| <b>Reset, and Miscellaneous Signal Groups</b>          |  |       |
| CMOS Input   | EXP_EN, EXP_SLR, RSTIN#, PWROK                           |       |
| CMOS Output  | ICH_SYNC#  |       |
| Miscellaneous  | TEST[2:0]  |       |
| <b>I/O Buffer Supply Voltages</b>                      |  |       |
| System Bus Input Supply Voltage                        | VTT  |       |
| 1.25 V PCI Express* / Intel® sDVO Supply Voltages      | VCC_EXP  |       |
| 3.3 V PCI Express* / Intel® sDVO Analog Supply Voltage | VCCA_EXP   |       |
| 1.8 V DDR2 Supply Voltage                              | VCCSM  |       |
| 1.8 V DDR2 Clock Supply Voltage                        | VCC_SMCLK  |       |
| 1.25 V (G)MCH Core Supply Voltage                      | VCC  |       |
| 1.25 V Controller Supply Voltage                       | VCC_CL   |       |
| 3.3 V CMOS Supply Voltage                              | VCC3_3   |       |
| 3.3 V R, G, B / CRT DAC Display Analog Supply Voltage  | VCCA_DAC   |       |
| 1.5 V DAC Digital Supply Voltages                      | VCCD_CRT, VCCDO_CRT                                      |       |
| PLL Analog Supply Voltages                             | VCCA_HPLL, VCCA_EXPLL, VCCA_DPLLA, VCCA_DPLLB, VCCA_MPLL |       |

**NOTES:**

1. Refer to Section 2.7 for Intel® sDVO and PCI Express\* Pin Mapping.
2. Current Mode Reference pin. DC Specifications not required



## 10.3 Buffer Supply and DC Characteristics

### 10.3.1 I/O Buffer Supply Voltages

The I/O buffer supply voltage is measured at the (G)MCH package pins. The tolerances shown in Table 10-4 are inclusive of all noise from DC up to 20 MHz. In the lab, the voltage rails should be measured with a bandwidth limited oscilloscope with a roll off of 3 dB/decade above 20 MHz under all operating conditions.

Table 10-4 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltages that are connected to a filter, they should be measured at the *input* of the filter.

If the recommended platform decoupling guidelines cannot be met, the system designer will have to make tradeoffs between the voltage regulator output DC tolerance and the decoupling performance of the capacitor network to stay within the voltage tolerances listed in Table 10-4.



Table 10-4. I/O Buffer Supply Voltage

| Symbol  | Parameter                                | Min   | Nom  | Max   | Unit | Notes |
|---|--|-------|------|-------|------|-------|
| VCCSM   | DDR2 I/O Supply Voltage                  | 1.7   | 1.8  | 1.9   | V    |       |
| VCC_SMCLK   | DDR2 Clock Supply Voltage                | 1.7   | 1.8  | 1.9   | V    | 2     |
| VCC_EXP   | SDVO, PCI Express* Supply Voltage        | 1.188 | 1.25 | 1.313 | V    |       |
| VCCA_EXP  | SDVO, PCI Express* Analog Supply Voltage | 3.135 | 3.3  | 3.465 | V    | 2     |
| VTT   | 1.2 V System Bus Input Supply Voltage    | 1.14  | 1.2  | 1.26  | V    | 4     |
|   | 1.1 V System Bus Input Supply Voltage    | 1.045 | 1.1  | 1.155 | V    |       |
| VCC   | (G)MCH Core Supply Voltage               | 1.188 | 1.25 | 1.313 | V    |       |
| VCC_CL  | Controller Supply Voltage                | 1.188 | 1.25 | 1.313 | V    |       |
| VCC3_3  | CMOS Supply Voltage                      | 3.135 | 3.3  | 3.465 | V    |       |
| VCCA_DAC  | Display DAC Analog Supply Voltage        | 3.135 | 3.3  | 3.465 | V    | 3     |
| VCCD_CRT  | Display Digital Supply Voltage           | 1.425 | 1.5  | 1.575 | V    | 1     |
| VCCDQ_CRT   | Display Quiet Digital Supply Voltage     | 1.425 | 1.5  | 1.575 | V    | 1     |
| VCCA_HPLL,<br>VCCA_EXPPLL,<br>VCCA_DPLLA,<br>VCCA_DPLLB,<br>VCCA_MPLL | Various PLLs' Analog Supply Voltages     | 1.188 | 1.25 | 1.313 | V    | 2     |

**NOTES:**

1. The VCCD\_CRT and VCCDQ\_CRT can also operate at a nominal 1.8 V  $\pm$ 5% input voltage. Only the 1.5 V nominal voltage setting will be validated internally.
2. These rails are filtered from other voltage rails on the platform and should be measured at the *input* of the filter.
3. VCCA\_DAC voltage tolerance should only be measured when the DAC is turned ON and at a stable resolution setting. Any noise on the DAC during power on or display resolution changes do not impact the circuit.
4. (G)MCH supports both VTT = 1.2 V nominal and VTT = 1.1 V nominal depending on the identified processor.



### 10.3.2 General DC Characteristics

Platform Reference Voltages at the top of Table 10-5 are specified at DC only.  $V_{REF}$  measurements should be made with respect to the supply voltage. Customers should refer to the Platform Design Guide for proper decoupling of the  $V_{REF}$  voltage dividers on the platform.

**Table 10-5. DC Characteristics**

| Symbol                              | Parameter  | Min                                | Nom                        | Max                                       | Unit    | Notes                            |
|-------------------------------------|--|------------------------------------|----------------------------|---|---------|----------------------------------|
| <b>Reference Voltages</b>           |  |                                    |                            |   |         |                                  |
| FSB_DVREF<br>FSB_ACCVREF            | Host Data, Address, and Common Clock Signal Reference Voltages | $0.666 \times V_{TT\_FSB} - 2\%$   | $0.666 \times V_{TT\_FSB}$ | $0.666 \times V_{TT\_FSB} + 2\%$          | V       |                                  |
| FSB_SWING                           | Host Compensation Reference Voltage                            | $0.25 \times V_{TT\_FSB} - 2\%$    | $0.25 \times V_{TT\_FSB}$  | $0.25 \times V_{TT\_FSB} + 2\%$           | V       |                                  |
| CL_VREF                             | Controller Link Reference Voltage                              | $0.270 \times V_{CC\_CL}$          | $0.279 \times V_{CC\_CL}$  | $0.287 \times V_{CC\_CL}$                 | V       |                                  |
| DDR_VREF                            | DDR2 Reference Voltage   | $0.49 \times SMVREF$               | $0.50 \times SMVREF$       | $0.51 \times SMVREF$                      | V       |                                  |
| <b>Host Interface</b>               |  |                                    |                            |   |         |                                  |
| $V_{IL\_H}$                         | Host GTL+ Input Low Voltage                                    | -0.10                              | 0                          | $(0.666 \times V_{TT\_FSB}) - 0.1$        | V       |                                  |
| $V_{IH\_H}$                         | Host GTL+ Input High Voltage                                   | $(0.666 \times V_{TT\_FSB}) + 0.1$ | $V_{TT\_FSB}$              | $V_{TT\_FSB} + 0.1$                       | V       |                                  |
| $V_{OL\_H}$                         | Host GTL+ Output Low Voltage                                   | —                                  | —                          | $(0.25 \times V_{TT\_FSB}) + 0.1$         | V       |                                  |
| $V_{OH\_H}$                         | Host GTL+ Output High Voltage                                  | $V_{TT\_FSB} - 0.1$                | —                          | $V_{TT\_FSB}$                             | V       |                                  |
| $I_{OL\_H}$                         | Host GTL+ Output Low Current                                   | —                                  | —                          | $V_{TT\_FSBmax} * (1 - 0.25) / R_{ttmin}$ | mA      | $R_{ttmin} = 47.5 \Omega$        |
| $I_{LEAK\_H}$                       | Host GTL+ Input Leakage Current                                | —                                  | —                          | 45  | $\mu A$ | $V_{OL} < V_{pad} < V_{tt\_FSB}$ |
| $C_{PAD}$                           | Host GTL+ Input Capacitance                                    | 2.0                                | —                          | 2.5                                       | pF      |                                  |
| $C_{PCKG}$                          | Host GTL+ Input Capacitance (common clock)                     | 0.90                               | —                          | 2.5                                       | pF      |                                  |
| <b>DDR2 System Memory Interface</b> |  |                                    |                            |   |         |                                  |
| $V_{IL(DC)}$                        | DDR2 Input Low Voltage   | —                                  | —                          | $DDR\_VREF - 0.125$                       | V       |                                  |
| $V_{IH(DC)}$                        | DDR2 Input High Voltage  | $DDR\_VREF + 0.125$                | —                          | —   | V       |                                  |



| Symbol                             | Parameter                                     | Min             | Nom   | Max             | Unit | Notes       |
|------------------------------------|---|-----------------|-------|-----------------|------|-------------|
| V <sub>IL(AC)</sub>                | DDR2 Input Low Voltage                        | —               | —     | DDR_VREF – 0.20 | V    |             |
| V <sub>IH(AC)</sub>                | DDR2 Input High Voltage                       | DDR_VREF + 0.20 | —     | —               | V    |             |
| V <sub>OL</sub>                    | DDR2 Output Low Voltage                       | —               | —     | 0.2 * VCC_DDR   | V    | 1           |
| V <sub>OH</sub>                    | DDR2 Output High Voltage                      | 0.8 * VCC_DDR   | —     | —               | V    | 1           |
| I <sub>Leak</sub>                  | Input Leakage Current                         | —               | —     | ±20             | µA   | 4           |
| I <sub>Leak</sub>                  | Input Leakage Current                         | —               | —     | ±550            | µA   | 5           |
| C <sub>I/O</sub>                   | DQ/DQS/DQSB DDR2 Input/Output Pin Capacitance | 1.0             | —     | 4.0             | pF   |             |
| <b>Input Clocks</b>                |   |                 |       |                 |      |             |
| V <sub>IL</sub>                    | Input Low Voltage                             | -0.150          | 0     | —               | V    |             |
| V <sub>IH</sub>                    | Input High Voltage                            | 0.660           | 0.710 | 0.850           | V    |             |
| V <sub>CROSS(ABS)</sub>            | Absolute Crossing Voltage                     | 0.300           | —     | 0.550           | V    | 6, 7, 8     |
| ΔV <sub>CROSS(REL)</sub>           | Range of Crossing Points                      | —               | —     | 0.140           | V    |             |
| C <sub>IN</sub>                    | Input Capacitance                             | 1               | —     | 3               | pF   |             |
| <b>SDVO_CTRLDATA, SDVO_CTRLCLK</b> |   |                 |       |                 |      |             |
| V <sub>IL</sub>                    | Input Low Voltage                             | —               | —     | 0.75            | V    |             |
| V <sub>IH</sub>                    | Input High Voltage                            | 1.75            | —     | —               | V    |             |
| I <sub>LEAK</sub>                  | Input Leakage Current                         | —               | —     | ± 10            | µA   |             |
| C <sub>IN</sub>                    | Input Capacitance                             | —               | —     | 10.0            | pF   |             |
| I <sub>OL</sub>                    | Output Low Current (CMOS Outputs)             | —               | —     | 7.8             | mA   | @ 50% swing |
| I <sub>OH</sub>                    | Output High Current (CMOS Outputs)            | -1              | —     | —               | mA   | @ 50% swing |
| V <sub>OL</sub>                    | Output Low Voltage (CMOS Outputs)             | —               | —     | 0.4             | V    |             |
| V <sub>OH</sub>                    | Output High Voltage (CMOS Outputs)            | 2.25            | —     | —               | V    |             |
| <b>CRT_DDC_DATA, CRT_DDC_CLK</b>   |   |                 |       |                 |      |             |
| V <sub>IL</sub>                    | Input Low Voltage                             | —               | —     | 0.9             | V    |             |
| V <sub>IH</sub>                    | Input High Voltage                            | 2.1             | —     | —               | V    |             |
| I <sub>LEAK</sub>                  | Input Leakage Current                         | —               | —     | ± 10            | µA   |             |
| C <sub>IN</sub>                    | Input Capacitance                             | —               | —     | 10.0            | pF   |             |
| I <sub>OL</sub>                    | Output Low Current (CMOS Outputs)             | —               | —     | 27.0            | mA   | @ 50% swing |



| Symbol                         | Parameter                          | Min   | Nom | Max   | Unit | Notes                   |
|--------------------------------|------------------------------------|-------|-----|-------|------|-------------------------|
| I <sub>OH</sub>                | Output High Current (CMOS Outputs) | -1    | —   | —     | mA   | @ 50% swing             |
| V <sub>OL</sub>                | Output Low Voltage (CMOS Outputs)  | —     | —   | 0.4   | V    |                         |
| V <sub>OH</sub>                | Output High Voltage (CMOS Outputs) | 2.7   | —   | —     | V    |                         |
| <b>CL_DATA, CL_CLK</b>         |                                    |       |     |       |      |                         |
| V <sub>IL</sub>                | Input Low Voltage                  | —     | —   | 0.277 | V    |                         |
| V <sub>IH</sub>                | Input High Voltage                 | 0.427 | —   | —     | V    |                         |
| I <sub>LEAK</sub>              | Input Leakage Current              | —     | —   | ± 20  | μA   |                         |
| C <sub>IN</sub>                | Input Capacitance                  | —     | —   | 1.5   | pF   |                         |
| I <sub>OL</sub>                | Output Low Current (CMOS Outputs)  | —     | —   | 1.0   | mA   | @V <sub>OL_HI</sub> max |
| I <sub>OH</sub>                | Output High Current (CMOS Outputs) | 6.0   | —   | —     | mA   | @V <sub>OH_HI</sub> min |
| V <sub>OL</sub>                | Output Low Voltage (CMOS Outputs)  | —     | —   | 0.06  | V    |                         |
| V <sub>OH</sub>                | Output High Voltage (CMOS Outputs) | 0.6   | —   | —     | V    |                         |
| <b>PWROK, CL_PWROK, RSTIN#</b> |                                    |       |     |       |      |                         |
| V <sub>IL</sub>                | Input Low Voltage                  | —     | —   | 0.3   | V    |                         |
| V <sub>IH</sub>                | Input High Voltage                 | 2.7   | —   | —     | V    |                         |
| I <sub>LEAK</sub>              | Input Leakage Current              | —     | —   | ±1    | mA   |                         |
| C <sub>IN</sub>                | Input Capacitance                  | —     | —   | 6.0   | pF   |                         |
| <b>CL_RST#</b>                 |                                    |       |     |       |      |                         |
| V <sub>IL</sub>                | Input Low Voltage                  | —     | —   | 0.13  | V    |                         |
| V <sub>IH</sub>                | Input High Voltage                 | 1.17  | —   | —     | V    |                         |
| I <sub>LEAK</sub>              | Input Leakage Current              | —     | —   | ±20   | μA   |                         |
| C <sub>IN</sub>                | Input Capacitance                  | —     | —   | 5.0   | pF   |                         |
| <b>ICH_SYNCB</b>               |                                    |       |     |       |      |                         |
| I <sub>OL</sub>                | Output Low Current (CMOS Outputs)  | —     | —   | 2.0   | mA   | @V <sub>OL_HI</sub> max |
| I <sub>OH</sub>                | Output High Current (CMOS Outputs) | -2.0  | —   | —     | mA   | @V <sub>OH_HI</sub> min |
| V <sub>OL</sub>                | Output Low Voltage (CMOS Outputs)  | —     | —   | 0.33  | V    |                         |
| V <sub>OH</sub>                | Output High Voltage (CMOS Outputs) | 2.97  | —   | —     | V    |                         |



| Symbol                      | Parameter                          | Min                             | Nom             | Max                             | Unit | Notes  |
|-----------------------------|------------------------------------|---------------------------------|-----------------|---------------------------------|------|--|
| <b>EXP_SLR, EXP_EN</b>      |                                    |                                 |                 |                                 |      |  |
| V <sub>IL</sub>             | Input Low Voltage                  | -0.10                           | 0               | (0.63 x V <sub>TT</sub> ) - 0.1 | V    |  |
| V <sub>IH</sub>             | Input High Voltage                 | (0.63 x V <sub>TT</sub> ) + 0.1 | V <sub>TT</sub> | V <sub>TT</sub> + 0.1           | V    |  |
| I <sub>LEAK</sub>           | Input Leakage Current              | —                               | —               | 20                              | μA   | V <sub>OL</sub> < V <sub>pad</sub> < V <sub>tt</sub> |
| C <sub>IN</sub>             | Input Capacitance                  | 2                               |                 | 2.5                             | pF   |  |
| <b>CRT_HSYNC, CRT_VSYNC</b> |                                    |                                 |                 |                                 |      |  |
| I <sub>OL</sub>             | Output Low Current (CMOS Outputs)  | —                               | —               | 8.0                             | mA   | @V <sub>OL_HI</sub> max                              |
| I <sub>OH</sub>             | Output High Current (CMOS Outputs) | -8.0                            | —               |                                 | mA   | @V <sub>OH_HI</sub> min                              |
| V <sub>OL</sub>             | Output Low Voltage (CMOS Outputs)  | —                               | —               | 0.5                             | V    |  |
| V <sub>OH</sub>             | Output High Voltage (CMOS Outputs) | 2.4                             | —               |                                 | V    |  |

**NOTES:**

1. Determined with 2x (G)MCH Buffer Strength Settings into a 50 Ω to 0.5xVCC\_DDR test load.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express\* specification and measured over any 250 consecutive TX UIs.
3. Specified at the measurement point over any 250 consecutive UIs. The test load shown in Receiver compliance eye diagram of PCI Express\* spec should be used as the RX device when taking measurements.
4. Applies to pin to VCC or VSS leakage current for the DDR\_A\_DQ\_63:0 and DDR\_B\_DQ\_63:0 signals.
5. Applies to pin to pin leakage current between DDR\_A\_DQS\_7:0, DDR\_A\_DQSB\_7:0, DDR\_B\_DQS\_7:0, and DDR\_B\_DQSB\_7:0 signals.
6. Crossing voltage defined as instantaneous voltage when rising edge of BCLK0 equals falling edge of BCLK1.
7. V<sub>Havg</sub> is the statistical average of the V<sub>H</sub> measured by the oscilloscope.
8. The crossing point must meet the absolute and relative crossing point specifications simultaneously. Refer to the appropriate processor datasheet for further information.



## 10.4 R, G, B / CRT DAC Display DC Characteristics (Intel® 82G31 GMCH Only)

Table 10-6. R, G, B / CRT DAC Display DC Characteristics: Functional Operating Range (VCCA\_DAC = 3.3 V ± 5%)

| Parameter  | Min     | Typ   | Max  | Units | Notes                               |
|--|---------|-------|------|-------|-------------------------------------|
| DAC Resolution                                   | 8       | —     | —    | Bits  | 1                                   |
| Max Luminance (full-scale)                       | 0.665   | 0.700 | 0.77 | V     | 1, 2, 4 (white video level voltage) |
| Min Luminance                                    | —       | 0.000 | —    | V     | 1, 3, 4 (black video level voltage) |
| LSB Current                                      | —       | 73.2  | —    | μA    | 4,5                                 |
| Integral Linearity (INL)                         | -1.0    | —     | +1.0 | LSB   | 1,6                                 |
| Differential Linearity (DNL)                     | -1.0    | —     | +1.0 | LSB   | 1,6                                 |
| Video channel-channel voltage amplitude mismatch | —       | —     | 6    | %     | 7                                   |
| Monotonicity                                     | Ensured |       |      | —     |                                     |

**NOTES:**

1. Measured at each R, G, B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Max steady-state amplitude
3. Min steady-state amplitude
4. Defined for a double 75 Ω termination.
5. Set by external reference resistor value.
6. INL and DNL measured and calculated according to VESA Video Signal Standards.
7. Max full-scale voltage difference among R, G, B outputs (percentage of steady-state full-scale voltage).



# 11 Ballout and Package Information

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This chapter provides the (G)MCH ballout and package information.

## 11.1 Ballout

The following three figures show the (G)MCH ballout as viewed from the top side of the package. The figures are divided into a left-side view, middle view, and right-side view of the package. Table 11-1 lists the ballout alphabetically by signal name.

**Note:** Notes for Figure 11-1, Figure 11-2, Figure 11-3, and Table 11-1.

1. Some balls marked as RSVD (Reserved) are used in XOR testing. See Chapter 12 for details.
2. Balls that are listed as NC are No Connects.
3. Analog Display Signals (CRT\_RED, CRT\_REDB, CRT\_GREEN, CRT\_GREENB, CRT\_BLUE, CRT\_BLUEB, CRT\_IREF, CRT\_HSYNC, CRT\_VSYNC, CRT\_DDC\_CLK, CRT\_DDC\_DATA) and the SDVO\_CTRLCLK and SDVO\_CTRLDATA signals are not used on the 82P31 MCH. Contact your Intel field representative for proper termination of the corresponding balls.
4. For the 82G31 GMCH, the PCI Express and SDVO signals are multiplexed. However, only the PCI Express signal name is included in the following ballout figures and table. See Section 2.7 for the PCI Express to SDVO signal name mapping.



Figure 11-1. (G)MCH Ballout Diagram (Top View Left – Columns 43–30)

|    | 43        | 42        | 41        | 40       | 39       | 38       | 37       | 36       | 35       | 34       | 33       | 32       | 31       | 30      |    |
|----|-----------|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|---------|----|
| BC | TEST0     | NC        | VSS       |          | VCCSM    |          |          |          |          | VCCSM    |          | VSS      |          | VCCSM   | BC |
| BB | NC        | VCC_SMCLK | VCC_SMCLK | SRCOMP2  | VCCSM    | RSVD     | VCCSM    |          | RSVD     | SWE_A#   | SRAS_A#  | VCCSM    | RSVD     | SCS_B1# | BB |
| BA | VCC_SMCLK | VCC_SMCLK |           | SRCOMP3  | RSVD     | SODT_A1  |          |          | SCS_A1#  | RSVD     | SBS_A0   |          | SMA_A0   | SODT_B1 | BA |
| AY |           | VCC_SMCLK | VSS       | VSS      |          | SMA_A13  | SODT_A0  |          | SCAS_A#  |          | SMA_A10  | VCCSM    | RSVD     |         | AY |
| AW | VSS       | RSVD      | VSS       |          | SDQS_B4  |          | SDQ_B32  |          | SCS_A0#  |          | SCLK_A2# | SBS_A1   | SCLK_B0# |         | AW |
| AV |           | SDQ_A32   | SDQ_A37   | SDQ_A36  |          | SDQ_B33  | VSS      |          | VSS      |          | SCLK_A2  | SCLK_B2  | SCLK_B0  |         | AV |
| AU | SDM_A4    | VSS       |           | SDQ_A33  | SDQS_B4# | VSS      | SDM_B4   |          | SDQ_B36  |          | RSVD     | VSS      | SCLK_A0  |         | AU |
| AT |           |           |           |          |          |          |          |          |          |          | RSVD     | SCLK_B2# | VSS      |         | AT |
| AR |           | SDQ_A38   | SDQS_A4   | SDQS_A4# | SDQ_B44  | VSS      | SDQ_B39  |          | SDQ_B37  |          | VSS      | VSS      | SCLK_A0# |         | AR |
| AP | VSS       | SDQ_A34   | SDQ_A39   |          |          |          |          |          |          |          |          | RSVD     | RSVD     |         | AP |
| AN |           | SDQ_A45   | SDQ_A40   | SDQ_A44  | SDQ_A35  | VSS      | SDQ_B35  | SDQ_B34  | SDQ_B38  |          | RSVD     | RSVD     | VSS      |         | AN |
| AM | SDM_A5    | VSS       |           | VSS      | SDQ_A41  | SDQ_B41  | SDM_B5   | VSS      | SDQ_B40  | SDQ_B45  | VSS      |          | RSVD     |         | AM |
| AL |           | SDQ_A46   | SDQS_A5   | SDQS_A5# | SDQ_A47  | SDQ_B43  | SDQ_B46  | VSS      | SDQS_B5  | SDQS_B5# | VSS      | SDQ_B47  | RSVD     |         | AL |
| AK | VSS       | SDQ_A42   | SDQ_A43   |          |          |          |          |          |          |          |          |          |          | VCC2    | AK |
| AJ |           | SDQ_A52   | SDQ_A53   | SDQ_A48  | VSS      | SDQ_B49  | SDQ_B52  | VSS      | SDQ_B53  | SDQ_B42  | VSS      | RSVD     | VCC2     | VCC2    | AJ |
| AH | SDQ_A49   | VSS       |           |          |          |          |          |          |          |          |          |          |          |         | AH |
| AG |           | SDQS_A6   | SDQS_A6#  | SDM_A6   | SDM_B6   | SDQ_B48  | VSS      | SDQS_B6# | SDQS_B6  | VSS      | SDQ_B54  | RSVD     | VCC2     | VCC2    | AG |
| AF | VSS       | SDQ_A55   | SDQ_A54   |          | SDQ_A50  | SDQ_B61  | VSS      | VSS      | SDQ_B50  | SDQ_B55  | SDQ_B51  | RSVD     | VCC2     | VCC2    | AF |
| AE |           | SDQ_A60   | SDQ_A61   | SDQ_A51  |          |          |          |          |          |          |          |          |          |         | AE |
| AD | SDQ_A57   | VSS       |           | SDQ_A56  | VSS      | SDM_B7   | VSS      | SDQ_B56  | VSS      | SDQ_B60  | VSS      | VCC2     | VCC2     | VCC2    | AD |
| AC |           | SDQS_A7   | SDQS_A7#  | SDM_A7   | SDQ_A62  | VSS      | SDQS_B7# | SDQS_B7  | VSS      | SDQ_B62  | SDQ_B57  | VCC2     | VCC2     | VCC     | AC |
| AB | VSS       | SDQ_A63   | SDQ_A58   |          |          |          |          |          |          |          |          |          |          |         | AB |
| AA |           | HBREQ0#   | HRS1#     | SDQ_A59  | RSVD     | VSS      | HA35#    | SDQ_B59  | VSS      | SDQ_B58  | SDQ_B63  | VCC2     | VCC2     | VCC2    | AA |
| Y  | HHITM#    | VSS       |           | HTRDY#   | HA34#    | HA33#    | VSS      | HA32#    | VSS      | HA29#    | VSS      | VCC2     | VCC2     | VCC2    | Y  |
| W  |           | HBNR#     | HDRDY#    | HADS#    |          |          |          |          |          |          |          |          |          |         | W  |
| V  | VSS       | HA30#     | HLOCK#    |          | VSS      | HA31#    | VSS      | HA22#    | HA28#    | VSS      | HA27#    | VSS      | RSVD     | VCC2    | V  |
| U  |           | HHIT#     | HRS0#     | HDBSY#   | HRS2#    | VSS      | HA17#    | HA24#    | VSS      | HADSTB1# | HA25#    | HCLKN    | RSVD     | RSVD    | U  |
| T  | HDEFER#   | VSS       |           |          |          |          |          |          |          |          |          |          |          |         | T  |
| R  |           | HD4#      | HD2#      | HDO#     | HA21#    | HA23#    | HA19#    | VSS      | HA26#    | HA14#    | VSS      | HCLKP    | VSS      | RSVD    | R  |
| P  | VSS       | HA20#     | HD1#      |          |          |          |          |          |          |          |          |          |          | VSS     | P  |
| N  |           | HD7#      | HD6#      | HD3#     | HA18#    | HA16#    | HA12#    | VSS      | HA15#    | HA10#    | VSS      | HA9#     | VSS      |         | N  |
| M  | HDSTBN0#  | VSS       |           | HDINV0#  | HD5#     | HA11#    | VSS      | HA13#    | VSS      | HADSTB0# | VSS      |          | HD34#    |         | M  |
| L  |           | HD10#     | HD8#      | HDSTBPO# | HA4#     | HREQ2#   | HA6#     | HA7#     | HREQ1#   |          | VSS      | VSS      |          |         | L  |
| K  | VSS       | HA8#      | HD12#     |          |          |          |          |          |          |          |          | HD29#    | HD36#    |         | K  |
| J  |           | HA3#      | HD11#     | HA5#     | HD9#     | VSS      | HREQ4#   |          | VSS      |          | HDINV1#  | VSS      | HD32#    |         | J  |
| H  |           |           |           |          |          |          |          |          |          |          | HDSTBN1# | HD30#    | VSS      |         | H  |
| G  | HREQ3#    | VSS       |           | HD13#    | HBPRI#   | VSS      | HD19#    |          | HDSTBP1# |          | HD25#    | VSS      | HD37#    |         | G  |
| F  |           | HD15#     | HD14#     | HREQ0#   |          | HD18#    | VSS      |          | VSS      |          | HD27#    | HD33#    | HD39#    |         | F  |
| E  | VSS       | HD20#     | HD50#     |          | HD21#    |          | HD22#    |          | HD28#    |          | HDINV3#  | VSS      | HD35#    |         | E  |
| D  |           | HD52#     | HD17#     | VSS      |          | HDSTBN3# | HD57#    |          | HD54#    |          | HD59#    | HD63#    | VSS      |         | D  |
| C  | VSS       | HD16#     |           | HD53#    | HD23#    | HD56#    |          |          | HD49#    | HD60#    | HD48#    |          | HCPURST# | VTT     | C  |
| B  | NC        | NC        | HD51#     | HD55#    | HD24#    | HDSTBP3# | VSS      |          | HD61#    | HD31#    | HD58#    | VSS      | VSS      | VTT     | B  |
| A  | TEST2     | NC        | VSS       |          | VSS      |          | HD26#    |          |          | VSS      |          | HD62#    |          | VTT     | A  |



Figure 11-2. (G)MCH Ballout Diagram (Top View Middle – Columns 29–15)

|    | 29      | 28    | 27       | 26       | 25      | 24            | 23            | 22             | 21           | 20       | 19     | 18       | 17                | 16            | 15              |    |
|----|---------|-------|----------|----------|---------|---------------|---------------|----------------|--------------|----------|--------|----------|-------------------|---------------|-----------------|----|
| BC |         | VSS   |          | VCCSM    |         | VSS           |               | VCCSM          |              | SCKE_A0  |        | VCCSM    |                   | SMA_B3        |                 | BC |
| BB | RSVD    | VCCSM | SCS_B0#  | VCCSM    | SMA_A1  | VCCSM         | SMA_A8        | SMA_A11        | SBS_A2       | VCCSM    | RSVD   | VCCSM    | SMA_B0            | VCCSM         | SMA_B6          | BB |
| BA | SODT_B0 |       | SWE_B#   | SMA_A2   | SMA_A3  |               | SMA_A5        | SMA_A9         | SMA_A14      |          | RSVD   | SBS_B1   | SMA_B2            |               | SMA_B5          | BA |
| AY | SMA_B13 |       | RSVD     |          | SMA_A4  | SMA_A6        | SMA_A7        |                | RSVD         | SCKE_A1  | SBS_B0 |          | SMA_B1            |               | SMA_B8          | AY |
| AW | SCAS_B# |       | RSVD     | SRAS_B#  |         | VCCSM         | SDQ_B29       |                | SMA_A12      | VCCSM    |        | SMA_B10  | SDQ_B23           |               | SMA_B4          | AW |
| AV | RSVD    |       | VSS      | VCCSM    |         | SDQ_B24       | VSS           |                | VSS          | SDQ_A31  |        | VCCSM    | VSS               |               | SDQ_B22         | AV |
| AU | RSVD    |       | SCLK_B1  | SDQS_B3# |         | VSS           | SDQ_B28       |                | SDQ_A26      | VSS      |        | SDQS_A3# | SDQ_B18           |               | SDQ_B16         | AU |
| AT | VSS     |       | SCLK_B1# | SDQ_B26  |         | SDQS_B3       | SDQ_B25       |                | SDQ_A27      | SDQS_A3  |        | SDQ_A24  | SDQ_B19           |               | VSS             | AT |
| AR | RSVD    |       | VSS      | VSS      |         | SDQ_B30       | VSS           |                | VSS          | VSS      |        | SDQ_A25  | VSS               |               | SDQS_B2#        | AR |
| AP | RSVD    |       | SCLK_A1  | SDQ_B27  |         | VSS           | SDM_B3        |                | RSVD         | SDQ_A30  |        | VSS      | SDQ_A28           |               | SDQS_B2         | AP |
| AN | VSS     |       | SCLK_A1# | SDQ_B31  |         | VSS           | VSS           |                | RSVD         | VSS      |        | SDM_A3   | SDQ_A29           |               | VSS             | AN |
| AM | VSS     |       | RSVD     | RSVD     |         | VSS           | VSS           |                | RSVD         | VSS      |        | RSTIN#   | PWROK             |               | PWROK2          | AM |
| AL | VCC2    |       | VCC2     | VCC2     |         | VCC2          | VCC2          |                | VCC2         | VCC2     |        | VCC2     | VCC2              |               | VCC2            | AL |
| AK | VCC2    |       | VCC2     | VCC2     |         | VCC2          | VCC2          |                | VCC2         | VCC2     |        | VCC2     | VCC2              |               | VCC2            | AK |
| AJ | VCC2    |       | VCC2     | VCC2     |         | VCC2          | VCC2          |                | VCC2         | VCC2     |        | VCC2     | VCC2              |               | VCC2            | AJ |
| AH |         |       |          |          |         |               |               |                |              |          |        |          |                   |               |                 | AH |
| AG | VCC2    |       | VCC2     | VCC2     | VCC     | VCC           | VCC           | VCC            | VCC          | VCC      | VCC    | VCC      | VCC               |               | VCC             | AG |
| AF | VCC2    |       | VCC2     | VCC      | VCC     | VCC           | VSS           | VCC            | VSS          | VCC      | VSS    | VCC      | VCC               |               | VCC             | AF |
| AE |         |       | VCC      | VCC      | VCC     | VSS           | VCC           | VSS            | VCC          | VSS      | VCC    | VSS      | VCC               |               |                 | AE |
| AD | VCC2    |       | VCC      | VCC      | VSS     | VCC           | VSS           | VCC            | VSS          | VCC      | VSS    | VCC      | VCC               |               | VCC             | AD |
| AC | VCC2    |       | VCC      | VCC      | VCC     | VSS           | VCC           | VSS            | VCC          | VSS      | VCC    | VSS      | VCC               |               | VCC             | AC |
| AB |         |       | VCC      | VCC      | VSS     | VCC           | VSS           | VCC            | VSS          | VCC      | VSS    | VCC      | VCC               |               |                 | AB |
| AA | VCC2    |       | VCC      | VCC      | VCC     | VSS           | VCC           | VSS            | VCC          | VSS      | VCC    | VSS      | VCC               |               | VCC             | AA |
| Y  | VCC2    |       | VCC      | VCC      | VSS     | VCC           | VSS           | VCC            | VSS          | VCC      | VSS    | VCC      | VCC               |               | VCC             | Y  |
| W  |         |       | VCC      | VCC      | VCC     | VSS           | VCC           | VSS            | VCC          | VSS      | VCC    | VCC      | VCC               |               |                 | W  |
| V  | VCC2    |       | VCC      | VCC      | VCC     | VCC           | VCC           | VCC            | VCC          | VCC      | VCC    | VCC      | VCC               |               | VCC             | V  |
| U  | VCC2    |       | VCC2     | VCC      | VCC     | VCC           | VCC           | VCC            | VCC          | VCC      | VCC    | VCC      | VCC               |               | VCC             | U  |
| T  |         |       |          |          |         |               |               |                |              |          |        |          |                   |               |                 | T  |
| R  | RSVD    |       | VTT      | VTT      |         | VTT           | VTT           |                | VSS          | VCC      |        | VCC      | VCC               |               | VCC             | R  |
| P  | VTT     |       | VTT      | VTT      |         | VTT           | VTT           |                | VSS          | VCC      |        | VSS      | VSS               |               | VCC             | P  |
| N  | VTT     |       | VSS      | VTT      |         | VTT           | VTT           |                | VSS          | NC       |        | RSVD     | RSVD              |               | RSVD            | N  |
| M  | VTT     |       | VSS      | HD47#    |         | VTT           | VTT           |                | VSS          | RSVD     |        | RSVD     | VSS               |               | VSS             | M  |
| L  | VSS     |       | HD42#    | HD45#    |         | VTT           | VTT           |                | VSS          | VSS      |        | RSVD     | RSVD              |               | RSVD            | L  |
| K  | HD38#   |       | HD43#    | VSS      |         | VTT           | VTT           |                | VSS          | ALLZTEST |        | VSS      | RSVD              |               | EXP_RXP1        | K  |
| J  | HD40#   |       | VSS      | HD46#    |         | VTT           | VTT           |                | VSS          | BSEL1    |        | BSEL2    | EXP_EN            |               | EXP_RXN1        | J  |
| H  | VSS     |       | HDSTBN2# | HD44#    |         | VTT           | VTT           |                | VSS          | VSS      |        | RSVD     | VSS               |               | VSS             | H  |
| G  | HDINV2# |       | HDSTBP2# | VTT      |         | VTT           | VTT           |                | VSS          | BSEL0    |        | RSVD     | SDVO_CT<br>RLDATA |               | EXP_RXN0        | G  |
| F  | HD41#   |       | VSS      | VTT      |         | VTT           | VTT           |                | VSS          | XORTEST  |        | VSS      | RSVD              |               | EXP_RXP0        | F  |
| E  | VTT     |       | VTT      | VTT      |         | VSS           | VTT           |                | VSS          | VSS      |        | EXP_SLR  | SDVO_CT<br>RLCLK  |               | VSS             | E  |
| D  | VTT     | VTT   | VTT      |          | HSCOMP# | HDVREF        | HRCOMP        |                | VSS          | BLUE#    | GREEN# |          | VSS               | VSS           | VSYNC           | D  |
| C  | VTT     |       | VTT      | VSS      | HSCOMP  |               | VCCA_HP<br>LL | VCCA_DP<br>LLB | VCCD_C<br>RT |          | GREEN  | RED#     | VCCA_D<br>A_C     |               | HSYNC           | C  |
| B  | VTT     | VTT   | VTT      | VSS      | HSWING  | HACCVRE<br>F  | VSS           | VSS            | VCCD_C<br>RT | BLUE     | VSS    | RED      | VCC3_3            | VCCA_D<br>A_C | VCCA_EX<br>PPLL | B  |
| A  |         | VTT   |          | VSS      |         | VCCA_MP<br>LL |               | VCCA_DP<br>LLA |              | REFSET   |        | VSS      |                   | VCCA_EX<br>P  |                 | A  |



Figure 11-3. (G)MCH Ballout Diagram (Top View Right – Columns 14–0)

|    | 14     | 13         | 12              | 11         | 10          | 9          | 8           | 7          | 6          | 5          | 4          | 3          | 2          | 1          |     |
|----|--------|------------|-----------------|------------|-------------|------------|-------------|------------|------------|------------|------------|------------|------------|------------|-----|
| BC | VCCSM  |            | SBS_B2          |            | VSS         |            |             | SDQ_A17    |            | VSS        |            | VSS        | NC         | TEST1      | BC  |
| BB | SMA_B9 | SMA_B11    | VCCSM           | RSVD       | SDQ_A23     | SDQS_A2    |             | VSS        | SDQ_A20    | SDQ_A10    | SDQ_A15    | SDQS_A1    | RSVD       | NC         | BB  |
| BA | SMA_B7 | SMA_B12    |                 | RSVD       | SDQ_A22     | SDQS_A2#   |             |            | SDQ_A21    | SDQ_A14    | SDQS_A1#   |            | SDM_A1     | VSS        | BA  |
| AY |        | SMA_B14    | SCKE_B0         | SDQ_A19    |             | SDM_A2     |             | SDQ_A16    | SDQ_A11    |            | VSS        | SDQ_A9     | SDQ_A8     |            | AY  |
| AW |        | SDM_B2     | SCKE_B1         | SDQ_A18    |             | SDM_B1     |             | SDQ_B3     |            |            | SDQ_B2     |            | SDQ_A13    | SDQ_A12    | VSS |
| AV |        | SDQ_B17    | SDQ_B14         | VSS        |             | VSS        |             | VSS        | SDQS_B0    |            | SDQ_A7     | SDQ_A2     | SDQ_A3     |            | AV  |
| AU |        | SDQ_B20    | SDQ_B15         | SDQ_B9     |             | SDQ_B13    |             | SDQ_B7     | VSS        | SDQS_B0#   | SDQS_A0    |            | VSS        | SDQ_A6     | AU  |
| AT |        | VSS        | VSS             | SDQ_B8     |             |            |             |            |            |            |            |            |            |            | AT  |
| AR |        | SDQ_B11    | SDQS_B1         | SDQ_B12    |             | VSS        |             | SDM_B0     | VSS        | SDQ_A0     | SDQ_A1     | SDQS_A0#   | SDM_A0     |            | AR  |
| AP |        | SDQ_B10    | SDQS_B1#        |            |             |            |             |            |            |            |            | SDQ_A4     | SDQ_A5     | VSS        | AP  |
| AN |        | VSS        | VSS             | VSS        |             | SDQ_B6     | SDQ_B1      | SDQ_B0     | SDQ_B5     | SDQ_B4     | VSS        | SRCOMP1    | SRCOMP0    |            | AN  |
| AM |        | SDQ_B21    |                 | VSS        | SMRCOMP VOH | VSS        | SMRCOMP VOL | VSS        | SVREF      | VREF2      | VSS        |            | VSS        | VSS        | AM  |
| AL |        | VCC2       | VCC2            | VCC2       | VCC2        | VCC2       | VCC2        | VCC2       | VCC2       | VCC2       | VCC2       | VCC2       | VCC2       | VCC2       | AL  |
| AK | VCC2   |            |                 |            |             |            |             |            |            |            |            | VCC2       | VCC2       | VCC2       | AK  |
| AJ | VCC2   | VCC2       | VCC             | VCC        | VCC         | VCC        | VCC         | VCC        | VCC        | VCC        | VCC        | VCC        | VCC        | VCC        | AJ  |
| AH |        |            |                 |            |             |            |             |            |            |            | VCC        |            | VCC        | VCC        | AH  |
| AG | VCC    | VCC        | VCC             | VCC        | VCC         | VCC        | VCC         | VCC        | VCC        | VCC        | VCC        | VCC        | VCC        | VCC        | AG  |
| AF | VCC    | VCC        | VCC             | VCC        | VSS         | VSS        | VSS         | VSS        | VSS        | VSS        |            | VSS        | VSS        | VSS        | AF  |
| AE |        |            |                 |            |             |            |             |            |            |            | VCC_EXP    | VCC_EXP    | VCC_EXP    |            | AE  |
| AD | VCC    | RSVD       | RSVD            | VCC_EXP    | VCC_EXP     | VCC_EXP    | VCC_EXP     | VCC_EXP    | VCC_EXP    | VCC_EXP    | VCC_EXP    |            | VCC_EXP    | VCC_EXP    | AD  |
| AC | VCC    | VCC        | EXP_COMP I      | EXP_COMP O | VSS         | DML_TXN2   | DML_TXP2    | VSS        | VCC        | VSS        | VCC_EXP    | VCC_EXP    | VCC_EXP    |            | AC  |
| AB |        |            |                 |            |             |            |             |            |            |            |            | DML_RXP3   | VSS        | VSS        | AB  |
| AA | VCC    | VCC        | V_1P25_PL TRST# | RSVD       | RSVD        | RSVD       | VSS         | DML_RXP2   | DML_RXN2   | VSS        | DML_RXN3   | VCC        | DML_TXN3   |            | AA  |
| Y  | VCC    | VCC        | RSVD            | VCC        | VSS         | DML_RXN1   | DML_RXP1    | VSS        | VCC        | VSS        | DML_TXN1   |            | DML_TXP3   | VSS        | Y   |
| W  |        |            |                 |            |             |            |             |            |            |            | DML_TXP1   | VSS        | DML_RXP0   |            | W   |
| V  | VCC    | VCC        | VCC             | VSS        | VCC         | VCC        | VSS         | DML_TXP0   | DML_TXN0   | VSS        |            | EXP_TXP1 5 | VSS        | DML_RXN0   | V   |
| U  | VCC    | VCC        | RSVD            | RSVD       | VCC         | VCC        | VSS         | VSS        | VCC        | VSS        | EXP_TXN1 5 | VCC        | EXP_TXP1 4 |            | U   |
| T  |        |            |                 |            |             |            |             |            |            |            | EXP_TXP1 4 |            | EXP_TXN1 4 | VSS        | T   |
| R  | VCC    | RSVD       | RSVD            | VSS        | EXP_RXN1 3  | EXP_RXP1 3 | VSS         | EXP_RXN1 5 | EXP_RXP1 5 | VSS        | EXP_RXN1 4 | VSS        | EXP_TXP1 3 |            | R   |
| P  | VCC    |            |                 |            |             |            |             |            |            |            |            | EXP_TXP1 2 | VSS        | EXP_TXN1 3 | P   |
| N  |        | VSS        | VCC             | VCC        | VSS         | VCC        | VCC         | VSS        | VCC        | VSS        | EXP_TXN1 2 | VCC        | EXP_TXP1 1 |            | N   |
| M  |        | DDC_CLK    |                 | VSS        | VSS         | EXP_RXN1 0 | EXP_RXP1 0  | VSS        | EXP_RXN1 2 | EXP_RXP1 2 | EXP_RXP1 1 |            | EXP_TXN1 1 | VSS        | M   |
| L  |        | DDC_DATA   | VCC             | VSS        |             | EXP_RXP9   | EXP_RXN9    | VSS        | VCC        | VSS        | EXP_RXN1 1 | VSS        | EXP_TXP1 0 |            | L   |
| K  |        | VSS        | VSS             |            |             |            |             |            |            |            |            | EXP_TXN9   | VSS        | EXP_TXN1 0 | K   |
| J  |        | ICH_SYNC # | EXP_RXP3        | EXP_RXP4   |             | VSS        |             | VSS        | VCC        | VSS        | EXP_TXP9   | VCC        | VCC        |            | J   |
| H  |        | VSS        | EXP_RXN3        | EXP_RXN4   |             |            |             |            |            |            |            |            |            |            | H   |
| G  |        | VSS        | VSS             | VSS        |             | VSS        |             | VSS        | EXP_RXP8   | EXP_RXN8   | EXP_TXN8   |            | VCC        | VSS        | G   |
| F  |        | RSVD       | EXP_RXP2        | VCC        |             | VCC        |             | EXP_RXP5   | EXP_RXN6   |            | EXP_TXP8   | VSS        | EXP_TXP7   |            | F   |
| E  |        | VSS        | EXP_RXN2        | VSS        |             | VSS        |             | EXP_RXN5   |            | EXP_RXP6   |            | VSS        | EXP_TXN7   | VSS        | E   |
| D  |        | DREFCLKN   | EXP_TXN0        | EXP_TXP0   |             | EXP_TXN2   |             | EXP_TXP4   | EXP_TXN4   |            | VCC        | VSS        | EXP_TXN7   |            | D   |
| C  |        | DREFCLKP   | VCC             | VSS        | EXP_TXP2    | VCC        |             |            | VSS        | VSS        | VSS        |            | EXP_RXP7   | VSS        | C   |
| B  |        | VSS        | GCLKN           | GCLKP      | EXP_TXP1    | VSS        | EXP_TXP3    |            | EXP_TXN3   | EXP_TXN5   | EXP_TXP5   | EXP_TXN6   | EXP_TXP6   | NC         | B   |
| A  |        | RSVD       | VSS             |            | EXP_TXN1    |            |             | VSS        |            | VSS        |            | VSS        |            |            | A   |



Table 11-1. (G)MCH Ballout Sorted by Signal Name

| Signal Name | Ball # | Signal Name | Ball # | Signal Name | Ball # |
|-------------|--------|-------------|--------|-------------|--------|
| ALLZTEST    | K20    | EXP_RXN9    | L8     | EXP_TXN14   | T2     |
| BLUE        | B20    | EXP_RXN10   | M9     | EXP_TXN15   | U4     |
| BLUE#       | D20    | EXP_RXN11   | L4     | EXP_TXP0    | D11    |
| BSEL0       | G20    | EXP_RXN12   | M6     | EXP_TXP1    | B11    |
| BSEL1       | J20    | EXP_RXN13   | R10    | EXP_TXP2    | C10    |
| BSEL2       | J18    | EXP_RXN14   | R4     | EXP_TXP3    | B9     |
| DDC_CLK     | M13    | EXP_RXN15   | R7     | EXP_TXP4    | D7     |
| DDC_DATA    | L13    | EXP_RXP0    | F15    | EXP_TXP5    | B5     |
| DMI_RXN0    | V1     | EXP_RXP1    | K15    | EXP_TXP6    | B3     |
| DMI_RXN1    | Y9     | EXP_RXP2    | F12    | EXP_TXP7    | F2     |
| DMI_RXN2    | AA6    | EXP_RXP3    | J12    | EXP_TXP8    | F4     |
| DMI_RXN3    | AA4    | EXP_RXP4    | J11    | EXP_TXP9    | J4     |
| DMI_RXP0    | W2     | EXP_RXP5    | F7     | EXP_TXP10   | L2     |
| DMI_RXP1    | Y8     | EXP_RXP6    | E5     | EXP_TXP11   | N2     |
| DMI_RXP2    | AA7    | EXP_RXP7    | C2     | EXP_TXP12   | P3     |
| DMI_RXP3    | AB3    | EXP_RXP8    | G6     | EXP_TXP13   | R2     |
| DMI_TXN0    | V6     | EXP_RXP9    | L9     | EXP_TXP14   | U2     |
| DMI_TXN1    | Y4     | EXP_RXP10   | M8     | EXP_TXP15   | V3     |
| DMI_TXN2    | AC9    | EXP_RXP11   | M4     | GCLKN       | B13    |
| DMI_TXN3    | AA2    | EXP_RXP12   | M5     | GCLKP       | B12    |
| DMI_TXP0    | V7     | EXP_RXP13   | R9     | GREEN       | C19    |
| DMI_TXP1    | W4     | EXP_RXP14   | T4     | GREEN#      | D19    |
| DMI_TXP2    | AC8    | EXP_RXP15   | R6     | HA3#        | J42    |
| DMI_TXP3    | Y2     | EXP_SLR     | E18    | HA4#        | L39    |
| DREFCLKN    | D13    | EXP_TXN0    | D12    | HA5#        | J40    |
| DREFCLKP    | C14    | EXP_TXN1    | A10    | HA6#        | L37    |
| EXP_COMPI   | AC12   | EXP_TXN2    | D9     | HA7#        | L36    |
| EXP_COMPO   | AC11   | EXP_TXN3    | B7     | HA8#        | K42    |
| EXP_EN      | J17    | EXP_TXN4    | D6     | HA9#        | N32    |
| EXP_RXN0    | G15    | EXP_TXN5    | B6     | HA10#       | N34    |
| EXP_RXN1    | J15    | EXP_TXN6    | B4     | HA11#       | M38    |
| EXP_RXN2    | E12    | EXP_TXN7    | E2     | HA12#       | N37    |
| EXP_RXN3    | H12    | EXP_TXN8    | G4     | HA13#       | M36    |
| EXP_RXN4    | H11    | EXP_TXN9    | K3     | HA14#       | R34    |
| EXP_RXN5    | E7     | EXP_TXN10   | K1     | HA15#       | N35    |
| EXP_RXN6    | F6     | EXP_TXN11   | M2     | HA16#       | N38    |
| EXP_RXN7    | D2     | EXP_TXN12   | N4     | HA17#       | U37    |
| EXP_RXN8    | G5     | EXP_TXN13   | P1     | HA18#       | N39    |



*Ballout and Package Information*

| Signal Name | Ball # |
|-------------|--------|
| HA19#       | R37    |
| HA20#       | P42    |
| HA21#       | R39    |
| HA22#       | V36    |
| HA23#       | R38    |
| HA24#       | U36    |
| HA25#       | U33    |
| HA26#       | R35    |
| HA27#       | V33    |
| HA28#       | V35    |
| HA29#       | Y34    |
| HA30#       | V42    |
| HA31#       | V38    |
| HA32#       | Y36    |
| HA33#       | Y38    |
| HA34#       | Y39    |
| HA35#       | AA37   |
| HACCVREF    | B24    |
| HADS#       | W40    |
| HADSTB0#    | M34    |
| HADSTB1#    | U34    |
| HBNR#       | W42    |
| HBPRI#      | G39    |
| HBREQ0#     | AA42   |
| HCLKN       | U32    |
| HCLKP       | R32    |
| HCPURST#    | C31    |
| HD0#        | R40    |
| HD1#        | P41    |
| HD2#        | R41    |
| HD3#        | N40    |
| HD4#        | R42    |
| HD5#        | M39    |
| HD6#        | N41    |
| HD7#        | N42    |
| HD8#        | L41    |
| HD9#        | J39    |
| HD10#       | L42    |
| HD11#       | J41    |

| Signal Name | Ball # |
|-------------|--------|
| HD12#       | K41    |
| HD13#       | G40    |
| HD14#       | F41    |
| HD15#       | F42    |
| HD16#       | C42    |
| HD17#       | D41    |
| HD18#       | F38    |
| HD19#       | G37    |
| HD20#       | E42    |
| HD21#       | E39    |
| HD22#       | E37    |
| HD23#       | C39    |
| HD24#       | B39    |
| HD25#       | G33    |
| HD26#       | A37    |
| HD27#       | F33    |
| HD28#       | E35    |
| HD29#       | K32    |
| HD30#       | H32    |
| HD31#       | B34    |
| HD32#       | J31    |
| HD33#       | F32    |
| HD34#       | M31    |
| HD35#       | E31    |
| HD36#       | K31    |
| HD37#       | G31    |
| HD38#       | K29    |
| HD39#       | F31    |
| HD40#       | J29    |
| HD41#       | F29    |
| HD42#       | L27    |
| HD43#       | K27    |
| HD44#       | H26    |
| HD45#       | L26    |
| HD46#       | J26    |
| HD47#       | M26    |
| HD48#       | C33    |
| HD49#       | C35    |
| HD50#       | E41    |

| Signal Name | Ball # |
|-------------|--------|
| HD51#       | B41    |
| HD52#       | D42    |
| HD53#       | C40    |
| HD54#       | D35    |
| HD55#       | B40    |
| HD56#       | C38    |
| HD57#       | D37    |
| HD58#       | B33    |
| HD59#       | D33    |
| HD60#       | C34    |
| HD61#       | B35    |
| HD62#       | A32    |
| HD63#       | D32    |
| HDBSY#      | U40    |
| HDEFER#     | T43    |
| HDINV0#     | M40    |
| HDINV1#     | J33    |
| HDINV2#     | G29    |
| HDINV3#     | E33    |
| HDRDY#      | W41    |
| HDSTBN0#    | M43    |
| HDSTBN1#    | H33    |
| HDSTBN2#    | H27    |
| HDSTBN3#    | D38    |
| HDSTBP0#    | L40    |
| HDSTBP1#    | G35    |
| HDSTBP2#    | G27    |
| HDSTBP3#    | B38    |
| HDVREF      | D24    |
| HHIT#       | U42    |
| HHITM#      | Y43    |
| HLOCK#      | V41    |
| HRCOMP      | D23    |
| HREQ0#      | F40    |
| HREQ1#      | L35    |
| HREQ2#      | L38    |
| HREQ3#      | G43    |
| HREQ4#      | J37    |
| HRS0#       | U41    |



| Signal Name | Ball # |
|-------------|--------|
| HRS1#       | AA41   |
| HRS2#       | U39    |
| HSCOMP      | C25    |
| HSCOMP#     | D25    |
| HSWING      | B25    |
| HSYNC       | C15    |
| HTRDY#      | Y40    |
| ICH_SYNC#   | J13    |
| NC          | BC42   |
| NC          | BC2    |
| NC          | BB43   |
| NC          | BB1    |
| NC          | B43    |
| NC          | B42    |
| NC          | B2     |
| NC          | N20    |
| NC          | A42    |
| PWROK       | AM17   |
| PWROK2      | AM15   |
| RED         | B18    |
| RED#        | C18    |
| REFSET      | A20    |
| RSVD        | AJ32   |
| RSVD        | V31    |
| RSVD        | AL31   |
| RSVD        | A14    |
| RSVD        | F13    |
| RSVD        | F17    |
| RSVD        | H18    |
| RSVD        | K17    |
| RSVD        | G18    |
| RSVD        | M18    |
| RSVD        | L18    |
| RSVD        | L15    |
| RSVD        | M20    |
| RSVD        | N15    |
| RSVD        | N18    |
| RSVD        | N17    |
| RSVD        | L17    |

| Signal Name | Ball # |
|-------------|--------|
| RSVD        | AD12   |
| RSVD        | AD13   |
| RSVD        | Y12    |
| RSVD        | AA9    |
| RSVD        | AA10   |
| RSVD        | AA11   |
| RSVD        | R29    |
| RSVD        | R30    |
| RSVD        | U30    |
| RSVD        | U31    |
| RSVD        | R13    |
| RSVD        | R12    |
| RSVD        | U11    |
| RSVD        | U12    |
| RSVD        | AA39   |
| RSVD        | AP21   |
| RSVD        | AW42   |
| RSVD        | BB2    |
| RSVD        | AF32   |
| RSVD        | AG32   |
| RSVD        | BB19   |
| RSVD        | AM21   |
| RSVD        | BB31   |
| RSVD        | BB29   |
| RSVD        | AY31   |
| RSVD        | AY27   |
| RSVD        | BA11   |
| RSVD        | BB11   |
| RSVD        | AP32   |
| RSVD        | AW27   |
| RSVD        | AR29   |
| RSVD        | AN33   |
| RSVD        | AV29   |
| RSVD        | AU29   |
| RSVD        | AM31   |
| RSVD        | AN32   |
| RSVD        | AN21   |
| RSVD        | BA39   |
| RSVD        | BB35   |

| Signal Name | Ball # |
|-------------|--------|
| RSVD        | BB38   |
| RSVD        | BA34   |
| RSVD        | BA19   |
| RSVD        | AY21   |
| RSVD        | AU33   |
| RSVD        | AM27   |
| RSVD        | AP31   |
| RSVD        | AT33   |
| RSVD        | AM26   |
| RSVD        | AP29   |
| RSTIN#      | AM18   |
| SBS_A0      | BA33   |
| SBS_A1      | AW32   |
| SBS_A2      | BB21   |
| SBS_B0      | AY19   |
| SBS_B1      | BA18   |
| SBS_B2      | BC12   |
| SCAS_A#     | AY35   |
| SCAS_B#     | AW29   |
| SCKE_A0     | BC20   |
| SCKE_A1     | AY20   |
| SCKE_B0     | AY12   |
| SCKE_B1     | AW12   |
| SCLK_A0     | AU31   |
| SCLK_A0#    | AR31   |
| SCLK_A1     | AP27   |
| SCLK_A1#    | AN27   |
| SCLK_A2     | AV33   |
| SCLK_A2#    | AW33   |
| SCLK_B0     | AV31   |
| SCLK_B0#    | AW31   |
| SCLK_B1     | AU27   |
| SCLK_B1#    | AT27   |
| SCLK_B2     | AV32   |
| SCLK_B2#    | AT32   |
| SCS_A0#     | AW35   |
| SCS_A1#     | BA35   |
| SCS_B0#     | BB27   |
| SCS_B1#     | BB30   |



| Signal Name | Ball # |
|-------------|--------|
| SDM_A0      | AR2    |
| SDM_A1      | BA2    |
| SDM_A2      | AY9    |
| SDM_A3      | AN18   |
| SDM_A4      | AU43   |
| SDM_A5      | AM43   |
| SDM_A6      | AG40   |
| SDM_A7      | AC40   |
| SDM_B0      | AR7    |
| SDM_B1      | AW9    |
| SDM_B2      | AW13   |
| SDM_B3      | AP23   |
| SDM_B4      | AU37   |
| SDM_B5      | AM37   |
| SDM_B6      | AG39   |
| SDM_B7      | AD38   |
| SDQ_A0      | AR5    |
| SDQ_A1      | AR4    |
| SDQ_A2      | AV3    |
| SDQ_A3      | AV2    |
| SDQ_A4      | AP3    |
| SDQ_A5      | AP2    |
| SDQ_A6      | AU1    |
| SDQ_A7      | AV4    |
| SDQ_A8      | AY2    |
| SDQ_A9      | AY3    |
| SDQ_A10     | BB5    |
| SDQ_A11     | AY6    |
| SDQ_A12     | AW2    |
| SDQ_A13     | AW3    |
| SDQ_A14     | BA5    |
| SDQ_A15     | BB4    |
| SDQ_A16     | AY7    |
| SDQ_A17     | BC7    |
| SDQ_A18     | AW11   |
| SDQ_A19     | AY11   |
| SDQ_A20     | BB6    |
| SDQ_A21     | BA6    |
| SDQ_A22     | BA10   |

| Signal Name | Ball # |
|-------------|--------|
| SDQ_A23     | BB10   |
| SDQ_A24     | AT18   |
| SDQ_A25     | AR18   |
| SDQ_A26     | AU21   |
| SDQ_A27     | AT21   |
| SDQ_A28     | AP17   |
| SDQ_A29     | AN17   |
| SDQ_A30     | AP20   |
| SDQ_A31     | AV20   |
| SDQ_A32     | AV42   |
| SDQ_A33     | AU40   |
| SDQ_A34     | AP42   |
| SDQ_A35     | AN39   |
| SDQ_A36     | AV40   |
| SDQ_A37     | AV41   |
| SDQ_A38     | AR42   |
| SDQ_A39     | AP41   |
| SDQ_A40     | AN41   |
| SDQ_A41     | AM39   |
| SDQ_A42     | AK42   |
| SDQ_A43     | AK41   |
| SDQ_A44     | AN40   |
| SDQ_A45     | AN42   |
| SDQ_A46     | AL42   |
| SDQ_A47     | AL39   |
| SDQ_A48     | AJ40   |
| SDQ_A49     | AH43   |
| SDQ_A50     | AF39   |
| SDQ_A51     | AE40   |
| SDQ_A52     | AJ42   |
| SDQ_A53     | AJ41   |
| SDQ_A54     | AF41   |
| SDQ_A55     | AF42   |
| SDQ_A56     | AD40   |
| SDQ_A57     | AD43   |
| SDQ_A58     | AB41   |
| SDQ_A59     | AA40   |
| SDQ_A60     | AE42   |
| SDQ_A61     | AE41   |

| Signal Name | Ball # |
|-------------|--------|
| SDQ_A62     | AC39   |
| SDQ_A63     | AB42   |
| SDQ_B0      | AN7    |
| SDQ_B1      | AN8    |
| SDQ_B2      | AW5    |
| SDQ_B3      | AW7    |
| SDQ_B4      | AN5    |
| SDQ_B5      | AN6    |
| SDQ_B6      | AN9    |
| SDQ_B7      | AU7    |
| SDQ_B8      | AT11   |
| SDQ_B9      | AU11   |
| SDQ_B10     | AP13   |
| SDQ_B11     | AR13   |
| SDQ_B12     | AR11   |
| SDQ_B13     | AU9    |
| SDQ_B14     | AV12   |
| SDQ_B15     | AU12   |
| SDQ_B16     | AU15   |
| SDQ_B17     | AV13   |
| SDQ_B18     | AU17   |
| SDQ_B19     | AT17   |
| SDQ_B20     | AU13   |
| SDQ_B21     | AM13   |
| SDQ_B22     | AV15   |
| SDQ_B23     | AW17   |
| SDQ_B24     | AV24   |
| SDQ_B25     | AT23   |
| SDQ_B26     | AT26   |
| SDQ_B27     | AP26   |
| SDQ_B28     | AU23   |
| SDQ_B29     | AW23   |
| SDQ_B30     | AR24   |
| SDQ_B31     | AN26   |
| SDQ_B32     | AW37   |
| SDQ_B33     | AV38   |
| SDQ_B34     | AN36   |
| SDQ_B35     | AN37   |
| SDQ_B36     | AU35   |



| Signal Name | Ball # | Signal Name   | Ball # | Signal Name    | Ball # |
|-------------|--------|---------------|--------|----------------|--------|
| SDQ_B37     | AR35   | SDQS_A6       | AG42   | SMA_B0         | BB17   |
| SDQ_B38     | AN35   | SDQS_A6#      | AG41   | SMA_B1         | AY17   |
| SDQ_B39     | AR37   | SDQS_A7       | AC42   | SMA_B2         | BA17   |
| SDQ_B40     | AM35   | SDQS_A7#      | AC41   | SMA_B3         | BC16   |
| SDQ_B41     | AM38   | SDQS_B0       | AV6    | SMA_B4         | AW15   |
| SDQ_B42     | AJ34   | SDQS_B0#      | AU5    | SMA_B5         | BA15   |
| SDQ_B43     | AL38   | SDQS_B1       | AR12   | SMA_B6         | BB15   |
| SDQ_B44     | AR39   | SDQS_B1#      | AP12   | SMA_B7         | BA14   |
| SDQ_B45     | AM34   | SDQS_B2       | AP15   | SMA_B8         | AY15   |
| SDQ_B46     | AL37   | SDQS_B2#      | AR15   | SMA_B9         | BB14   |
| SDQ_B47     | AL32   | SDQS_B2#      | AR15   | SMA_B10        | AW18   |
| SDQ_B48     | AG38   | SDQS_B3       | AT24   | SMA_B11        | BB13   |
| SDQ_B49     | AJ38   | SDQS_B3#      | AU26   | SMA_B12        | BA13   |
| SDQ_B50     | AF35   | SDQS_B3#      | AU26   | SMA_B13        | AY29   |
| SDQ_B51     | AF33   | SDQS_B4       | AW39   | SMA_B14        | AY13   |
| SDQ_B52     | AJ37   | SDQS_B4#      | AU39   | SMRCOMPVOH     | AM10   |
| SDQ_B53     | AJ35   | SDQS_B5       | AL35   | SMRCOMPVOL     | AM8    |
| SDQ_B54     | AG33   | SDQS_B5#      | AL34   | SODT_A0        | AY37   |
| SDQ_B55     | AF34   | SDQS_B6       | AG35   | SODT_A1        | BA38   |
| SDQ_B56     | AD36   | SDQS_B6#      | AG36   | SODT_B0        | BA29   |
| SDQ_B57     | AC33   | SDQS_B7       | AC36   | SODT_B1        | BA30   |
| SDQ_B58     | AA34   | SDQS_B7#      | AC37   | SRAS_A#        | BB33   |
| SDQ_B59     | AA36   | SDVO_CTRLCLK  | E17    | SRAS_B#        | AW26   |
| SDQ_B60     | AD34   | SDVO_CTRLDATA | G17    | SRCOMP0        | AN2    |
| SDQ_B61     | AF38   | SMA_A0        | BA31   | SRCOMP1        | AN3    |
| SDQ_B62     | AC34   | SMA_A1        | BB25   | SRCOMP2        | BB40   |
| SDQ_B63     | AA33   | SMA_A2        | BA26   | SRCOMP3        | BA40   |
| SDQS_A0     | AU4    | SMA_A3        | BA25   | SVREF          | AM6    |
| SDQS_A0#    | AR3    | SMA_A4        | AY25   | SWE_A#         | BB34   |
| SDQS_A1     | BB3    | SMA_A5        | BA23   | SWE_B#         | BA27   |
| SDQS_A1#    | BA4    | SMA_A6        | AY24   | TEST0          | BC43   |
| SDQS_A2     | BB9    | SMA_A7        | AY23   | TEST1          | BC1    |
| SDQS_A2#    | BA9    | SMA_A8        | BB23   | TEST2          | A43    |
| SDQS_A3     | AT20   | SMA_A9        | BA22   | V_1P25_PLTRST# | AA12   |
| SDQS_A3#    | AU18   | SMA_A10       | AY33   | VCC            | P20    |
| SDQS_A4     | AR41   | SMA_A11       | BB22   | VCC            | Y11    |
| SDQS_A4#    | AR40   | SMA_A12       | AW21   | VCC            | AG25   |
| SDQS_A5     | AL41   | SMA_A13       | AY38   | VCC            | AG24   |
| SDQS_A5#    | AL40   | SMA_A14       | BA21   | VCC            | AG23   |



| Signal Name | Ball # |
|-------------|--------|
| VCC         | AG22   |
| VCC         | AG21   |
| VCC         | AG20   |
| VCC         | AG19   |
| VCC         | AG18   |
| VCC         | AG17   |
| VCC         | AG15   |
| VCC         | AG14   |
| VCC         | AF26   |
| VCC         | AF25   |
| VCC         | AF24   |
| VCC         | AF22   |
| VCC         | AF20   |
| VCC         | AF18   |
| VCC         | AF17   |
| VCC         | AF15   |
| VCC         | AF14   |
| VCC         | AE27   |
| VCC         | AE26   |
| VCC         | AE25   |
| VCC         | AE23   |
| VCC         | AE21   |
| VCC         | AE19   |
| VCC         | AE17   |
| VCC         | AD27   |
| VCC         | AD26   |
| VCC         | AD18   |
| VCC         | AD17   |
| VCC         | AD15   |
| VCC         | AD14   |
| VCC         | AC27   |
| VCC         | AC26   |
| VCC         | AC17   |
| VCC         | AC15   |
| VCC         | AC14   |
| VCC         | AB27   |
| VCC         | AB26   |
| VCC         | AB18   |
| VCC         | AB17   |

| Signal Name | Ball # |
|-------------|--------|
| VCC         | AA27   |
| VCC         | AA26   |
| VCC         | AA17   |
| VCC         | AA15   |
| VCC         | AA14   |
| VCC         | Y27    |
| VCC         | Y26    |
| VCC         | Y18    |
| VCC         | Y17    |
| VCC         | Y15    |
| VCC         | Y14    |
| VCC         | W27    |
| VCC         | W26    |
| VCC         | W25    |
| VCC         | W23    |
| VCC         | W21    |
| VCC         | W19    |
| VCC         | W18    |
| VCC         | W17    |
| VCC         | V27    |
| VCC         | V26    |
| VCC         | V25    |
| VCC         | V24    |
| VCC         | V23    |
| VCC         | V22    |
| VCC         | V21    |
| VCC         | V20    |
| VCC         | V19    |
| VCC         | V18    |
| VCC         | V17    |
| VCC         | V15    |
| VCC         | V14    |
| VCC         | U26    |
| VCC         | U25    |
| VCC         | U24    |
| VCC         | U23    |
| VCC         | U22    |
| VCC         | U21    |
| VCC         | U20    |

| Signal Name | Ball # |
|-------------|--------|
| VCC         | U19    |
| VCC         | U18    |
| VCC         | U17    |
| VCC         | U15    |
| VCC         | U14    |
| VCC         | R20    |
| VCC         | R18    |
| VCC         | R17    |
| VCC         | R15    |
| VCC         | R14    |
| VCC         | P15    |
| VCC         | P14    |
| VCC         | AJ12   |
| VCC         | AJ11   |
| VCC         | AJ10   |
| VCC         | AJ9    |
| VCC         | AJ8    |
| VCC         | AJ7    |
| VCC         | AJ6    |
| VCC         | AJ5    |
| VCC         | AJ4    |
| VCC         | AJ3    |
| VCC         | AJ2    |
| VCC         | AH4    |
| VCC         | AH2    |
| VCC         | AH1    |
| VCC         | AG13   |
| VCC         | AG12   |
| VCC         | AG11   |
| VCC         | AG10   |
| VCC         | AG9    |
| VCC         | AG8    |
| VCC         | AG7    |
| VCC         | AG6    |
| VCC         | AG5    |
| VCC         | AG4    |
| VCC         | AG3    |
| VCC         | AG2    |
| VCC         | AF13   |



| Signal Name | Ball # | Signal Name | Ball # | Signal Name | Ball # |
|-------------|--------|-------------|--------|-------------|--------|
| VCC         | AF12   | VCC         | N3     | VCC2        | AJ17   |
| VCC         | AF11   | VCC         | L6     | VCC2        | AJ15   |
| VCC         | AD24   | VCC         | J6     | VCC2        | AJ14   |
| VCC         | AD22   | VCC         | J3     | VCC2        | AA30   |
| VCC         | AD20   | VCC         | J2     | VCC2        | AA29   |
| VCC         | AC25   | VCC         | G2     | VCC2        | Y30    |
| VCC         | AC23   | VCC         | F11    | VCC2        | Y29    |
| VCC         | AC21   | VCC         | F9     | VCC2        | V30    |
| VCC         | AC19   | VCC         | D4     | VCC2        | V29    |
| VCC         | AC13   | VCC         | C13    | VCC2        | U29    |
| VCC         | AC6    | VCC         | C9     | VCC2        | U27    |
| VCC         | AB24   | VCC         | L12    | VCC2        | AL12   |
| VCC         | AB22   | VCC_EXP     | AD11   | VCC2        | AL11   |
| VCC         | AB20   | VCC_EXP     | AD10   | VCC2        | AL10   |
| VCC         | AA25   | VCC_EXP     | AD9    | VCC2        | AL9    |
| VCC         | AA23   | VCC_EXP     | AD8    | VCC2        | AL8    |
| VCC         | AA21   | VCC_EXP     | AD7    | VCC2        | AL7    |
| VCC         | AA19   | VCC_EXP     | AD6    | VCC2        | AL6    |
| VCC         | AA13   | VCC_EXP     | AD5    | VCC2        | AL5    |
| VCC         | AA3    | VCC_EXP     | AD4    | VCC2        | AL4    |
| VCC         | Y24    | VCC_EXP     | AD2    | VCC2        | AL3    |
| VCC         | Y22    | VCC_EXP     | AD1    | VCC2        | AL2    |
| VCC         | Y20    | VCC_EXP     | AC4    | VCC2        | AK26   |
| VCC         | Y13    | VCC_EXP     | AC3    | VCC2        | AK24   |
| VCC         | Y6     | VCC_EXP     | AC2    | VCC2        | AK23   |
| VCC         | V13    | VCC_EXP     | AE4    | VCC2        | AK21   |
| VCC         | V12    | VCC_EXP     | AE3    | VCC2        | AK20   |
| VCC         | V10    | VCC_EXP     | AE2    | VCC2        | AK18   |
| VCC         | V9     | VCC_SMCLK   | BB42   | VCC2        | AK17   |
| VCC         | U13    | VCC_SMCLK   | BA43   | VCC2        | AK15   |
| VCC         | U10    | VCC_SMCLK   | BB41   | VCC2        | AK3    |
| VCC         | U9     | VCC_SMCLK   | BA42   | VCC2        | AK2    |
| VCC         | U6     | VCC_SMCLK   | AY42   | VCC2        | AK1    |
| VCC         | U3     | VCC2        | AJ26   | VCC2        | AJ13   |
| VCC         | N12    | VCC2        | AJ24   | VCC2        | AD31   |
| VCC         | N11    | VCC2        | AJ23   | VCC2        | AC31   |
| VCC         | N9     | VCC2        | AJ21   | VCC2        | AA31   |
| VCC         | N8     | VCC2        | AJ20   | VCC2        | Y31    |
| VCC         | N6     | VCC2        | AJ18   | VCC2        | Y32    |



| Signal Name | Ball # | Signal Name | Ball # | Signal Name | Ball # |
|-------------|--------|-------------|--------|-------------|--------|
| VCC2        | AJ30   | VCCA_DPLL B | C22    | VSS         | AE22   |
| VCC2        | AJ29   | VCCA_EXP    | A16    | VSS         | AE20   |
| VCC2        | AJ27   | VCCA_EXPPLL | B15    | VSS         | AE18   |
| VCC2        | AG30   | VCCA_HPLL   | C23    | VSS         | AC18   |
| VCC2        | AG29   | VCCA_MPLL   | A24    | VSS         | AA18   |
| VCC2        | AG27   | VCCD_CRT    | C21    | VSS         | W24    |
| VCC2        | AG26   | VCCDQ_CRT   | B21    | VSS         | W22    |
| VCC2        | AF30   | VCCSM       | BC39   | VSS         | W20    |
| VCC2        | AF29   | VCCSM       | BC34   | VSS         | R21    |
| VCC2        | AF27   | VCCSM       | BC30   | VSS         | E1     |
| VCC2        | AD30   | VCCSM       | BC26   | VSS         | C43    |
| VCC2        | AD29   | VCCSM       | BC22   | VSS         | C1     |
| VCC2        | AC30   | VCCSM       | BC18   | VSS         | A41    |
| VCC2        | AC29   | VCCSM       | BC14   | VSS         | A5     |
| VCC2        | AL26   | VCCSM       | BB39   | VSS         | A3     |
| VCC2        | AL24   | VCCSM       | BB37   | VSS         | BC37   |
| VCC2        | AL23   | VCCSM       | BB32   | VSS         | BC32   |
| VCC2        | AL21   | VCCSM       | BB28   | VSS         | BC28   |
| VCC2        | AL20   | VCCSM       | BB26   | VSS         | BC24   |
| VCC2        | AL18   | VCCSM       | BB24   | VSS         | BC10   |
| VCC2        | AL17   | VCCSM       | BB20   | VSS         | BC5    |
| VCC2        | AL15   | VCCSM       | BB18   | VSS         | BB7    |
| VCC2        | AK30   | VCCSM       | BB16   | VSS         | AY41   |
| VCC2        | AK29   | VCCSM       | BB12   | VSS         | AY4    |
| VCC2        | AK27   | VCCSM       | AY32   | VSS         | AW43   |
| VCC2        | AJ31   | VCCSM       | AW24   | VSS         | AW41   |
| VCC2        | AG31   | VCCSM       | AW20   | VSS         | AW1    |
| VCC2        | AF31   | VCCSM       | AV26   | VSS         | AV37   |
| VCC2        | AD32   | VCCSM       | AV18   | VSS         | AV35   |
| VCC2        | AC32   | VREF2       | AM5    | VSS         | AV27   |
| VCC2        | AA32   | VSS         | D16    | VSS         | AV23   |
| VCC2        | AL29   | VSS         | BC41   | VSS         | AV21   |
| VCC2        | AL27   | VSS         | BC3    | VSS         | AV17   |
| VCC2        | AL13   | VSS         | BA1    | VSS         | AV11   |
| VCC2        | AK14   | VSS         | AY40   | VSS         | AV9    |
| VCC3_3      | B17    | VSS         | AF23   | VSS         | AV7    |
| VCCA_DAC    | C17    | VSS         | AF21   | VSS         | AU42   |
| VCCA_DAC    | B16    | VSS         | AF19   | VSS         | AU38   |
| VCCA_DPLLA  | A22    | VSS         | AE24   | VSS         | AU32   |



| Signal Name | Ball # |
|-------------|--------|
| VSS         | AU24   |
| VSS         | AU20   |
| VSS         | AU6    |
| VSS         | AU2    |
| VSS         | AT31   |
| VSS         | AT29   |
| VSS         | AT15   |
| VSS         | AT13   |
| VSS         | AT12   |
| VSS         | AR38   |
| VSS         | AR33   |
| VSS         | AR32   |
| VSS         | AR27   |
| VSS         | AR26   |
| VSS         | AR23   |
| VSS         | AR21   |
| VSS         | AR20   |
| VSS         | AR17   |
| VSS         | AR9    |
| VSS         | AR6    |
| VSS         | AP43   |
| VSS         | AP24   |
| VSS         | AP18   |
| VSS         | AP1    |
| VSS         | AN38   |
| VSS         | AN31   |
| VSS         | AN29   |
| VSS         | AN24   |
| VSS         | AN23   |
| VSS         | AN20   |
| VSS         | AN15   |
| VSS         | AN13   |
| VSS         | AN12   |
| VSS         | AN11   |
| VSS         | AN4    |
| VSS         | AM42   |
| VSS         | AM40   |
| VSS         | AM36   |
| VSS         | AM33   |

| Signal Name | Ball # |
|-------------|--------|
| VSS         | AM29   |
| VSS         | AM24   |
| VSS         | AM23   |
| VSS         | AM20   |
| VSS         | AM11   |
| VSS         | AM9    |
| VSS         | AM7    |
| VSS         | AM4    |
| VSS         | AM2    |
| VSS         | AM1    |
| VSS         | AL36   |
| VSS         | AL33   |
| VSS         | AK43   |
| VSS         | AJ39   |
| VSS         | AJ36   |
| VSS         | AJ33   |
| VSS         | AH42   |
| VSS         | AG37   |
| VSS         | AG34   |
| VSS         | AF43   |
| VSS         | AF37   |
| VSS         | AF36   |
| VSS         | AF10   |
| VSS         | AF9    |
| VSS         | AF8    |
| VSS         | AF7    |
| VSS         | AF6    |
| VSS         | AF5    |
| VSS         | AF3    |
| VSS         | AF2    |
| VSS         | AF1    |
| VSS         | AD42   |
| VSS         | AD39   |
| VSS         | AD37   |
| VSS         | AD35   |
| VSS         | AD33   |
| VSS         | AD25   |
| VSS         | AD23   |
| VSS         | AD21   |

| Signal Name | Ball # |
|-------------|--------|
| VSS         | AD19   |
| VSS         | AC38   |
| VSS         | AC35   |
| VSS         | AC24   |
| VSS         | AC22   |
| VSS         | AC20   |
| VSS         | AC10   |
| VSS         | AC7    |
| VSS         | AC5    |
| VSS         | AB43   |
| VSS         | AB25   |
| VSS         | AB23   |
| VSS         | AB21   |
| VSS         | AB19   |
| VSS         | AB2    |
| VSS         | AB1    |
| VSS         | AA38   |
| VSS         | AA35   |
| VSS         | AA24   |
| VSS         | AA22   |
| VSS         | AA20   |
| VSS         | AA8    |
| VSS         | AA5    |
| VSS         | Y42    |
| VSS         | Y37    |
| VSS         | Y35    |
| VSS         | Y33    |
| VSS         | Y25    |
| VSS         | Y23    |
| VSS         | Y21    |
| VSS         | Y19    |
| VSS         | Y10    |
| VSS         | Y7     |
| VSS         | Y5     |
| VSS         | Y1     |
| VSS         | W3     |
| VSS         | V43    |
| VSS         | V39    |
| VSS         | V37    |



| Signal Name | Ball # |
|-------------|--------|
| VSS         | V34    |
| VSS         | V32    |
| VSS         | V11    |
| VSS         | V8     |
| VSS         | V5     |
| VSS         | V2     |
| VSS         | U38    |
| VSS         | U35    |
| VSS         | U8     |
| VSS         | U7     |
| VSS         | U5     |
| VSS         | T42    |
| VSS         | T1     |
| VSS         | R36    |
| VSS         | R33    |
| VSS         | R31    |
| VSS         | R11    |
| VSS         | R8     |
| VSS         | R5     |
| VSS         | R3     |
| VSS         | P43    |
| VSS         | P30    |
| VSS         | P21    |
| VSS         | P18    |
| VSS         | P17    |
| VSS         | V32    |
| VSS         | V11    |
| VSS         | V8     |
| VSS         | V5     |
| VSS         | V2     |
| VSS         | U38    |
| VSS         | U35    |
| VSS         | U8     |
| VSS         | U7     |
| VSS         | U5     |
| VSS         | T42    |
| VSS         | T1     |
| VSS         | M35    |
| VSS         | M33    |

| Signal Name | Ball # |
|-------------|--------|
| VSS         | M27    |
| VSS         | M21    |
| VSS         | M17    |
| VSS         | M15    |
| VSS         | M10    |
| VSS         | M7     |
| VSS         | M1     |
| VSS         | L33    |
| VSS         | L32    |
| VSS         | L31    |
| VSS         | L29    |
| VSS         | L21    |
| VSS         | L20    |
| VSS         | L11    |
| VSS         | L7     |
| VSS         | L5     |
| VSS         | L3     |
| VSS         | K43    |
| VSS         | K26    |
| VSS         | K21    |
| VSS         | K18    |
| VSS         | K13    |
| VSS         | K12    |
| VSS         | K2     |
| VSS         | J38    |
| VSS         | J35    |
| VSS         | J32    |
| VSS         | J27    |
| VSS         | J21    |
| VSS         | J9     |
| VSS         | J7     |
| VSS         | J5     |
| VSS         | H31    |
| VSS         | H29    |
| VSS         | H21    |
| VSS         | H20    |
| VSS         | H17    |
| VSS         | H15    |
| VSS         | H13    |

| Signal Name | Ball # |
|-------------|--------|
| VSS         | G42    |
| VSS         | G38    |
| VSS         | G32    |
| VSS         | G21    |
| VSS         | G13    |
| VSS         | G12    |
| VSS         | G11    |
| VSS         | G9     |
| VSS         | G7     |
| VSS         | G1     |
| VSS         | F37    |
| VSS         | F35    |
| VSS         | F27    |
| VSS         | F21    |
| VSS         | F18    |
| VSS         | F3     |
| VSS         | E43    |
| VSS         | E32    |
| VSS         | E24    |
| VSS         | E21    |
| VSS         | E20    |
| VSS         | E15    |
| VSS         | E13    |
| VSS         | E11    |
| VSS         | E9     |
| VSS         | E3     |
| VSS         | D40    |
| VSS         | D31    |
| VSS         | D21    |
| VSS         | D17    |
| VSS         | D3     |
| VSS         | C26    |
| VSS         | C11    |
| VSS         | C6     |
| VSS         | C5     |
| VSS         | C4     |
| VSS         | B37    |
| VSS         | B32    |
| VSS         | B31    |



| Signal Name | Ball # |
|-------------|--------|
| VSS         | B26    |
| VSS         | B23    |
| VSS         | B22    |
| VSS         | B19    |
| VSS         | B14    |
| VSS         | B10    |
| VSS         | A39    |
| VSS         | A34    |
| VSS         | A26    |
| VSS         | A18    |
| VSS         | A12    |
| VSS         | A7     |
| VSS         | M11    |
| VSYNC       | D15    |
| VTT         | R27    |
| VTT         | R26    |
| VTT         | R24    |
| VTT         | R23    |
| VTT         | P29    |
| VTT         | P27    |
| VTT         | P26    |

| Signal Name | Ball # |
|-------------|--------|
| VTT         | P24    |
| VTT         | P23    |
| VTT         | N29    |
| VTT         | N26    |
| VTT         | N24    |
| VTT         | N23    |
| VTT         | M29    |
| VTT         | M24    |
| VTT         | M23    |
| VTT         | L24    |
| VTT         | L23    |
| VTT         | K24    |
| VTT         | K23    |
| VTT         | J24    |
| VTT         | J23    |
| VTT         | H24    |
| VTT         | H23    |
| VTT         | G26    |
| VTT         | G24    |
| VTT         | G23    |
| VTT         | F26    |

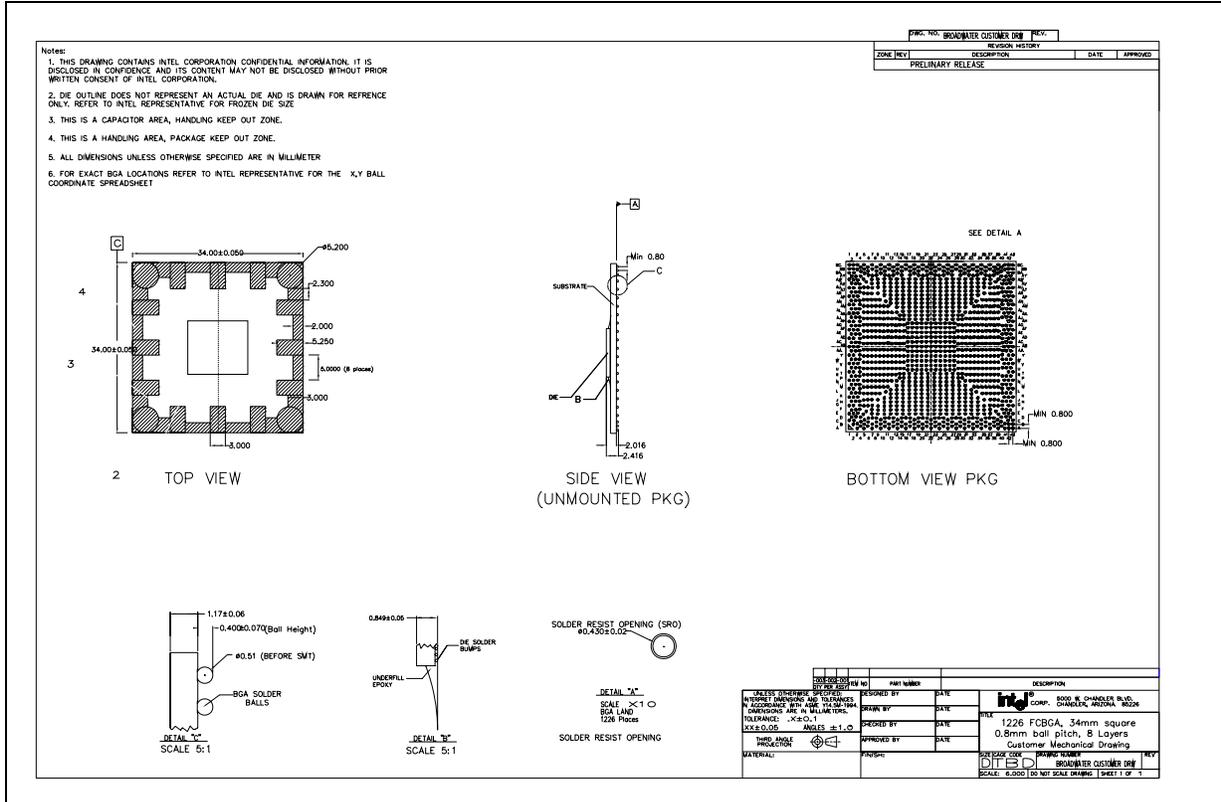
| Signal Name | Ball # |
|-------------|--------|
| VTT         | F24    |
| VTT         | F23    |
| VTT         | E29    |
| VTT         | E27    |
| VTT         | E26    |
| VTT         | E23    |
| VTT         | D29    |
| VTT         | D28    |
| VTT         | D27    |
| VTT         | C30    |
| VTT         | C29    |
| VTT         | C27    |
| VTT         | B30    |
| VTT         | B29    |
| VTT         | B28    |
| VTT         | B27    |
| VTT         | A30    |
| VTT         | A28    |
| XORTEST     | F20    |



## 11.2 Package Information

For additional information, refer to the *Intel® G31/P31 Express Chipset Thermal and Mechanical Design Guide*.

Figure 11-4. (G)MCH Package Drawing





# 12 Testability

In the (G)MCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates each with one input pin connected to it which allows for pad to ball to trace connection testing.

The XOR testing methodology is to boot the part using straps to enter XOR mode (A description of the boot process follows). Once in XOR mode, all of the pins of an XOR chain are driven to logic 1. This action will force the output of that XOR chain to either a 1 if the number of the pins making up the chain is even or a 0 if the number of the pins making up the chain is odd.

Once a valid output is detected on the XOR chain output, a walking “0” pattern is moved from one end of the chain to the other. Every time the walking “0” is applied to a pin on the chain, the output will toggle. If the output does not toggle, there is a disconnect somewhere between die, package, and board and the system can be considered a failure.

## 12.1 XOR Test Mode Initialization

Figure 12-1. XOR Test Mode Initialization Cycles

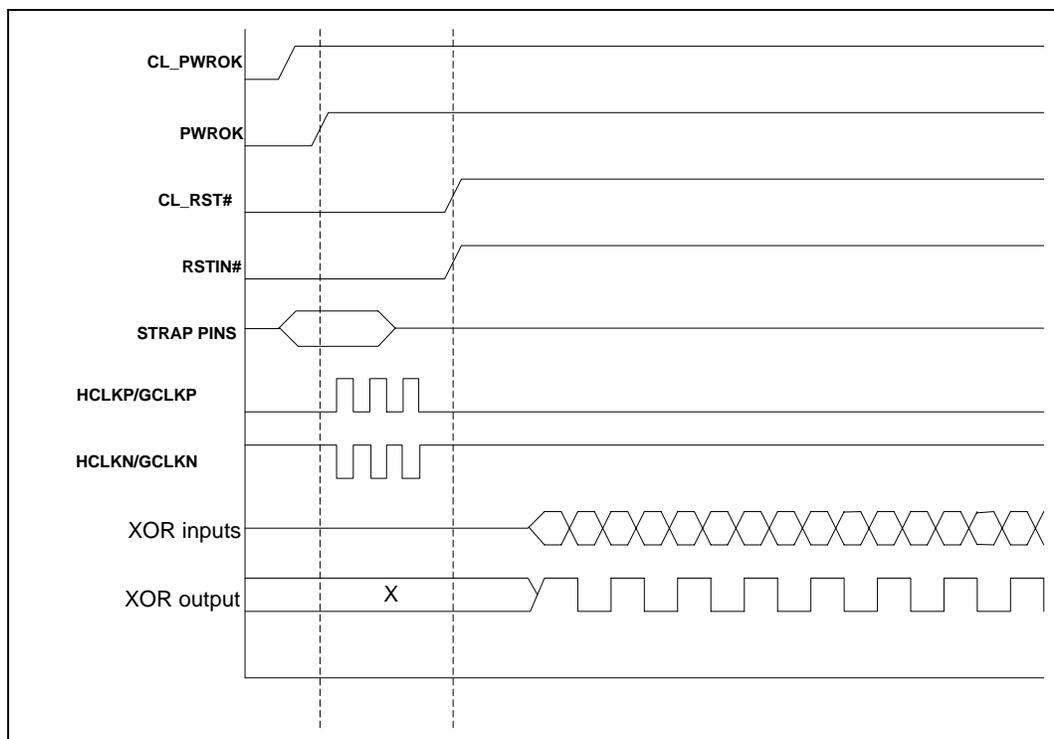


Figure 12-1 shows the wave forms to be able to boot the part into XOR mode. The straps that need to be controlled during this boot process are BSEL[2:0], SDVO\_CTRLDATA, EXP\_EM, EXP\_SLR, and XORTEST.

On Broadwater platforms, all strap values must be driven before PWROK asserts. BSEL0 must be a 1. BSEL[2:1] need to be defined values, but logic value in any order will do. XORTEST must be driven to 0.

If sDVO is present in the design (82G31 GMCH only), SDVO\_CTRLDATA must be pulled to logic 1. Depending on if Static Lane Reversal is used and if the sDVO/PCIe Coexistence is selected, EXP\_SLR and EXP\_EN must be pulled in a valid manner.

Because of the different functionalities of the sDVO/PCIe interface, not all of the pins will be used in all implementations. Due to the need to minimize test points and unnecessary routing, the XOR Chain 14 is dynamic depending on the values of SDVO\_CTRLDATA, EXP\_SLR, and EXP\_EN. See Table 12-1 for what parts of XOR Chain 14 become valid XOR inputs depending on the use of SDVO\_CTRLDATA, EXP\_SLR, and EXP\_EN.

**Table 12-1. XOR Chain 14 functionality**

| SDVO_CTRLDATA | EXP_EN | EXP_SLR | XOR Chain 14   |
|---------------|--------|---------|--|
| 0             | 1      | 0       | EXP_RXP[15:0]<br>EXP_RXN[15:0]<br>EXP_TXP[15:0]<br>EXP_TXN[15:0] |
| 0             | 1      | 1       | EXP_RXP[15:0]<br>EXP_RXN[15:0]<br>EXP_TXP[15:0]<br>EXP_TXN[15:0] |
| 1             | 0      | 0       | EXP_RXP[15:8]<br>EXP_RXN[15:8]<br>EXP_TXP[15:8]<br>EXP_TXN[15:8] |
| 1             | 0      | 1       | EXP_RXP[7:0]<br>EXP_RXN[7:0]<br>EXP_TXP[7:0]<br>EXP_TXN[7:0]     |
| 1             | 1      | 0       | EXP_RXP[15:0]<br>EXP_RXN[15:0]<br>EXP_TXP[15:0]<br>EXP_TXN[15:0] |
| 1             | 1      | 1       | EXP_RXP[15:0]<br>EXP_RXN[15:0]<br>EXP_TXP[15:0]<br>EXP_TXN[15:0] |



## 12.2 XOR Chain Definition

The (G)MCH has 15 XOR chains. The XOR chain outputs are driven out on the output pins shown in Table 12-2. During fullwidth testing, XOR chain outputs will be visible on both pins.

**Table 12-2. XOR Chain Outputs**

| XOR Chain | Output Pins | Coordinate Location |
|-----------|-------------|---------------------|
| xor_out0  | ALLZTEST    | K20                 |
| xor_out1  | XORTEST     | F20                 |
| xor_out2  | ICH_SYNC#   | J13                 |
| xor_out3  | RSV         | F17                 |
| xor_out4  | RSV         | AA9                 |
| xor_out5  | RSV         | AA10                |
| xor_out6  | BSEL1       | J20                 |
| xor_out7  | BSEL2       | J18                 |
| xor_out8  | RSV         | AA11                |
| xor_out9  | RSV         | Y12                 |
| xor_out10 | EXP_SLR     | E18                 |
| xor_out11 | EXP_EN      | J17                 |
| xor_out12 | MTYPE       | G18                 |
| xor_out13 | RSV         | K17                 |
| xor_out14 | BSELO       | G20                 |

## 12.3 XOR Chains

The following tables lists the XOR chain.

**Table 12-3. XOR Chain 0**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | B33    | HD58#       |
| 2         | C35    | HD49#       |
| 3         | B40    | HD55#       |
| 4         | E41    | HD50#       |
| 5         | C40    | HD53#       |
| 6         | B41    | HD51#       |
| 7         | A32    | HD62#       |
| 8         | B35    | HD61#       |
| 9         | C33    | HD48#       |
| 10        | D35    | HD54#       |
| 11        | C38    | HD56#       |
| 12        | D37    | HD57#       |
| 13        | D42    | HD52#       |
| 14        | C34    | HD60#       |
| 15        | D32    | HD63#       |
| 16        | D33    | HD59#       |
| 17        | B34    | HD31#       |
| 18        | A37    | HD26#       |
| 19        | B39    | HD24#       |
| 20        | D41    | HD17#       |
| 21        | C42    | HD16#       |
| 22        | C39    | HD23#       |
| 23        | E37    | HD22#       |
| 24        | E35    | HD28#       |
| 25        | E42    | HD20#       |
| 26        | F38    | HD18#       |
| 27        | E39    | HD21#       |
| 28        | G33    | HD25#       |
| 29        | F33    | HD27#       |

**Table 12-3. XOR Chain 0**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 30        | G37    | HD19#       |
| 31        | H32    | HD30#       |
| 32        | K32    | HD29#       |
| 33        | F29    | HD41#       |
| 34        | H26    | HD44#       |
| 35        | J26    | HD46#       |
| 36        | G31    | HD37#       |
| 37        | F32    | HD33#       |
| 38        | F31    | HD39#       |
| 39        | E31    | HD35#       |
| 40        | J29    | HD40#       |
| 41        | M26    | HD47#       |
| 42        | L26    | HD45#       |
| 43        | J31    | HD32#       |
| 44        | K27    | HD43#       |
| 45        | L27    | HD42#       |
| 46        | K29    | HD38#       |
| 47        | K31    | HD36#       |
| 48        | M31    | HD34#       |
| 49        | J41    | HD11#       |
| 50        | R42    | HD4#        |
| 51        | F42    | HD15#       |
| 52        | M39    | HD5#        |
| 53        | F41    | HD14#       |
| 54        | G40    | HD13#       |
| 55        | J39    | HD9#        |
| 56        | K41    | HD12#       |
| 57        | N40    | HD3#        |
| 58        | N41    | HD6#        |



Table 12-3. XOR Chain 0

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 59        | R41    | HD2#        |
| 60        | L42    | HD10#       |
| 61        | L41    | HD8#        |
| 62        | P41    | HD1#        |
| 63        | N42    | HD7#        |
| 64        | R40    | HD0#        |

Table 12-4. XOR Chain 1

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 23        | V42    | HA30#       |
| 24        | R35    | HA26#       |
| 25        | U36    | HA24#       |
| 26        | U33    | HA25#       |
| 27        | Y39    | HA34#       |
| 28        | V33    | HA27#       |
| 29        | V36    | HA22#       |
| 30        | R38    | HA23#       |
| 31        | U34    | HADSTB1#    |
| 32        | R37    | HA19#       |
| 33        | AA37   | HA35#       |
| 34        | U37    | HA17#       |
| 35        | N39    | HA18#       |
| 36        | V38    | HA31#       |
| 37        | R39    | HA21#       |
| 38        | Y36    | HA32#       |
| 39        | V35    | HA28#       |
| 40        | P42    | HA20#       |

Table 12-4. XOR Chain 1

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | L37    | HA6#        |
| 2         | N35    | HA15#       |
| 3         | L36    | HA7#        |
| 4         | L39    | HA4#        |
| 5         | M38    | HA11#       |
| 6         | L38    | HREQ2#      |
| 7         | J37    | HREQ4#      |
| 8         | N34    | HA10#       |
| 9         | L35    | HREQ1#      |
| 10        | F40    | HREQ0#      |
| 11        | M34    | HADSTB0#    |
| 12        | M36    | HA13#       |
| 13        | N37    | HA12#       |
| 14        | J40    | HA5#        |
| 15        | K42    | HA8#        |
| 16        | R34    | HA14#       |
| 17        | N32    | HA9#        |
| 18        | N38    | HA16#       |
| 19        | G43    | HREQ3#      |
| 20        | J42    | HA3#        |
| 21        | Y38    | HA33#       |
| 22        | Y34    | HA29#       |

Table 12-5. XOR Chain 2

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | G35    | HDSTBP1#    |
| 2         | H33    | HDSTBN1#    |
| 3         | U42    | HHIT#       |
| 4         | Y40    | HTRDY#      |
| 5         | AA41   | HRS1#       |
| 6         | Y43    | HHITM#      |
| 7         | G27    | HDSTBP2#    |
| 8         | H27    | HDSTBN2#    |
| 9         | L40    | HDSTBP0#    |
| 10        | M43    | HDSTBN0#    |

**Table 12-5. XOR Chain 2**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 11        | V41    | HLOCK#      |
| 12        | W42    | HBNR#       |
| 13        | C31    | HCPURST#    |
| 14        | G39    | HBPRI#      |

**Table 12-6. XOR Chain 3**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | B38    | HDSTBP3#    |
| 2         | D38    | HDSTBN3#    |
| 3         | E33    | HDINV3#     |
| 4         | J33    | HDINV1#     |
| 5         | U40    | HDBSY#      |
| 6         | U39    | HRS2#       |
| 7         | W41    | HDRDY#      |
| 8         | U41    | HRS0#       |
| 9         | T43    | HDEFER#     |
| 10        | G29    | HDINV2#     |
| 11        | M40    | HDINV0#     |
| 12        | W40    | HADS#       |
| 13        | AA42   | HBREQ0#     |

**Table 12-7. XOR Chain 4**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | AY37   | SODT_A0     |
| 2         | BA35   | SCS_A1#     |
| 3         | BA38   | SODT_A1     |
| 4         | AY33   | SMA_A10     |
| 5         | AW35   | SCS_A0#     |
| 6         | BA31   | SMA_A0      |
| 7         | AW33   | SCLK_A2#    |

**Table 12-7. XOR Chain 4**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 8         | AV33   | SCLK_A2     |
| 9         | AU31   | SCLK_A0     |
| 10        | AR31   | SCLK_A0#    |
| 11        | AN27   | SCLK_A1#    |
| 12        | AP27   | SCLK_A1     |
| 13        | BA22   | SMA_A9      |
| 14        | BA26   | SMA_A2      |
| 15        | BA25   | SMA_A3      |
| 16        | AY25   | SMA_A4      |
| 17        | AY23   | SMA_A7      |
| 18        | AY20   | SCKE_A1     |
| 19        | BA23   | SMA_A5      |
| 20        | BB25   | SMA_A1      |
| 21        | BB23   | SMA_A8      |
| 22        | AY24   | SMA_A6      |
| 23        | BC20   | SCKE_A0     |
| 24        | AU18   | SDQS_A3#    |
| 25        | AN18   | SDM_A3      |
| 26        | BA9    | SDQS_A2#    |
| 27        | AY9    | SDM_A2      |
| 28        | BA4    | SDQS_A1#    |
| 29        | BA2    | SDM_A1      |
| 30        | AR3    | SDQS_A0#    |
| 31        | AR2    | SDM_A0      |

**Table 12-8. XOR Chain 5**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | AC41   | SDQS_A7#    |
| 2         | AC40   | SDM_A7      |
| 3         | AG41   | SDQS_A6#    |
| 4         | AG40   | SDM_A6      |



Table 12-8. XOR Chain 5

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 5         | AL40   | SDQS_A5#    |
| 6         | AM43   | SDM_A5      |
| 7         | AR40   | SDQS_A4#    |
| 8         | AU43   | SDM_A4      |
| 9         | AY38   | SMA_A13     |
| 10        | AY35   | SCAS_A#     |
| 11        | AW32   | SBS_A1      |
| 12        | BA33   | SBS_A0      |
| 13        | BB33   | SRAS_A#     |
| 14        | BB34   | SWE_A#      |
| 15        | BB22   | SMA_A11     |
| 16        | BB21   | SBS_A2      |
| 17        | BA21   | SMA_A14     |
| 18        | AW21   | SMA_A12     |

Table 12-9. XOR Chain 6

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 15        | AF41   | SDQ_A54     |
| 16        | AJ42   | SDQ_A52     |
| 17        | AJ40   | SDQ_A48     |
| 18        | AF39   | SDQ_A50     |
| 19        | AL41   | SDQS_A5     |
| 20        | AL39   | SDQ_A47     |
| 21        | AN40   | SDQ_A44     |
| 22        | AM39   | SDQ_A41     |
| 23        | AL42   | SDQ_A46     |
| 24        | AN41   | SDQ_A40     |
| 25        | AK42   | SDQ_A42     |
| 26        | AN42   | SDQ_A45     |
| 27        | AK41   | SDQ_A43     |
| 28        | AR41   | SDQS_A4     |
| 29        | AV40   | SDQ_A36     |
| 30        | AV42   | SDQ_A32     |
| 31        | AP41   | SDQ_A39     |
| 32        | AN39   | SDQ_A35     |
| 33        | AU40   | SDQ_A33     |
| 34        | AV41   | SDQ_A37     |
| 35        | AP42   | SDQ_A34     |
| 36        | AR42   | SDQ_A38     |
| 37        | AT20   | SDQS_A3     |
| 38        | AR18   | SDQ_A25     |
| 39        | AU21   | SDQ_A26     |
| 40        | AV20   | SDQ_A31     |
| 41        | AP20   | SDQ_A30     |
| 42        | AT18   | SDQ_A24     |
| 43        | AN17   | SDQ_A29     |
| 44        | AT21   | SDQ_A27     |
| 45        | AP17   | SDQ_A28     |
| 46        | BB9    | SDQS_A2     |
| 47        | AY11   | SDQ_A19     |

Table 12-9. XOR Chain 6

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | AC42   | SDQS_A7     |
| 2         | AB41   | SDQ_A58     |
| 3         | AE42   | SDQ_A60     |
| 4         | AD43   | SDQ_A57     |
| 5         | AB42   | SDQ_A63     |
| 6         | AA40   | SDQ_A59     |
| 7         | AC39   | SDQ_A62     |
| 8         | AE41   | SDQ_A61     |
| 9         | AD40   | SDQ_A56     |
| 10        | AG42   | SDQS_A6     |
| 11        | AH43   | SDQ_A49     |
| 12        | AE40   | SDQ_A51     |
| 13        | AJ41   | SDQ_A53     |
| 14        | AF42   | SDQ_A55     |

**Table 12-9. XOR Chain 6**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 48        | BA10   | SDQ_A22     |
| 49        | AW11   | SDQ_A18     |
| 50        | BC7    | SDQ_A17     |
| 51        | BA6    | SDQ_A21     |
| 52        | BB10   | SDQ_A23     |
| 53        | AY7    | SDQ_A16     |
| 54        | BB6    | SDQ_A20     |
| 55        | BB3    | SDQS_A1     |
| 56        | BB4    | SDQ_A15     |
| 57        | BB5    | SDQ_A10     |
| 58        | AY6    | SDQ_A11     |
| 59        | BA5    | SDQ_A14     |
| 60        | AY2    | SDQ_A8      |
| 61        | AY3    | SDQ_A9      |
| 62        | AW3    | SDQ_A13     |
| 63        | AW2    | SDQ_A12     |
| 64        | AU4    | SDQS_A0     |
| 65        | AV3    | SDQ_A2      |
| 66        | AR4    | SDQ_A1      |
| 67        | AR5    | SDQ_A0      |
| 68        | AP2    | SDQ_A5      |
| 69        | AV4    | SDQ_A7      |
| 70        | AU1    | SDQ_A6      |
| 71        | AP3    | SDQ_A4      |
| 72        | AV2    | SDQ_A3      |

**Table 12-10. XOR Chain 8**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 4         | AU27   | SCLK_B1     |
| 5         | AT27   | SCLK_B1#    |
| 6         | AV32   | SCLK_B2     |
| 7         | BB30   | SCS_B1#     |
| 8         | BA30   | SODT_B1     |
| 9         | BA29   | SODT_B0     |
| 10        | BB27   | SCS_B0#     |
| 11        | AW15   | SMA_B4      |
| 12        | AY17   | SMA_B1      |
| 13        | AY15   | SMA_B8      |
| 14        | BA15   | SMA_B5      |
| 15        | AW18   | SMA_B10     |
| 16        | AW12   | SCKE_B1     |
| 17        | BA14   | SMA_B7      |
| 18        | BA17   | SMA_B2      |
| 19        | AY12   | SCKE_B0     |
| 20        | BB14   | SMA_B9      |
| 21        | BB17   | SMA_B0      |
| 22        | BB15   | SMA_B6      |
| 23        | BC16   | SMA_B3      |
| 24        | AU26   | SDQS_B3#    |
| 25        | AP23   | SDM_B3      |
| 26        | AR15   | SDQS_B2#    |
| 27        | AW13   | SDM_B2      |
| 28        | AP12   | SDQS_B1#    |
| 29        | AW9    | SDM_B1      |
| 30        | AU5    | SDQS_B0#    |
| 31        | AR7    | SDM_B0      |

**Table 12-10. XOR Chain 8**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | AW31   | SCLK_B0#    |
| 2         | AV31   | SCLK_B0     |
| 3         | AT32   | SCLK_B2#    |



Table 12-11. XOR Chain 9

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | AC37   | SDQS_B7#    |
| 2         | AD38   | SDM_B7      |
| 3         | AG36   | SDQS_B6#    |
| 4         | AG39   | SDM_B6      |
| 5         | AL34   | SDQS_B5#    |
| 6         | AM37   | SDM_B5      |
| 7         | AU39   | SDQS_B4#    |
| 8         | AU37   | SDM_B4      |
| 9         | AY29   | SMA_B13     |
| 10        | AW26   | SRAS_B#     |
| 11        | AW29   | SCAS_B#     |
| 12        | BA27   | SWE_B#      |
| 13        | BA18   | SBS_B1      |
| 14        | AY19   | SBS_B0      |
| 15        | AY13   | SMA_B14     |
| 16        | BC12   | SBS_B2      |
| 17        | BA13   | SMA_B12     |
| 18        | BB13   | SMA_B11     |

Table 12-12. XOR Chain 10

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 11        | AF34   | SDQ_B55     |
| 12        | AJ38   | SDQ_B49     |
| 13        | AF33   | SDQ_B51     |
| 14        | AJ35   | SDQ_B53     |
| 15        | AG33   | SDQ_B54     |
| 16        | AG38   | SDQ_B48     |
| 17        | AJ37   | SDQ_B52     |
| 18        | AF35   | SDQ_B50     |
| 19        | AL35   | SDQS_B5     |
| 20        | AL38   | SDQ_B43     |
| 21        | AJ34   | SDQ_B42     |
| 22        | AM34   | SDQ_B45     |
| 23        | AL32   | SDQ_B47     |
| 24        | AM38   | SDQ_B41     |
| 25        | AM35   | SDQ_B40     |
| 26        | AL37   | SDQ_B46     |
| 27        | AR39   | SDQ_B44     |
| 28        | AW39   | SDQS_B4     |
| 29        | AV38   | SDQ_B33     |
| 30        | AN35   | SDQ_B38     |
| 31        | AN36   | SDQ_B34     |
| 32        | AR37   | SDQ_B39     |
| 33        | AW37   | SDQ_B32     |
| 34        | AU35   | SDQ_B36     |
| 35        | AN37   | SDQ_B35     |
| 36        | AR35   | SDQ_B37     |
| 37        | AT24   | SDQS_B3     |
| 38        | AP26   | SDQ_B27     |
| 39        | AU23   | SDQ_B28     |
| 40        | AT23   | SDQ_B25     |
| 41        | AV24   | SDQ_B24     |
| 42        | AR24   | SDQ_B30     |
| 43        | AW23   | SDQ_B29     |

Table 12-12. XOR Chain 10

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | AC36   | SDQS_B7     |
| 2         | AF38   | SDQ_B61     |
| 3         | AC34   | SDQ_B62     |
| 4         | AA34   | SDQ_B58     |
| 5         | AA33   | SDQ_B63     |
| 6         | AA36   | SDQ_B59     |
| 7         | AD36   | SDQ_B56     |
| 8         | AC33   | SDQ_B57     |
| 9         | AD34   | SDQ_B60     |
| 10        | AG35   | SDQS_B6     |

**Table 12-12. XOR Chain 10**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 44        | AT26   | SDQ_B26     |
| 45        | AN26   | SDQ_B31     |
| 46        | AP15   | SDQS_B2     |
| 47        | AM13   | SDQ_B21     |
| 48        | AU15   | SDQ_B16     |
| 49        | AT17   | SDQ_B19     |
| 50        | AU17   | SDQ_B18     |
| 51        | AW17   | SDQ_B23     |
| 52        | AV13   | SDQ_B17     |
| 53        | AV15   | SDQ_B22     |
| 54        | AU13   | SDQ_B20     |
| 55        | AR12   | SDQS_B1     |
| 56        | AR11   | SDQ_B12     |
| 57        | AV12   | SDQ_B14     |
| 58        | AU11   | SDQ_B9      |
| 59        | AU12   | SDQ_B15     |
| 60        | AR13   | SDQ_B11     |
| 61        | AU9    | SDQ_B13     |
| 62        | AP13   | SDQ_B10     |
| 63        | AT11   | SDQ_B8      |
| 64        | AV6    | SDQS_B0     |
| 65        | AU7    | SDQ_B7      |
| 66        | AW7    | SDQ_B3      |
| 67        | AN6    | SDQ_B5      |
| 68        | AW5    | SDQ_B2      |
| 69        | AN9    | SDQ_B6      |
| 70        | AN5    | SDQ_B4      |
| 71        | AN7    | SDQ_B0      |
| 72        | AN8    | SDQ_B1      |

**Table 12-13. XOR Chain 12**

| Pin Count | Ball # | Signal Name   |
|-----------|--------|---------------|
| 1         | G17    | SDVO_CTRLDATA |
| 2         | E17    | SDVO_CTRLCLK  |
| 3         | L13    | DDC_DATA      |
| 4         | M13    | DDC_CLK       |

**Table 12-14. XOR Chain 13**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | AA2    | DMI_TXN_3   |
| 2         | Y2     | DMI_TXP_3   |
| 3         | AA4    | DMI_RXN_3   |
| 4         | AB3    | DMI_RXP_3   |
| 5         | AC9    | DMI_TXN_2   |
| 6         | AC8    | DMI_TXP_2   |
| 7         | AA6    | DMI_RXN_2   |
| 8         | AA7    | DMI_RXP_2   |
| 9         | Y4     | DMI_TXN_1   |
| 10        | W4     | DMI_TXP_1   |
| 11        | Y9     | DMI_RXN_1   |
| 12        | Y8     | DMI_RXP_1   |
| 13        | V6     | DMI_TXN_0   |
| 14        | V7     | DMI_TXP_0   |
| 15        | V1     | DMI_RXN_0   |
| 16        | W2     | DMI_RXP_0   |

**Table 12-15. XOR Chain 14**

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 1         | U4     | EXP_TXN15   |
| 2         | V3     | EXP_TXP15   |
| 3         | R7     | EXP_RXN15   |
| 4         | R6     | EXP_RXP15   |



Table 12-15. XOR Chain 14

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 5         | T2     | EXP_TXN14   |
| 6         | U2     | EXP_TXP14   |
| 7         | R4     | EXP_RXN14   |
| 8         | T4     | EXP_RXP14   |
| 9         | P1     | EXP_TXN13   |
| 10        | R2     | EXP_TXP13   |
| 11        | R10    | EXP_RXN13   |
| 12        | R9     | EXP_RXP13   |
| 13        | N4     | EXP_TXN12   |
| 14        | P3     | EXP_TXP12   |
| 15        | M6     | EXP_RXN12   |
| 16        | M5     | EXP_RXP12   |
| 17        | M2     | EXP_TXN11   |
| 18        | N2     | EXP_TXP11   |
| 19        | L4     | EXP_RXN11   |
| 20        | M4     | EXP_RXP11   |
| 21        | K1     | EXP_TXN10   |
| 22        | L2     | EXP_TXP10   |
| 23        | M9     | EXP_RXN10   |
| 24        | M8     | EXP_RXP10   |
| 25        | K3     | EXP_TXN9    |
| 26        | J4     | EXP_TXP9    |
| 27        | L8     | EXP_RXN9    |
| 28        | L9     | EXP_RXP9    |
| 29        | G4     | EXP_TXN8    |
| 30        | F4     | EXP_TXP8    |
| 31        | G5     | EXP_RXN8    |
| 32        | G6     | EXP_RXP8    |
| 33        | E2     | EXP_TXN7    |
| 34        | F2     | EXP_TXP7    |
| 35        | D2     | EXP_RXN7    |
| 36        | C2     | EXP_RXP7    |

Table 12-15. XOR Chain 14

| Pin Count | Ball # | Signal Name |
|-----------|--------|-------------|
| 37        | B4     | EXP_TXN6    |
| 38        | B3     | EXP_TXP6    |
| 39        | F6     | EXP_RXN6    |
| 40        | E5     | EXP_RXP6    |
| 41        | B6     | EXP_TXN5    |
| 42        | B5     | EXP_TXP5    |
| 43        | E7     | EXP_RXN5    |
| 44        | F7     | EXP_RXP5    |
| 45        | D6     | EXP_TXN4    |
| 46        | D7     | EXP_TXP4    |
| 47        | H11    | EXP_RXN4    |
| 48        | J11    | EXP_RXP4    |
| 49        | B7     | EXP_TXN3    |
| 50        | B9     | EXP_TXP3    |
| 51        | H12    | EXP_RXN3    |
| 52        | J12    | EXP_RXP3    |
| 53        | D9     | EXP_TXN2    |
| 54        | C10    | EXP_TXP2    |
| 55        | E12    | EXP_RXN2    |
| 56        | F12    | EXP_RXP2    |
| 57        | A10    | EXP_TXN1    |
| 58        | B11    | EXP_TXP1    |
| 59        | J15    | EXP_RXN1    |
| 60        | K15    | EXP_RXP1    |
| 61        | D12    | EXP_TXN0    |
| 62        | D11    | EXP_TXP0    |
| 63        | G15    | EXP_RXN0    |
| 64        | F15    | EXP_RXP0    |

