82706
INTEL VIDEO GRAPHICS ARRAY

- **Single Chip Video Graphics Array for IBM PC/XT/AT*, Personal System/2* and Compatible Systems**
- **100% Gate, Register, and BIOS Level Compatibility with IBM VGA**
- **EGA/CGA/MDA BIOS Compatibility**
- **Inmos IMSG 171 Palette/DAC Interface**
- **4 mA Drive Capability on Output Pins**
- **Implemented in High Speed CHMOS III Technology**
- **Available in 132-Pin Plastic Quad Flat Pack Package**
  (See Packaging Spec. Order #231369)

The 82706 is the Intel VGA compatible display controller. It is 100% register compatible with all IBM VGA modes and provides software compatibility at the BIOS level with EGA, CGA, and MDA. All video monitors designed for IBM PS/2* systems are supported by the Intel VGA controller. The 82706 provides an 8-bit video data path to any Inmos IMSG 171 compatible palette/DAC. It also acts as a CRT controller and video memory controller. The 82706 supports 256 Kbytes of video memory.

The 82706 is designed for compatibility with the Intel 80286 and 80386 microprocessors and other microprocessors.

Implemented in low power CHMOS technology, the 82706 VGA Controller is packaged in a fine pitch (25 mil) surface mount gull wing package. It can be enabled or disabled under software control via the 82306 Peripheral Bus Controller.

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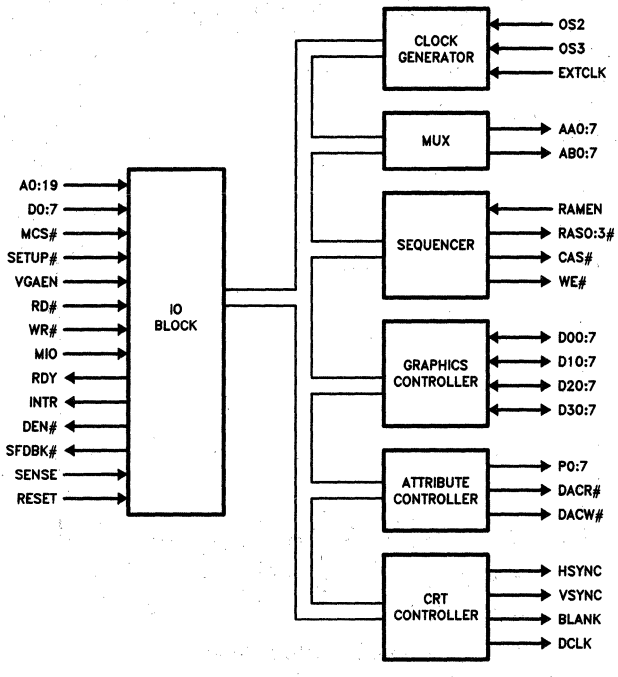
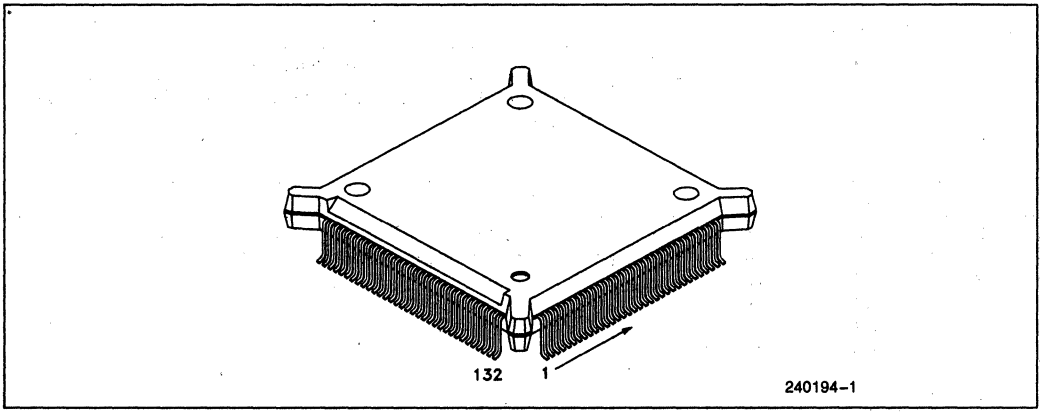


240194-2

Figure 1. Block Diagram

November 1988
Order Number: 240194-002

PLASTIC QUAD FLAT PACK (PQFP)



Pinout (Top View)

82706 PIN DESCRIPTION

Left side of package (top view):

Number	Name	Active	I/O	Description
1	AB4	HI	O	DRAM address bus, planes 2 and 3 (continued from top side of package).
2	AB5	HI	O	
3	AB6	HI	O	
4	AB7	HI	O	
5	V_{DD}			
6	A0	HI	I	System address bus, from current MicroChannel* master. Used to select display buffer words, VGA registers, or video DAC registers.
7	A1	HI	I	
8	A2	HI	I	
9	A3	HI	I	
10	A4	HI	I	
11	A5	HI	I	
12	A6	HI	I	
13	A7	HI	I	
14	A8	HI	I	
15	A9	HI	I	
16	A10	HI	I	
17	A11	HI	I	
18	A12	HI	I	
19	A13	HI	I	
20	A14	HI	I	
21	A15	HI	I	
22	A16	HI	I	
23	A17	HI	I	
24	A18	HI	I	
25	A19	HI	I	
26	$\overline{MCS}$	LO	I	Display buffer (memory) select, generated from A24:20. These inputs do not qualify I/O cycles.
27	RESET	HI	I	Device reset. Tri-States all VGA pins when active.
28	RAMEN	HI	I	RAM Enable. When inactive, tri-states all VGA DRAM interface pins to allow board test of DRAMs or to allow another device to share control of the DRAM.
29	SENSE	HI	I	Switch sense input. The state of this pin can be read from Input Status 0 register, bit 4, and indicates if a monochrome or color monitor is attached to the Display Connector. BIOS requires this information to set the video mode correctly.
30	$\overline{SETUP}$	LO	I	VGA Setup. Used during Programmable Option Select (POS) operation. Analogous to MicroChannel-CD SETUP signals for the other adapter slots. After RESET, the 82706 requires the setup pin to be pulled low. An I/O write to port address XX2h must write a "1" to data bit 0 while setup is low. Then setup must be pulled high. Once this is complete, the 82706 can respond to CPU accesses.
31	VGAEN	HI	I	VGA Enable. Allows VGA to respond to memory or I/O cycles when active.
32	FCO		O	
33	FCI		O	

82706 PIN DESCRIPTION (Continued)

Bottom side of package (top view):

Number	Name	Active	I/O	Description
34	V_{SS}			
35	$\overline{RAS0}$	LO	O	Row Address Strobe for plane 0.
36	$\overline{RAS1}$	LO	O	Row Address Strobe for plane 1.
37	$\overline{RAS2}$	LO	O	Row Address Strobe for plane 2.
38	$\overline{RAS3}$	LO	O	Row Address Strobe for plane 3.
39	$\overline{WE}$	LO	O	RAM Write Enable for all planes.
40	V_{DD}			
41	$\overline{CAS}$	LO	O	Column Address Strobe for all planes.
42	HSYNC		O	Horizontal and Vertical Sync to Display Connector.
43	VSYNC		O	These are programmable to be active high or low.
44	BLANK	LO	O	Video Blank to Video DAC and Display Connector.
45	V_{SS}			
46	$\overline{RD}$	LO	I	Read Strobe, active for memory or I/O cycles.
47	$\overline{WR}$	LO	I	Write Strobe, active for memory or I/O cycles.
48	MIO	HI	I	Memory/$\overline{IO}$; high for memory cycles, low for I/O.
49	O1			Pull up to VDD using 10K resistor.
50	OS2		I	Video clocks. OS2 (28.3 MHz) is used for modes with 720
51	OS3		I	pixel horizontal resolution. OS3 (25.17 MHz) is used for
52	EXTCLK		I	modes with 320 or 640 pixel horizontal resolution. EXTCLK is a MicroChannel video extension signal, which allows using a user-defined clock.
53	V_{SS}			
54	DCLK		O	Pixel clock to Video DAC.
55	$\overline{DACR}$	LO	O	Video DAC read and write strobes.
56	$\overline{DACW}$	LO	O	
57	V_{DD}			
58	P7	HI	O	Pixel output bus to Video DAC.
59	P6	HI	O	
60	P5	HI	O	
61	P4	HI	O	
62	P3	HI	O	
63	P2	HI	O	
64	P1	HI	O	
65	P0	HI	O	
66	V_{SS}			

82706 PIN DESCRIPTION (Continued)

Right side of package (top view):

Number	Name	Active	I/O	Description
67	V_{DD}			
68	D7	HI	I/O	System data bus. The VGA may be accessed by any MicroChannel bus master.
69	D6	HI	I/O	
70	D5	HI	I/O	
71	D4	HI	I/O	
72	D3	HI	I/O	
73	D2	HI	I/O	
74	D1	HI	I/O	
75	D0	HI	I/O	
76	V_{SS}			
77	RDY	HI	O	Bus ready signal.
78	INTR	LO	O	Interrupt request. When enabled, INTR is activated during vertical retrace.
79	$\overline{DEN}$	LO	O	Data Enable to the VGA's data bus transceiver. The direction of the transceiver is controlled by the bus controller array.
80	$\overline{SFDBK}$	LO	O	VGA Selected Feedback. Active when VGA is address selected for a memory or I/O cycle, as an acknowledgement of its presence at the address specified. Used during diagnostics.
81	V_{DD}			
82	D00	HI	I/O	DRAM data bus, plane 0.
83	D01	HI	I/O	
84	D02	HI	I/O	
85	D03	HI	I/O	
86	D04	HI	I/O	
87	D05	HI	I/O	
88	D06	HI	I/O	
89	D07	HI	I/O	
90	V_{SS}			
91	D10	HI	I/O	DRAM data bus, plane 1.
92	D11	HI	I/O	
93	D12	HI	I/O	
94	D13	HI	I/O	
95	D14	HI	I/O	
96	D15	HI	I/O	
97	D16	HI	I/O	
98	D17	HI	I/O	
99	V_{DD}			

82706 PIN DESCRIPTION (Continued)

Top side of package (top view):

Number	Name	Active	I/O	Description
100	V_{SS}			
101	D20	HI	I/O	DRAM data bus, plane 2.
102	D21	HI	I/O	
103	D22	HI	I/O	
104	D23	HI	I/O	
105	D24	HI	I/O	
106	D25	HI	I/O	
107	D26	HI	I/O	
108	D27	HI	I/O	
109	V_{DD}			
110	D30	HI	I/O	DRAM data bus, plane 3.
111	D31	HI	I/O	
112	D32	HI	I/O	
113	D33	HI	I/O	
114	D34	HI	I/O	
115	D35	HI	I/O	
116	D36	HI	I/O	
117	D37	HI	I/O	
118	V_{SS}			
119	V_{DD}			
120	AA0	HI	O	DRAM address bus, planes 0 and 1.
121	AA1	HI	O	
122	AA2	HI	O	
123	AA3	HI	O	
124	AA4	HI	O	
125	AA5	HI	O	
126	AA6	HI	O	
127	AA7	HI	O	
128	V_{SS}			
129	AB0	HI	O	DRAM address bus, planes 2 and 3.
130	AB1	HI	O	
131	AB2	HI	O	
132	AB3	HI	O	

FUNCTIONAL DESCRIPTION

The 82706 interfaces the host processor and video memory, and provides palette DAC support and display of video data. All accesses between the host and video memory go through the 82706. These accesses are arbitrated with display refresh requirements to allow the CPU to read or write video memory at any time without having to wait for display retrace.

Video memory contains 256 Kbytes organized as four 64K x 8 maps. The starting address of the video memory in the host address space is programmable, providing three different start addresses. Display data from video memory is formatted into an 8-bit value clocked out on pins P0–P7, which may drive a DAC or go directly to a TTL monitor interface.

CRT Controller

In addition to generating horizontal and vertical sync timings, the CRT controller (CRTC) generates addressing for DRAM refresh and timings to support the cursor and underline capabilities.

Graphics Controller

The graphics controller provides the interface between video memory and both the host processor and the attribute controller. In alphanumeric (A/N) modes, display data is latched from video memory and sent in parallel to the attribute controller. In All Points Addressable (APA) modes, latched display data is serialized before being sent to the attribute controller.

Two read modes and four write modes are supported. Processor reads to video memory cause one byte from each of the four memory maps to be latched. Read mode 0 causes the host processor to read this latched data from a selected map, allowing access to each bit plane separately. Read mode 1 causes the pixel values in each selected map to be compared to a reference value stored in the Color Compare register. Each bit of the byte read contains a 1 when the latched pixel value matches the reference value.

Memory maps may be masked for write operations, allowing the host processor to update any or all memory maps with a single 8-bit access. In write mode 0, logical operations may be performed between pixel data latched by the previous read operation and either write data, which may be rotated, or data stored in the Set/Reset register. Logical operations supported are AND, OR, XOR, or write data unmodified. Write mode 1 simply copies latched data to the memory maps. Write Modes 2 and 3 are similar to write mode 0. In write mode 2, each enabled memory map is updated with 8 bits of the value in the corresponding bit position of the write data. Write mode 3 writes each enabled map with 8 bits of the value in the Set/Reset register. The bit mask value is derived by ANDing write data with the value in the bit mask register.

Attribute Controller

Display data in APA modes, and character generator and attribute data in A/N modes is sent to the attribute controller from the graphics controller. The attribute controller handles cursor insertion, panning, underlining, and blinking. The 8-bit per pixel output value is available on pins P0–P7.

Sequencer

The sequencer generates DRAM memory timings and arbitrates all accesses to video memory. It inserts CPU memory cycles at appropriate times between display memory fetches. The sequencer contains map mask registers which can prevent maps from being updated by memory accesses.

Preliminary product information describes products for which full characterization data is not yet available. Intel believes this information is accurate and reliable. However, it is subject to change without notice.

Table 1. Modes of Operation

GRAPHICS MODES		
Mode	**Resolution**	**Colors**
4, 5	320 x 200	4 out of 256K
6	640 x 200	2 out of 256K
D	320 x 200	16 out of 256K
E	640 x 200	16 out of 256K
F	640 x 350	Monochrome
10	640 x 350	16 out of 256K
11	640 x 480	2 out of 256K
12	640 x 480	16 out of 256K
13	320 x 200	256 out of 256K

ALPHA (TEXT) MODES					
Mode	**Rows**	**Columns**	**Char. Box**	**Resolution**	**Colors**
0, 1	25	40	9 x 16	320 x 200 (CGA)	16 out of 256K
				320 x 350 (EGA)	16 out of 256K
				360 x 400 (VGA)	16 out of 256K
2, 3	25	80	9 x 16	640 x 200 (CGA)	16 out of 256K
				640 x 350 (EGA)	16 out of 256K
				720 x 400 (VGA)	16 out of 256K
7	25	80	9 x 16	720 x 350 (EGA)	Monochrome
				720 x 400 (VGA)	Monochrome

REGISTER SET

Register Name	R/W	Index	Read Port	Write Port
GENERAL REGISTERS				
Miscellaneous Output	W			03C2
	R		03CC	
Input Status 0	R		03C2	
Input Status 1	R		03?A	
Feature Control	W			03?A
	R		03CA	
GRAPHICS CONTROLLER				
Graphics Address	R/W		03CE	03CE
Set/Reset	R/W	00	03CF	03CF
Enable Set/Reset	R/W	01	03CF	03CF
Color Compare	R/W	02	03CF	03CF
Data Rotate	R/W	03	03CF	03CF
Read Map Select	R/W	04	03CF	03CF
Graphics Mode	R/W	05	03CF	03CF
Miscellaneous	R/W	06	03CF	03CF
Color Don't Care	R/W	07	03CF	03CF
Bit Mask	R/W	08	03CF	03CF
SEQUENCER				
Sequencer Address	R/W		03C4	03C4
Reset	R/W	00	03C5	03C5
Clocking Mode	R/W	01	03C5	03C5
Map Mask	R/W	02	03C5	03C5
Character Map Select	R/W	03	03C5	03C5
Memory Mode	R/W	04	03C5	03C5
ATTRIBUTE CONTROLLER				
Address	R/W		03C0	03C0
Palette Registers	R/W	00–0F	03C1	03C0
Attribute Mode Control	R/W	10	03C1	03C0
Overscan Color	R/W	11	03C1	03C0
Color Plane Enble	R/W	12	03C1	03C0
Horizontal PEL Panning	R/W	13	03C1	03C0
Color Select	R/W	14	03C1	03C0

REGISTER SET (Continued)

Register Name	R/W	Index	Read Port	Write Port
CRT CONTROLLER				
CRT Controller Address	R/W		03?4	03?4
Horizontal Total	R/W	00	03?5	03?5
Horizontal Display Enable	R/W	01	03?5	03?5
Start Horizontal Blanking	R/W	02	03?5	03?5
End Horizontal Blanking	R/W	03	03?5	03?5
Start Horizontal Retrace Pulse	R/W	04	03?5	03?5
End Horizontal Retrace	R/W	05	03?5	03?5
Vertical Total	R/W	06	03?5	03?5
Overflow	R/W	07	03?5	03?5
Preset Row Scan	R/W	08	03?5	03?5
Maximum Scan Line	R/W	09	03?5	03?5
Cursor Start	R/W	0A	03?5	03?5
Cursor End	R/W	0B	03?5	03?5
Start Address High	R/W	0C	03?5	03?5
Start Address Low	R/W	0D	03?5	03?5
Cursor Location High	R/W	0E	03?5	03?5
Cursor Location Low	R/W	0F	03?5	03?5
Vertical Retrace Start	R/W	10	03?5	03?5
Vertical Retrace End	R/W	11	03?5	03?5
Vertical Display Enable End	R/W	12	03?5	03?5
Offset	R/W	13	03?5	03?5
Underline Location	R/W	14	03?5	03?5
Start Vertical Blank	R/W	15	03?5	03?5
End Vertical Blank	R/W	16	03?5	03?5
CRTC Mode Control	R/W	17	03?5	03?5
Line Compare	R/W	18	03?5	03?5

NOTES:
? = B in Monochrome Emulation Modes
? = D in Color Emulation Modes
All addresses are given in Hex

Register Name	R/W	Index	Read Port	Write Port
VIDEO DIGITAL TO ANALOG CONVERTER				
PEL Address (Write Mode)	R/W		03C8	03C8
PEL Address (Read Mode)	W			03C7
DAC State	R		03C7	
PEL Data	R/W		03C9	03C9
PEL Mask	R/W		03C6	03C6

NOTE:
1. DAC state register is located on the 82706. PEL Address, PEL Data, and PEL mask are located on the Palette DAC. The 82706 decodes accesses to these registers to generate DACR and DACW.

82706 PARAMETRICS

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to Any Pin with Respect to Ground .... −0.3V to +(V_{CC} +0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3 to +7.0V
DC Input Current ..... ±10 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA (Note 1)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 4 mA (Note 1)
V_{OL1}	Output Low Voltage		0.4	V	I_{OL} = 2 mA (Note 2)
V_{OH1}	Output High Voltage	2.4		V	I_{OH} = 2 mA (Note 2)
I_{CC}	Power Supply Current		100	mA	
I_{LI}	Input Leakage Current		10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	Tri-State Output Leakage Current	−10	10	μA	$V_{SS} < V_{OUT} < V_{CC}$

NOTES:
1. Applies to all outputs except those listed in Note 2.
2. Applies only to pins INTR, DEN, FC0, FC1, and WE.

A.C. CHARACTERISTICS T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Timing Requirements
AC Timings are referenced to 1.5V

Symbol	Parameter	Min	Max	Units	Notes
T1	Clock Cycle Time	35	10000	ns	
T2	Clock High Time	10	10000	ns	
T3	Clock Low Time	14	10000	ns	
T4	A19:0, MI0 Valid to RD or WR Low	35		ns	
T4A	A19:0, MCS Hold from CAS Low	0		ns	(Note 6)
T4B	A19:0, MCS Hold from RD High	0		ns	(Note 7)
T4C	RDY High to RD, WR High	0		ns	(Note 5)
T5	WR Pulse Width	70		ns	(Note 2)
T6	D7:0 Set-Up to WR High	60		ns	(Note 2)
T7	WR High to D7:0 Hold	16		ns	(Notes 2, 8)
T7A	DEN High to D7:0 Hold	0		ns	(Notes 1, 8)
T7B	RDY High to D7:0 Hold	0		ns	(Note 6)
T7C	WR Low to D7:0 Valid		30	ns	(Note 6)
T8	D37:00 Valid to CLK High	0		ns	
T9	CLK High to D37:00 Hold	40		ns	
T9A	CAS High to D37:00 Hold	0		ns	

Timing Responses
AC Timings are referenced to 1.5V

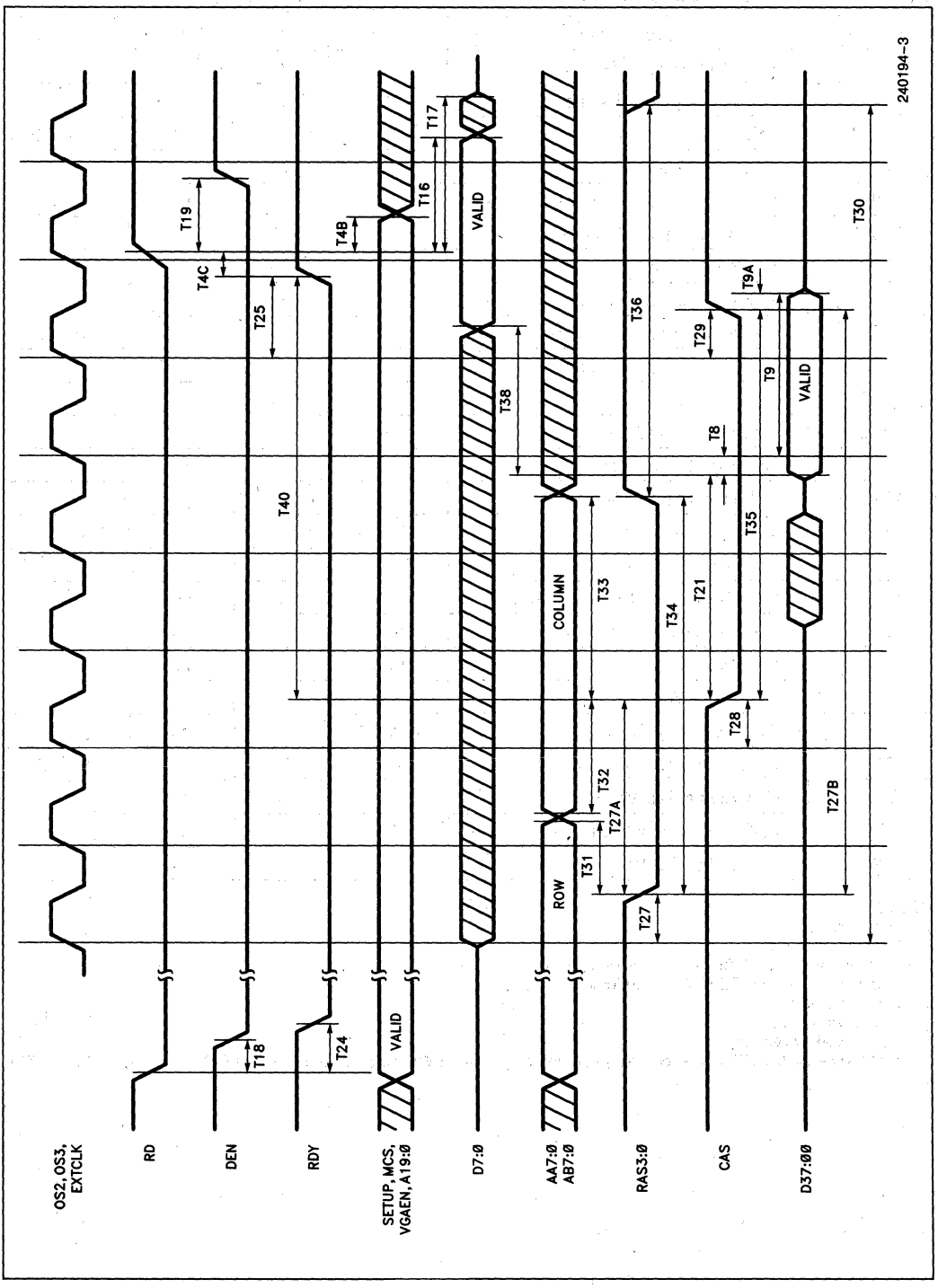
Symbol	Parameter	Min	Max	Units	Notes
T10	DCLK High Time	7		ns	(Note 3)
T11	DCLK Low Time	9		ns	(Note 4)
T12	P7:0 Valid to DCLK High	12		ns	
T13	DCLK High to P7:0 Invalid	15		ns	
T13A	DCLK High to BLANK Valid		40	ns	
T13B	DCLK High to HSYNC, VSYNC Valid		65	ns	
T14	A19:0 MI0 Valid to SFDBK Valid		60	ns	
T15	RD Low to D7:0 Valid		60	ns	
T16	RD High to D7:0 Invalid	0		ns	
T17	RD High to D7:0 Float		20	ns	

A.C. CHARACTERISTICS T_C = 0°C to +70°C, V_{CC} = 5V ±10% (Continued)

Symbol	Parameter	Min	Max	Units	Notes
T18	RD, WR Low to DEN Low		65	ns	
T19	RD, WR High to DEN High	5	30	ns	
T20	WR High to DEN High	6		ns	(Note 2)
T21	CAS Low to D37:00 Valid		70	ns	
T22	RD, WR Low to DACR, DACW Low		55	ns	
T23	RD, WR High to DACR, DACW High	4	25	ns	
T24	RD, WR Low to RDY Low		40	ns	
T25	CLK High to RDY High	0	60	ns	
T26	DATA Hold from RDY High	0		ns	(Note 6)
T27	CLK High to RAS 3:0 Low		50	ns	
T27A	RAS Low to CAS Low	50	70	ns	
T27B	RAS Low to CAS High	60		ns	
T28	CLK High to CAS Low		45	ns	
T29	CLK High to CAS High		45	ns	
T30	DRAM Cycle Time	8T1-10		ns	
T31	Row Address Hold Time	T1-10		ns	
T32	Column Address Set-up Time	10		ns	
T33	Column Address Hold Time	2T1-10		ns	
T34	RAS Pulse Width	4T1-10		ns	
T35	CAS Pulse Width	4T1-10		ns	
T36	RAS Precharge Time	4T1-15		ns	
T38	D37:00 Valid to D7:0 Valid		76	ns	(Note 7)
T39	CLK High to WE Valid		50	ns	
T40	CAS Low to RDY High	58		ns	
T41	D37:00 Valid to WE	0		ns	

NOTES:
1. I/O cycles.
2. I/O write cycles only.
3. T10 is typically at least T3 (Clock Low Time) − 4.
4. T11 is typically at least T2 (Clock High Time) − 1.
5. Memory cycles only.
6. Memory write cycles.
7. Memory read cycles only.
8. For I/O write cycles, D7:0 must be held past the rising edge of WR for at least T7 or until DEN goes high (T20 + T7A), whichever is least.

MEMORY READ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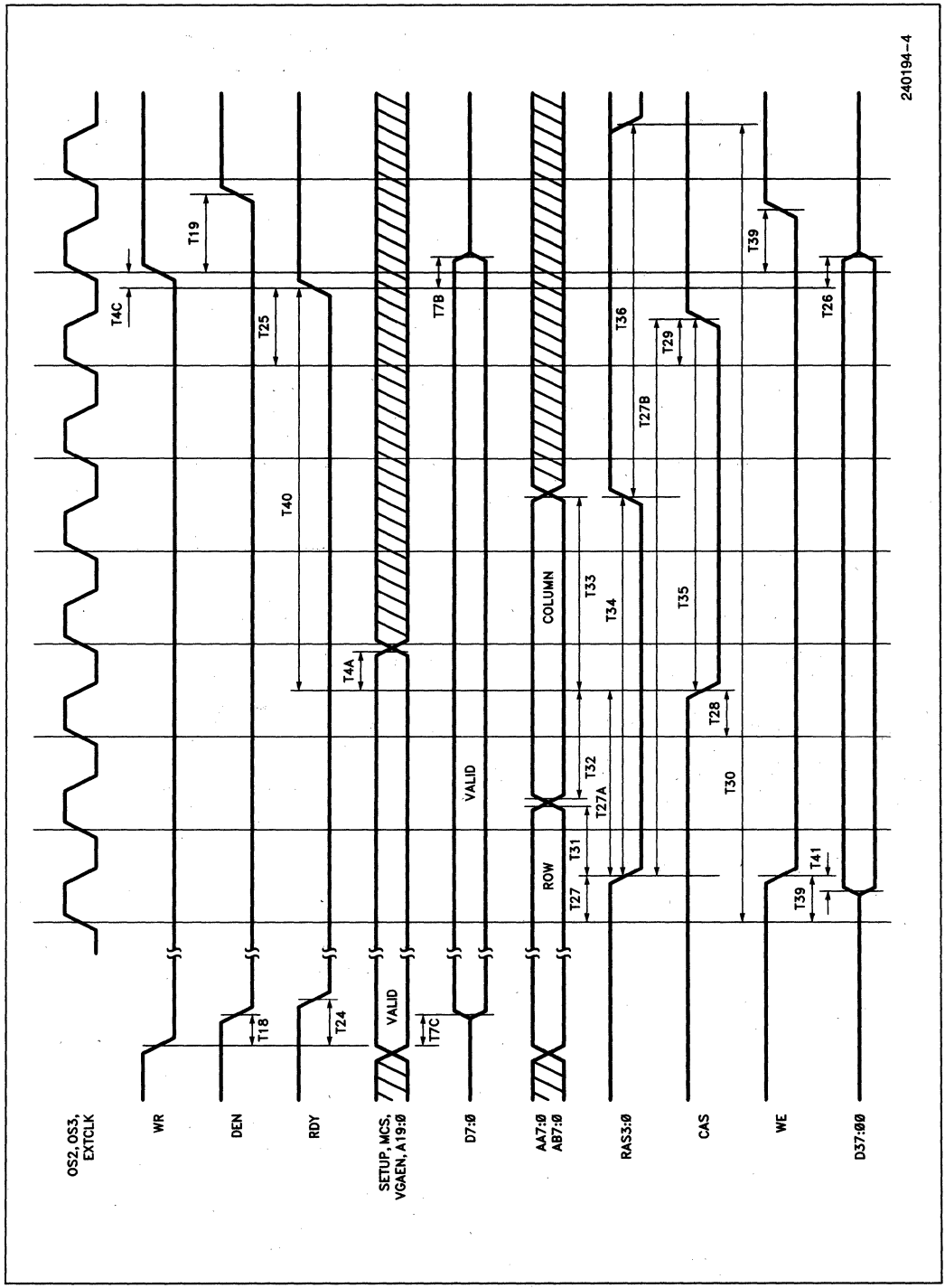
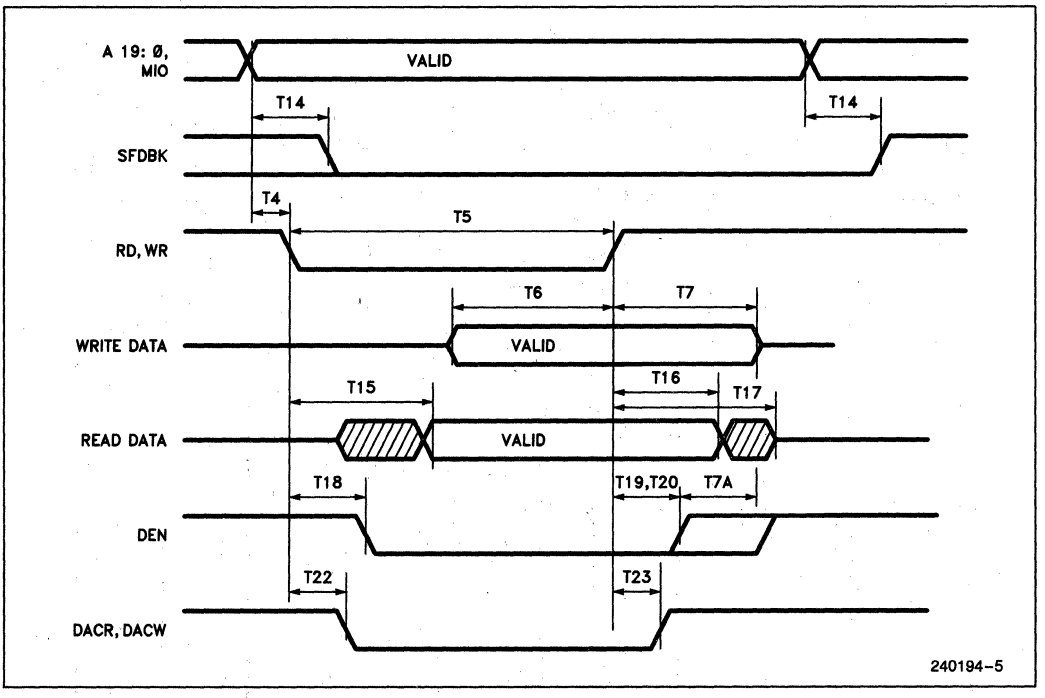
RD
DEN
RDY
SETUP, MCS, VGAEN, A19:0
D7:0
AA7:0 AB7:0
RAS3:0
CAS
D37:00
T19
T4C
T25
T40
T4B
T17
T16
VALID
T38
T36
T29
T9A
T9
T8
T35
T34
T21
T33
COLUMN
T32
T27A
T31
ROW
T27
T28
T30
T27B
T18
T24
VALID

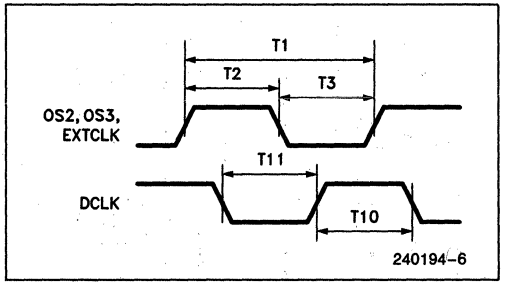
MEMORY WRITE



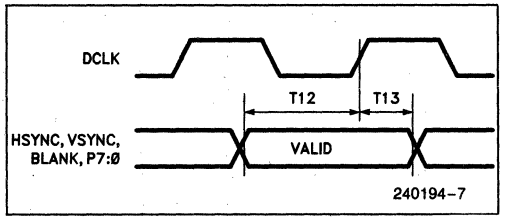
I/O CYCLE



CLOCK TIMINGS



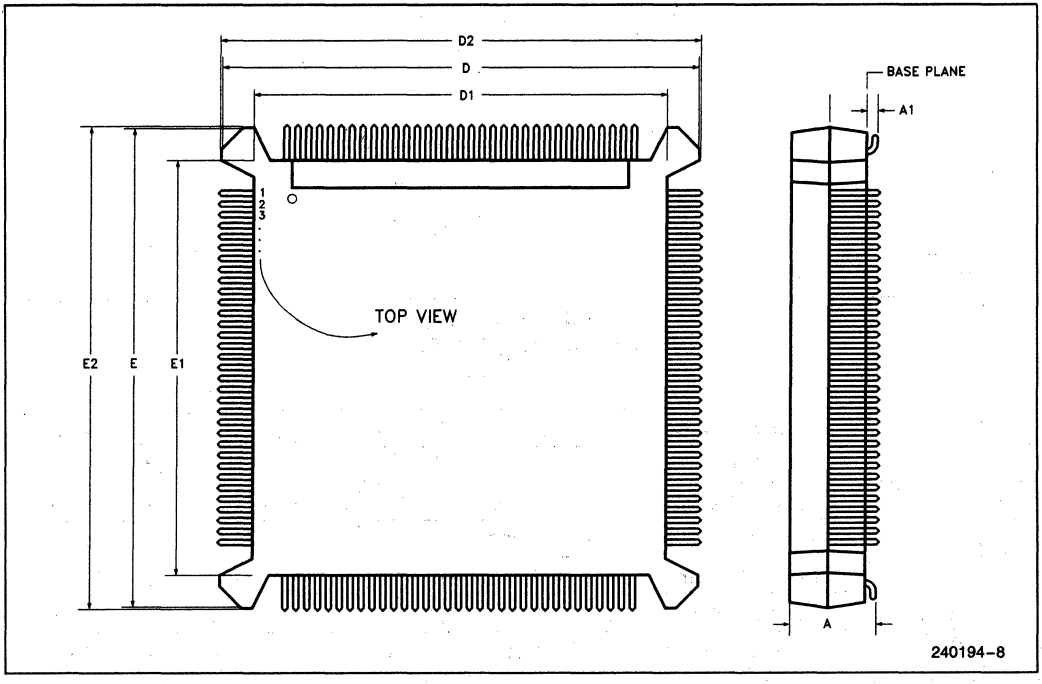
VIDEO TIMINGS



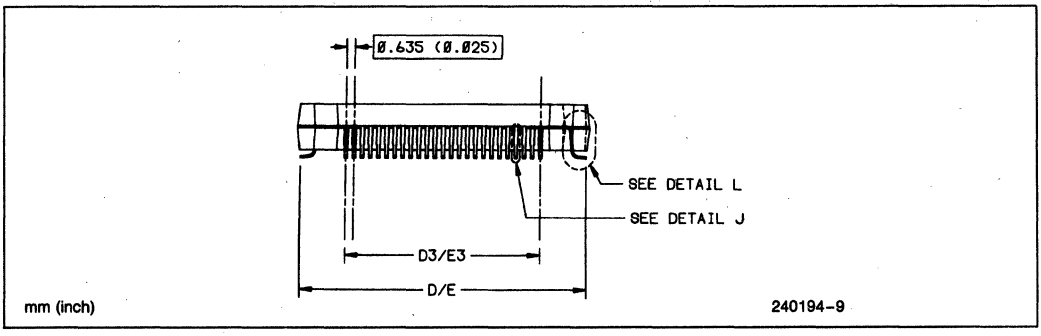
PLASTIC PACKAGING INFORMATION

The 82706 comes in a JEDEC Standard Gull Wing package (25 mil pitch), with "bumpers" on the corners for ease of handling.

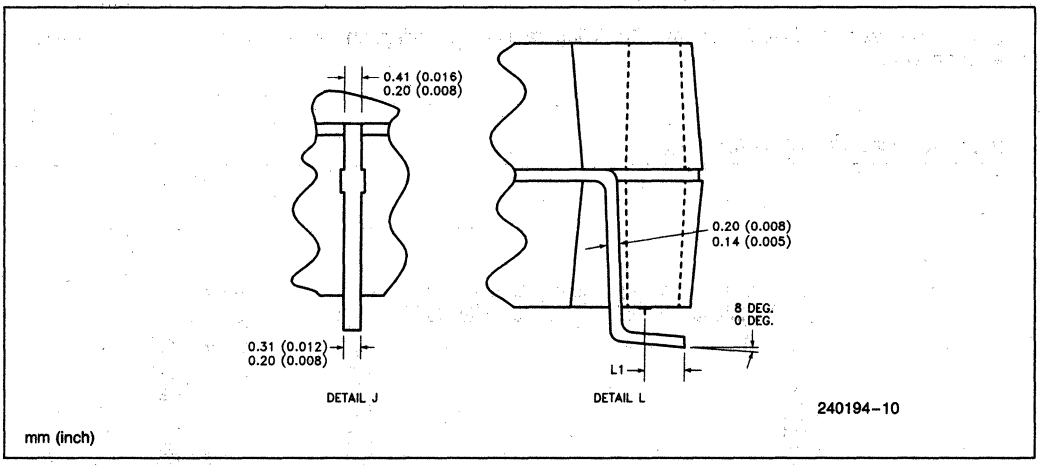
PRINCIPAL DIMENSIONS & DATUMS



TERMINAL DETAILS



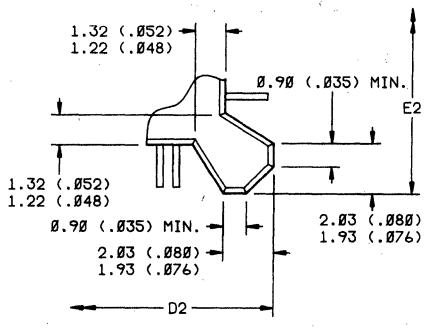
TYPICAL LEAD



Case Outline Drawings
Plastic Fine Pitch Chip Carrier
0.84 mm Pitch

Symbol	Description	Min	Max	Min	Max
N	Lead Count	132		132	
A	Package Height	0.160	0.170	4.06	4.32
A1	Standoff	0.020	0.030	0.51	0.76
D, E	Terminal Dimension	1.075	1.085	27.31	27.56
D1, E1	Package Body	0.947	0.953	24.05	24.21
D2, E2	Bumper Distance	1.097	1.103	27.86	28.02
D3, E3	Lead Dimension	0.800 Ref		20.32 Ref	
L1	Foot Length	0.020	0.030	0.51	0.76
		Inch		mm	

BUMPER DETAIL



mm (inch)

DATA SHEET REVISION REVIEW

This 82706 data sheet, version -002, contains updates and improvements to the previous version. A revision summary is listed here for your convenience.

The sections significantly revised since version -001 are:

Packaging Information — Drawing of ceramic package replaced with drawing of plastic package.
— Plastic package information section added containing mechanical information.

Pin Description — A note was added to the description of the SETUP pin.

Register Set — Video DAC register information added.

Timing Specs — Values for timings T7, T8, and T9 changed.
— Spec T21 added.

Timing Diagrams — Memory Read timing diagram altered as follows:
— SETUP and VGAEN added.
— T8 and T9 are now referenced from clock cycle earlier.
— T21 is added.
— T38 reference is changed.