MX86200

HIGH PERFORMANCE 64-BIT GUI/VIDEO ACCELERATOR

FEATURES

- High Performance Architecture
- True 64-bit graphics engine.
- True 8/16/32 bpp acceleration.
- BitBLT, rectangle, pattern fill, line draw, color expansion and complete 256 ROP.
- On-chip pattern memory.
- Multiple advanced FIFOs.
- Memory-mapped I/O.
- 64x64x2 bit-mapped hardware cursor.

- High-quality Video Playback
- Support primary surface DCI drivers for smooth and high quality video playback.
- Support Microsoft Video For Windows.

- Advanced Memory Control
- 1,2, or 4 MBytes display memory.
- True 64-bit display memory access.
- 256K x 4, 256K x 8, and 256K x 16 dual CAS or dual WE DRAM.
- Fast-page and Hyper-page EDO.
- Auto memory size detection.
- Linear addressing modes up to 4 MByte.

- Full Resolution/color support
- 1600x1200, 64K colors @ 60 Hz.
- 1280x1024, 64K color @ 75 Hz.
- 1024x768, 16M color @ 60 Hz.

- Fully Integrated for Modern Systems
- Glueless PCI bus interface.
- Full PCI 2.1 compliance.
- Integrated RA MDAC.
- Integrated programmable 135 MHz clock synthesizer.
- Low-Power sub-micron CMOS.
- 208 pin PQFP.

- Engineered for Modern Standards
- Plug and Play compliant.
- VESA Display Data Channel (DDC2B) protocol support.
- VESA standard Feature Connector support.
- DPMS and advanced power management support.

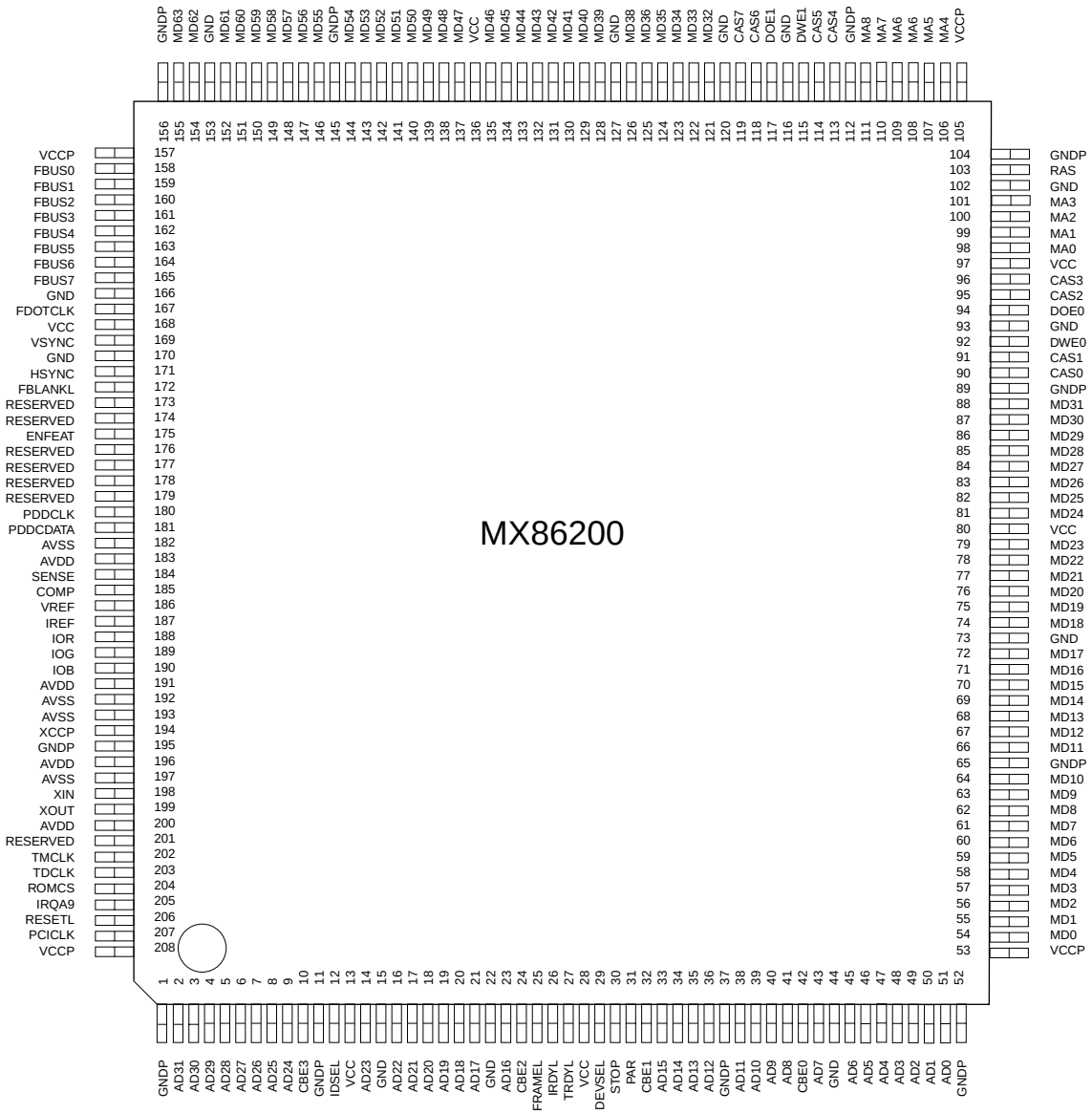
OVERVIEW

The MX86200 is an advanced 64-bit GUI and Video Accelerator. Integrating a 64-bit graphics coprocessor, 135 MHz RAMDAC and programmable clock synthesizer, the MX86200 is a complete low-cost and high-performance PC graphics / video solution. Performance of the memory subsystem was a key design consideration of the MX86200.

Utilizing the regular DRAM with 65 MHz memory clock, DRAM bandwidth can exceed 250 MB/sec. This bandwidth gives top-end Windows performance and smooth video playback in a low-cost DRAM system.

MX86200

PIN ASSIGNMENT



Power-on Reset Strapping

There are 13 pins used for strapping, all these pins should have internal pull-down resistor (pull-down has value of about 50K Ohm), if the intended logic level is "0" that pin can be left open, if a "1" is desired, an external 10K Ohm pull-up need be used.

MD40: Reserved must set to 0

MD41: DRAMTYPE0, DRAM Type used
0:256Kx16 (1 CAS#, 2 WE#), 256Kx4, 256Kx8
1:256Kx16 (2 CAS#, 1 WE#), 256Kx4, 256Kx8

MD43: MS2: MCKSEL0

MD44: MS1: MCKSEL1

MD45: MS0: MCKSEL2

Memory Clock Frequency Table:

MCKSEL[2:0]	Memory Clock selected
0 0 0	50.00 MHz
0 0 1	55.00 MHz
0 1 0	58.00 MHz
0 1 1	60.00 MHz
1 0 0	62.00 MHz
1 0 1	65.00 MHz
1 1 0	70.00 MHz
1 1 1	72.00 MHz

MD46: TYPICAL DRAM.
0: EDO DRAM on board
1: typical DRAM on board

MD47: KILLGUI. 0: Enable GUI. 1: Disable GUI.

MD48: DISVCG. 0: Enable internal VCG. 1: Disable internal VCG.

GUI PIN DESCRIPTION

PCI BUS INTERFACE PINS:

Pin Name	Pin No.	Type	Description
RESET#	206	I	This input is PCI bus ESET#, it is an active low signal used to initialize the GUI to a known state. The trailing edge of this input loads the power on strapping inputs through MD40 to MD52. The power on strap ping input pins each has an internally weakly pulled down resistor (about 50K Ohm). If a power on reset input status is needed, then the corresponding pin doesn't need an externally pulled up resistor. If a power on reset input status is needed, then the corresponding pin must be pulled up by a 10K Ohm resistor.
PCICLK	207	I	This input is LCLK, it is the PCI bus clock. It is an 1X clock of 33MHz.
FRAME#	25	I	This input is FRAME#, it is low to indicate the GUI that a valid address is present on the PCI address bus and a New bus cycle or Burst bus cycles are starting. GUI should use this signal to latch the address lines or any decodes developed from them and any bus commands.
IRDY#	26	I	This input is Initiator RDY#, it is generated from an PCI Bus Master. When it is low, IRDY# indicates that the Initiator is able to complete the current bus trans action if and only if the TRDY# is also low.
TRDY#	27	STO	This output is Target RDY#, it is generated by GUI if the current bus cycle belongs to the GUI. When it is low, TRDY# indicates that the GUI is able to complete the current bus transaction which already targeted onto it if and only if the IRDY# is also low. It remains low until this current cycle ends, then goes into high for one PCI clock cycle, after that then goes into tri-state.
DEVSEL#	29	STO	This output is DEVSEL#. When driven low, it indicates that GUI will respond to the current cycle. It remains low until this current cycle ends, then goes into high for one PCI clock cycle, after that then goes into tri-state.
STOP#	30	STO	This output is STOP#. When driven low, it indicates that GUI will request the current bus master to stop the current bus transfer. It remains low until this current cycle ends, then goes into high for one PCI clock cycle, after that then goes into tri-state.
PAR	31	TO	This output is PAR. It is only driven during PCI bus master doing read accesses from GUI. When driven, it will provide an even parity accross the AD[31:0], and C/BE#[3:0]. This signal is an tri-state output.

PCI BUS INTERFACE PINS:(Continued)

Pin Name	Pin No.	Type	Description
IRQA9#	205	TO	This output is INTA#. It is and interrupt request signal to system interrupt controller. This signal always hard wired to the PCI bus INTA# signal pin. It is an open drained output. This pin is typically unused in display subsystem design, but may be connected to IRQ9 via PCI configuration register.
IDSEL#	12	I	It is used as an Initialization Device Select during PCI bus Auto- configuration cycles. When high, it indicates that GUI is now selected as a target for PCI bus configuration cycles.
CBE0#	42	I	This multiplexed input is part of a PCI bus Command's definition or a Byte Enalbe for byte lane 0. During address phase of a PCI bus transaction, it defines the Command. During data phase of a PCI bus transaction, it defines If byte lane 0 is engaged in the transfer or not.
CBE3#	10	I	This multiplexed input is part of a PCI bus Command's definition or a Byte Enalbe for byte lane 3. During address phase of a PCI bus transaction, it defines the Command. During data phase of a PCI bus transaction, it defines if byte lane 3 is engaged in the transfer or not. The PCI bus Commands are defined as below: C\BE[3:0]# PCI bus Command Type ---------- ---------- 0000 Interrupt Acknowledge 0001 Special Cycle 0010 I/O Read 0011 I/O Write 0100 reserved 0101 reserved 0110 Memory Read 0111 Memory Write 1000 reserved 1001 reserved 1010 Configuration Read 1010 Configuration Write 1100 Memory Read Multiple 1101 Dual Address Cycle 1110 Memory Read Line 1111 Memory Write and Invalidate

PCI BUS INTERFACE PINS:(Continued)

Pin Name	Pin No.	Type	Description
CBE1#	32	I	This multiplexed input is part of a PCI bus Command's definition or a Byte Enalbe for byte lane 1. During address phase of a PCI bus transaction, it defines the Command. During data phase of a PCI bus transaction, it defines if byte lane 1 is engaged in the transfer or not.
CBE2#	24	I	This multiplexed input is part of a PCI bus Command's definition or a Byte Enalbe for byte lane 2. During address phase of a PCI bus transaction, it defines the Command. During data phase of a PCI bus transaction, it defines if byte lane 2 is engaged in the transfer or not.
AD0\ROMA0	51	I/O	This is a multiplexed/muti-function pin. This io pin directly connected to the PCI bus AD0 and the ROM BIOS Address0. During PCI bus transactions (as io pin)it is used by GUI as a multiplexed Address and Data bus bit0 for PCI. During PCI reading from the GUI BIOS area (as output pin), GUI will internally latch the accessing address and insert any required PCI bus wait states in order to convert this BIOS read/fetch command into GUI BIOS ROM local read cycle(s). GUI will output the converted BIOS ROM address bit0 through this sigal to the BIOS ROM. GUI will also send out a BIOS ROM Chip Select signal to the GUI BIOS ROM. After the local ROM BIOS read cycle(s) complete, GUI will send out the TRDY# together the read data to PCI to indicate the end of the current PCI bus transaction.
AD1\ROMA1	50	I/O	This is a multiplexed/muti-function pin. This io pin directly connected to the PCI bus AD1 and the ROM BIOS Address1. This pin is used as DAC data bus bit 1. When setting configuration at DACTST, this pin is used as DAC data bus input bit 1.
AD2\ROMA2	49	I/O	This is a multiplexed/muti-function pin When setting configuration not at DACTST, this io pin directly connected to the PCI bus AD2 and the ROM BIOS Ad dress2.
AD3\ROMA3	48	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD3 and the ROM BIOS Address3.
AD4\ROMA4	47	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD4 and the ROM BIOS Address4.
AD5\ROMA5	46	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD5 and the ROM BIOS Address5.
AD6\ROMA6	45	I/O	This is a multiplexed/muti-function pin This io input pin directly connected to the PCI bus AD6 and the ROM BIOS Address6.

PCI BUS INTERFACE PINS:(Continued)

Pin Name	Pin No.	Type	Description
AD7\ROMA7	43	I/O	This is a multiplexed/muti-function pin. This io pin directly connected to the PCI bus AD7 and the ROM BIOS Address7.
AD8\ROMA8	41	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD8 and the ROM BIOS Address8.
AD9\ROMA9	40	I/O	This is a multiplexed/muti-function pin. This io pin directly connected to the PCI bus AD9 and the ROM BIOS Address9.
AD10\ ROMA10	39	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD10 and the ROM BIOS Address10.
AD11\ ROMA11	38	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD11 and the ROM BIOS Address11.
AD12\ ROMA12	36	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD12 ROM BIOS Address12.
AD13\ ROMA13	35	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD13 and the ROM BIOS Address13.
AD14\ ROMA14	34	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD14 and the ROM BIOS Address14.
AD15\ ROMA15	33	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD15 ROM BIOS Address15.
AD16	23	I/O	This is a multiplexed pin. Whis io pin connects to the PCI bus AD16. It is used to pass the Address/Data during the Address phase/Data phase, respectively, of PCI bus transactions.
AD17	21	I/O	This is a multiplexed pin. This io pin connects to the PCI bus AD17. It is used to pass the Address/Data during the Address phase/Data phase, respectively, of PCI bus transactions.
AD18	20	I/O	This is a multiplexed pin. This io pin connects to the PCI bus AD18. It is used to pass the Address/Data during the Address phase/Data phase, respectively, of PCI bus transactions.
AD19	19	I/O	This is a multiplexed pin. this io pin connects to the PCI bus AD19. It is used to pass the Address/Data during the Address phase/Data phase, respectively, of PCI bus transactions.
AD20	18	I/O	This is a multiplexed pin. This io pin connects to the PCI bus AD20. It is used to pass the Address/Data during the Address phase/Data phase, respectively, of PCI bus transactions.

PCI BUS INTERFACE PINS:(Continued)

Pin Name	Pin No.	Type	Description
AD21	17	I/O	This is a multiplexed pin. This pin connects to the PCI bus AD21. It is used to pass the Address/Data during the Address phase/Data phase, respectively, of PCI bus transactions.
AD22	16	I/O	This is a multiplexed pin. This io pin connects to the PCI bus AD22. It is used to pass the Address/Data during the Address phase/Data phase, respectively, of PCI bus transactions.
AD23	14	I/O	This is a multiplexed pin. This io pin connects to the PCI bus AD23. It is used to pass the Address/Data during the Address phase/Data phase, respectively, of PCI bus transactions.
AD24\ROMD0	9	I/O	This is a multiplexed/muti-function pin. This io pin directly connected to the PCI bus AD24 and the ROM BIOS Data0. During PCI bus transactions it is used by GUI as a multiplexed Address and Data bus bit24 for PCI. During PCI reading from the GUI BIOS area, GUI will internally latch the accessing ROM BIOS Data bit0 through this pin and stores this read data into a internal double word buffer. After the local ROM BIOS read cycle(s) complete, GUI will send out the TRDY# together with the read data to PCI to indicate the end of the current PCI bus transaction.
AD25\ROMD1	8	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD25 and the ROM BIOS Data1.
AD26\ROMD2	7	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD26 and the ROM BIOS Data2.
AD27\ROMD3	6	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD27 and the ROM BIOS Data3.
AD28\ROMD4	5	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD28 and the ROM BIOS Data4.
AD29\ROMD5	4	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD29 and the ROM BIOS Data5.
AD30\ROMD6	3	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD30 and the ROM BIOS Data6.
AD31\ROMD7	2	I/O	This is a multiplexed/muti-function pin This io pin directly connected to the PCI bus AD31 and the ROM BIOS Data7.

DRAM INTERFACE PINS:

Pin Name	Pin No.	Type	Description
RAS#	103	O	This output is RAS#, it is the RAS address strobe for the two banks of DRAM memory of DRAM type 256Kx4, 256Kx8, 256Kx16 (1 CAS, 2 WE), 256Kx16 (2 CAS, 1 WE).
CAS0#	90	O	This output is CAS0#, it is the CAS address strobe of byte lane 0 for DRAM configuration type (2CAS#, 1WE#). This output is WE0#, it is the WE# control signal of byte lane 0 for DRAM configuration type (1CAS#, 2WE#).
CAS1#	91	O	This output is CAS1#, it is the CAS address strobe of byte lane 1 for DRAM configuration type (2CAS#, 1WE#). This output is WE1#, it is the WE# control signal of byte lane 1 for DRAM configuration type (1CAS#, 2WE#).
CAS2#	95	O	This output is CAS2#, it is the CAS address strobe of byte lane 2 for DRAM configuration type (2CAS#, 1WE#). This output is WE3#, it is the WE# control signal of byte lane 2 for DRAM configuration type (1CAS#, 2WE#).
CAS3#	96	O	This output is CAS3#, it is the CAS address strobe of byte lane 3 for DRAM configuration type (2CAS#, 1WE#). This output is WE3#, it is the WE# control signal of byte lane 3 for DRAM configuration type (1CAS#, 2WE#).
CAS4#	112	O	This output is CAS4#, it is the CAS address strobe of byte lane 4 for DRAM configuration type (2CAS#, 1WE#). This output is WE4#, it is the WE# control signal of byte lane 4 for DRAM configuration type (1CAS#, 2WE#).
CAS5#	113	O	This output is CAS5#, it is the CAS address strobe of byte lane 5 for DRAM configuration type (2CAS#, 1WE#). This output is WE5#, it is the WE# control signal of byte lane 5 for DRAM configuration type (1CAS#, 2WE#).
CAS6#	117	O	This output is CAS6#, it is the CAS address strobe of byte lane 6 for DRAM configuration type (2CAS#, 1WE#). This output is WE6#, it is the WE# control signal of byte lane 6 for DRAM configuration type (1CAS#, 2WE#).
CAS7#	118	O	This output is CAS7#, it is the CAS address strobe of byte lane 7 for DRAM configuration type (2CAS#, 1WE#). This output is WE7#, it is the WE# control signal of byte lane 7 for DRAM configuration type (1CAS#, 2WE#).
WE0#	92	O	This output is WE0#, it is the WE# control signal of bank 0 for DRAM configu ration type (2CAS#, 1WE#). This output is CAS0#, it is the CAS address strobe of bank 0 for DRAM configuration type (1CAS#, 2WE#).

DRAM INTERFACE PINS:(Continued)

Pin Name	Pin No.	Type	Description
WE1#	114	O	This output is WE1#, it is the WE# control signal of bank 1 for DRAM configu ration type (2CAS#, 1WE#). This output is CAS1#, it is the CAS address strobe of bank 1 for DRAM configuration type (1CAS#, 2WE#).
DOE0#	94	O	This output is OE0#, it is the DOE# control signal of bank 0 for DRAM.
DOE1#	116	O	This output is OE1#, it is the DOE# control signal of bank 1 for DRAM.
MA0	98	O	This output is MA0, it is the DRAM memory address bus for both banks. It is used to pass the RAS address and CAS address to DRAMs.
MA1	99	O	This output is MA1, it is the DRAM memory address bus for both banks. It is used to pass the RAS address and CAS address to DRAMs.
MA2	100	O	This output is MA2, it is the DRAM memory address bus for both banks. It is used to pass the RAS address and CAS address to DRAMs.
MA3	101	O	This output is MA3, it is the DRAM memory address bus for both banks. It is used to pass the RAS address and CAS address to DRAMs.
MA4	106	O	This output is MA4, it is the DRAM memory address bus for both banks. It is used to pass the RAS address and CAS address to DRAMs.
MA5	107	O	This output is MA5, it is the DRAM memory address bus for both banks. It is used to pass the RAS address and CAS address to DRAMs.
MA6	108	O	This output is MA6, it is the DRAM memory address bus for both banks. It is used to pass the RAS address and CAS address to DRAMs.
MA7	109	O	This output is MA7, it is the DRAM memory address bus for both banks. It is used to pass the RAS address and CAS address to DRAMs.
MA8	110	O	This output is MA8, it is the DRAM memory address bus for both banks. It is used to pass the RAS address and CAS address to DRAMs.
MD0	54	I/O	MD[7:0] is the DRAM data bus of memoryplane 0 of bank 0 or bank 1.
MD1	55		
MD2	56		
MD3	57		
MD4	58		
MD5	59		
MD6	60		
MD7	61		

DRAM INTERFACE PINS:(Continued)

Pin Name	Pin No.	Type	Description
MD8	62	I/O	MD[15:8] is the DRAM data bus of memory plane 1 of bank 0 or bank 1.
MD9	63		
MD10	64		
MD11	66		
MD12	67		
MD13	68		
MD14	69		
MD15	70		
MD16	71	I/O	MD[23:16] is the DRAM data bus of memory plane 2 of bank 0 or bank 1.
MD17	72		
MD18	74		
MD19	75		
MD20	76		
MD21	77		
MD22	78		
MD23	79		
MD24	81	I/O	MD[31:24] is the DRAM data bus of memory plane 3 of bank 0 or bank 1.
MD25	82		
MD26	83		
MD27	84		
MD28	85		
MD29	86		
MD30	87		
MD31	88		
MD32	120	I/O	MD[39:32] is the DRAM data bus of memory plane 4 of bank 0 or bank 1.
MD33	121		
MD34	122		
MD35	123		
MD36	124		
MD37	125		
MD38	126		
MD39	128		

DRAM INTERFACE PINS:(Continued)

Pin Name	Pin No.	Type	Description
MD40	129	I/O	MD[47:40] is the DRAM data bus of memory plane 5 of bank 0 or bank 1.
MD41	130		
MD42	131		
MD43	132		
MD44	133		
MD45	134		
MD46	135		
MD47	137		
MD48	138	I/O	MD[55:48] is the DRAM data bus of memory plane 6 of bank 0 or bank 1.
MD49	139		
MD50	140		
MD51	141		
MD52	142		
MD53	143		
MD54	144		
MD55	146		
MD56	147	I/O	MD[63:56] is the DRAM data bus of memory plane 7 of bank 0 or bank 1.
MD57	148		
MD58	149		
MD59	150		
MD60	151		
MD61	152		
MD62	154		
MD63	155		

ROM BIOS INTERFACE PINS:

Pin Name	Pin No.	Type	Description
ROMCS#	204	O	This output is ROMCS#. It may be connected both to the BIOS ROM chip select and output enable pins directly.

INTERNAL VCG RELATED INTERFACE PINS:

Pin Name	Pin No.	Type	Description
XIN	198	I	This input is used as a Reference Frequency Input for internally implemented oscilator. An external crystal or oscilator of 14.318MHz may be used. If an external crystal is used, it must be connected between XIN and XOUT. If an external oscilator is used, it must connect to XIN. In this case, the XOUT must be left open.
XOUT	199	O	This is used as a Reference Frequency output for internally implemented oscilator. If an external crystal is used, it must be connected between XIN and XOUT. If an external oscilator is used, the XOUT must be left open.

INTERNAL RAMDAC RELATED INTERFACE PINS:

Pin Name	Pin No.	Type	Description
VREF	186	I	This pin is indicated the Voltage Reference of 1.2V for internal DAC and Moni tor Sence logic. It must be connected with a 0.1u capacitor to AVCC of RAMDAC.
COMP	185	I	This pin is the Compensation input for internal DAC. It must be connected with a 0.1u capacitor to AVCC of RAMDAC.
IREF	187	I	This pin is indicated the Current Reference.
IOR	188	O	This pin is the analog output of the pixel color Red component to monitor. It has a voltage level of 0.0V(blank) to 0.7V(full scale) when terminated with 75 ohm double loads.
IOG	189	O	This pin is the analog output of the pixel color Green component to monitor. It has a voltage level of 0.0V(blank) to 0.7V(full scale) when terminated with 75 ohm double loads.
IOB	190	O	This pin is the analog output of the pixel color Blue component to monitor. It has a voltage level of 0.0V(blank) to 0.7V(full scale) when terminated with 75 ohm double loads.

EXTERNAL MONITOR RELATED INTERFACE PINS:

Pin Name	Pin No.	Type	Description
HSYNC	171	O	This output is HSYNC, it is the horizontal sync to analog monitor.
VSYNC	169	O	This output is VSYNC, it is the vertical sync to analog monitor.
DDCLK	180	O	This output is DDCCLK, it is the Clock to analog monitor when Display Data Channel mechanism 2 is enabled and selected.
DDCDATA	181	O	This bidirection pin is DDCDATA, it is used to pass the DDC Command/Data to/ from analog monitor when any kind of Display Data Channel mechanisms is enabled and selected.
SENSE	184	IO	This input is the MONITOR SENSE of the R,G,B comparator output from RAMDAC. It is used to detect the analog monitor type attached to the GUI. When setting configuration at GUIONLY, this pin is used as input from external DAC. When setting configuration at DACTST, this pin is used as output from internal DAC. When setting configuration at 3 in 1, DISVCG, this pin is of no use.

FEATURE CONNECTOR INTERFACE PINS:

Pin Name	Pin No.	Type	Description
ENFEAT#	175	I	This pin is used to enable the feature connector interface functions. For VGA feature connector compatible mode. This pin is pulled up with a 10K resistor. When high, it is used to enable the FDOTCLK, FBLANK#, VHSYNC, VSYNC, FBUS[7:0] output signals to VGA compatible feature connector. When low, all of these signal pins are tri-stated.
FDOTCLK	167	IO	Set up for VGA feature connector compatible mode as well as ENFEAT# is high, the pixel clock , being internally driven to RAMDAC, is also driven to this pin. If ENFEAT is low, it is tri-stated.
FBLANK#	172	IO	Set up for VGA feature connector compatible mode as well as ENFEAT# is high, the BLANK# signal, being internally driven to RAMDAC, is also driven to this pin. If ENFEAT is low, it is tri-stated.
FBUS0\DACD0	158	IO	This pin is FBUS0.
FBUS1\DACD1	159	IO	This pin is FBUS1.
FBUS2\DACD2	160	IO	This pin is FBUS2.
FBUS3\DACD3	161	IO	This pin is FBUS3.
FBUS4\DACD4	162	IO	This pin is FBUS4.
FBUS5\DACD5	163	IO	This pin is FBUS5.
FBUS6\DACD6	164	IO	This pin is FBUS6.
FBUS7\DACD7	165	IO	This pin is FBUS7. Setting up for VGA feature connector compatible mode as well as ENFEAT is high, the FBUS0 to FBUS7 bus, being internally driven to RAMDAC, are also driven to these pins. If ENFEAT is low, they are tri-stated.
TMCLK	202	IO	This pin is used as memory clock and can be driven output for observation by pulling up power on strapped pin MD40(VCGDBG), or it will be tristated.
TDCLK	203	IO	This pin used as dot clock and can be driven output for observation by pulling up power on strapped pin MD40(DBVCG), or it will be tristated.
Reserved	173,174,176,177,178,179,201		

POWER PINS:

PIN NAME	PIN TYPE	PIN NO.	DRIVE(ma)	C_LOAD(pf)
VCCP	-	53,105,157,194,208	-	-
GNDP	-	1,11,37,52,65,89,104,111,145,156,195	-	-
VCC	-	13,28,80,97,136,168	-	-
GND	-	15,22,44	-	-
		73,93,102,115, 119,127,153,166, 170		
AVDD	-	183,191,196,200	-	-
AVSS	-	182,192,193,197	-	

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