Savage4 Graphics/Video Accelerators
E Step Information

Introduction

The following stepping information is for the E step silicon of the S3® Savage4™ graphics/video accelerator family. Each stepping item applies to all family members unless otherwise noted. Following this Introduction are a section describing how to identify the chips covered by this document, a summary of known problems and a detailed description of each problem.

Identification

The parts can be identified by two means. The first is by the physical markings on the part itself. The second is through software by reading register CR2D (= 8A), CR2E (= 22H) and CR2F (= 04H).

Rev. E parts are identified on the package by the marking QzzzFE, where z can be any letter.

The part numbers for the various Savage4 family members are:

Part Number	Part Name
86C394	Savage4 LT™
86C395	Savage4 GT™
86C396	Savage4 PRO-M™
86C396P	Savage4 PRO-M™143
86C397	Savage4 PRO™
86C397P	Savage4 PRO 143

Note: Engineering samples are marked 86E39x.

Summary of Known Problems

Note: Missing #s are for problems fixed in Rev. B, C or D. See the Rev. B stepping (SI045-C), Rev. C stepping (SI047-B) or Rev. D stepping (DI050-B) for details.

#	Description	N/R	Fix
2	Host Monochrome Source ROP		S/W
21	32-bit Memory Interface		Rev. E
29	Gamma Correction With Streams Processor and Flat Panel		S/W
30	Negative-x Starting Coordinates		S/W
36	Boot-up Limitation with Phoenix BIOS and BX Motherboards		S/W
40	BCI 2D Repeat Data		S/W
42	Destination Flush		S/W
50	Secondary Stream overlay on VGA with Tiling Enabled		Rev. E

Legend:

N/R This column indicates whether the problem description and/or solution is NEW or REVISED. These items will also be highlighted in BOLD face type.

FIX This column indicates whether the problem was fixed and when.

Problem Descriptions

#	Problem Description	N/R	Fix
2	Host Monochrome Source ROP		S/W

All 2D drawing operations that use a host monochrome source ROP in 8 bpp modes will cause a hang.

Solution/Workaround:

Drivers must not use this ROP in 8 bpp modes.

#	Problem Description	N/R	Fix
21	32-bit Memory Interface		Rev. E

32-bit memory interface accesses may result in dropped pixels for certain 2D and 3D operations.

Solution/Workaround:

None. This problem is fixed in Rev. E.

#	Problem Description	N/R	Fix
29	Gamma Correction With Streams Processor and Flat Panel		S/W

Enabling gamma correction (SR1B_3 = 1) with the Streams Processor and flat panel enabled results in an incorrect display.

Solution/Workaround:

The software will disable gamma when playing back with the Streams Processor and flat panel.

#	Problem Description	N/R	Fix
30	Negative-x Starting Coordinates		S/W

Any 2D engine operation starting with negative-x coordinates may result in an incorrect drawing location.

Solution/Workaround:

If negative-x operations are performed, the software driver should use software clipping to clip out the negative portion of the drawing.

#	Problem Description	N/R	Fix
36	**Boot-up Limitation with Phoenix BIOS and BX Motherboards**		**S/W**

If the AGP aperture is set to 256 MB in the CMOS setup options screen, the system BIOS does not properly initialize Savage4-based add-in cards on BX motherboards using Phoenix system BIOS version P10 and earlier.

Solution/Workaround:

The most recent Phoenix BIOS updates for the Intel Seattle (SE440BX) and Seattle-2 (SE440BX-2) motherboards can be found at http://www.developer.intel.com/design/motherbd/se/se_bios.htm and http://www.developer.intel.com/design/motherbd/se2/se2_bios.htm, respectively.

#	Problem Description	N/R	Fix
40	**BCI 2D Repeat Data**		**S/W**

Repeated 2D commands normally do not require the command header be re-sent when the same operation is repeated. Instead, only the changed data need be sent. If command DMA is used to fetch the 2D command and repeated data, the repeat data will be improperly interpreted. This problem also exists for earlier chip revisions.

Solution/Workaround:

After specifying the DMA base address for each set of repeat 2D command data, insert a dummy SetRegister command before kicking off the DMA of the repeat data.

#	Problem Description	N/R	Fix
42	**Destination Flush**		**S/W**

If the ECLK frequency is greater than the MCLK frequency, enabling destination flush (MM48584_30 = 1) can cause a hang. This problem also exists for earlier chip revisions.

Solution/Workaround:

MM485EC_31-30 were added for Rev. C. Programming these to 01b is required whenever destination flush is enabled.

#	Problem Description	N/R	Fix
50	**Automatic Centering and Expansion with Secondary Stream Tiling**		**Rev. E**

When a secondary stream is enabled with flat panel output and automatic centering and expansion turned on, CR67_3-2 is programmed to 01b. (secondary stream overlaid on VGA primary stream). Under these conditions, the secondary stream tiling bit (MM81D8_31) is not effective and tiled secondary stream input is not displayed correctly.

Solution/Workaround:

This problem is fixed in Rev. E.