



# Intel<sup>®</sup> 852GM/852GMV Chipset Graphics and Memory Controller Hub (GMCH)

Datasheet

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*June 2004*

Order Number: 252407-004



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## Revision History

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Document No.	Rev.	Description	Date
252407	001	Initial release	January 2003
252407	002	Revisions include: Added support for Intel Celeron M processor	January 2004
252407	003	Revisions include: Added 852GMV features and system diagram to features section	February 2004
252407	004	Revisions include: Added support for Intel Celeron D processor on 90 nm process and in the 478-pin package	June 2004



## Intel® 852GM Chipset GMCH Product Features

- Processor/Host Bus Support
  - Intel® Celeron® processor (478-pin package)
    - Supports the processor subset of the Enhanced Mode Scalable bus protocol 2X Address, 4X data Intel Celeron processor System Bus interrupt delivery
  - Mobile Intel® Pentium® 4 Processor-M (478-pin package)
    - Supports the subset of the Enhanced Mode Scalable bus protocol
    - Mobile Intel Pentium 4 Processor-M System Bus interrupt delivery
    - Supports system bus at 400-MHz or 3.2 GB/s
    - Supports host Dynamic Bus Inversion (DBI)
      - Supports 32-bit host bus addressing
      - 12-deep In-Order-Queue
      - AGTL+ bus driver technology with integrated AGTL termination resistors
    - Supports Enhanced Intel SpeedStep® technology
  - Intel® Celeron® M processor
    - 400-MHz front side bus frequency.
    - Source synchronous double pumped address (2X)
    - Source synchronous quad pumped data (4X)
    - FSB interrupt delivery
    - Supports Host bus dynamic bus inversion (DBI)
    - Supports 32-bit host bus addressing
    - 8-deep in-order queue
    - AGTL+ bus driver technology with integrated AGTL+ termination resistors
- Memory System
  - Directly supports one DDR SDRAM channel, 64-bits wide
  - Supports 200/266-MHz DDR SDRAM devices with max of 2 Double-Sided SO-DIMMs (4 rows populated) with unbuffered PC1600/PC2100 DDR
    - Triangle Lists, Strips and Fans support
  - SDRAM (without ECC)
    - Supports 128-Mbit, 256-Mbit, and 512-Mbit technologies providing maximum capacity of 1-GB with x16 devices and up to 2-GB with high density 512-Mbit technology
    - All supported devices have 4 banks
    - Supports up to 16 simultaneous open pages
    - Supports page sizes of 2-kB, 4-kB, 8-kB, and 16-kB. Page size is individually selected for every row (UMA support only)
- System Interrupts
  - Supports Intel 8259 and FSB interrupt delivery mechanism
  - Supports interrupts signaled as upstream Memory Writes from PCI and Hub Interface
  - MSI sent to the CPU through the System Bus
- Internal Graphics Features
  - Up to 64-MB of Dynamic Video Memory Allocation
  - Display Image Rotation
  - Core Frequency
    - Display Core frequency of 133-MHz
    - Render Core frequency of 133-MHz
  - 2D Graphics Engine
    - Optimized 128-bit BLT engine
    - Ten programmable and predefined monochrome patterns
    - Alpha Stretch Blt (via 3D pipeline)
    - Anti-aliased lines
    - Hardware-based BLT Clipping and Scissoring
    - 32-bit Alpha Blended cursor
    - Programmable 64 x 64 3-color Transparent cursor
    - Color Space Conversion
    - 3 Operand Raster BLTs
    - 8-bit, 16-bit, and 32-bit color ROP support
    - DIB translation and Linear/Tile addressing
  - 3D Graphics Engine
    - 3D Setup and Render Engine
    - Viewpoint Transform and Perspective Divide

- Indexed Vertex and Flexible Vertex formats
- Pixel accurate Fast Scissoring and Clipping operation
- Backface Culling support
- DirectX\* and OGL Pixelization rules
- Anti-Aliased Lines support and Sprite Points support
- Provides the highest sustained fill rate performance in 32-bit color and 24-bit W mode
- High quality performance Texture Engine
- 266-Mega Texel/s peak performance
- Per Pixel Perspective Corrected Texture Mapping
- Single Pass Texture Compositing(Multi-Textures) at rate Enhanced Texture Blending functions
- IOxAPIC in ICH4-M provides redirection for upstream interrupts to the System Bus
- Video Stream Decoder
      - HW Motion Compensation for MPEG2
      - All format decoder (18 ATSC formats) supported
      - Dynamic Bob and Weave support for Video Streams
      - Support for standard definition DVD quality encoding at low CPU utilization
    - Video Overlay
      - Single high quality scalable Overlay and second Sprite to support second Overlay
      - Multiple Overlay functionality provided via Arithmetic Stretch BLT (Block Transfer)
      - 5-tap horizontal, 3-tap vertical filtered scaling
      - Multiple Overlay formats
      - Direct YUV from Overlay to TV-out
      - Independent Gamma Correction
      - Independent Brightness / Contrast / Saturation
      - Independent Tint / Hue support
      - Color Specular Lighting
      - Z Bias support
      - Dithering
      - Line and Full-Scene Anti-Aliasing
      - 16 and 24-bit Z Buffering
  - Destination Colorkeying
    - Source Chromakeying
    - Multiple hardware color cursor support (32-bit with alpha and legacy 2-bpp mode)
      - Accompanying I2C and DDC channels provided through multiplexed interface
    - Display
      - Analog Display Support
      - 350-MHz integrated 24-bit RAMDAC that can drive a standard progressive scan analog monitor with pixel resolution up to 1600x1200 at 85-Hz and up to 1920x1440 at 60-Hz
      - Dual independent pipe support
      - Concurrent: Different images and native display timings on each display device
      - DVO (DVOC) support
      - Digital video out port DVOC with 165-MHz dot clock on 12-bit double pumped interface
      - Digital video out port DVOC with 165-MHz dot clock on 12-bit double pumped interface
      - Variety of DVO devices supported
      - Compliant with DVI Specification 1.0
      - Support display resolution up to 1400x1050 @ 75 Hz
      - Dedicated LFP (local flat panel) LVDS interface
      - Twelve Level of Detail MIP Map Sizes from 1x1 to 2 Kx2 K
      - Numerous Texture formats including 32-bit RGBA
      - Alpha and Luminance Maps
      - Texture Chromakeying
      - Bilinear, Trilinear, and Anisotropic MIP-Mapped Filtering
      - Cubic Environment Reflection Mapping
      - Embossed Bump-Mapping
      - DXTn Texture Decompression
      - FX1 Texture Compression
      - 3D Graphics Rasterization enhancements
      - One Pixel per clock
      - Flat and Gouraud Shading
      - Color Alpha Blending for Transparency
      - Vertex and Programmable Pixel Fog
      - Atmospheric effects



- 16 and 24-bit W Buffering
- 8-bit Stencil Buffering
- Double and Triple Render Buffer support
- 16 and 32-bit color
- Destination Alpha
- Vertex Cache
- Maximum 3D resolution of backlight inverter control
- Bi-linear Panel fitting
- 1600x1200 at 85-Hz (contact your Intel Field Representative for detailed display information, i.e. pixel depths, etc.)
- Optimal 3D resolution supported
- Fast Clear support
- ROP support
- Hub Interface to ICH4-M
  - 266 MB/s point-to-point Hub Interface to ICH4-M
  - 66-MHz base clock
- specification
- Integrated PWM interface for LCD backlight inverter control
- Bi-linear Panel fitting
- Package
  - 732-pin Micro-FCBGA (37.5 x 37.5 mm)
- Power Management
  - SMRAM space remapping to A0000h (128 kB)
  - Supports extended SMRAM space above 256-MB, additional 1-MB TSEG from Top of Memory, cacheable (cacheability controlled by CPU)
  - APM Rev 1.2 compliant power management
  - Supports Suspend to System Memory (S3), Suspend to Disk (S4) and Hard Off/Total Reboot (S5)
  - ACPI 1.0b, 2.0 Support
  - Single or dual channel LVDS panel support up to SXGA+(1400x1050 60-Hz) panel resolution with frequency range from 25-MHz to 112-MHz (single channel/dual channel)
  - SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
  - Supports data format of 18-bpp
  - LCD panel power sequencing compliant with SPWG timing specification



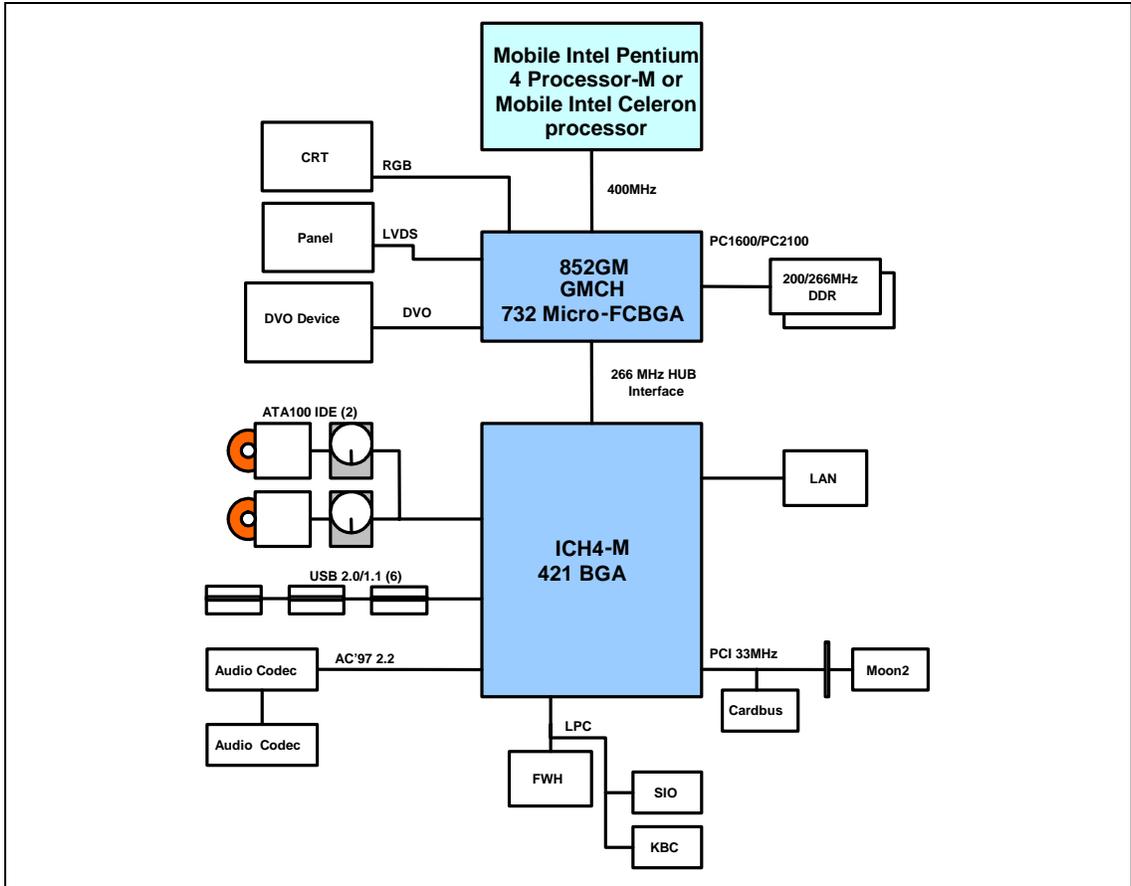
# Intel<sup>®</sup> 852GMV Chipset GMCH Product Features

**Note:** The Intel 852GMV chipset GMCH shares the same chipset features as the Intel 852GM chipset along with the additional features:

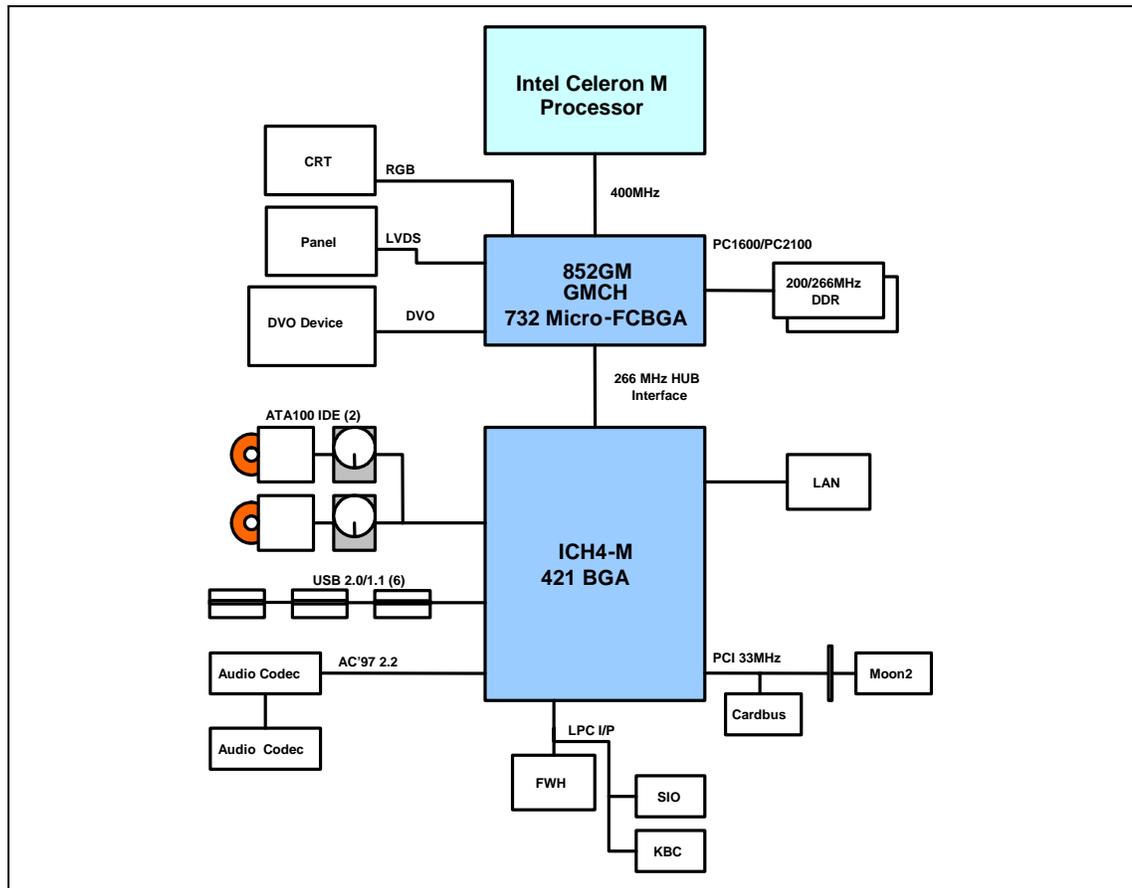
- Processor/Host Bus Support
  - Intel Celeron processor (478-pin FCPGA package, 0.13 micron process)
  - 2X Address, 4X data
  - Intel Celeron processor FSB interrupt delivery
  - Supports system bus at 400 MHz with Intel Celeron processor (0.13 micron process)
  - Supports system bus at 533 MHz with Intel Celeron D processor on 90 nm process and in the 478-pin package
- Memory System
  - Supports 200/266-MHz DDR SDRAM devices with max of 2 Double-Sided SO-DIMMs (4 rows populated) with unbuffered PC1600/PC2100 DDR SDRAM



### Mobile Intel Pentium 4 Processor-M or Mobile Intel Celeron Processor and Intel 852GM Chipset Block Diagram

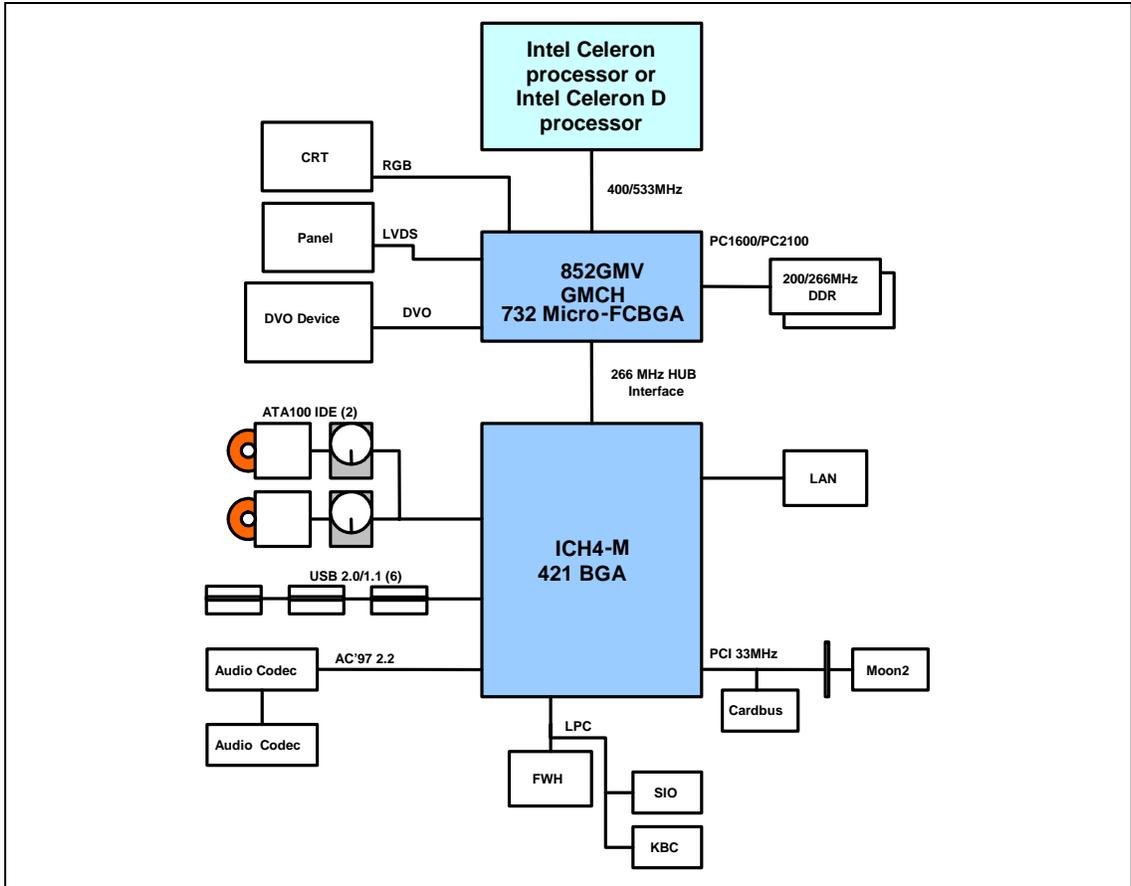


### Intel Celeron M Processor and Intel 852GM GMCH Chipset System Block Diagram





Intel Celeron Processor, Intel Celeron D Processor on 90 nm process and in the 478-pin package and Intel 852GMV GMCH Chipset System Block Diagram





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# 1. Introduction

This document provides the design specifications for the Intel® 852GM/GMV chipsets.

## 1.1. Terminology

Term	Description
BLI	Back Light Inverter
Core	The internal base logic in the Intel 852GM/852GMV GMCH
CPIS	Common Panel Interface Specification
CPU	Central Processing Unit
DBI	Dynamic Bus inversion
DBL	Display Brightness Link
DVO	Digital Video Out
DVI*	Digital Visual Interface is the interface specified by the DDWG (Digital Display Working Group) DVI Spec. Rev. 1.0 utilizing only the Silicon Image developed T.M.D.S. protocol
DVMT	Intel Dynamic Video Memory Technology
EDID	Extended Display Identification Data
Full Reset	A Full Intel 852GM/852GMV GMCH Reset is defined in this document when RSTIN# is asserted
GMCH	Graphics Memory Controller Hub
Hub Interface (HI)	The proprietary interconnect between the Intel 852GM/852GMV GMCH and the component. In this document, the Hub Interface cycles originating from or destined for the ICH4-M are generally referred to as Hub Interface cycles. Hub cycles originating from or destined for the primary PCI interface on are sometimes referred to as Hub Interface/PCI cycles
Host	This term is used synonymously with processor
IGD	Integrated Graphics Device
Intel 852GM/852GMV GMCH	Refers to the GMCH component
Intel 82801DBM ICH4-M	The component contains the primary PCI interface, LPC interface, USB 2.0, ATA-100, AC'97, and other I/O functions. It communicates with the Intel 852GM/852GMV GMCH over a proprietary interconnect called the Hub Interface. Throughout this datasheet, the Intel 82801DBM ICH4-M component will be referred to as the ICH4-M
IPI	Inter Processor Interrupt
LFP	Local Flat Panel
LVDS	Low voltage differential signals used for interfacing to LCD panels
MSI	Message Signaled Interrupts. MSI allow a device to request interrupt service via a standard memory write transaction instead of through a hardware signal
Primary PCI	Physical PCI bus that is driven directly by the component. It supports only 5-V, 33-MHz PCI or PCI0 2.2 compliant components. Communication between PCI0 and Intel



Term	Description
	852GM/852GMV GMCH occurs over the Hub Interface. Note that although the Primary PCI bus is referred to as PCI0, it is not PCI Bus #0 from a configuration standpoint
FSB	Processor System Bus. Connection between Intel 852GM/852GMV GMCH and the CPU. Also known as the Front Side Bus (FSB) or Host interface
PWM	Pulse Width Modulation
SSC	Spread Spectrum Clocking
System Bus	Processor-to-Intel 852GM/852GMV GMCH interface. The Enhanced Mode of the Scalable Bus is the P6 Bus plus enhancements, consisting of source synchronous transfers for address and data, and system bus interrupt delivery. The Mobile Pentium 4 Processor-M processor implements a subset of Enhanced Mode
UMA	Unified Memory Architecture with graphics memory for the IGD inside System Memory
VDL	Video Data Link

## 1.2. Reference Documents

Document	Location
<i>Mobile Intel® Pentium® 4 Processor –M Datasheet (250686), Mobile Intel Celeron® processor(251308), Intel Celeron® processor(290749)</i>	<a href="http://developer.intel.com">http://developer.intel.com</a>
<i>Intel® Celeron® M Processor Datasheet(300302)</i>	<a href="http://developer.intel.com">http://developer.intel.com</a>
<i>Intel® Celeron® D Processor on 90 nm Process and in the 478-pin Package Datasheet</i>	<a href="http://developer.intel.com">http://developer.intel.com</a>
<i>PCI Local Bus Specification 2.2</i>	<a href="http://www.pcisig.com">www.pcisig.com</a>
<i>Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet (252337)</i>	<a href="http://developer.intel.com/design/mobile/datashts/252337.htm">http://developer.intel.com/design/mobile/datashts/252337.htm</a>
<i>Mobile Intel® Pentium® 4 Processor-M, Intel® Celeron® M Processor, Mobile Intel® Celeron® Processor, and Intel® 852GME, Intel® 852GMV and Intel® 852PM Chipset Platforms Design Guide(25302601)</i>	<a href="http://developer.intel.com">http://developer.intel.com</a>
<i>Advanced Configuration and Power Management(ACPI) Specification 1.0b &amp; 2.0</i>	<a href="http://www.teleport.com/~acpi/">http://www.teleport.com/~acpi/</a>
<i>Advanced Power Management (APM) Specification 1.2</i>	<a href="http://www.microsoft.com/hwdev/busbios/amp_12.htm">http://www.microsoft.com/hwdev/busbios/amp_12.htm</a>
<i>IA-32 Intel® Architecture Software Developer Manual Volume 3: System Programming Guide</i>	<a href="http://developer.intel.com/design/Pentium4/manuals/24547203.pdf">http://developer.intel.com/design/Pentium4/manuals/24547203.pdf</a>
<i>Intel® Graphics Software PC 12.0 Product Requirements</i>	Contact your Intel Field Representative
<i>Common Panel Interface Specification Version 1.5</i>	Contact your Intel Field Representative

## 1.3. System Architecture Overview

### 1.3.1. Intel 852GM GMCH System Architecture

The Intel 852GM GMCH component provides the processor interface, DDR SDRAM interface, display interface, and Hub Interface in an Intel 852GM chipset platform. The Intel 852GM GMCH is optimized for the Mobile Intel Pentium 4 Processor-M, Mobile Intel Celeron processor and Intel Celeron M processor. It supports a single channel of DDR SDRAM memory. Intel 852GM Chipset contains advanced power management logic. The Intel 852GM Chipset platform supports the fourth generation mobile I/O Controller Hub to provide the features required by a mobile platform.

The Intel 852GM GMCH is in a 732-pin Micro-FCBGA package and contains the following functionality:

- Supports single Intel processor configurations at 400-MHz or 3 GB/s

- 1.2-1.30-V AGTL+ host bus supporting 32-bit host bus addressing with Enhanced Intel SpeedStep® technology (Intel Celeron M processor and Intel Celeron Processor do not support Enhanced Intel SpeedStep Technology).

- System Memory supports 200/266-MHz (SSTL\_2) DDR DRAM

- Up to 1 GB (with 256-Mb technology and two SO-DIMMs) of PC1600/2100 DDR SDRAM without ECC

- Integrated graphics capabilities, including 3D rendering acceleration and 2D hardware acceleration

- Integrated 350-MHz, 24-bit RAMDAC with pixel resolution up to 1600x1200 at 85-Hz and up to 1920x1440 @ 60 Hz

- One Dedicated Dual Channel LFP LVDS interface with frequency range of 25 MHz to 112 MHz (single channel/dual channel) for support up to SXGA+ (1400x1050 @ 60 Hz) panel resolutions with maximum pixel depth of 18-bpp

- Integrated PWM (Pulse Width Modulation) interface for LFP backlight inverter control for panel brightness

- One 165-MHz, 12-bit, DVO interface for TV-out encoder and DVI (LVDS transmitter and TMDS transmitter) support

- I2C and DDC channels supported

- Dual Pipe Independent Display with Tri-view support through LFP, DVO, and CRT

- Deeper Sleep state support

- Distributed arbitration for highly concurrent operation

### 1.3.2. Intel 852GMV GMCH System Architecture

The Intel 852GMV GMCH component provides the processor interface, DDR SDRAM interface, display interface, and Hub interface in an Intel 852GMV chipset platform. All features listed for Intel 852GM is supported for the Intel 852GMV. The GMCH is optimized for use with the Intel Celeron processor. It supports a single channel of DDR SDRAM memory. The 852GMV GMCH contains advanced power management logic. The Intel 852GMV chipset platform supports the fourth generation mobile I/O Controller Hub (ICH4-M) to provide the features required by a mobile platform.



The Intel 852GMV GMCH is in a 732-pin Micro-FCBGA package and contain the following functionality:

- Supports a single Intel Celeron processor configuration at 400 MHz
- Supports a single Intel Celeron D processor on 90 nm process and in the 478-pin package configuration at 533 MHz
- System SDRAM supports 200/266 MHz (SSTL\_2) DDR SDRAM
- Up to 1-GB (with 512 Mb technology and two SO-DIMMs) of PC1600/2100DDR SDRAM without ECC
- One 165-MHz, 12-bit, DVO interface for TV-out encoder and DVI (LVDS transmitter and TMDS transmitter) support
- Integrated 350-MHz, 24-bit RAMDAC with maximum pixel resolution support up to 1600x1200 at 85 Hz and up to 2048x1536 at 75 Hz
- One Dedicated Dual Channel LFP LVDS interface with frequency range of 25 MHz to 112 MHz (single channel/dual channel) for support up to UXGA (1600 x 1200 60 Hz) panel resolutions with maximum pixel depth of 18 bpp

## 1.4. Processor Host Interface

### 1.4.1. Intel 852GM GMCH Processor Host Interface

Mobile Intel Pentium 4 Processor-M key features include:

- Source synchronous double pumped address (2X)

- Source synchronous quad pumped data (4X)

- System bus interrupt and side-band signal delivery

In this mode, Intel 852GM GMCH supports:

- A 64B cache line size

- A Front Side Bus frequency of 400-MHz (dual processor is not supported)

- AGTL+ termination resistors on all of the AGTL+ signals

- 32-bit host bus addressing allowing the CPU to access the entire 4 GB of the Intel 852GM GMCH memory address space

Mobile Intel Celeron processor key features include:

- Support for a 400-MHz Front Side Bus frequency

- Source synchronous double pumped address (2X)

- Source synchronous quad pumped data (4X)

- System bus interrupt and side-band signal delivery

- AGTL+ termination resistors on all of the AGTL+ signals

- 32-bit host bus addressing allowing the CPU to access the entire 4-GB of the memory address space

Intel Celeron M processor key features include:

- Support for a 400-MHz Front Side Bus frequency

- Source synchronous double pumped address (2X)

- Source synchronous quad pumped data (4X)

- Front side bus interrupt delivery

- Low voltage swing V<sub>tt</sub> (1.05V)

- Dynamic Power Down (DPWR#) support

- Integrates AGTL+ termination resistors on all of the AGTL+ signals

- Supports 32-bit host bus addressing allowing the CPU to access the entire 4 GB of the GMCH memory address space

- An 8-deep, In-Order queue

- Support DPWR# signal

- Supports one outstanding defer cycle at a time to any particular I/O interface

Intel 852GM GMCH has an In-Order Queue to support outstanding pipelined address requests on the host bus. Intel 852GM GMCH supports one outstanding defer cycle at a time; however, it supports only one to any particular I/O interface. Host initiated I/O cycles are positively decoded to the Intel 852GM GMCH configuration space and subtractively decoded to the Hub Interface. Host initiated memory



cycles are positively decoded to the DDR SDRAM. Memory accesses initiated from the Hub Interface to DDR SDRAM will be snooped on the system bus.

## 1.4.2. Intel 852GMV GMCH Processor Host Interface

Intel Celeron processor (400 MHz) and Intel Celeron D processor on 90 nm process and in the 478-pin package (533 MHz) key features include:

- Source synchronous double pumped address
- Source synchronous quad pumped data
- System bus interrupt and side-band signal delivery
- AGTL+ termination resistors on all of the AGTL+ signals
- 32-bit host bus addressing allowing the CPU to access the entire 4-GB of the memory address space

Intel 852GMV GMCH has an In-Order Queue to support up to twelve outstanding pipelined address requests on the host bus. Intel 852GMV GMCH supports one outstanding defer cycle at a time; however, it supports only one to any particular I/O interface. Host initiated I/O cycles are positively decoded to the Intel 852GMV GMCH configuration space and subtractively decoded to the Hub Interface. Host initiated memory cycles are positively decoded to the DDR SDRAM. Memory accesses initiated from the Hub Interface to DDR SDRAM will be snooped on the system bus.

## 1.5. Intel 852GM/852GMV GMCH Host Bus Error Checking

The Intel 852GM/852GMV GMCH does not generate nor check parity for Data, Address/Request, and Response signals on the processor bus.

## 1.6. Intel 852GM/852GMV GMCH System Memory Interface

The Intel 852GM/852GMV GMCH System Memory controller directly supports the following:

- One channel of PC1600/2100 SO-DIMM DDR SDRAM memory
- DDR SDRAM devices with densities of 128-Mb, 256-Mb, and 512-Mb technology
- Maximum system memory support of two, double-sided SO-DIMMs (four rows populated) with up to 1 GB memory
- Variable page sizes of 2-kB, 4-kB, 8-kB, and 16-kB. Page size is individually selected for every row and a maximum of 16 pages may be opened simultaneously

**Table 1. DDR Memory Capacity**

Technology	Width	System Memory Capacity
128 Mb	8	256 MB
256 Mb	8	512 MB
512 Mb	8	1 GB
128 Mb	16	256 MB

Technology	Width	System Memory Capacity
256 Mb	16	512 MB
512 Mb	16	1 GB

The Intel 852GM/852GMV GMCH System Memory interface supports a thermal throttling scheme to selectively throttle reads and/or writes. Throttling can be triggered either by on-die thermal sensor, or by preset write bandwidth limits. Read throttle can also be triggered by an external input pin. The memory controller logic supports aggressive dynamic row power down features (SCKE) to help reduce power and supports Address and Control lines Tri-stating when DDR SDRAM is in active power down or self refresh.

The Intel 852GM/852GMV GMCH System Memory architecture is optimized to maintain open pages (up to 16-kB page size) across multiple rows. As a result, up to 16 pages across four rows. To complement this, the GMCH will tend to keep pages open within rows, or will only close a single bank on a page miss. Intel 852GM/852GMV GMCH supports only two bank memory technologies.

## 1.7. Intel 852GM/852GMV GMCH Internal Graphics

The GMCH IGD provides a highly integrated graphics accelerator delivering high performance 3D, 2D, and video capabilities. With its interfaces to UMA using a DVMT configuration, analog display, LVDS, and digital display (e.g. flat panel), the GMCH provides a complete graphics solution. The GMCH contains an extensive set of instructions for the following:

The GMCH also provides 2D hardware acceleration for block transfers of data (BLTs). The BLT engine provides the ability to copy a source block of data to a destination and perform raster operations (e.g., ROP1, ROP2, and ROP3) on the data using a pattern, and/or another destination. Performing these common tasks in hardware reduces CPU load, and thus improves performance.

High bandwidth access to data is provided through the System Memory ports. The GMCH uses Tiling architecture to increase System Memory efficiency and thus maximize effective rendering bandwidth.

The Intel 852GM/852GMV GMCH has three display ports, one analog and two digital. These provide support for a progressive scan analog monitor, a dedicated dual channel LVDS panel and a DVO device. Each port can transmit data according to one or more protocols. The DVO port is connected to an external device that converts one protocol to another. Examples of this are TV-out encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device. The data that is sent out the display port is selected from one of the two possible sources, pipe A or pipe B.

### 1.7.1. Intel 852GM/852GMV GMCH Analog Display Port

Intel 852GM/852GMV GMCH has an integrated 350-MHz, 24-bit RAMDAC that can directly drive a progressive scan analog monitor pixel resolution up to 1600x1200 at 85-Hz refresh and up to 1920x1440 at 60-Hz refresh. The DAC port can be driven on Pipe A or Pipe B.

### 1.7.2. Intel 852GM/852GMV GMCH Integrated LVDS Port

The Intel 852GM/852GMV GMCH has an integrated dual channel LFP Transmitter interface to support LVDS LCD panel resolutions up to SXGA+ with center and down spread SSC support of 0.5%, 1%, and 2.5% utilizing an external SSC clock. The display pipe provides panel up-scaling to fit a source image



into a specific panel size as well as panning and centering support. The LVDS port is only supported on Pipe B. The LVDS port can only be driven on Pipe B, either independently or simultaneously with the DAC port.

### 1.7.3. Intel 852GM/852GMV GMCH Integrated DVO Port

The DVO C interface is compliant with the DVI Specification 1.0. When combined with a DVI compliant external device (e.g. TMDS Flat Panel Transmitter, TV-out encoder, etc.), the GMCH provides a high-speed interface to a digital or analog display (e.g. flat panel, TV monitor, etc.).

Intel 852GM/852GMV GMCH provides a DVO port that is capable of driving a 165-MHz pixel clock at the DVO C interface. The DVO C port can be driven on Pipe A or Pipe B. If driven on port B, then the LVDS port must be disabled.

## 1.8. Hub Interface

A proprietary interconnect connects the GMCH to the ICH4-M Chipset. All communication between the GMCH and the ICH4-M occurs over the Hub Interface. The Hub Interface runs at 66- MHz or 266- MB/s.

## 1.9. Address Decode Policies

Host initiated I/O cycles are positively decoded to the GMCH configuration space and subtractively decoded to Hub Interface. Host initiated System Memory cycles are positively decoded to DDR SDRAM and are again subtractively decoded to Hub Interface if under 4 GB. System Memory accesses from Hub Interface to DDR SDRAM will be snooped on the FSB.

## 1.10. Intel 852GM/852GMV GMCH Clocking

The GMCH has the following clock input/output pins:

- 400 MHz, Spread Spectrum, Low Voltage (1.3 V) Differential BCLK, BCLK# for Processor System Bus
- 66-MHz Spread Spectrum, 3.3-V GCLKIN for Hub Interface buffers
- Four pairs of differential output clocks (SCK[4,3,1:0], SCK[4,3,1:0]#), 200/266 MHz, 2.5 V for System Memory interface
- 48-MHz, non-Spread Spectrum, 3.3-V DREFCLK for the Display Frequency Synthesis
- 48-MHz or 66-MHz, Spread Spectrum, 3.3-V DREFSSCLK for the Display Frequency Synthesis
- Up to 85-MHz, 1.5-V DVOBCLKINT for TV-Out mode
- DPMS clock for S1-M

Clock Synthesizer chip(s) are responsible for generating the system host clocks, display and Hub Interface clocks, PCI clocks, and System Memory clocks. The host target speed is 400 MHz. The GMCH does not require any relationship between the BCLK host clock and the 66-MHz clock generated for Hub Interface; they are asynchronous from each other. The Hub Interface runs at a constant 66-MHz base frequency. Table 2 indicates the frequency ratios between the various interfaces that the GMCH supports.

Please see Section 5.5.2.7 for details on the Intel 852GM/852GMV GMCH SSC Usage Model.

**Table 2. Intel 852GM/852GMV GMCH Interface Clocks**

Interface	Clock Speed	CPU System Bus Frequency Ratio	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (Bytes)	Peak Bandwidth (MB/s)
CPU Bus	100 MHz	Reference	4	400	8	3200
CPU Bus (852GMV Only)	133 MHz	Reference	4	533	8	4264
DDR SDRAM	100 MHz	1:1 Synchronous	2	200	8	1600
	133 MHz	1:1 Synchronous	2	266	8	2128
LVDS Flat Panel	25 MHz-112 MHz (single channel)	Asynchronous	1	112	2.25	252
DVO C	Up to 165 MHz	Asynchronous	2	330	1.5	495
DAC Interface	350 MHz	Asynchronous	1	350	3	1050

## 1.11. System Interrupts

The Intel 852GM/852GMV GMCH supports both the legacy Intel 8259 Programmable Interrupt delivery mechanism and the processor side bus interrupt delivery mechanism. The serial APIC Interrupt mechanism is not supported.

The Intel 8259 Interrupt delivery mechanism support consists of flushing in bound Hub Interface write buffers when an Interrupt Acknowledge cycle is forwarded from the system bus to the Hub Interface.

PCI MSI interrupts are generated as Memory Writes. The GMCH decodes upstream Memory Writes to the range 0FEE0\_0000h - 0FEEF\_FFFFh from the Hub Interface as message based interrupts. The GMCH forwards the Memory Writes along with the associated write data to the system bus as an Interrupt Message transaction. Since this address does not decode as part of main System Memory, the write cycle and the write data does not get forwarded to System Memory via the write buffer. The GMCH provides the response and HTRDY# for all Interrupt Message cycles including the ones originating from the GMCH. The GMCH also supports interrupt re-direction for upstream interrupt memory writes.

For message based interrupts, system write buffer coherency is maintained by relying on strict ordering of Memory Writes. The GMCH ensures that all Memory Writes received from a given interface prior to an interrupt message Memory Write are delivered to the system bus for snooping in the same order that they occur on the given interface.



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## 2. Signal Description

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This section describes the GMCH signals. These signals are arranged in functional groups according to their associated interface. The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal:

AGTL+	Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details. The GMCH integrates AGTL+ termination resistors, and supports $V_{tt}$ of $1.2-1.30\text{ V} \pm 5\%$ . AGTL+ signals are “inverted bus” style where a low voltage represents a logical “1”.
DVO	DVO buffers. These are 1.5-V tolerant
1.5 V	1.5-V compatible DC and AC Specification voltage levels
SSTL_2	Stub Series Termination Logic compatible signals. These are 2.5-V tolerant.
LVTTTL	Low Voltage TTL compatible signals. These are 3.3-V tolerant.
CMOS	CMOS buffers. These are 3.3-V tolerant
LVDS	Low Voltage Differential signal interface
Analog	Analog signal interface
Ref	Voltage reference signal

**Note:** System address and data bus signals are logically inverted signals. In other words, the actual values are inverted of what appears on the system bus. This must be taken into account and the addresses and data bus signals must be inverted inside the GMCH. All processor control signals follow normal convention. A “0” indicates an active level (low voltage), and a “1” indicates an active level (high voltage).

## 2.1. Host Interface Signals

Table 3. Host Interface Signal Descriptions

Signal Name	Type	Description
<b>ADS#</b>	I/O AGTL+	<b>Address Strobe:</b> The system bus owner asserts <b>ADS#</b> to indicate the first of two cycles of a request phase. The GMCH can assert this signal for snoop cycles and interrupt messages.
<b>BNR#</b>	I/O AGTL+	<b>Block Next Request:</b> Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
<b>BPRI#</b>	O AGTL+	<b>Bus Priority Request:</b> The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the <b>HLOCK#</b> signal was asserted.
<b>BREQ0#</b>	I/O AGTL+	<b>Bus Request 0B:</b> The GMCH pulls the processor bus <b>BREQ0#</b> signal low during <b>CPURST#</b> . The signal is sampled by the processor on the active-to-inactive transition of <b>CPURST#</b> . The minimum setup time for this signal is 4 BCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 BCLKs. <b>BREQ0#</b> should be tristated after the hold time requirement has been satisfied.  During regular operation, the GMCH will use <b>BREQ0#</b> as an early indication for FSB Address and Ctl input buffer and sense amp activation.
<b>CPURST#</b>	O AGTL+	<b>CPU Reset:</b> The <b>CPURST#</b> pin is an output from the GMCH. The GMCH asserts <b>CPURST#</b> while <b>RESET#</b> ( <b>PCIRSTB#</b> from ICH4-M) is asserted and for approximately 1 ms after <b>RESET#</b> is deasserted. The <b>CPURST#</b> allows the processor to begin execution in a known state.  Note that the ICH4-M must provide CPU strap set-up and hold-times around <b>CPURST#</b> . This requires strict synchronization between GMCH, <b>CPURST#</b> deassertion and ICH4-M driving the straps.
<b>DBSY#</b>	I/O AGTL+	<b>Data Bus Busy:</b> Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
<b>DEFER#</b>	O AGTL+	<b>Defer:</b> GMCH will generate a deferred response as defined by the rules of the GMCH's dynamic defer policy. The GMCH will also use the <b>DEFER#</b> signal to indicate a CPU retry response.
<b>DINV[3:0]#</b>	I/O AGTL+	<b>Dynamic Bus Inversion:</b> Driven along with the <b>HD[63:0]#</b> signals. Indicates if the associated signals are inverted or not. <b>DINV[3:0]#</b> are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8.  <b>DINV#</b> <b>Data Bits</b> <b>DINV[3]#</b> <b>HD[63:48]#</b> <b>DINV[2]#</b> <b>HD[47:32]#</b> <b>DINV[1]#</b> <b>HD[31:16]#</b> <b>DINV[0]#</b> <b>HD[16:0]#</b>
<b>DPSLP#</b>	I CMOS	<b>Deep Sleep:</b> This signal comes from the ICH4-M device, providing an indication of C3 and C4 state control to the CPU. Negation of this signal is used as an early indication for C3 and C4 wake up (to active HPLL). Note that this is a low-voltage CMOS buffer operating on the FSB VTT power plane.
<b>DPWR#</b>	O AGTL+	<b>Data Power:</b> Asserted by GMCH to indicate that a data return cycle is pending within 2 HCLK cycles or more.  CPU should use this signal during a read-cycle to activate the data input buffers and sense-amps in preparation for <b>DRDY#</b> and the related data.

Signal Name	Type	Description										
DRDY#	I/O AGTL+	<b>Data Ready:</b> Asserted for each cycle that data is transferred.										
HA[31:3]#	I/O AGTL+	<b>Host Address Bus:</b> HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of Hub Interface. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.										
HADSTB[1:0]#	I/O AGTL+	<b>Host Address Strobe:</b> HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate.  <table border="0"> <tr> <td><b>Strobe</b></td> <td><b>Address Bits</b></td> </tr> <tr> <td>HADSTB[0]#</td> <td>HA[16:3]#, HREQ[4:0]#</td> </tr> <tr> <td>HADSTB[1]#</td> <td>HA[31:17]#</td> </tr> </table>	<b>Strobe</b>	<b>Address Bits</b>	HADSTB[0]#	HA[16:3]#, HREQ[4:0]#	HADSTB[1]#	HA[31:17]#				
<b>Strobe</b>	<b>Address Bits</b>											
HADSTB[0]#	HA[16:3]#, HREQ[4:0]#											
HADSTB[1]#	HA[31:17]#											
HD[63:0]#	I/O AGTL+	<b>Host Data:</b> These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus.										
HDSTBP[3:0]# HDSTBN[3:0]#	I/O AGTL+	<b>Differential Host Data Strobes:</b> The differential source synchronous strobes are used to transfer HD[63:0]# and DINV[3:0]# at the 4x transfer rate.  <table border="0"> <tr> <td><b>Strobe</b></td> <td><b>Data Bits</b></td> </tr> <tr> <td>HDSTBP[3]#, HDSTBN[3]#</td> <td>HD[63:48]#, DINV[3]#</td> </tr> <tr> <td>HDSTBP[2]#, HDSTBN[2]#</td> <td>HD[47:32]#, DINV[2]#</td> </tr> <tr> <td>HDSTBP[1]#, HDSTBN[1]#</td> <td>HD[31:16]#, DINV[1]#</td> </tr> <tr> <td>HDSTBP[0]#, HDSTBN[0]#</td> <td>HD[15:0]#, DINV[0]#</td> </tr> </table>	<b>Strobe</b>	<b>Data Bits</b>	HDSTBP[3]#, HDSTBN[3]#	HD[63:48]#, DINV[3]#	HDSTBP[2]#, HDSTBN[2]#	HD[47:32]#, DINV[2]#	HDSTBP[1]#, HDSTBN[1]#	HD[31:16]#, DINV[1]#	HDSTBP[0]#, HDSTBN[0]#	HD[15:0]#, DINV[0]#
<b>Strobe</b>	<b>Data Bits</b>											
HDSTBP[3]#, HDSTBN[3]#	HD[63:48]#, DINV[3]#											
HDSTBP[2]#, HDSTBN[2]#	HD[47:32]#, DINV[2]#											
HDSTBP[1]#, HDSTBN[1]#	HD[31:16]#, DINV[1]#											
HDSTBP[0]#, HDSTBN[0]#	HD[15:0]#, DINV[0]#											
HIT#	I/O AGTL+	<b>Hit:</b> Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.										
HITM#	I/O AGTL+	<b>Hit Modified:</b> Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.										
HLOCK#	I/O AGTL+	<b>Host Lock:</b> All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no Hub Interface snoopable access to DRAM are allowed when HLOCK# is asserted by the CPU.										
HREQ[4:0]#	I/O AGTL+	<b>Host Request Command:</b> Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.  The transactions supported by the GMCH Host Bridge are defined in the Host Interface section of this document.										
HTRDY#	O AGTL+	<b>Host Target Ready:</b> Indicates that the target of the processor transaction is able to enter the data transfer phase.										



Signal Name	Type	Description																		
<b>RS[2:0]#</b>	O AGTL+	<p><b>Response Status:</b> Indicates type of response according to the following the table:</p> <table border="1"> <thead> <tr> <th><u>RS[2:0]#</u></th> <th><u>Response type</u></th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Idle state</td> </tr> <tr> <td>001</td> <td>Retry response</td> </tr> <tr> <td>010</td> <td>Deferred response</td> </tr> <tr> <td>011</td> <td>Reserved (not driven by GMCH)</td> </tr> <tr> <td>100</td> <td>Hard Failure (not driven by GMCH)</td> </tr> <tr> <td>101</td> <td>No data response</td> </tr> <tr> <td>110</td> <td>Implicit Write back</td> </tr> <tr> <td>111</td> <td>Normal data response</td> </tr> </tbody> </table>	<u>RS[2:0]#</u>	<u>Response type</u>	000	Idle state	001	Retry response	010	Deferred response	011	Reserved (not driven by GMCH)	100	Hard Failure (not driven by GMCH)	101	No data response	110	Implicit Write back	111	Normal data response
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101	No data response																			
110	Implicit Write back																			
111	Normal data response																			

## 2.2. DDR SDRAM Interface

Table 4. DDR SDRAM Interface Descriptions

Signal Name	Type	Description
<b>SCS[3:0]#</b>	O SSTL_2	<b>Chip Select:</b> These pins select the particular DDR SDRAM components during the active state. <b>NOTE:</b> There is one <b>SCS#</b> per DDR-SDRAM Physical SO-DIMM device row. These signals can be toggled on every rising System Memory Clock edge ( <b>SCMDCLK</b> ).
<b>SMA[12:0]</b>	O SSTL_2	<b>Multiplexed Memory Address:</b> These signals are used to provide the multiplexed row and column address to DDR SDRAM.
<b>SBA[1:0]</b>	O SSTL_2	<b>Bank Select (Memory Bank Address):</b> These signals define which banks are selected within each DDR SDRAM row. The <b>SMA</b> and <b>SBA</b> signals combine to address every possible location within a DDR SDRAM device.
<b>SRAS#</b>	O SSTL_2	<b>DDR Row Address Strobe: SRAS#</b> may be heavily loaded and requires 2 DDR SDRAM clock cycles for setup time to the DDR SDRAMs. Used with <b>SCAS#</b> and <b>SWE#</b> (along with <b>SCS#</b> ) to define the System Memory commands.
<b>SCAS#</b>	O SSTL_	<b>DDR Column Address Strobe: SCAS#</b> may be heavily loaded and requires 2 DDR clock cycles for setup time to the DDR SDRAMs. Used with <b>SRAS#</b> and <b>SWE#</b> (along with <b>SCS#</b> ) to define the System Memory commands.
<b>SWE#</b>	O SSTL_2	<b>Write Enable:</b> Used with <b>SCAS#</b> and <b>SRAS#</b> (along with <b>SCS#</b> ) to define the DDR SDRAM commands. <b>SWE#</b> is asserted during writes to DDR SDRAM. <b>SWE#</b> may be heavily loaded and requires two DDR SDRAM clock cycles for setup time to the DDR SDRAMs.
<b>SDQ[71:0]</b>	I/O SSTL_2	<b>Data Lines:</b> These signals are used to interface to the DDR SDRAM data bus. <b>NOTE:</b> ECC error detection is NOT supported: SDQ[71:64] signals should be left as NC ("No Connect") on Intel 852GM/852GMV GMCH.
<b>SDQS[8:0]</b>	I/O SSTL_2	<b>Data Strobes:</b> Data strobes are used for capturing data. During writes, <b>SDQS</b> is centered in data. During reads, <b>SDQS</b> is edge aligned with data. The following list matches the data strobe with the data bytes. <b>There is an associated data strobe (DQS) for each data strobe (DQ) and check bit (CB) group.</b>  SDQS[7] -> SDQ[63:56] SDQS[6] -> SDQ[55:48] SDQS[5] -> SDQ[47:40] SDQS[4] -> SDQ[39:32] SDQS[3] -> SDQ[31:24] SDQS[2] -> SDQ[23:16] SDQS[1] -> SDQ[15:8] SDQS[0] -> SDQ[7:0]  <b>NOTE:</b> ECC error detection is NOT supported: SDQS[8] signal should be left as NC ("No Connect") on the Intel 852GM/852GMV GMCH.
<b>SCKE[3:0]</b>	O SSTL_2	<b>Clock Enable:</b> These pins are used to signal a self-refresh or power down command to a DDR SDRAM array when entering system suspend. <b>SCKE</b> is also used to dynamically power down inactive DDR SDRAM rows. There is one <b>SCKE</b> per DDR SDRAM row. These signals can be toggled on every rising <b>SCK</b> edge.

Signal Name	Type	Description
<b>SMAB[5,4,2,1]</b>	O SSTL_2	<b>Memory Address Copies:</b> These signals are identical to SMA[5,4,2,1] and are used to reduce loading for selective CPC(clock-per-command). These copies are not inverted.
<b>SDM[8:0]</b>	O SSTL_2	<b>Data Mask:</b> When activated during writes, the corresponding data groups in the DDR SDRAM are masked. There is one <b>SDM</b> for every eight data lines. <b>SDM</b> can be sampled on both edges of the data strobes. <b>NOTE:</b> ECC error detection is NOT supported: SDM[8] signal should be left as NC ("No Connect") on the Intel 852GM/852GMV GMCH.
<b>RCVENOUT#</b>	O SSTL_2	<b>Clock Output:</b> Used to emulate source-synch clocking for reads. This pin is a NC.
<b>RCVENIN#</b>	O SSTL_2	<b>Clock Input:</b> Used to emulate source-synch clocking for reads. This is pin is a NC.

## 2.3. Hub Interface Signals

Table 5. Hub Interface Signals

Signal Name	Type	Description
<b>HL[10:0]</b>	I/O 1.5	<b>Packet Data:</b> Data signals used for HI read and write operations.
<b>HLSTB</b>	I/O 1.5	<b>Packet Strobe:</b> One of two differential strobe signals used to transmit or receive packet data over HI.
<b>HLSTB#</b>	I/O 1.5	<b>Packet Strobe Complement:</b> One of two differential strobe signals used to transmit or receive packet data over HI.

## 2.4. Clocks

Table 6. Clock Signals

Signal Name	Type	Description
<b>Host Processor Clocking</b>		
<b>BCLK</b> <b>BCLK#</b>	I CMOS	<b>Differential Host Clock In:</b> These pins receive a buffered host clock from the external clock synthesizer. This clock is used by all of the GMCH logic that is in the Host clock domain (host, Hub and System Memory). The clock is also the reference clock for the graphics core PLL. This is a low voltage differential input.
<b>System Memory Clocking</b>		
<b>SCK[5:0]</b>	O SSTL_2	<b>Differential DDR Clock:</b> <b>SCK</b> and <b>SCK#</b> pairs are differential clock outputs. The crossing of the positive edge of <b>SCK</b> and the negative edge of <b>SCK#</b> is used to sample the address and control signals on the DDR SDRAM. There are 3 pairs to each SO-DIMM. <b>NOTE:</b> ECC error detection is NOT supported: SCK[2], SCK[5] signals should be left as NC ("No Connect") on the Intel 852GM/852GMV GMCH.
<b>SCK[5:0]#</b>	O SSTL_2	<b>Complementary Differential DDR Clock:</b> These are the complimentary differential DDR SDRAM clock signals. <b>NOTE:</b> ECC error detection is NOT supported: SCK[2]#, SCK[5]# signals should be left as NC ("No Connect") on the Intel 852GM/852GMV GMCH.
<b>DVO/Hub Input Clocking</b>		
<b>GCLKIN</b>	I CMOS	<b>Input Clock:</b> 66-MHz, 3.3-V input clock from external buffer DVO/Hub Interface.
<b>DVO Clocking</b>		
<b>DVOCCLK</b> <b>DVOCCLK#</b>	O DVO	<b>Differential DVO Clock Output:</b> These pins provide a differential pair reference clock that can run up to 165 MHz. <b>DVOCCLK</b> corresponds to the primary clock out. <b>DVOCCLK#</b> corresponds to the primary complementary clock out. <b>DVOCCLK</b> and <b>DVOCCLK#</b> should be left as NC ("Not Connected") if the DVO C port is not implemented.
<b>DVOBCCLKINT</b>	I DVO	<b>DVOBC Pixel Clock Input/Interrupt:</b> This signal may be selected as the reference input to either dot clock PLL (DPLL) or may be configured as an interrupt input. A TV-out device can provide the clock reference. The maximum input frequency for this signal is 85 MHz. <b>DVOBC Pixel Clock Input:</b> When selected as the dot clock PLL (DPLL) reference input, this clock reference input supports SSC clocking for DVO LVDS devices. <b>DVOBC Interrupt:</b> When configured as an interrupt input, this interrupt can support for either of the DVOB or DVOC. <b>DVOBCCLKINT</b> needs to be pulled down if the signal is NOT used.
<b>DPMS</b>	I DVO	<b>Display Power Management Signaling:</b> This signal is used only in mobile systems to act as the DREFCLK in certain power management states(i.e. display power down mode); DPMS Clock is used to refresh video during S1-M. Clock Chip is powered down in S1-M. DPMS should come from a clock source that runs during S1-M and needs to be 1.5 V. So, an example would be to use a 1.5-V version of SUSCLK from ICH4-M.
<b>DAC Clocking</b>		



Signal Name	Type	Description
DREFCLK	I LVTTL	<b>Display Clock Input:</b> This pin is used to provide a 48-MHz input clock to the Display PLL that is used for 2D/Video and DAC.
<b>LFP LVDS Clocking</b>		
DREFSSCLK	I LVTTL	<b>Display SSC Clock Input:</b> This pin provides a 48-MHz or 66-MHz input clock (SSC or non-SSC) to the Display PLL B.

## 2.5. Internal Graphics Display Signals

The internal graphics device has support for a dedicated LFP LVDS interface, DVOC interface, and an analog VGA port.

### 2.5.1. Dedicated LFP LVDS Interface

**Table 7. Dedicated LVDS Flat Panel Interface Signal Descriptions**

Name	Type	Voltage	Description
ICLKAP	O LVDS	1.25 V $\pm$ 225 mV	<b>Channel A differential clock pair output (true):</b> 245-800 MHz
ICLKAM	O LVDS	1.25 V $\pm$ 225 mV	<b>Channel A differential clock pair output (compliment):</b> 245-800 MHz.
IYAP[3:0]	O LVDS	1.25 V $\pm$ 225 mV	<b>Channel A differential data pair 3:0 output (true):</b> 245-800 MHz.
IYAM[3:0]	O LVDS	1.25 V $\pm$ 225 mV	<b>Channel A differential data pair 3:0 output (compliment):</b> 245-800 MHz.
ICLKBP	O LVDS	1.25 V $\pm$ 225 mV	<b>Channel B differential clock pair output (true):</b> 245-800 MHz.
ICLKBM	O LVDS	1.25 V $\pm$ 225 mV	<b>Channel B differential clock pair output (compliment):</b> 245-800 MHz.
IYBP[3:0]	O LVDS	1.25 V $\pm$ 225 mV	<b>Channel B differential data pair 3:0 output (true):</b> 245-800 MHz.
IYBM[3:0]	O LVDS	1.25 V $\pm$ 225 mV	<b>Channel B differential data pair 3:0 output (compliment):</b> 245-800 MHz.

## 2.5.2. Digital Video Port C (DVOC)

Table 8. Digital Video Port C (DVOC) Signal Descriptions

Name	Type	Description
DVOC[11:0]	O DVO	<b>DVOC Data:</b> This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOCCLK and DVOCCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the upper 12-bits of pixel data. <b>DVOC[11:0]</b> should be left as left as NC ("Not Connected") if not used.
DVOCHSYNC	O DVO	<b>Horizontal Sync:</b> HSYNC signal for the DVOC interface. <b>DVOCHSYNC</b> should be left as left as NC ("Not Connected") if not used.
DVOCVSYNC	O DVO	<b>Vertical Sync:</b> VSYNC signal for the DVOC interface. <b>DVOCVSYNC</b> should be left as left as NC ("Not Connected") if the signal is NOT used when using internal graphics device.
DVOCBLANK#	O DVO	<b>Flicker Blank or Border Period Indication:</b> <b>DVOCBLANK#</b> is a programmable output pin driven by the Intel 852GM/852GMV GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. <b>DVOCBLANK#</b> should be left as left as NC ("Not Connected") if not used.
DVOCINTR#	I DVO	<b>DVOC Interrupt:</b> This pin is used to signal an interrupt, typically used to indicate a hot plug or unplug of a digital display.
DVOCFLDSTL	I DVO	<b>TV Field and Flat Panel Stall Signal.</b> This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. <b>DVOC TV Field Signal:</b> When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. <b>DVOC Flat Panel Stall Signal:</b> When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. <b>DVOCFLDSTL</b> needs to be pulled down if not used.
ADDID[7:0]	I DVO	<b>ADDID[7:0]:</b> These pins are used to communicate to the Video BIOS when an external device is interfaced to the DVO port. <b>Note:</b> Bit[7] needs to be strapped low when a DVO device is present. The other pins should be left as NC.
DVODETECT	I DVO	<b>DVODETECT:</b> This strapping signal indicates to the GMCH whether a DVO device is plugged in or not. When a DVO device is connected, then DVODETECT = 0.

### 2.5.3. Analog Display

**Table 9. Analog Display Signal Descriptions**

Pin Name	Type	Description
<b>VSYNC</b>	○ CMOS	<b>CRT Vertical Synchronization:</b> This signal is used as the vertical sync signal. Refer to Table 36.
<b>HSYNC</b>	○ CMOS	<b>CRT Horizontal Synchronization:</b> This signal is used as the horizontal sync signal. Refer to Table 36.
<b>RED</b>	○ Analog	<b>Red (Analog Video Output):</b> This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-Ω equivalent load on each pin (e.g., 75-Ω resistor on the board, in parallel with the 75-Ω CRT load).
<b>RED#</b>	○ Analog	<b>Red# (Analog Output):</b> Tied to ground.
<b>GREEN</b>	○ Analog	<b>Green (Analog Video Output):</b> This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5-Ω equivalent load on each pin (e.g., 75-Ω resistor on the board, in parallel with the 75- Ω CRT load).
<b>GREEN#</b>	○ Analog	<b>Green# (Analog Output):</b> Tied to ground.
<b>BLUE</b>	○ Analog	<b>Blue (Analog Video Output) :</b> This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-Ω equivalent load on each pin (e.g., 75-ohm resistor on the board, in parallel with the 75-Ω (CRT load).
<b>BLUE#</b>	○ Analog	<b>Blue# (Analog Output):</b> Tied to ground.

## 2.5.4. General Purpose Input/Output Signals

Table 10. Intel 852GM/852GMV GMCH GPIO (DDC, I2C, etc.) Signal Descriptions

GPIO I/F Total	Type	Comments
RSTIN#	I CMOS	<b>Reset:</b> Primary Reset
PWROK	I CMOS	<b>Power OK:</b> Indicates that power to GMCH is stable.
AGPBUSY#	O CMOS	<b>AGPBUSY:</b> Output of the GMCH graphics controller to the ICH4-M, which indicates that certain graphics activity is taking place. It will indicate to the ACPI software to not enter the C3 state. It will also cause a C3/C4 exit if C3/C4 was being entered, or was already entered when AGPBUSY# went active. Not active when the graphics controller is in any ACPI state other than D0.
EXTTS_0	I CMOS	<b>External Thermal Sensor Input:</b> This signal is an active low input to the GMCH and is used to monitor the thermal condition around the System Memory and is used for triggering a read throttle. The GMCH can be optionally programmed to send a SERR, SCI, or SMI message to the ICH4-M upon the triggering of this signal.
LCLKCTLA	O CMOS	<b>SSC Chip Clock Control:</b> Can be used to control an external clock chip with SSC control.
LCLKCTLB	O CMOS	<b>SSC Chip Data Control:</b> Can be used to control an external clock chip for SSC control.
PANELVDDEN	O CMOS	<b>LVDS Panel power control:</b> This signal is used enable power to the panel interface.
PANELBKLTEN	O CMOS	<b>LVDS Panel backlight enable:</b> This signal is used to enable the back light inverter(BLI).
PANELBKLTCTL	O CMOS	<b>LVDS Panel backlight brightness control:</b> This signal is used as power control.
DDCACLK	I/O CMOS	<b>CRT DDC Clock:</b> This signal is used as the DDC clock signal between the CRT monitor and the GMCH.
DDCADATA	I/O CMOS	<b>CRT DDC Data:</b> This signal is used as the DDC data signal between the CRT monitor and the GMCH.
DDCPCLK	I/O CMOS	<b>Panel DDC Clock:</b> This signal is used as the DDC clock signal between the LFP and the GMCH.
DDCPDATA	I/O CMOS	<b>Panel DDC Data:</b> This signal is used as the DDC data signal between the LFP and the GMCH.
MI2CCLK	I/O DVO	<b>DVO I2C Clock:</b> The specific function is I2C_CLK for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MI2CDATA	I/O DVO	<b>DVO I2C Data:</b> The specific function is I2C_DATA for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MDVICLK	I/O DVO	<b>DVI DDC Clock:</b> The specific function is DDC clock for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDVIDATA	I/O	<b>DVI DDC Data:</b> The specific function is DDC data for a digital display connector (i.e.



<b>GPIO I/F Total</b>	<b>Type</b>	<b>Comments</b>
	DVO	primary digital monitor). This signal is tri-stated during a hard reset.
<b>MDDCDATA</b>	I/O DVO	<b>DVI DDC Clock:</b> The specific function is DDC data for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.
<b>MDDCCLK</b>	I/O DVO	<b>DVI DDC Data:</b> The specific function is DDC clock for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.

## 2.6. Voltage References, PLL Power

Table 11. Voltage References, PLL Power

Signal Name	Type	Description
<b>Host Processor</b>		
HXRCOMP	Analog	<b>Host RCOMP:</b> Used to calibrate the host AGTL+ I/O buffers.
HYRCOMP	Analog	<b>Host RCOMP:</b> Used to calibrate the host AGTL+ I/O buffers.
HXSWING	Analog	<b>Host Voltage Swing (RCOMP reference voltage):</b> These signals provide a reference voltage used by the FSB RCOMP circuit.
HYSWING	Analog	<b>Host Voltage Swing (RCOMP reference voltage):</b> These signals provide a reference voltage used by the FSB RCOMP circuit.
HDVREF[2:0]	Ref Analog	<b>Host Data (input buffer) VREF:</b> Reference voltage input for the data signals of the host AGTL+ interface. Input buffer differential amplifier to determine a high versus low input voltage.
HAVREF	Ref Analog	<b>Host Address input buffer VREF:</b> Reference voltage input for the address signals of the host AGTL+ interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
HCCVREF	Ref Analog	<b>Host Common Clock (Command input buffer) VREF:</b> Reference voltage input for the common clock signals of the host AGTL+ interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
VTTLF	Power	<b>FSB Power Supply:</b> VTTLF is the low frequency connection from the board. This signal is the primary connection of power for GMCH.
VTTHF	Power	<b>FSB Power Supply:</b> VTTHF is the high frequency supply. It is for direct connection from an internal package plane to a capacitor placed immediately adjacent to the GMCH. <b>Note:</b> Not to be connected to power rail.
<b>System Memory</b>		
SMRCOMP	Analog	<b>System Memory RCOMP:</b> This signal is used to calibrate the memory I/O buffers.
SMVREF_0	Ref Analog	<b>Memory Reference Voltage(Input buffer VREF):</b> Reference voltage input for memory interface. Input buffer differential amplifier to determine a high versus low input voltage.
SMVSWINGH	Ref Analog	<b>RCOMP reference voltage:</b> This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
SMVSWINGL	Ref Analog	<b>RCOMP reference voltage:</b> This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
VCCSM	Power	Power supply for Memory I/O.
VCCQSM	Power	Power supply for System Memory clock buffers.
VCCASM	Power	Power supply for System Memory logic running at the core voltage (isolated supply, not connected to the core).
<b>Hub Interface</b>		
HLRCOMP	Analog	<b>Hub Interface RCOMP:</b> This signal is connected to a reference resistor in order to calibrate the buffers.
PSWING	Analog	<b>RCOMP reference voltage:</b> This is connected to the RCOMP buffer differential amplifier and is used to calibrate the buffers.

Signal Name	Type	Description
HLVREF	Ref Analog	<b>Input buffer VREF:</b> Input buffer differential amplifier to determine a high versus low input voltage.
VCCHL	Power	Power supply for Hub Interface buffers
<b>DVO</b>		
DVORCOMP	Analog Analog	<b>Compensation for DVO:</b> This signal is used to calibrate the DVO I/O buffers.
GVREF	Ref Analog	<b>Input buffer VREF:</b> Input buffer differential amplifier to determine a high versus low input voltage.
VCCDVO	Power	Power supply for DVO.
<b>GPIO</b>		
VCCGPIO	Power	Power supply for GPIO buffers
<b>DAC</b>		
REFSET	Ref Analog	<b>Resistor Set:</b> Set point resistor for the internal color palette DAC.
VCCADAC	Power	Power supply for the DAC
VSSADAC	Power	Ground supply for the DAC
<b>LVDS</b>		
LIBG	Analog	LVDS reference current: signal connected to reference resistor.
VCCDLVDS	Power	Digital power supply.
VCCTLVDS	Power	Data/Clk Tx power supply.
VCCALVDS	Power	Analog power supply.
VSSALVDS	Power	Ground supply for LVDS.
<b>Clocks</b>		
VCCAHPLL	Power	Power supply for the Host PLL.
VCCAGPLL	Power	Power supply for the Hub/DVO PLL.
VCCADPLLA	Power	Power supply for the display PLL A.
VCCADPLLB	Power	Power supply for the display PLL B.
<b>Core</b>		
VCC	Power	Power supply for the core.
VSS	Power	Ground supply for the chip.



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## 3. Register Description

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### 3.1. Conceptual Overview of the Platform Configuration Structure

The Intel 852GM/852GMV GMCH and ICH4-M are physically connected by Hub Interface A. From a configuration standpoint, the Hub Interface A is logically PCI bus #0. As a result, all devices internal to the GMCH and ICH4-M appear to be on PCI bus #0. The system's primary PCI expansion bus is physically attached to the ICH4-M and from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. Note that the primary PCI bus is referred to as PCI\_A in this document and is not PCI bus #0 from a configuration standpoint.

The GMCH contains two PCI devices within a single physical component. The configuration registers for the two devices are mapped as devices residing on PCI bus #0.

**Device #0:** Host-Hub Interface Bridge/DDR SDRAM Controller. Logically this appears as a PCI device residing on PCI bus #0. Physically, Device 0 contains the standard PCI registers, DDR SDRAM registers, the Graphics Aperture controller, HI control and other GMCH specific registers. Device 0 is divided into functions as follows:

Function #0: Host Bridge Legacy Registers, including Graphics Aperture control, HI configuration and Interrupt control registers

Function #1: DDR SDRAM Interface Registers

Function #3: Intel Reserved Registers

**Device #2:** Integrated Graphics Controller. Logically this appears as a PCI device residing on PCI bus #0. Physically Device #2 contains the configuration registers for 3D, 2D, and display functions.

Table 12 shows the Device # assignment for the various internal GMCH devices.

**Table 12. Device Number Assignment**

GMCH Function	Bus #0, Device#
Host-HI, DDR SDRAM I/f, Legacy control.	Device #0
Integrated Graphics Controller	Device #2

## 3.2. Nomenclature for Access Attributes

Table 13 provides the nomenclature for the access attributes.

**Table 13. Nomenclature for Access Attributes**

RO	<b>Read Only.</b> If a register is read only, writes to this register have no effect.
R/W	<b>Read/Write.</b> A register with this attribute can be read and written.
R/W/L	<b>Read/Write/Lock.</b> A register with this attribute can be read, written, and Lock.
R/WC	<b>Read/Write Clear.</b> A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
R/WO	<b>Read/Write Once.</b> A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only.
L	<b>Lock.</b> A register bit with this attribute becomes Read Only after a lock bit is set.
Reserved Bits	Some of the GMCH registers described in this section contain reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operation for the Configuration Address register.
Reserved Registers	In addition to reserved bits within a register, the GMCH contains address locations in the configuration space of the Host-Hub Interface Bridge entity that are marked either "Reserved" or "Intel Reserved". The GMCH responds to accesses to "Reserved" address locations by completing the host cycle. When a "Reserved" register location is read, a zero value is returned. ("Reserved" registers can be 8-bit, 16-bit, or 32-bit in size). Writes to "Reserved" registers have no effect on the GMCH. Registers that are marked as "Intel Reserved" must not be modified by system software. Writes to "Intel Reserved" registers may cause system failure. Reads to "Intel Reserved" registers may return a non-zero value.
Default Value upon a Reset	Upon Reset, the GMCH sets all of its internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bringing up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the GMCH registers accordingly.
S	SW Semaphore.

A physical PCI bus #0 does not exist. The Hub Interface and the internal devices in the GMCH and ICH4-M logically constitute PCI Bus #0 to configuration software.

### 3.3. Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based “configuration space” that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the CPU. Configuration space is supported by a mapping mechanism implemented within the GMCH. The PCI 2.2 specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The GMCH supports only Mechanism #1.

The configuration access mechanism makes use of the CONFIG\_ADDRESS Register (at I/O address 0CF8h through 0CFBh) and CONFIG\_DATA Register (at I/O address 0CFCh through 0CFFh). To reference a configuration register a Dword I/O write cycle is used to place a value into CONFIG\_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFIG\_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG\_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG\_ADDRESS. Any read or write to CONFIG\_DATA will result in the GMCH translating the CONFIG\_ADDRESS into the appropriate configuration cycle.

The GMCH is responsible for translating and routing the CPU’s I/O accesses to the CONFIG\_ADDRESS and CONFIG\_DATA registers to internal GMCH configuration registers and Hub Interface.

### 3.4. Routing Configuration Accesses

The GMCH supports one bus interface: the Hub Interface. PCI configuration cycles are selectively routed to this interface. The GMCH is responsible for routing PCI configuration cycles to the proper interface. PCI configuration cycles to the ICH4-M internal devices, and Primary PCI (including downstream devices) are routed to the ICH4-M via the Hub Interface. A detailed description of the mechanism for translating CPU I/O bus cycles to configuration cycles on one of the buses is described in the following section.

#### 3.4.1. PCI Bus #0 Configuration Mechanism

The GMCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG\_ADDRESS register. If the Bus Number field of CONFIG\_ADDRESS is 0 the configuration cycle is targeting a PCI Bus #0 device.

The Host-Hub Interface Bridge entity within the GMCH is hardwired as Device #0 on PCI Bus #0.

Configuration cycles to any of the GMCH’s internal devices are confined to the GMCH and not sent over Hub Interface. Accesses to disabled GMCH internal devices will be forwarded over the Hub Interface as Type 0 Configuration Cycles.

#### 3.4.2. Primary PCI and Downstream Configuration Mechanism

The ICH4-M compares the non-zero Bus Number with the SECONDARY BUS NUMBER and SUBORDINATE BUS NUMBER registers of its P2P bridges to determine if the configuration cycle is meant for Primary PCI or a downstream PCI bus.

## 3.5. Register Definitions

The GMCH contains four sets of software accessible registers accessed via the Host CPU I/O address space, and they are as follows:

**Control registers:** I/O mapped into the CPU I/O space, which control access to PCI configuration space via Configuration Mechanism #1 in the PCI 2.2 specification.

**Internal configuration registers:** residing within the GMCH, they are partitioned into two logical device register sets (“logical” since they reside within the single physical device). The first register set is dedicated to Host-HI Bridge functionality (i.e. DDR SDRAM configuration, other chip-set operating parameters and optional features). The second register block is for the integrated graphics functions.

**Internal Memory Mapped configuration registers:** residing in GMCH Device #0.

**Internal Memory Mapped configuration registers and Legacy VGA registers:** residing in the GMCH Device #2 that controls the Integrated Graphics Controller.

The GMCH internal registers (I/O Mapped and Configuration registers) are accessible by the Host CPU. The registers can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities, with the exception of CONFIG\_ADDRESS, which can only be accessed as a Dword. All multi-byte numeric fields use “little-endian” ordering (i.e., lower addresses contain the least significant parts of the field).

### Reserved Bits

Some of the GMCH registers described in this section contain reserved bits. These bits are labeled “Reserved”. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.

**Note:** The software does not need to perform read, merge, and write operation for the configuration address register.

### Default Value upon Reset

Upon a full Reset, the GMCH sets all of its internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DDR SDRAM configurations, operating parameters, and optional system features that are applicable, and to program the GMCH registers accordingly.

### 3.6. I/O Mapped Registers

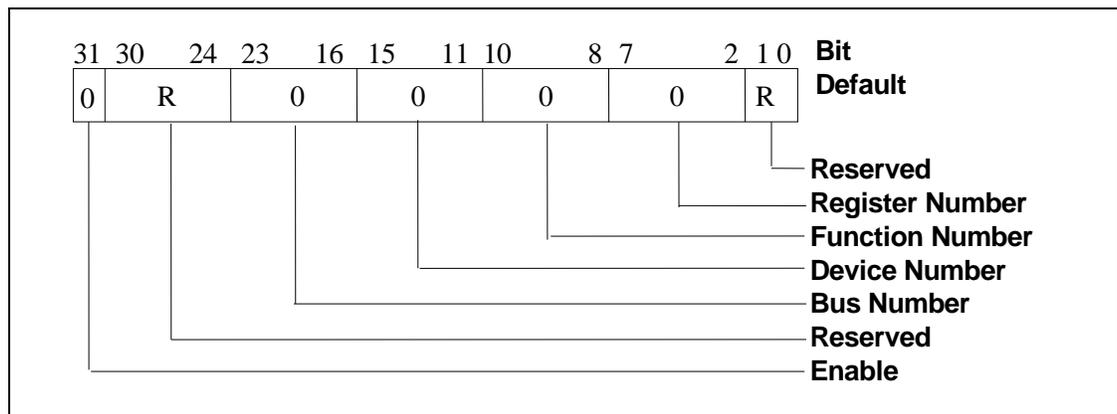
The GMCH contains two registers that reside in the CPU I/O address space: the Configuration Address (CONFIG\_ADDRESS) Register and the Configuration Data (CONFIG\_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

#### 3.6.1. CONFIG\_ADDRESS – Configuration Address Register

**I/O Address:** 0CF8h Accessed as a Dword  
**Default Value:** 00000000h  
**Access:** Read/Write  
**Size:** 32 bits

CONFIG\_ADDRESS is a 32-bit register that can be accessed only as a Dword. A Byte or Word reference will “pass through” the Configuration Address Register and the Hub Interface, onto the PCI bus as an I/O cycle. The CONFIG\_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Figure 1. Configuration Address Register





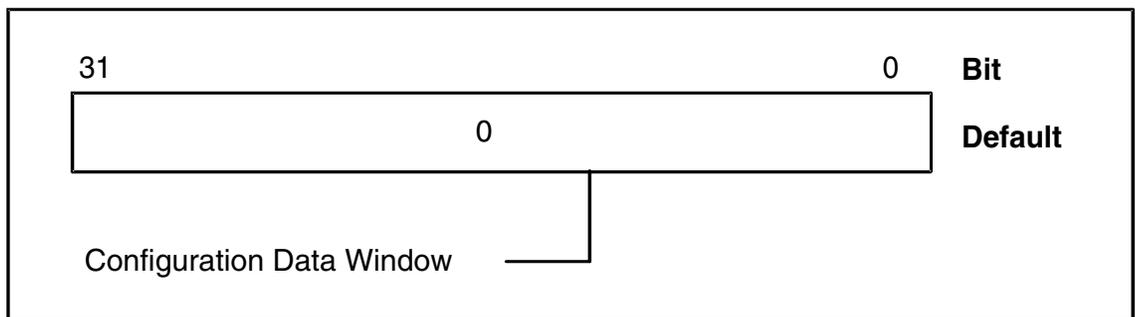
Bit	Descriptions
31	<b>Configuration Enable (CFGE):</b> When this bit is set to 1, accesses to PCI configuration space are enabled. If this bit is reset to 0, accesses to PCI configuration space are disabled.
30:24	<b>Reserved</b>
23:16	<b>Bus Number:</b> When the Bus Number is programmed to 00h the target of the Configuration Cycle is a Hub Interface agent (GMCH, ICH4-M, etc.). The Configuration Cycle is forwarded to Hub Interface if the Bus Number is programmed to 00h and the GMCH is not the target (the device number is >= 2).
15:11	<b>Device Number:</b> This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is "00" the GMCH decodes the Device Number field. The GMCH is always Device Number 0 for the Host-Hub Interface bridge entity. Therefore, when the Bus Number =0 and the Device Number=0-1 the internal GMCH devices are selected. For Bus Numbers resulting in Hub Interface configuration cycles, the GMCH propagates the device number field as A[15:11].
10:8	<b>Function Number:</b> This field is mapped to A[10:8] during Hub Interface configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The GMCH ignores configuration cycles to its internal Devices if the function number is not equal to 0.
7:2	<b>Register Number:</b> This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to A[7:2] during Hub Interface Configuration cycles.
1:0	<b>Reserved</b>

### 3.6.2. CONFIG\_DATA – Configuration Data Register

**I/O Address:** 0CFCh  
**Default Value:** 00000000h  
**Access:** Read/Write  
**Size:** 32 bits

CONFIG\_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG\_DATA is determined by the contents of CONFIG\_ADDRESS.

Figure 2. Configuration Data Register



Bit	Descriptions
31:0	<b>Configuration Data Window (CDW).</b> If bit 31 of CONFIG_ADDRESS is 1 any I/O access that to the CONFIG_DATA register will be mapped to configuration space using the contents of CONFIG_ADDRESS.

### 3.7. VGA I/O Mapped Registers

If Device 2 is enabled, and Function 0 within device 2 is enabled for VGA, and IO\_EN is set within Function 0 then GMCH claims a set of I/O registers for legacy VGA function. Table 14 lists direct CPU access registers and Table 15 lists registers that are index – data registers that are used to access internal VGA register.

**Table 14. VGA I/O Mapped Register List**

Name	Function	Read @	Write @
ST00	VGA Input Status Register 0	3C2h	
ST01	VGA Input Status Register 1	3BAh/3Dah	
FCR	VGA Feature Control Register	3CAh	3BAh/3DAh
MSR	VGA Miscellaneous Output Register	3CCh	3C2h

**Table 15. Index – Data Registers**

Name	Function	Index IO	Data IO
SRX	Sequencer Registers	3C4	3C5
GRX	Graphics Controller Registers	3CE	3CF
ARX	Attribute Control Registers	3C0	3C0: Write 3C1: Read
DACMASK	Pixel Data Mask Register	--	3C6h
DACSTATE	DAC State Register	--	3C7 Read Only
DACRX	Palette Read Index Register	3C7 Write Only	--
DACWX	Palette Write Index Register	3C8 Write Only	
DACDATA	Palette Data Register	3C9	
CRX	CRT Registers	3B4/3D4 (MDA/CGA)	3B5/3D5 (MDA/CGA)

### 3.8. Intel 852GM/852GMV GMCH Host-Hub Interface Bridge Device Registers (Device #0, Function #0)

Table 16 summarizes the configuration space for Device #0, Function#0.

**Table 16. GMCH Configuration Space - Device #0, Function#0**

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	00	01	8086h	RO
Device Identification	DID	02	03	3580h	RO
PCI Command Register	PCICMD	04	05	0006h	RO,R/W
PCI Status Register	PCISTS	06	07	0090h	RO,R/WC
Revision Identification	RID	08	08	01h	RO
Sub-Class Code	SUBC	0A	0A	00h	RO
Base Class Code	BCC	0B	0B	06h	RO
Header Type	HDR	0E	0E	80h	RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	40h	RO
Capability Identification (Product Specific)	CAPID	40	44	00000000A0h	RO
Registers-RCOMP Base Address	RRBAR	48	4B	00000000h	R/W, RO
GMCH Misc. Control	GMC	50	51	0000h	R/W, RO
GMCH Graphics Control	GGC	52	53	0030h	R/W, RO
Device and Function Control Register	DAFC	54	55	0000h	R/W
Fixed Dram Hole Control	FDHC	58	58	00h	R/W, RO
Programmable Attribute MAP	PAM (6:0)	59	5F	00h Each	R/W, RO
System Management RAM Control	SMRAM	60	60	02h	R/W-L, RO
Extended System Management RAM Control	ESMRAMC	61	61	38h	RO-R/W-RWC-L
Error Status Register	ERRSTS	62	63	0000h	R/WC
Error Command Register	ERRCMD	64	65	0000h	RO, R/W
SMI Command Register	SMICMD	66	66	00h	RO, R/W
SCI Command Register	SCICMD	67	67	00h	RO, R/W
Write Cache Control	WCC	80	83	A400002h	RO, R/W



Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Capability Disable	CAPD	F4	F7	00000000h	R/W

### 3.8.1. VID – Vendor Identification

Address Offset:	00h
Default Value:	8086h
Access:	Read Only
Size:	16 bits

The VID Register contains the vendor identification number. This 16-bit register, combined with the Device Identification Register, uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:0	<b>Vendor Identification (VID):</b> This register field contains the PCI standard identification for Intel, 8086h.

### 3.8.2. DID – Device Identification

Address Offset:	02h
Default Value:	3580h
Access:	Read Only
Size:	16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:0	<b>Device Identification Number (DID):</b> This is a 16-bit value assigned to the GMCH Host-Hub Interface bridge, Device #0.

### 3.8.3. PCICMD – PCI Command Register

Address Offset:	04h
Default Value:	0006h
Access:	Read Only, Read/Write
Size:	16 bits

Since GMCH Device #0 does not physically reside on PCI\_A many of the bits are not implemented.

Bit	Descriptions
15:10	<b>Reserved</b>
9	<b>Fast Back-to-Back Enable (FB2B):</b> This bit controls whether or not the master can do fast back-to-back write. Since Device #0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no affect. Default Value=0.
8	<b>SERR Enable (SERRE):</b> This bit is a global enable bit for Device #0 SERR messaging. The GMCH does not have an SERR# signal, but communicates the SERR# condition by sending an SERR message to the ICH4-M. 1 = Enable. GMCH is enabled to generate SERR messages over Hub Interface for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. 0 = SERR message is not generated by the GMCH for Device #0. <b>NOTE:</b> This bit only controls SERR messaging for the Device #0. Device #1 has its own SERRE bit to control error reporting for error conditions occurring on Device #1. The two control bits are used in a logical OR manner to enable the SERR Hub Interface message mechanism. Default Value=0.
7	<b>Address/Data Stepping Enable (ADSTEP):</b> Address/data stepping is not implemented in the GMCH, and this bit is hardwired to 0. Writes to this bit position have no effect. Default Value=0.
6	<b>Parity Error Enable (PERRE):</b> PERR# is not implemented by GMCH and this bit is hardwired to 0. Writes to this bit position have no effect. Default Value=0.
5	<b>VGA Palette Snoop Enable (VGASNOOP):</b> The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value=0.
4	<b>Memory Write and Invalidate Enable (MWIE):</b> The GMCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect. Default Value=0.
3	<b>Special Cycle Enable (SCE):</b> The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value=0.
2	<b>Bus Master Enable (BME):</b> The GMCH is always enabled as a master on HI. This bit is hardwired to a "1". Writes to this bit position have no effect. Default Value=1.
1	<b>Memory Access Enable (MAE):</b> The GMCH always allows access to main System Memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect. Default Value=1.



Bit	Descriptions
0	<b>I/O Access Enable (IOAE):</b> This bit is not implemented in the GMCH and is hardwired to a 0. Writes to this bit position have no effect.

### 3.8.4. PCI Status Register

Address Offset: 06h  
 Default Value: 0090h  
 Access: Read Only, Read/Write/Clear  
 Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #0's PCI interface. Bit 14 is read/write clear. All other bits are Read Only. Since GMCH Device #0 does not physically reside on PCI\_A many of the bits are not implemented.

Bit	Descriptions
15	<b>Detected Parity Error (DPE):</b> The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value=0.
14	<b>Signaled System Error (SSE):</b> R/WC: This bit is set to 1 when GMCH Device #0 generates an SERR message over HI for any enabled Device #0 error condition. Device #0 error conditions are enabled in the PCICMD and ERRCMD registers. Device #0 error flags are read/reset from the PCISTS or ERRSTS registers. Software sets SSE to 0 by writing a 1 to this bit. Default Value=0.
13	<b>Received Master Abort Status (RMAS):</b> R/WC: This bit is set when the GMCH generates a HI request that receives a Master Abort completion packet or Master Abort Special Cycle. Software clears this bit by writing a 1 to it. Default Value=0.
12	<b>Received Target Abort Status (RTAS):</b> R/WC: This bit is set when the GMCH generates a HI request that receives a Target Abort completion packet or Target Abort Special Cycle. Software clears this bit by writing a 1 to it. If bit 6 in the ERRCMD is set to a one and an Serr# special cycle is generated on the HL bus. Default Value=0.
11	<b>Signaled Target Abort Status (STAS):</b> The GMCH will not generate a Target Abort HI completion packet or Special Cycle. This bit is not implemented in the GMCH and is hardwired to a 0. Writes to this bit position have no effect. Default Value=0.
10:9	<b>DEVSEL Timing (DEVT):</b> These bits are hardwired to "00". Writes to these bit positions have no affect. Device #0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that the GMCH does not limit optimum DEVSEL timing for PCI_A. Default Value=0.
8	<b>Master Data Parity Error Detected (DPD):</b> PERR signaling and messaging are not implemented by the GMCH therefore this bit is hardwired to 0. Writes to this bit position have no effect. Default Value=0.
7	<b>Fast Back-to-Back (FB2B):</b> This bit is hardwired to 1. Writes to these bit positions have no effect. Device #0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the GMCH does not limit the optimum setting for PCI_A. Default Value=1.
6:5	<b>Reserved</b>

Bit	Descriptions
4	<b>Capability List (CLIST):</b> This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Default Value=1.
3:0	<b>Reserved</b>

### 3.8.5. RID – Register Identification

Address Offset: 08h  
 Default Value: 01h  
 Access: Read Only  
 Size: 8 bits

This register contains the revision number of the GMCH Device #0. These bits are read only and writes to this register have no effect.

Bit	Descriptions
7:0	<b>Revision Identification Number (RID):</b> This is an 8-bit value that indicates the revision identification number for the GMCH Device #0. Default Value=01h

### 3.8.6. SUBC – Sub Class Code

Address Offset: 0Ah  
 Default Value: 00h  
 Access: Read Only  
 Size: 8 bits

This register contains the Sub-Class Code for the GMCH Device #0. This code is 00h indicating a Host Bridge device.

Bit	Descriptions
7:0	<b>Sub-Class Code (SUBC):</b> This is an 8-bit value that indicates the category of Bridge into which the GMCH falls. The code is 00h indicating a Host Bridge. Default Value=0



### 3.8.7. BCC – Base Class Code

Address Offset: 0Bh  
 Default Value: 06h  
 Access: Read Only  
 Size: 8 bits

This register contains the Base Class Code of the Intel 852GM/852GMV GMCH Device #0. This code is 06h indicating a Bridge device.

Bit	Descriptions
7:0	<b>Base Class Code (BASEC):</b> This is an 8-bit value that indicates the Base Class Code for the Intel 852GM/852GMV GMCH. This code has the value 06h, indicating a Bridge device.

### 3.8.8. HDR – Header Type

Address Offset: 0Eh  
 Default Value: 80h  
 Access: Read Only  
 Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	<b>PCI Header (HDR):</b> This field always returns 80 to indicate that Device 0 is a multifunction device. If Functions other than 0 are disabled this field returns a 00 to indicate that the Intel 852GM/852GMV GMCH is a single function device with standard header layout. The default is 80; Writes to this location have no effect.

### 3.8.9. SVID – Subsystem Vendor Identification

Address Offset: 2Ch  
 Default Value: 0000h  
 Access: Read/Write Once  
 Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Descriptions
15:0	<b>Subsystem Vendor ID (SUBVID):</b> This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only. Default Value=0



### 3.8.10. SID – Subsystem Identification

Address Offset:	2Eh
Default Value:	0000h
Access:	Read/Write Once
Size:	16 bits

This value is used to identify a particular subsystem.

Bit	Descriptions
15:0	<b>Subsystem ID (SUBID):</b> This field should be programmed during BIOS initialization. After it has been written once, it becomes read only. Default Value=0

### 3.8.11. CAPPTR – Capabilities Pointer

Address Offset:	34h
Default Value:	40h
Access:	Read Only
Size:	8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Descriptions
7:0	<b>Pointer to the offset of the first capability ID register block:</b> In this case the first capability is the Product-Specific Capability, which is located at offset 40h.



### 3.8.12. CAPID Capability Identification Register (Device 0)

Address Offset:	40h – 44h
Default:	0F_F105_F009h
Access:	Read Only
Size	40 bits

The Capability Identification Register uniquely identifies chipset capabilities as defined in the table below. The bits in this register are intended to define a capability ceiling for each feature, not a capability select. The capability selection for each feature is implemented elsewhere. The mechanism to select the capability for each feature must comprehend these capabilities registers and not allow a selected setting above the ceiling specified in these registers. The BIOS must read this register to identify the SKU of the part and comprehend the capabilities specified within when configuring the effected portions of the GMCH.

The default setting, in most cases, allows the maximum capability. Exceptions are noted in the individual bits. This register is Read Only. Writes to this register have no effect.

Bit	Descriptions
39:37	<b>Capability ID [2:0]:</b> 000-100 =reserved 101= Intel 852GM/852GMV GMCH 110-111 = reserved
36:30	<b>Reserved</b>
29	0 = Reserved 1 = Device #1 and associated System Memory and IO spaces are disabled. In addition, Next_Pointer = 00h, APBASE is read only, and Aperture Global Access is Disabled.
28	<b>Reserved</b>
27:24	<b>CAPREG Version:</b> This field has the value 0001b to identify the first revision of the CAPREG definition.
23:16	<b>Cap_length:</b> This field has the value 05h indicating the structure length.
15:8	<b>Reserved</b>
7:5	<b>CAP_ID:</b> 000 = Reserved 100 = Reserved 101 = Intel 852GM/852GMV GMCH
4:0	<b>Reserved</b>

### 3.8.13. RRBAR – Register Range Base Address Register (Device 0)

Address Offset: 48 4Bh  
 Default Value: 00000000h  
 Access: Read/Write, Read Only  
 Size: 32 bits

This register requests a 64-kB allocation for the Device registers. The base address is defined by bits 31 to 16 and can be used to access device configuration registers. Only Dword aligned writes are allowed to this space. See the table below for address map within the 64-kB space. This addressing mechanism may be used to write to registers that modify the device address map (includes all the BARs, PAMs, SMM registers, Pre-Allocated System Memory registers etc). However, before using or allowing the use of the modified address map the bios must synchronize using an IO or Read cycle.

**Note:** The GTLB cannot be enabled/disabled using this mechanism.

Bit	Description
31:16	<b>Memory Base Address—R/W:</b> Set by the OS, these bits correspond to address signals [31:16].
15:0	<b>Reserved</b>

Address Range		Description
0000h to FFFFh Space	<b>Sub Ranges</b>	
	0000h to 00FFh	<b>Read/Write (As in Configuration Space):</b> Maps to 00–FFh of Device 0, Function 0 register space.
	0100h to 01FFh	<b>Read/Write (As in Configuration Space):</b> Maps to 00–FFh of Device 0, Function 1 register space.
	0200h to 02FFh	<b>Reserved</b>
	0300h to 03FFh	<b>Read/Write (As in Configuration Space):</b> Maps to 00–FFh of Device 0, Function 3 register space.
	0400h to 07FFh	<b>Reserved</b>
	0800h to 08FFh	<b>Read/Write (As in Configuration Space):</b> Maps to 00–FFh of Device 1, Function 0 register space.
	0900h to 0FFFh	<b>Reserved</b>
	1000h to 10FFh	<b>Read/Write (As in Configuration Space):</b> Maps to 00–FFh of Device 2, Function 0 register space.
	1100h to 11FFh	<b>Read/Write (As in Configuration Space):</b> Maps to 00–FFh of Device 2, Function 1 register space.
	1200h to 7FFFh	<b>Reserved</b>
	8000h to 8FFFh	System Memory RCOMP memory Range.
	9000h to FFFFh	<b>Reserved</b>



### 3.8.14. GMC – GMCH Miscellaneous Control Register (Device 0)

Address Offset: 50–51h  
 Default Value: 0000h  
 Access: Read/Write, Read Only  
 Size: 16 bits

Bit	Descriptions															
15:10	<b>Reserved</b>															
9	<b>Reserved</b>															
8	<b>RRBAR Access Enable—R/W:</b> 1 = Enables the RRBAR space. 0 = Disable															
7:1	<b>Reserved</b>															
0	<b>MDA Present (MDAP)—R/W:</b> This bit should not be set when the VGA Enable bit is not set. If the VGA enable bit is set, then accesses to IO address range x3BCh–x3BFh are forwarded to Hub Interface. If the VGA enable bit is not set then accesses to IO address range x3BCh–x3BFh are treated just like any other IO accesses. MDA resources are defined as the following: Memory: 0B0000h – 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to Hub Interface even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: <table border="0"> <tr> <td>VGA</td> <td>MDA</td> <td>Behavior</td> </tr> <tr> <td>0</td> <td>0</td> <td>All References to MDA and VGA go to Hub Interface (Default)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>All References to VGA go to PCI. MDA-only references (I/O address 3BF and aliases) will go to Hub Interface.</td> </tr> <tr> <td>1</td> <td>1</td> <td>VGA References go to PCI; MDA References go to Hub Interface</td> </tr> </table>	VGA	MDA	Behavior	0	0	All References to MDA and VGA go to Hub Interface (Default)	0	1	Reserved	1	0	All References to VGA go to PCI. MDA-only references (I/O address 3BF and aliases) will go to Hub Interface.	1	1	VGA References go to PCI; MDA References go to Hub Interface
VGA	MDA	Behavior														
0	0	All References to MDA and VGA go to Hub Interface (Default)														
0	1	Reserved														
1	0	All References to VGA go to PCI. MDA-only references (I/O address 3BF and aliases) will go to Hub Interface.														
1	1	VGA References go to PCI; MDA References go to Hub Interface														

### 3.8.15. GGC – GMCH Graphics Control Register (Device 0)

Address Offset: 52–53h  
 Default Value: 0030h  
 Access: Read/Write, Read Only  
 Size: 16 bits

Bit	Descriptions
15:7	<b>Reserved</b>
6:4	<p><b>Graphics Mode Select (GMS):</b> This field is used to select the amount of Main System Memory that is pre-allocated to support the Internal Graphics Device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that System Memory is pre-allocated only when Internal Graphics is enabled.</p> <p>000 = No System Memory pre-allocated. Device #2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device #2 Function #0 Class Code register is 80.</p> <p>001 = DVMT (UMA) mode, 1 MB of System Memory pre-allocated for frame buffer.</p> <p>010 = DVMT (UMA) mode, 4 MB of System Memory pre-allocated for frame buffer.</p> <p>011 = DVMT (UMA) mode, 8 MB of System Memory pre-allocated for frame buffer.</p> <p>100 = DVMT (UMA) mode, 16 MB of System Memory pre-allocated for frame buffer.</p> <p>101 = DVMT (UMA) mode, 32 MB of System Memory pre-allocated for frame buffer.</p> <p>All other combinations reserved.</p>
3:2	<b>Reserved</b>
1	<p><b>IGD VGA Disable (IVD):</b></p> <p>1 = Disable. Device #2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device #2 Function #0 Class Code register is 80.</p> <p>0 = Enable (Default). Device #2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device #2 Class Code register is 00.</p>
0	<b>Reserved</b>



### 3.8.16. DAFC – Device and Function Control Register (Device 0)

Address Offset: 54–55h  
 Default Value: 0000h  
 Access: Read/Write  
 Size: 16 bits

This 16-bit register controls the visibility of devices and functions within the GMCH to configurations software.

Bit	Description
15:8	<b>Reserved</b>
7	<b>Device #2 Disable:</b> 1 = Disabled. 0 = Enabled.
6:3	<b>Reserved</b>
2	Device #0 Function #3 Disable. 1 = Disable Function #3 registers within Device #0 and all associated DDR SDRAM and I/O ranges. 0 = Default is #0, Function #1 within Device #0 is enabled.
1	<b>Reserved</b>
0	<b>Device #0 Function #1 Disable:</b> 1 = Disable Function #1 within Device #0. 0 = Default is 0, Function #1 within Device #0 is enabled.

### 3.8.17. FDHC – Fixed DRAM Hole Control Register (Device 0)

Address Offset: 58h  
 Default Value: 00h  
 Access: Read/Write  
 Size: 8 bits

This 8-bit register controls a single fixed DDR SDRAM hole: 15–16 MB.

Bit	Description
7	<b>Hole Enable (HEN):</b> This field enables a memory hole in DDR SDRAM space. Host cycles matching an enabled hole are passed on to ICH4-M through Hub Interface. The Intel 852GM/852GMV GMCH will ignore Hub Interface cycles matching an enabled hole. <b>NOTE:</b> A selected hole is not re-mapped. 0 = None 1 = 15 MB–16 MB (1MBs)
6:0	<b>Reserved</b>

### 3.8.18. PAM(6:0) – Programmable Attribute Map Register (Device 0)

Address Offset:	59–5Fh
Default Value:	00h Each
Attribute:	Read/Write
Size:	4 bits/register, 14 registers

The Intel 852GM/852GMV GMCH allows programmable DDR SDRAM attributes on 13 Legacy System Memory segments of various sizes in the 640 kB –1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify System Memory attributes for each System Memory segment. These bits apply to both host and Hub Interface initiator accesses to the PAM areas. These attributes are:

**RE - Read Enable.** When RE = 1, the CPU read accesses to the corresponding System Memory segment are claimed by the Intel 852GM/852GMV GMCH and directed to main System Memory. Conversely, when RE = 0, the host read accesses are directed to PCI0.

**WE - Write Enable.** When WE = 1, the host write accesses to the corresponding System Memory segment are claimed by the Intel 852GM/852GMV GMCH and directed to main System Memory. Conversely, when WE = 0, the host write accesses are directed to PCI0.

The RE and WE attributes permit a System Memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a System Memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 kB in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in the following table.

Table 17. Attribute Bit Assignment

Bits [7, 3] Reserved	Bits [6, 2] Reserved	Bits [5, 1] WE	Bits [4, 0] RE	Description
X	X	0	0	<b>Disabled.</b> DDR SDRAM is disabled and all accesses are directed to Hub Interface. The Intel 852GM/852GMV GMCH does not respond as a Hub Interface target for any read or write access to this area.
X	X	0	1	<b>Read Only.</b> Reads are forwarded to DDR SDRAM and writes are forwarded to Hub Interface for termination. This write protects the corresponding DDR SDRAM segment. The Intel 852GM/852GMV GMCH will respond as a Hub Interface target for read accesses but not for any write accesses.
X	X	1	0	<b>Write Only.</b> Writes are forwarded to DDR SDRAM and reads are forwarded to the Hub Interface for termination. The Intel 852GM/852GMV GMCH will respond as a Hub Interface target for write accesses but not for any read accesses.
X	X	1	1	<b>Read/Write.</b> This is the normal operating mode of main System Memory. Both read and write cycles from the host are claimed by the Intel 852GM/852GMV GMCH and forwarded to DDR SDRAM. The Intel 852GM/852GMV GMCH will respond as a Hub Interface target for both read and write accesses.

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process, the BIOS can be shadowed in main System Memory to increase the system performance. When BIOS is shadowed in main System Memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The host then does a write of the same address, which is directed to main System Memory. After the BIOS is shadowed, the attributes for that System Memory area are set to read only so that all writes are forwarded to the expansion bus. Figure 3 and Table 18 show the PAM registers and the associated attribute bits.

Figure 3. PAM Registers

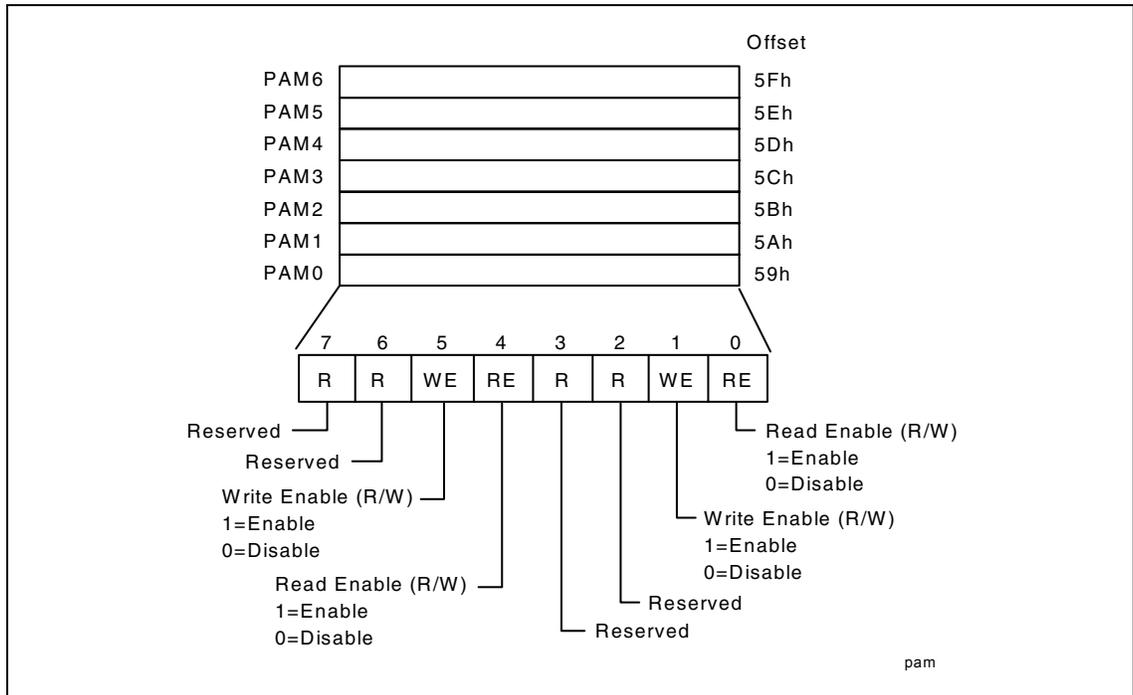


Table 18. PAM Registers and Associated System Memory Segments

PAM Reg	Attribute Bits				System Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	R	WE	RE	0F0000h–0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	R	WE	RE	0C0000h–0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	R	WE	RE	0C4000h–0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	R	WE	RE	0C8000h–0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	R	WE	RE	0CC000h–0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	R	WE	RE	0D0000h–0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	R	WE	RE	0D4000h–0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	R	WE	RE	0D8000h–0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	R	WE	RE	0DC000h–0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	R	WE	RE	0E0000h–0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	R	WE	RE	0E4000h–0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	R	WE	RE	0E8000h–0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	R	WE	RE	0EC000h–0EFFFFh	BIOS Extension	5Fh

For details on overall system address mapping scheme see the Address Decoding section of this document.

**DOS Application Area (00000h–9FFFh)**

The DOS area is 640 kB in size and it is further divided into two parts. The 512-kB area at 0 to 7FFFFh is always mapped to the main System Memory controlled by the Intel 852GM/852GMV GMCH, while the 128-kB address range from 080000 to 09FFFFh can be mapped to PCI0 or to main DDR SDRAM. By default this range is mapped to main System Memory and can be declared as a main System Memory hole (accesses forwarded to PCI0) via Intel 852GM/852GMV GMCH's FDHC configuration register.

**Video Buffer Area (A0000h–BFFFFh)**

Attribute bits do not control this 128-kB area. The host -initiated cycles in this region are always forwarded to either PCI0 or PCI2 unless this range is accessed in SMM mode. *Routing of accesses is controlled by the Legacy VGA control mechanism of the “virtual” PCI-PCI bridge device embedded within the Intel 852GM/852GMV GMCH.*

This area can be programmed as SMM area via the SMRAM register. When used as an SMM space, this range can not be accessed from Hub Interface.

**Expansion Area (C0000h–DFFFFh)**

This 128-kB area is divided into eight 16-kB segments that can be assigned with different attributes via PAM control register as defined in table 17 and table 18.

**Extended System BIOS Area (E0000h–EFFFFh)**

This 64-kB area is divided into four 16-kB segments that can be assigned with different attributes via PAM control register as defined in table 17 and table 18.

**System BIOS Area (F0000h–FFFFFFh)**

This area is a single 64-kB segment that can be assigned with different attributes via PAM control register as defined in table 17 and table 18.

### 3.8.19. SMRAM – System Management RAM Ctrl Register (Device 0)

Address Offset:	60h
Default Value:	02h
Access:	Read/Write/Lock, Read Only
Size:	8 bits

The SMRAM register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G\_SMROME bit is set to a 1. Also, the Open bit must be reset before the LOCK bit is set.

Bit	Description
7	<b>Reserved</b>
6	<b>SMM Space Open (D_OPEN):</b> When D_OPEN=1 and D_LCK=0, the SMM space DDR SDRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. When D_LCK is set to a 1, D_OPEN is reset to 0 and becomes read only.
5	<b>SMM Space Closed (D_CLS):</b> When D_CLS = 1 SMM space DDR SDRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DDR SDRAM. This will allow SMM software to reference “through” SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. D_CLS applies to all SMM spaces (Cseg, Hseg, and Tseg).
4	<b>SMM Space Locked (D_LCK):</b> When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, G_SMROME, C_BASE_SEG, GMS, DRB, DRA, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	<b>Global SMRAM Enable (G_SMROME):</b> If set to a 1, then Compatible SMRAM functions is enabled, providing 128 kB of DRAM accessible at the A0000h address while in SMM (ADS# with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	<b>Compatible SMM Space Base Segment (C_BASE_SEG)—RO:</b> This field indicates the location of SMM space. “SMM DRAM” is not remapped. It is simply “made visible” if the conditions are right to access SMM space, otherwise the access is forwarded to Hub Interface. C_BASE_SEG is hardwired to 010 to indicate that the Intel 852GM/852GMV GMCH supports the SMM space at A0000h–BFFFFh.



### 3.8.20. ESMRAMC – Extended System Management RAM Control (Device 0)

Address Offset: 61h  
 Default Value: 38h  
 Access: Read/Write  
 Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E\_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Description
7	<b>H_SMRAM_EN (H_SMRAME):</b> Controls the SMM memory space location (i.e., above 1 MB or below 1 MB). When G_SMRAME is 1 and H_SMRAME this bit is set to 1, the high SMRAM memory space is enabled. SMRAM accesses from 0FEDA0000h to 0FEDBFFFFh are remapped to DDR SDRAM address 000A0000h to 000BFFFFh. Once D_LCK is set, this bit becomes read only.
6	<b>E_SMRAM_ERR (E_SMERR):</b> This bit is set when CPU accesses the defined DDR SDRAM ranges in Extended SMRAM (High System Memory and T-segment) while not in SMM space. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	<b>SMRAM_Cache (SM_CACHE):</b> Intel 852GM/852GMV GMCH forces this bit to 1.
4	<b>SMRAM_L1_EN (SM_L1):</b> Intel 852GM/852GMV GMCH forces this bit to 1.
3	<b>SMRAM_L2_EN (SM_L2):</b> Intel 852GM/852GMV GMCH forces this bit to 1.
2:1	<b>Reserved</b>
0	<b>TSEG_EN (T_EN):</b> Enabling of SMRAM memory (TSEG, 1 Mbytes of additional SMRAM memory) for Extended SMRAM space only. When G_SMRAME = 1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Once D_LCK is set, this bit becomes read only.

### 3.8.21. ERRSTS – Error Status Register (Device 0)

Address Offset:	62–63h
Default Value:	0000h
Access:	Read/Write Clear
Size:	16 bits

This register is used to report various error conditions via Hub Interface special cycles. An SERR, SMI, or SCI Error Hub Interface special cycle may be generated on a zero to one transition of any of these flags when enabled in the PCICMD/ERRCMD, SMICMD, or SCICMD registers respectively.

Bit	Description
15:14	<b>Reserved</b>
13	<b>FSB Strobe Glitch Detected (FSBAGL):</b> When this bit is set to 1 the Intel 852GM/852GMV GMCH has detected a glitch on one of the FSB strobes. Writing a 1 to it clears this bit.
12	<b>Intel 852GM/852GMV GMCH Software Generated Event for SMI:</b> 1 = This indicates the source of the SMI was a Device #2 Software Event. 0 = Software must write a 1 to clear this bit.
11	<b>Intel 852GM/852GMV GMCH Thermal Sensor Event for SMI/SCI/SERR:</b> 1 = Indicates that a Intel 852GM/852GMV GMCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. Note that the status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command and SCI command registers. Note that a trip point can generate one of SMI, SCI or SERR interrupts (two or more per event is illegal). Multiple trip points can generate the same interrupt, if software chooses this mode subsequent trips may be lost. 0 = Software must write a 1 to clear this status bit. If this bit is set then an interrupt message will not be sent on a new thermal sensor event.
10	<b>Reserved</b>
9	<b>LOCK to non-DDR SDRAM Memory Flag (LCKF)—R/WC:</b> 1 = Indicates that a CPU initiated LOCK cycle targeting non-DDR SDRAM memory space occurred. 0 = Software must write a 1 to clear this status bit
8	<b>Received Refresh Timeout—R/WC:</b> 1 = This bit is set when 1024 memory core refresh are Queued up. 0 = Software must write a 1 to clear this status bit.
7	<b>DRAM Throttle Flag (DTF)—R/WC:</b> 1 = Indicates that the DDR SDRAM Throttling condition occurred. 0 = Software must write a 1 to clear this status bit.
6	<b>Reserved</b>
5	<b>Received Unimplemented Special Cycle Hub Interface Completion Packet FLAG (UNSC)—R/WC:</b> 1 = Indicates that the Intel 852GM/852GMV GMCH initiated a Hub Interface request that was terminated with an Unimplemented Special Cycle completion packet. 0 = Software must write a 1 to clear this status bit.
4:0	<b>Reserved</b>



### 3.8.22. ERRCMD – Error Command Register (Device 0)

Address Offset:	64–65h
Default Value:	0000h
Access:	Read/Write
Size:	16 bits

This register enables various errors to generate a SERR Hub Interface special cycle. Since the Intel 852GM/852GMV GMCH does not have a SERR# signal, SERR messages are passed from the Intel 852GM/852GMV GMCH to the ICH4-M over Hub Interface. **The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register.**

**Note:** An error can generate one and only one Hub Interface error special cycle. It is software's responsibility to make sure that when an SERR error message is enabled for an error condition, SMI and SCI error messages are disabled for that same error condition.

Bit	Description
15:14	<b>Reserved</b>
13	<b>SERR on FSB Strobe Glitch</b> : When this bit is asserted, the Intel 852GM/852GMV GMCH will generate a HI SERR message when a glitch is detected on one of the FSB Strobes.
12	<b>Reserved</b>
11	<b>SERR on Intel 852GM/852GMV GMCH Thermal Sensor Event:</b> 1 = The Intel 852GM/852GMV GMCH generates a SERR Hub Interface special cycle on a thermal sensor trip that requires an SERR. The SERR must not be enabled at the same time as the SMI/SCI for a thermal sensor trip event. 0 = Software must write a 1 to clear this status bit.
10	<b>Reserved</b>
9	<b>SERR on LOCK to non-DDR SDRAM Memory:</b> 1 = The Intel 852GM/852GMV GMCH generates an SERR Hub Interface special cycle when a CPU initiated LOCK transaction targeting non-DDR SDRAM memory space occurs. 0 = Disable. Reporting of this condition is disabled.
8	<b>SERR on DDR SDRAM Refresh timeout:</b> 1 = The Intel 852GM/852GMV GMCH generates an SERR Hub Interface special cycle when a DDR SDRAM Refresh timeout occurs. 0 = Disable. Reporting of this condition is disabled.
7	<b>SERR on DDR SDRAM Throttle Condition:</b> 1 = The Intel 852GM/852GMV GMCH generates an SERR Hub Interface special cycle when a DDR SDRAM Read or Write Throttle condition occurs. 0 = Disable. Reporting of this condition is disabled.
6	<b>SERR on Receiving Target Abort on Hub Interface:</b> 1 = The Intel 852GM/852GMV GMCH generates an SERR Hub Interface special cycle when an Intel 852GM/852GMV GMCH originated Hub Interface cycle is terminated with a Target Abort. 0 = Disable. Reporting of this condition is disabled.



Bit	Description
5	<b>SERR on Receiving Unimplemented Special Cycle Hub Interface Completion Packet:</b> 1 = The Intel 852GM/852GMV GMCH generates an SERR Hub Interface special cycle when an Intel 852GM/852GMV GMCH initiated Hub Interface request is terminated with a Unimplemented Special Cycle completion packet. 0 = Disable. Reporting of this condition is disabled.
4:2	<b>Reserved</b>
1	<b>SERR on Multiple-bit ECC Error:</b> 1 = Reserved 0 = For systems that do not support ECC, this field must be set to 0 (Intel 852GM/852GMV GMCH only).
0	<b>SERR on Single-bit ECC Error:</b> 1 = Reserved 0 = For systems that do not support ECC, this field must be set to 0 (Intel 852GM/852GMV GMCH only).



### 3.8.23. SMICMD – SMI Error Command Register (Device 0)

Address Offset: 66h  
 Default Value: 00h  
 Access: Read/Write  
 Size: 8 bits

This register enables various errors to generate an SMI Hub Interface special cycle. When an error flag is set in the ERRSTS register it can generate a SERR, SMI, or SCI Hub Interface special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers respectively.

**Note:** An error can generate one and only one Hub Interface error special cycle. It is software's responsibility to make sure that when an SMI error message is enabled for an error condition, SERR and SCI error messages are disabled for that same error condition.

Bit	Description
7:4	<b>Reserved</b>
3	<b>SMI on Intel 852GM/852GMV GMCH Thermal Sensor Trip:</b> 1 = An SMI Hub Interface special cycle is generated by Intel 852GM/852GMV GMCH when the thermal sensor trip requires an SMI. A thermal sensor trip point cannot generate more than one special cycle.
2	<b>Reserved</b>
1	<b>SMI on Multiple-bit ECC Error:</b> 1 = Reserved 0 = For systems that do not support ECC, this field must be set to 0(Intel 852GM/852GMV GMCH only).
0	<b>SMI on Single-bit ECC Error:</b> 1 = Reserved 0 = For systems that do not support ECC, this field must be set to 0 (Intel 852GM/852GMV GMCH only).

### 3.8.24. SCICMD – SCI Error Command Register (Device 0)

Address Offset: 67h  
 Default Value: 00h  
 Access: Read/Write  
 Size: 8 bits

This register enables various errors to generate a SCI Hub Interface special cycle. When an error flag is set in the ERRSTS register it can generate a SERR, SMI, or SCI Hub Interface special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers respectively.

**Note:** An error can generate one and only one Hub Interface error special cycle. It is software’s responsibility to make sure that when an SCI error message is enabled for an error condition, SERR and SMI error messages are disabled for that same error condition.

Bit	Description
7:4	<b>Reserved</b>
3	<b>SCI on Intel 852GM/852GMV GMCH Thermal Sensor Trip:</b> 1 = An SCI Hub Interface special cycle is generated by Intel 852GM/852GMV GMCH when the thermal sensor trip requires an SCI. A thermal sensor trip point cannot generate more than one special cycle.
2	<b>Reserved</b>
1	<b>SCI on Multiple-bit ECC Error:</b> 1 = Reserved 0 = For systems that do not support ECC, this field must be set to 0 (Intel 852GM/852GMV GMCH only).
0	<b>SCI on Single-bit ECC Error:</b> 1 = Reserved 0 = For systems that do not support ECC, this field must be set to 0 (Intel 852GM/852GMV GMCH only).

### 3.8.25. CAPD – Capability Disable Bits

Address Offset: F4h-F7h  
 Default Value: 00000000h  
 Access: Read/Write  
 Size: 32 bits

Bit	Descriptions
31:12	<b>Reserved</b>
11:0	<b>Capability Disable bits corresponding to Capability Register 39:28.</b> This bit is logically ORed with the corresponding strap and result of the “OR” is read through the capability register. Note that this register cannot be used to enhance capability. 0 = Normal Operation. 1 = Forces Corresponding Capability to be disabled.



### 3.9. Intel 852GM/852GMV GMCH Main Memory Control, Memory I/O Control Registers (Device #0, Function #1)

The following table shows the Intel 852GM/852GMV GMCH configuration space for Device #0, Function #1. See Section 3.2 for access nomenclature.

**Table 19. Host-Hub I/F Bridge/System Memory Controller Configuration Space (Device #0, Function#1)**

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	00	01	8086h	RO
Device Identification	DID	02	03	3584h	RO
PCI Command Register	PCICMD	04	05	0006h	RO R/W
PCI Status Register	PCISTS	06	07	0080h	RO R/WC
Revision Identification	RID	08	08	01h	RO
Sub-Class Code	SUBC	0A	0A	80h	RO
Base Class Code	BCC	0B	0B	08h	RO
Header Type	HDR	0E	0E	00h	RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	00h	RO
DRAM Row 0-3 Boundaries	DRB 0-3	40	43	00000000h	RW
DRAM Row 0-3 Attributes	DRA 0-3	50	51	7777h	RW
DRAM Timing Register	DRT	60	63	18004425h	RW
DRAM Controller Power Management Control Register	PWRMG	68	6B	00000000h	R/W
Dram Controller Mode	DRC	70	73	00000081h	R/W
DRAM Throttle Control	DTC	A0	A3	00000000h	R/W/L

### 3.9.1. VID – Vendor Identification

Address Offset: 00h  
 Default Value: 8086h  
 Access: Read Only  
 Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:0	<b>Vendor Identification (VID):</b> This register field contains the PCI standard identification for Intel, 8086h.

### 3.9.2. DID – Device Identification

Address Offset: 02h  
 Default Value: 3584h  
 Access: Read Only  
 Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions									
15:0	<p><b>Device Identification Number (DID):</b> This is a 16-bit value assigned to the Intel 852GM/852GMV GMCH Host– HI Bridge Function #1.</p> <table border="0"> <thead> <tr> <th>Device ID</th> <th>Product</th> <th>Device ID</th> </tr> </thead> <tbody> <tr> <td>00 =</td> <td>Intel 852GM/852GMV GMCH</td> <td>0x3584</td> </tr> <tr> <td>01-11 =</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Device ID	Product	Device ID	00 =	Intel 852GM/852GMV GMCH	0x3584	01-11 =	Reserved	
Device ID	Product	Device ID								
00 =	Intel 852GM/852GMV GMCH	0x3584								
01-11 =	Reserved									



### 3.9.3. PCICMD – PCI Command Register

Address Offset: 04h  
 Default Value: 0006h  
 Access: Read Only, Read/Write  
 Size: 16 bits

Since Intel 852GM/852GMV Chipset Device #0 does not physically reside on PCI\_A, many of the bits are not implemented.

Bit	Descriptions
15:10	<b>Reserved</b>
9	<b>Fast Back-to-Back Enable (FB2B):</b> This bit controls whether or not the master can do fast back-to-back write. Since Device #0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no effect. Default Value= 0
8	<b>SERR Enable (SERRE):</b> SERR# is not implemented by Function #1 of Device #0 of the Intel 852GM/852GMV GMCH and this bit is hardwired to 0. Writes to this bit position have no effect. Default Value = 0
7	<b>Address/Data Stepping Enable (ADSTEP):</b> Address/data stepping is not implemented in the Intel 852GM/852GMV GMCH, and this bit is hardwired to 0. Writes to this bit position have no effect. Default Value = 0
6	<b>Parity Error Enable (PERRE):</b> PERR# is not implemented by Intel 852GM/852GMV GMCH and this bit is hardwired to 0. Writes to this bit position have no effect. Default Value = 0
5	<b>VGA Palette Snoop Enable (VGASNOOP):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value = 0
4	<b>Memory Write and Invalidate Enable (MWIE):</b> The Intel 852GM/852GMV GMCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect. Default Value = 0
3	<b>Special Cycle Enable (SCE):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value = 0
2	<b>Bus Master Enable (BME):</b> The Intel 852GM/852GMV GMCH is always enabled as a master on HI. This bit is hardwired to a "1". Writes to this bit position have no effect. Default Value = 1
1	<b>Memory Access Enable (MAE):</b> The Intel 852GM/852GMV GMCH always allows access to main System Memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect. Default Value = 1
0	<b>I/O Access Enable (IOAE):</b> This bit is not implemented in the Intel 852GM/852GMV GMCH and is hardwired to a 0. Writes to this bit position have no effect. Default Value = 0

### 3.9.4. PCISTS – PCI Status Register

Address Offset:	06h
Default Value:	0080h
Access:	Read Only, Read/Write/Clear
Size:	16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #0's PCI interface. Bit 14 is read/write clear. All other bits are Read Only. Since Intel 852GM/852GMV GMCH Device #0 does not physically reside on PCI\_A, many of the bits are not implemented.

Bit	Descriptions
15	<b>Detected Parity Error (DPE):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value = 0
14	<b>Signaled System Error (SSE):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value = 0
13	<b>Received Master Abort Status (RMAS):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value = 0
12	<b>Received Target Abort Status (RTAS):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value = 0
11	<b>Signaled Target Abort Status (STAS):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value = 0
10:9	<b>DEVSEL Timing (DEVT):</b> These bits are hardwired to "00". Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that the Intel 852GM/852GMV GMCH does not limit optimum DEVSEL timing for PCI_A. Default Value = 0
8	<b>Master Data Parity Error Detected (DPD):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect. Default Value = 0
7	<b>Fast Back-to-Back (FB2B):</b> This bit is hardwired to 1. Writes to these bit positions have no effect. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the Intel 852GM/852GMV GMCH does not limit the optimum setting for PCI_A. Default Value = 1
6:5	<b>Reserved</b>
4	<b>Capability List (CLIST):</b> This bit is hardwired to 0 to indicate to the configuration software that this device/function does not implement new capabilities. Default Value = 0
3:0	<b>Reserved</b>



### 3.9.5. RID – Revision Identification

Address Offset:	08h
Default Value:	01h
Access:	Read Only
Size:	8 bits

This register contains the revision number of the Intel 852GM/852GMV GMCH Device #0. These bits are read only and writes to this register have no effect.

Bit	Descriptions
7:0	<b>Revision Identification Number (RID):</b> This is an 8-bit value that indicates the revision identification number for the Intel 852GM/852GMV GMCH Device #0.

### 3.9.6. SUBC – Sub-Class Code

Address Offset:	0Ah
Default Value:	80h
Access:	Read Only
Size:	8 bits

This register contains the Sub-Class Code for the Intel 852GM/852GMV GMCH Device #0. This code is 80h indicating Other Peripheral device.

Bit	Descriptions
7:0	<b>Sub-Class Code (SUBC):</b> This is an 8-bit value that indicates the category of Peripheral device into which the Intel 852GM/852GMV GMCH Function #1 falls. The code is 80h indicating Other Peripheral device.

### 3.9.7. BCC – Base Class Code

Address Offset:	0Bh
Default Value:	08h
Access:	Read Only
Size:	8 bits

This register contains the Base Class Code of the Intel 852GM/852GMV GMCH Device #0 Function #1. This code is 08h indicating Other Peripheral device.

Bit	Descriptions
7:0	<b>Base Class Code (BASEC):</b> This is an 8-bit value that indicates the Base Class Code for the Intel 852GM/852GMV GMCH. This code has the value 08h, indicating Other Peripheral device.

### 3.9.8. HDR – Header Type

Address Offset: 0Eh  
 Default Value: 80h  
 Access: Read Only  
 Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	<b>PCI Header (HDR):</b> This field always returns 80 to indicate that Device #0 is a multifunction device. The default is 80 Reads and writes to this location have no effect.

### 3.9.9. SVID – Subsystem Vendor Identification

Address Offset: 2Ch  
 Default Value: 0000h  
 Access: Write Once  
 Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Descriptions
15:0	<b>Subsystem Vendor ID (SUBVID):</b> This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

### 3.9.10. SID – Subsystem Identification

Address Offset: 2Eh  
 Default Value: 0000h  
 Access: Write Once  
 Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Descriptions
15:0	<b>Subsystem ID (SUBID):</b> This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.



### 3.9.11. CAPPTR – Capabilities Pointer

Address Offset:	34h
Default Value:	00h
Access:	Read Only
Size:	8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Descriptions
7:0	<b>Pointer to the offset of the first capability ID register block:</b> In this case there are no capabilities, therefore these bits are hardwired to 00h to indicate the end of the capability linked list.

### 3.9.12. DRB – DRAM Row Boundary Register - Device #0

Address Offset:	40-43h
Default Value:	00h Each
Access:	Read/Write
Size:	8 bits

The **DDR SDRAM Row Boundary Register** defines the upper boundary address of each DDR SDRAM row with a granularity of 32-MB. Each row has its own single-byte **DRB** register. For example, a value of 1 in **DRB0** indicates that 32-MB of DDR SDRAM has been populated in the first row. Since Intel 852GM/852GMV GMCH supports a total of 4 rows of System Memory, DRB0-3 are used. The registers from 44h-4Fh are reserved for DRBs 4-15.

Row0:40h

Row1:41h

Row2:42h

Row3:43h

44h to 4F is reserved.

DRB0 = Total System Memory in row0 (in 32 -MB increments)

DRB1 = Total System Memory in row0 + row1 (in 32 -MB increments)

DRB2 = Total System Memory in row0 + row1 + row2 (in 32 -MB increments)

DRB3 = Total System Memory in row0 + row1 + row2 + row3 (in 32- MB increments)

Each Row is represented by a byte. Each byte has the following format.

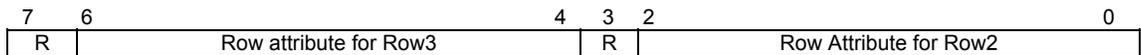
Bit	Description
7:0	<b>DDR SDRAM Row Boundary Address:</b> This 8-bit value defines the upper and lower addresses for each DDR SDRAM row. This 8-bit value is compared against a set of address lines to determine the upper address limit of a particular row. Also the minimum System Memory supported is 64-MB in 64-Mb granularity; hence bit 0 of this register must be programmed to a zero.

### 3.9.13. DRA – DRAM Row Attribute Register - Device #0

Address Offset: 50-51h  
 Default Value: 77h Each  
 Access: Read/Write  
 Size: 8 bits

The DDR SDRAM **Row Attribute Register** defines the page sizes to be used when accessing different pairs of rows. Each nibble of information in the **DRA** registers describes the page size of a pair of rows:

Row0, 1:50h  
 Row2, 3:51h  
 52h-5Fh: Reserved.



Bit	Description
7	<b>Reserved</b>
6:4	<b>Row Attribute for odd-numbered row:</b> This field defines the page size of the corresponding row. 000: Reserved 001: 4 kB 010: 8 kB 011: 16 kB 111: Not Populated Others: Reserved
3	<b>Reserved</b>
2:0	<b>Row Attribute for even-numbered row:</b> This field defines the page size of the corresponding row. 000: Reserved 001: 4 kB 010: 8 kB 011: 16 kB 111: Not Populated Others: Reserved



### 3.9.14. DRT – DRAM Timing Register - Device #0

Address Offset: 60-63h  
 Default Value: 18004425h  
 Access: Read/Write  
 Size: 32 bits

This register controls the timing of the DDR SDRAM Controller.

Bit	Description										
31	<p><b>DDR Internal Write to Read Command delay (tWTR):</b>            The tWTR is a std. DDR SDRAM timing parameter with a value of 1 CK for CL=2 and 2.5. The tWTR is used to time RD command after a WR command (to same row):            '0': tWTR is set to 1 Clock (CK), used for DDR SDRAM CL=2 or 2.5            '1': Reserved</p>										
30	<p><b>DDR Write Recovery time (tWR):</b>            Write recovery time is a std. DDR timing parameter with the value of 15 ns. It should be set to 2 CK when DDR200 is used. The tWR is used to time PRE command launch after a WR command, when DDR SDRAM components are populated.            '0': tWR is set to 2 Clocks (CK)            '1': tWR is set to 3 Clocks (CK)</p>										
29:28	<p><b>Back To Back Write-Read commands spacing (DDR different rows/bank):</b>            This field determines the WR-RD command spacing, in terms of common clocks for DDR SDRAM based on the following formula: <math>DQSS + 0.5 \times BL + TA(wr-rd) - CL</math>            DQSS: is time from write command to data and is always 1 CK            BL: is burst length and can be set to 4.            TA (wr-rd): is required DQ turn-around, can be set to 1 or 2 CK            CL: is CAS latency, can be set to 2 or 2.5</p> <p><b>Examples of usage:</b>            For BL=4, with single DQ turn-around and CL=2, this field must be set to 2 CK (1+2+1-2)</p> <p><b>Encoding CK between WR and RD commands</b></p> <table border="0"> <tr> <td></td> <td style="text-align: center;"><b>BL=4</b></td> </tr> <tr> <td><b>00:</b></td> <td>4</td> </tr> <tr> <td><b>01:</b></td> <td>3</td> </tr> <tr> <td><b>10:</b></td> <td>2</td> </tr> <tr> <td><b>11:</b></td> <td>Reserved</td> </tr> </table>		<b>BL=4</b>	<b>00:</b>	4	<b>01:</b>	3	<b>10:</b>	2	<b>11:</b>	Reserved
	<b>BL=4</b>										
<b>00:</b>	4										
<b>01:</b>	3										
<b>10:</b>	2										
<b>11:</b>	Reserved										

Bit	Description								
27:26	<p><b>Back To Back Read-Write commands spacing (DDR, same or different rows/bank):</b> This field determines the RD-WR command spacing, in terms of common clocks based on the following formula: <math>CL + 0.5 \times BL + TA(rd-wr) - DQSS</math></p> <p>DQSS: is time from write command to data and is always 1 CK            BL: is burst length which is set to 4            TA (rd-wr): is required DQ turn-around, can be set to 1, 2 or 3 CK            CL: is CAS latency, can be set to 2 or 2.5</p> <p><b>Examples of usage:</b>            For BL=4, with single DQ turn-around and CL=2, this field must be set to 4 CK (2+2+1-1)</p> <p><b>Encoding      CK between RD and WR commands</b></p> <p style="padding-left: 40px;"><b>BL=4</b></p> <table style="margin-left: 20px;"> <tr><td>00:</td><td>7</td></tr> <tr><td>01:</td><td>6</td></tr> <tr><td>10:</td><td>5</td></tr> <tr><td>11:</td><td>4</td></tr> </table> <p><b>NOTES:</b>            Since reads in DDR SDRAM cannot be terminated by writes, the space between commands is not a function of cycle length but of burst length.</p>	00:	7	01:	6	10:	5	11:	4
00:	7								
01:	6								
10:	5								
11:	4								
25	<p><b>Back To Back Read-Read commands spacing (DDR, different rows):</b></p> <p>This field determines the RD-RD command spacing, in terms of common clocks based on the following formula: <math>0.5 \times BL + TA(rd-rd)</math></p> <p>BL: is burst length and can be set to 4.            TA (rd-rd): is required DQ turn-around, can be set to 1 or 2 CK</p> <p><b>Examples of usage:</b>            For BL=4, with single DQ turn-around, this field must be set to 3 CK (2+1)</p> <p><b>Encoding      CK between RD and RD commands</b></p> <p style="padding-left: 40px;"><b>BL=4</b></p> <table style="margin-left: 20px;"> <tr><td>0:</td><td>4</td></tr> <tr><td>1:</td><td>3</td></tr> </table> <p><b>NOTES:</b>            Since a read to a different row doesn't terminate a read, the space between commands is not a function of cycle length but of burst length.</p>	0:	4	1:	3				
0:	4								
1:	3								
24:15	<b>Reserved</b>								

Bit	Description																								
14:12	<p><b>Refresh Cycle Time (tRFC):</b> Refresh cycle time is measured for a given row from REF command (to perform a refresh) until following ACT to same row (to perform a read or write). It is tracked separately from tRC for DDR SDRAM. Current DDR SDRAM spec requires tRFC of 75 ns (DDR266) and 80ns (DDR200). Therefore, this field will be set to 8 clocks for DDR200, 10 clocks for DDR266.</p> <p><b>Encoding tRFC</b></p> <table> <tr><td>"000":</td><td>14</td><td>clocks</td></tr> <tr><td>"001":</td><td>13</td><td>clocks</td></tr> <tr><td>"010":</td><td>12</td><td>clocks</td></tr> <tr><td>"011":</td><td>11</td><td>clocks</td></tr> <tr><td>"100":</td><td>10</td><td>clocks</td></tr> <tr><td>"101":</td><td>9</td><td>clocks</td></tr> <tr><td>"110":</td><td>8</td><td>clocks</td></tr> <tr><td>"111":</td><td>7</td><td>clocks</td></tr> </table>	"000":	14	clocks	"001":	13	clocks	"010":	12	clocks	"011":	11	clocks	"100":	10	clocks	"101":	9	clocks	"110":	8	clocks	"111":	7	clocks
"000":	14	clocks																							
"001":	13	clocks																							
"010":	12	clocks																							
"011":	11	clocks																							
"100":	10	clocks																							
"101":	9	clocks																							
"110":	8	clocks																							
"111":	7	clocks																							
11	<p><b>Activate to Precharge delay (tRAS), MAX:</b> This bit controls the maximum number of clocks that a DDR SDRAM bank can remain open. After this time period, the System Memory controller will guarantee to pre-charge the bank. Note that this time period may or may not be set to overlap with time period that requires a refresh to happen. The DDR SDRAM controller includes a separate tRAS-MAX counter for every supported bank. With a maximum of four row and four banks per row, there are 16 counters.</p> <p>'0': 120 micro-seconds '1': Reserved.</p>																								
10:9	<p><b>Activate to Precharge delay (tRAS), MIN:</b> This bit controls the number of DDR SDRAM clocks for tRAS MIN</p> <table> <tr><td>00:</td><td>8 Clocks</td></tr> <tr><td>01:</td><td>7 Clocks</td></tr> <tr><td>10:</td><td>6 Clocks</td></tr> <tr><td>11:</td><td>5 Clocks</td></tr> </table>	00:	8 Clocks	01:	7 Clocks	10:	6 Clocks	11:	5 Clocks																
00:	8 Clocks																								
01:	7 Clocks																								
10:	6 Clocks																								
11:	5 Clocks																								
8:7	<b>Reserved</b>																								
6:5	<p><b>CAS# Latency (tCL):</b></p> <table> <tr><th>Encoding</th><th>DDR SDRAM CL</th></tr> <tr><td>00:</td><td>2.5</td></tr> <tr><td>01:</td><td>2</td></tr> <tr><td>10:</td><td>Reserved</td></tr> <tr><td>11:</td><td>Reserved</td></tr> </table>	Encoding	DDR SDRAM CL	00:	2.5	01:	2	10:	Reserved	11:	Reserved														
Encoding	DDR SDRAM CL																								
00:	2.5																								
01:	2																								
10:	Reserved																								
11:	Reserved																								
4	<b>Reserved</b>																								
3:2	<p><b>DDR SDRAM RAS# to CAS# Delay (tRCD):</b> This bit controls the number of clocks inserted between a row activate command and a read or write command to that row</p> <p><b>Encoding tRCD</b></p> <table> <tr><td>00:</td><td>Reserved</td></tr> <tr><td>01:</td><td>3 DDR SDRAM Clocks</td></tr> <tr><td>10:</td><td>2 DDR SDRAM Clocks</td></tr> <tr><td>11:</td><td>Reserved</td></tr> </table>	00:	Reserved	01:	3 DDR SDRAM Clocks	10:	2 DDR SDRAM Clocks	11:	Reserved																
00:	Reserved																								
01:	3 DDR SDRAM Clocks																								
10:	2 DDR SDRAM Clocks																								
11:	Reserved																								



Bit	Description
1:0	<p><b>DDR SDRAM RAS# Precharge (tRP):</b> This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same row</p> <p>Encoding    tRP</p> <p>00:            Reserved</p> <p>01:            3 DDR SDRAM Clocks</p> <p>10:            2 DDR SDRAM Clocks</p> <p>11:            Reserved</p>

### 3.9.15. PWRMG – DRAM Controller Power Management Control Register - Device #0

Address Offset:                    68h-6Bh  
 Default Value:                    00000000h  
 Access:                            Read/Write  
 Size:                                32 bits

Bit	Description																												
31:24	<b>Reserved</b>																												
23:20	<p><b>Row State Control:</b> This field determines the number of clocks the DDR SDRAM controller will retain in the idle state before it begins pre-charging all pages or powering down rows.</p> <p><b>PDEn:</b> Power Down Enable  <b>PCEn:</b> Page Close Enable  <b>TC:</b> Timer Control</p> <table border="1"> <thead> <tr> <th>PDEn(23):</th> <th>PCEn(22):</th> <th>TC(21:20)Function</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>XX</td> <td>All disabled</td> </tr> <tr> <td>0</td> <td>1</td> <td>XX</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>XX</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>1</td> <td>0X</td> <td>Reserved</td> </tr> <tr> <td></td> <td></td> <td>10</td> <td>Reserved</td> </tr> <tr> <td></td> <td></td> <td>11</td> <td>Precharge and Power Down after 64 DDR SDRAM Clocks of idle time</td> </tr> </tbody> </table>	PDEn(23):	PCEn(22):	TC(21:20)Function		0	0	XX	All disabled	0	1	XX	Reserved	1	0	XX	Reserved	1	1	0X	Reserved			10	Reserved			11	Precharge and Power Down after 64 DDR SDRAM Clocks of idle time
PDEn(23):	PCEn(22):	TC(21:20)Function																											
0	0	XX	All disabled																										
0	1	XX	Reserved																										
1	0	XX	Reserved																										
1	1	0X	Reserved																										
		10	Reserved																										
		11	Precharge and Power Down after 64 DDR SDRAM Clocks of idle time																										
19:0																													



### 3.9.16. DRC – DRAM Controller Mode Register - Device #0

Address Offset: 70-73h  
 Default Value: 00000081h  
 Access: Read/Write, read-only  
 Size: 32 bits

Bit	Description
31:30	<b>Revision Number (REV):</b> Reflects the revision number of the format used for DDR SDRAM register definition.
29	<b>Initialization Complete (IC):</b> This bit is used for communication of software state between the memory controller and the BIOS. BIOS sets this bit to 1 after initialization of the DDR SDRAM memory array is complete. Setting this bit to a “1” enables DDR SDRAM refreshes. On power up and S3 exit, the BIOS initializes the DDR SDRAM array and sets this bit to a “1”. This bit works in combination with the RMS bits in controlling refresh state: <b>IC Refresh State</b> 0 OFF 1 ON
28:24	<b>Reserved</b>
23:22	<b>Number of Channels (CHAN):</b> Reflects that Intel 852GM/852GMV GMCH supports only one System Memory channel. 00 One channel is populated appropriately Others: Reserved
21:20	<b>DDIM DDR SDRAM Data Integrity Mode:</b> <b>No-ECC.</b> No read-merge-write on partial writes. ECC data sense-amps are disabled and the data output is tristate. (Default)
19:16	<b>Reserved</b>
15	<b>RAS Lock-Out Enable:</b> Set to a ‘1’ if all populated rows support RAS Lock-Out. Defaults to ‘0’. If this bit is set to a ‘1’ the DDR SDRAM controller assumes that the DDR SDRAM guarantees tRAS min before an auto precharge (AP) completes (Note that an AP is sent with a read or a write command). Also, the DDR SDRAM controller does not issue an activate command to the auto pre-charged bank for tRP. If this bit is set to a ‘0’ the DDR SDRAM controller does not schedule an AP if tRAS min is not met.
14:10	<b>Reserved</b>
9:7	<b>Refresh Mode Select (RMS):</b> This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. <b>000:</b> Refresh disabled <b>001:</b> Refresh enabled. Refresh interval 15.6 $\mu$ sec <b>010:</b> Refresh enabled. Refresh interval 7.8 $\mu$ sec <b>011:</b> Reserved. <b>111:</b> Refresh enabled. Refresh interval 64 clocks (fast refresh mode) <b>Other:</b> Reserved Any change in the programming of this field resets the refresh counter to zero. This function is for testing purposes, it allows test program to align refresh events with the test and thus improve failure repeatability.
6:4	<b>Mode Select (SMS).</b> These bits select the special operational mode of the DDR SDRAM interface. The special modes are intended for initialization at power up. <b>000:</b> Post Reset state – When the Intel 852GM/852GMV GMCH exits reset (power-up or otherwise), the mode select field is cleared to “000”. Software not expected to write this value, however if this value is written there are no side effects (no self refresh or any other special DDR SDRAM cycle). During any reset sequence, while power is applied and reset is active, the Intel 852GM/852GMV GMCH deasserts all CKE signals. After internal reset is deasserted, CKE signals remain deasserted until this field is

Bit	Description								
	<p>written to a value different than "000". On this event, all CKE signals are asserted.</p> <p>During suspend (S3, S4), Intel 852GM/852GMV GMCH internal signal triggers DDR SDRAM controller to flush pending commands and enter all rows into Self-Refresh mode. As part of resume sequence, Intel 852GM/852GMV GMCH will be reset – which will clear this bit field to "000" and maintain CKE signals deasserted. After internal reset is deasserted, CKE signals remain deasserted until this field is written to a value different than "000". On this event, all CKE signals are asserted.</p> <p>During entry to other low power states (C3, S1-M), Intel 852GM/852GMV GMCH internal signal triggers DDR SDRAM controller to flush pending commands and enter all rows in S1 and relevant rows in C3 (Based on RPDNC3) into Self-Refresh mode. During exit to normal mode, the GMCH signal triggers DDR SDRAM controller to exit Self-Refresh and resume normal operation without S/W involvement.</p> <p><b>001:</b> NOP Command Enable – All CPU cycles to DDR SDRAM result in a NOP command on the DDR SDRAM interface.</p> <p><b>010:</b> All Banks Pre-charge Enable – All CPU cycles to DDR SDRAM result in an "all banks precharge" command on the DDR SDRAM interface.</p> <p><b>011:</b> Mode Register Set Enable – All CPU cycles to DDR SDRAM result in a "mode register" set command on the DDR SDRAM interface. Host address lines are mapped to DDR SDRAM address lines in order to specify the command sent. Host address HA[13:3] are mapped to memory address MA[11, 9:0]. MA3 must be driven to 1 for interleave wrap type.</p> <p><b>For Double Data Rate</b></p> <p>MA[6:4] needs to be driven based on the value programmed in the CAS# Latency field.</p> <table border="0"> <thead> <tr> <th><u>CAS Latency</u></th> <th><u>MA[6:4]</u></th> </tr> </thead> <tbody> <tr> <td>1.5 Clocks</td> <td>001</td> </tr> <tr> <td>2.0 Clocks</td> <td>010</td> </tr> <tr> <td>2.5 Clocks</td> <td>110</td> </tr> </tbody> </table> <p>MA[7] should always be driven to a 0.</p> <p>MA[8] Should be driven to a 1 for DLL Reset and 1 for Normal Operation.</p> <p>MA[12:9] must be driven to 00000.</p> <p>BIOS must calculate and drive the correct host address for each row of memory such that the correct command is driven on the MA[12:0] lines. Note that MAB[7:4]# are inverted from MAA[7:4]; BIOS must account for this.</p> <p><b>100:</b> Extended Mode Register Set Enable – All CPU cycles to DDR SDRAM result in an "extended mode register set" command on the DDR SDRAM interface. Host address lines are mapped to DDR SDRAM address lines in order to specify the command sent. Host address lines are mapped to DDR SDRAM address lines in order to specify the command sent. Host address HA[13:3] are mapped to memory address [9:0]. MA[0] = 0 for DLL enable and 1 for DLL disable. All the other MA lines are driven to 0s. Note that MAB[7:4]# are inverted from MAA[7:4]; BIOS must account for this.</p> <p><b>101: Reserved</b></p> <p><b>110:</b> CBR Refresh Enable – In this mode all CPU cycles to DDR SDRAM result in a CBR cycle on the DDR SDRAM interface</p> <p><b>111:</b> Normal operation</p>	<u>CAS Latency</u>	<u>MA[6:4]</u>	1.5 Clocks	001	2.0 Clocks	010	2.5 Clocks	110
<u>CAS Latency</u>	<u>MA[6:4]</u>								
1.5 Clocks	001								
2.0 Clocks	010								
2.5 Clocks	110								
3:0	<b>Reserved</b>								



### 3.9.17. DTC – DRAM Throttling Control Register (Device 0)

Offset Address:	A0–A3h
Default Value:	00000000h
Access:	Read/Write/Lock
Size:	32 bits

Throttling is independent for System Memory Banks, Intel 852GM/852GMV GMCH Writes, and thermal sensor trips. Read and Write Bandwidth is measured independently for each Bank. If the number of Octal -Words (16 bytes) read/written during the window defined below (Global DDR SDRAM Sampling Window: GDSW) exceeds the DDR SDRAM Bandwidth Threshold, then the DDR SDRAM throttling mechanism will be invoked to limit DDR SDRAM reads/writes to a lower bandwidth checked over smaller time windows. The throttling will be active for the remainder of the current GDSW and for the next GDSW after which it will return to non-throttling mode. The throttling mechanism accounts for the actual bandwidth consumed during the sampling window, by reducing the allowed bandwidth within the smaller throttling window based on the bandwidth consumed during the sampling period. Although bandwidth from/to independent rows and Intel 852GM/852GMV GMCH write bandwidth is measured independently, once tripped all transactions except high priority graphics reads are subject to throttling.

Bit	Description
31:28	<p><b>DDR SDRAM Throttle Mode (TMODE):</b></p> <p>Four bits control which mechanisms for throttling are enabled in an “OR” fashion. Counter-based throttling is lower priority than thermal trips throttling when both are enabled and tripped. Counter-based trips point throttling values and Thermal-based trip point throttling values are specified in this register.</p> <p>If the counter and thermal mechanisms for either rank or Intel 852GM/852GMV GMCH are both enabled, throttle settings for the one that trips first is used until the end of the second gdsw.</p> <p>[Rank Counter, Intel 852GM/852GMV GMCH Write Counter, Rank Thermal Sensor, Intel 852GM/852GMV GMCH Thermal Sensor]</p> <p>0000 = Throttling turned off. This is the default setting. All Counters are off.</p> <p>0001 = Only Intel 852GM/852GMV GMCH Thermal Sensor based throttling is enabled. If Intel 852GM/852GMV GMCH thermal sensor is tripped, write throttling begins based on the setting in WTTC.</p> <p>0010 = Only Rank Thermal Sensor based throttling enabled. When the external SO-DIMM thermal sensor is tripped DDR SDRAM throttling begins based on the setting in RTTC.</p> <p>0011 = Both Rank and Intel 852GM/852GMV GMCH Thermal Sensor based throttling enabled. When the external SO-DIMM thermal sensor is tripped DDR SDRAM throttling begins based on the setting in RTTC. If the Intel 852GM/852GMV GMCH thermal sensor is tripped, write throttling begins based on the setting in WTTC.</p> <p>0100 = Only the Intel 852GM/852GMV GMCH Write Counter mechanism is enabled. When the threshold set in the GDT field is reached, DDR SDRAM throttling begins based on the setting in WCTC.</p> <p>0101 = Intel 852GM/852GMV GMCH Thermal Sensor and Intel 852GM/852GMV GMCH Write DDR SDRAM Counter mechanisms are both enabled. If the Intel 852GM/852GMV GMCH write DDR SDRAM counter mechanism threshold is reached, DDR SDRAM throttling begins based on the setting in WCTC. If the Intel 852GM/852GMV GMCH thermal sensor is tripped, DDR SDRAM throttling begins based on the setting in WTTC. If both threshold mechanisms are tripped, the DDR SDRAM throttling begins based on the settings in WTTC.</p> <p>0110 = Rank Thermal Sensor and Intel 852GM/852GMV GMCH Write DDR SDRAM Counter mechanisms are both enabled. If the Intel 852GM/852GMV GMCH write DDR SDRAM counter mechanism threshold is reached, DDR SDRAM throttling begins based on setting in WCTC. If the external SO-DIMM thermal sensor is tripped, Rank DRAM throttling begins based on the setting in RTTC.</p> <p>0111 = Similar to 0101 for writes and when the Rank thermal sensor is tripped DDR SDRAM throttling begins based on the setting in RTTC.</p> <p>1000 = Only Rank Counter mechanism is enabled. When the threshold set in the GDT field is reached, DDR SDRAM throttling begins based on the setting in RCTC.</p> <p>1001 = Rank Counter mechanism is enabled and Intel 852GM/852GMV GMCH Thermal Sensor based throttling are both enabled. If Intel 852GM/852GMV GMCH thermal sensor is tripped, write throttling begins based on the setting in WTTC. When the threshold set in the GDT field is reached, DDR SDRAM throttling begins based on the setting in RCTC.</p> <p>1010 = Rank thermal Sensor and Rank DDR SDRAM Counter mechanisms are both enabled. If the rank DDR SDRAM counter mechanism threshold is reached, DDR SDRAM throttling begins based on the setting in RCTC. If the external SO-DIMM thermal sensor is tripped, DRAM throttling begins based on the setting in RTTC.</p> <p>1011 = Similar to 1010 and If the Intel 852GM/852GMV GMCH thermal sensor is tripped, write throttling begins based on the setting in WTTC.</p> <p>1111 = Rank and Intel 852GM/852GMV GMCH Thermal Sensor based throttling and Rank and Intel 852GM/852GMV GMCH Write Counter based throttling are enabled. If both the write counter and Intel 852GM/852GMV GMCH thermal sensor based mechanisms are tripped, DDR SDRAM throttling begins based on the setting allowed in WTTC. If both the rank counter and rank thermal sensor based mechanisms are tripped, DDR SDRAM throttling begins based on the setting allowed in RTTC.</p>
27:24	<p><b>Read Counter Based Power Throttle Control (RCTC):</b> These bits select the Counter based Power Throttle Bandwidth Limits for Read operations to System Memory.</p>



Bit	Description
	R/W, RO if Throttle Lock. 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved
23:20	<b>Write Counter Based Power Throttle Control (WCTC):</b> These bits select the Counter based Power Throttle Bandwidth Limits for Write operations to System Memory. R/W, RO if Throttle Lock 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved
19:16	<b>Read Thermal Based Power Throttle Control (RTTC):</b> These bits select the thermal sensor based Power Throttle Bandwidth Limits for Read operations to System Memory. R/W, RO if Throttle Lock. 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved
15:12	<b>Write Thermal Based Power Throttle Control (WTTC):</b> These bits select the thermal based Power Throttle Bandwidth Limits for Write operations to System Memory. R/W, RO if Throttle Lock

Bit	Description
	0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved
11	<b>Counter Based Throttle Lock (CTLOCK):</b> This bit secures RCTC and WCTC. This bit defaults to 0. Once a 1 is written to this bit, RCTC and WCTC (including CTLOCK) become read-only.
10	<b>Thermal Throttle Lock (TTLOCK):</b> This bit secures the DDR SDRAM throttling control register. This bit defaults to 0. Once a 1 is written to this bit, all of the configuration register bits in DTC (including TTLOCK) except CTLOCK, RCTC and WCTC become read-only.
9	<b>Thermal Power Throttle Control fields Enable:</b> 0 = RTTC and WTTC are not used. RCTC and WTCT are used for both counter and thermal based throttling. 1 = RTTC and WTTC are used for thermal based throttling.
8	<b>High Priority Stream Throttling Enable:</b> Normally High Priority Streams are not throttled when either the counter based mechanism or thermal sensor mechanism demands throttling. 0 = Normal operation. 1 = Block High priority streams during throttling.
7:0	<b>Global DDR SDRAM Sampling Window (GDSW):</b> This 8-bit value is multiplied by 4 to define the length of time in milliseconds (0–1020) over which the number of Octal Words (16 bytes) read/written is counted and throttling is imposed. Note that programming this field to “00h” disables System Memory throttling. Recommended values are between 0.25 and 0.75 seconds.



### 3.10. Intel 852GM/852GMV GMCH Configuration Process and Registers (Device #0, Function #3)

See Section 3.2 for access nomenclature. Table 20 summarizes all Device#0, Function #3 registers.

**Table 20. Configuration Process Configuration Space (Device#0, Function #3)**

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	00	01	8086h	RO
Device Identification	DID	02	03	3585	RO
PCI Command Register	PCICMD	04	05	0006h	RO R/W
PCI Status Register	PCISTS	06	07	0080h	RO R/WC
Revision Identification	RID	08	08	01h	RO
Sub-Class Code	SUBC	0A	0A	80h	RO
Base Class Code	BCC	0B	0B	08h	RO
Header Type	HDR	0E	0E	80h	RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	00h	RO
HPLL Clock Control Register	HPLLCC	C0	C1	00h	RO

#### 3.10.1. VID – Vendor Identification

Address Offset: 00h  
 Default Value: 8086h  
 Access: Read Only  
 Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:0	<b>Vendor Identification (VID):</b> This register field contains the PCI standard identification for Intel 8086h.



### 3.10.2. DID – Device Identification

Address Offset: 02h  
Default Value: 3585h  
Access: Read Only  
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions						
15:0	<p><b>Device Identification Number (DID):</b> This is a 16-bit value assigned to the Intel 852GM/852GMV GMCH Host-HI Bridge Function #3.</p> <table><thead><tr><th>Product</th><th>Device ID</th></tr></thead><tbody><tr><td>00 =</td><td>Intel 852GM/852GMV GMCH (Default) = 3585h</td></tr><tr><td>01-11 =</td><td>Reserved</td></tr></tbody></table>	Product	Device ID	00 =	Intel 852GM/852GMV GMCH (Default) = 3585h	01-11 =	Reserved
Product	Device ID						
00 =	Intel 852GM/852GMV GMCH (Default) = 3585h						
01-11 =	Reserved						



### 3.10.3. PCICMD – PCI Command Register

Address Offset:	04h
Default Value:	0006h
Access:	Read Only, Read/Write
Size:	16 bits

Since Intel 852GM/852GMV GMCH Device #0 does not physically reside on PCI\_A many of the bits are not implemented.

Bit	Descriptions
15:10	<b>Reserved</b>
9	<b>Fast Back-to-Back Enable (FB2B):</b> This bit controls whether or not the master can do fast back-to-back write. Since device 0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no affect.
8	<b>SERR Enable (SERRE):</b> SERR# is not implemented by Function 1 of Device 0 of the Intel 852GM/852GMV GMCH and this bit is hardwired to 0. Writes to this bit position have no effect.
7	<b>Address/Data Stepping Enable (ADSTEP):</b> Address/data stepping is not implemented in the Intel 852GM/852GMV GMCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	<b>Parity Error Enable (PERRE):</b> PERR# is not implemented by Intel 852GM/852GMV GMCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5	<b>VGA Palette Snoop Enable (VGASNOOP):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	<b>Memory Write and Invalidate Enable (MWIE):</b> The Intel 852GM/852GMV GMCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	<b>Special Cycle Enable (SCE):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	<b>Bus Master Enable (BME):</b> The Intel 852GM/852GMV GMCH is always enabled as a master on HI. This bit is hardwired to a "1". Writes to this bit position have no effect.
1	<b>Memory Access Enable (MAE):</b> The Intel 852GM/852GMV GMCH always allows access to main memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	<b>I/O Access Enable (IOAE):</b> This bit is not implemented in the Intel 852GM/852GMV GMCH and is hardwired to a 0. Writes to this bit position have no effect.

### 3.10.4. PCISTS – PCI Status Register

Address Offset:	06h
Default Value:	0080h
Access:	Read Only, Read/Write/Clear
Size:	16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #0's PCI interface. Bit 14 is read/write clear. All other bits are Read Only. Since Intel 852GM/852GMV GMCH Device #0 does not physically reside on PCI\_A many of the bits are not implemented.

Bit	Descriptions
15	<b>Detected Parity Error (DPE):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	<b>Signaled System Error (SSE):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
13	<b>Received Master Abort Status (RMAS):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
12	<b>Received Target Abort Status (RTAS):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
11	<b>Signaled Target Abort Status (STAS):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
10:9	<b>DEVSEL Timing (DEVT):</b> These bits are hardwired to "00". Writes to these bit positions have no affect. Device #0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that the Intel 852GM/852GMV GMCH does not limit optimum DEVSEL timing for PCI_A.
8	<b>Master Data Parity Error Detected (DPD):</b> The Intel 852GM/852GMV GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
7	<b>Fast Back-to-Back (FB2B):</b> This bit is hardwired to 1. Writes to these bit positions have no effect. Device #0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the Intel 852GM/852GMV GMCH does not limit the optimum setting for PCI_A.
6:5	<b>Reserved</b>
4	<b>Capability List (CLIST):</b> This bit is hardwired to 0 to indicate to the configuration software that this device/function does not implement new capabilities.
3:0	<b>Reserved</b>



### 3.10.5. RID – Revision Identification

Address Offset:	08h
Default Value:	01h
Access:	Read Only
Size:	8 bits

This register contains the revision number of the Intel 852GM/852GMV GMCH. These bits are read only and writes to this register have no effect.

Bit	Descriptions
7:0	<b>Revision Identification Number (RID):</b> This is an 8-bit value that indicates the revision identification number for the Intel 852GM/852GMV GMCH.

### 3.10.6. SUBC – Sub-Class Code

Address Offset:	0Ah
Default Value:	80h
Access:	Read Only
Size:	8 bits

This register contains the Sub-Class Code for the Intel 852GM/852GMV GMCH Device #0. This code is 80h indicating a peripheral device.

Bit	Descriptions
7:0	<b>Sub-Class Code (SUBC):</b> This is an 8-bit value that indicates the category of Bridge into which the Intel 852GM/852GMV GMCH falls. The code is 80h indicating other peripheral device.

### 3.10.7. BCC – Base Class Code

Address Offset:	0Bh
Default Value:	08h
Access:	Read Only
Size:	8 bits

This register contains the Base Class Code of the Intel 852GM/852GMV GMCH Device #0 Function #3. This code is 08h indicating a peripheral device.

Bit	Descriptions
7:0	<b>Base Class Code (BASEC):</b> This is an 8-bit value that indicates the Base Class Code for the Intel 852GM/852GMV GMCH. This code has the value 08h, indicating other peripheral device.

### 3.10.8. HDR – Header Type

Address Offset: 0Eh  
 Default Value: 080h  
 Access: Read Only  
 Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	<b>PCI Header (HDR):</b> This field always returns 80 to indicate that Device 0 is a multifunction device. If Functions other than #0 are disabled this field returns a 00 to indicate that the Intel 852GM/852GMV GMCH is a single function device with standard header layout. The default is 80 Reads and writes to this location have no effect.

### 3.10.9. SVID – Subsystem Vendor Identification

Address Offset: 2Ch  
 Default Value: 0000h  
 Access: Write Once  
 Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Descriptions
15:0	<b>Subsystem Vendor ID (SUBVID):</b> This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

### 3.10.10. ID – Subsystem Identification

Address Offset: 2Eh  
 Default Value: 0000h  
 Access: Write Once  
 Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Descriptions
15:0	<b>Subsystem ID (SUBID):</b> This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.



### 3.10.11. CAPPTR – Capabilities Pointer

Address Offset:	34h
Default Value:	00h
Access:	Read Only
Size:	8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Descriptions
7:0	<b>Pointer to the offset of the first capability ID register block:</b> In this case there are no capabilities therefore these bits are hardwired to 00h to indicate the end of the capability-linked list.

### 3.10.12. HPLLCC – HPLL Clock Control Register (Device 0)

Address Offset:	C0–C1h
Default Value:	00h
Access:	Read Only
Size:	16 bits

Bit	Descriptions
15:11	Reserved
10	HPLL VCO Change Sequence Initiate Bit: Software must write a '0' to clear this bit and then write a '1' to initiate sequence again.
9	Hphase Reset Bit: 1 = Assert 0 = Deassert (default)
8	Reserved
7:2	Reserved
1:0	HPLL Clock Control: Software is allowed to update this register. See Table 21 for Clock definitions.

**Table 21. Intel 852GM/852GMV GMCH Configurations**

Straps Read Through HPLLCC[1:0]: D0:F3: Register Offset C0-C1h, bits[1:0]	FSB Frequency	System Memory Frequency	GFX Core Clock(Low)	GFX Core Clock (High)
00	400 MHz	266 MHz	133 MHz	133 MHz
10	400 MHz	200 MHz	133 MHz	133 MHz



### 3.11. Intel 852GM/852GMV GMCH Integrated Graphics Device Registers (Device #2, Function #0)

This section contains the PCI configuration registers listed in order of ascending offset address. Device #2 incorporates Function #0. See Section 3.2 for access nomenclature.

**Table 22. Integrated Graphics Device Configuration Space (Device #2, Function#0)**

Register Name	Register Symbol	Address Offset	Register End	Default Value	Access	Regs in Function#1
Vendor Identification	VID2	00h	01h	8086h	RO	C0F0
Device Identification	DID2	02h	03h	3582h	RO	C0F0
PCI Command Register	PCICMD2	04h	05h	0000h	RO,R/W	U1F1
PCI Status Register	PCISTS2	06h	07h	0090h	RO	U1F1
Revision Identification	RID2	08h	08h	01h	RO	C0F0
Class Code	CC	09h	0Bh	030000h	RO	U1F1
Cache Line Size Register	CLS	0Ch	0Ch	00h	RO	C0F0
Master Latency Timer	MLT2	0Dh	0Dh	00h	RO	C0F0
Header Type	HDR2	0Eh	0Eh	00h	RO	C0F0
Graphics Memory Range Address	GMADR	10h	13h	00000008h	R/W,RO	U1F1
Memory Mapped Range Address	MMADR	14h	17h	00000000h	R/W,RO	U1F1
IO Range Register	IOBAR	18h	1Bh	00000001h	R/W,RO	
Subsystem Vendor ID	SVID2	2Ch	2Dh	0000h	R/WO	C0F0
Subsystem ID	SID2	2Eh	2Fh	0000h	R/ WO	C0F0
Video Bios ROM Base Address	ROMADR	30h	33h	00000000h	RO	C0F0
Interrupt Line Register	INTRLINE	3Ch	3Ch	00h	R/W, RO in F #1	
Interrupt Pin Register	INTRPIN	3Dh	3Dh	01h	RO, Reserved In F#1	
Minimum Grant Register	MINGNT	3Eh	3Eh	00h	RO	C0F0
Maximum Latency Register	MAXLAT	3Fh	3Fh	00h	RO	C0F0
Mirror of GMCH Misc Control	MGMiscC	50h	51h	---	RO	CODO FO GMCH Misc Control Register
Power Management Capabilities	PMCAP	D2h	D3h	0221h	RO	COFO
Power Management Control	PMCS	D4h	D5h	0000h	R/W,RO	U1F1



### 3.11.1. VID2 – Vendor Identification Register – Device #2

Address Offset: 00h 01h  
 Default Value: 8086h  
 Access Attributes: Read Only  
 Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	<b>Vendor Identification Number:</b> This is a 16-bit value assigned to Intel.

### 3.11.2. DID2 – Device Identification Register - Device #2

Address Offset: 02h 03h  
 Default Value: 3582h  
 Access Attributes: Read Only  
 Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	<b>Device Identification Number:</b> This is a 16-bit value assigned to the Intel 852GM/852GMV GMCH IGD.

### 3.11.3. PCICMD2 – PCI Command Register - Device #2

Address Offset:	04h 05h
Default:	0000h
Access:	Read Only, Read/Write
Size:	16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main System Memory.

Bit	Description
15:10	Reserved
9	<b>Fast Back-to-Back (FB2B)</b> RO.
8	<b>SERR# Enable (SERRE)</b> RO.
7	<b>Address/Data Stepping</b> RO.
6	<b>Parity Error Enable (PERRE)</b> RO.
5	<b>Video Palette Snooping (VPS)</b> RO.
4	<b>Memory Write and Invalidate Enable (MWIE)</b> RO.
3	<b>Special Cycle Enable (SCE)</b> RO.
2	<b>Bus Master Enable (BME)</b> R/W: This bit determines if the IGD is to function as a PCI compliant master. 0= Disable IGD bus mastering (default). 1 = Enable IGD bus mastering.
1	<b>Memory Access Enable (MAE)</b> R/W: This bit controls the IGD's response to System Memory space accesses. 0= Disable (default). 1 = Enable.
0	<b>I/O Access Enable (IOAE)</b> R/W: This bit controls the IGD's response to I/O space accesses. 0 = Disable (default). 1 = Enable.



### 3.11.4. PCISTS2 – PCI Status Register - Device #2

Address Offset: 06h 07h  
 Default Value: 0090h  
 Access: Read Only  
 Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Description
15	<b>Detected Parity Error (DPE):</b> Since the IGD does not detect parity, this bit is always set to 0.
14	<b>Signaled System Error (SSE) – RO</b>
13	<b>Received Master Abort Status (RMAS) – RO</b>
12	<b>Received Target Abort Status (RTAS) – RO</b>
11	<b>Signaled Target Abort Status (STAS) – RO</b>
10:9	<b>DEVSEL# Timing (DEVT) – RO</b>
8	<b>Data Parity Detected (DPD) – RO</b>
7	<b>Fast Back-to-Back (FB2B) – RO</b>
6	<b>User Defined Format (UDF) – RO</b>
5	<b>66-MHz PCI Capable (66C) – RO</b>
4	<b>CAP LIST:</b> This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3:0	<b>Reserved</b>

### 3.11.5. RID2 – Revision Identification Register - Device #2

Address Offset: 08h  
 Default Value: 01h  
 Access: Read Only  
 Size: 8 bits

This register contains the revision number of the IGD. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	<b>Revision Identification Number:</b> This is an 8-bit value that indicates the revision identification number for the Intel 852GM/852GMV GMCH.

### 3.11.6. CC – Class Code Register - Device #2

Address Offset:	09h 0Bh
Default Value:	030000h
Access:	Read Only
Size:	24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Description
23:16	<b>Base Class Code (BASEC):</b> 03=Display controller
15:8	<b>Sub-Class Code (SCC):</b> Function 0: 00h=VGA compatible or 80h=Non VGA Function 1: 80h=Non VGA
7:0	<b>Programming Interface (PI):</b> 00h=Hardwired as a Display controller.

### 3.11.7. CLS – Cache Line Size Register - Device #2

Address Offset:	0Ch
Default Value:	00h
Access:	Read only
Size:	8 bits

The IGD does not support this register as a PCI slave.

Bit	Description
7:0	<b>Cache Line Size (CLS) – RO</b>

### 3.11.8. MLT2 – Master Latency Timer Register - Device #2

Address Offset:	0Dh
Default Value:	00h
Access:	Read Only
Size:	8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Description
7:0	<b>Master Latency Timer Count Value – RO</b>



### 3.11.9. HDR2 – Header Type Register - Device #2

Address Offset:	0Eh
Default Value:	00h
Access:	Read Only
Size:	8 bits

This register contains the Header Type of the IGD.

Bit	Description
7	<b>Multi Function Status (MFunc):</b> Indicates if the device is a Multi-Function Device.
6:0	<b>Header Code (H):</b> This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

### 3.11.10. GMADR – Graphics Memory Range Address Register - Device #2

Address Offset:	10 13h
Default Value:	00000008h
Access:	Read/Write, Read Only
Size:	32 bits

IGD graphics System Memory base address is specified in this register.

Bit	Description
31:27	<b>Memory Base Address</b> R/W: Set by the OS, these bits correspond to address signals [31:26].
26	<b>128-MB Address Mask – RO:</b> 0 indicates 128-MB address
25:4	<b>Address Mask</b> RO: Indicates (at least) a 32-MB address range.
3	<b>Prefetchable Memory</b> RO: Enable prefetching.
2:1	<b>Memory Type</b> RO: Indicate 32-bit address.
0	<b>Memory/IO Space</b> RO: Indicate System Memory space.

### 3.11.11. MMADR – Memory Mapped Range Address Register - Device #2

Address Offset:	14 17h
Default Value:	00000000h
Access:	Read/Write, Read Only
Size:	32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512-kB and the base address is defined by bits [31:19].

Bit	Description
31:19	<b>Memory Base Address</b> R/W: Set by the OS, these bits correspond to address signals [31:19].
18:4	<b>Address Mask</b> RO: Indicate 512 -kB address range.
3	<b>Prefetchable Memory</b> RO: Prevents prefetching.
2:1	<b>Memory Type</b> RO: Indicates 32-bit address.
0	<b>Memory / IO Space</b> RO: Indicates System Memory space.

### 3.11.12. IOBAR – I/O Base Address Register - (Device #2)

Address offset:	18-1Bh
Default:	00000001h
Access:	Read/Write
Size:	16-bits

This register provides the Base offset of the I/O registers within Device #2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16-bit I/O Address Space. Bits 2:1 are fixed and return zero, bit 0 is hardwired to a one indicating that 8-bytes of I/O space are decoded.

Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if internal graphics is disabled. Note that access to this IO BAR is independent of VGA functionality within Device #2. Also note that this mechanism is available only through Function #0 of Device#2 and is not duplicated in Function #1.

If accesses to this IO bar are allowed, then the Intel 852GM/852GMV GMCH claims all 8-bit, 16-bit, or 32-bit IO cycles from the CPU that falls within the 8B claimed.

Bit	Description
31:16	<b>Reserved</b>
15:3	<b>IO Base Address</b> R/W: Set by the OS, these bits correspond to address signals [15:3].
2:1	<b>Memory Type</b> RO: Indicates 32-bit address.
0	<b>Memory / IO Space</b> RO



### 3.11.13. SVID2 – Subsystem Vendor Identification Register - Device #2

Address Offset: 2C 2Dh  
 Default Value: 0000h  
 Access: Read/Write Once  
 Size: 16 bits

Bit	Description
15:0	<b>Subsystem Vendor ID:</b> This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

### 3.11.14. SID2 – Subsystem Identification Register - Device #2

Address Offset: 2E 2Fh  
 Default Value: 0000h  
 Access: Read/Write Once  
 Size: 16 bits

Bit	Description
15:0	<b>Subsystem Identification:</b> This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

### 3.11.15. ROMADR – Video BIOS ROM Base Address Registers - Device #2

Address Offset: 30 33h  
 Default Value: 00000000h  
 Access: Read Only  
 Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0's.

Bit	Description
31:18	<b>ROM Base Address RO</b>
17:11	<b>Address Mask RO:</b> Indicates 256 kB address range.
10:1	<b>Reserved</b>
0	<b>ROM BIOS Enable RO:</b> Indicates ROM not accessible.

### 3.11.16. INTRLINE Interrupt Line Register - Device #2

Address Offset: 3Ch  
 Default Value: 00h  
 Access: Read/Write  
 Size: 8 bits

Bit	Description
7:0	<b>Interrupt Connection:</b> Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller that the device's interrupt pin is connected to.

### 3.11.17. INTRPIN Interrupt Pin Register - Device #2

Address Offset: 3Dh  
 Default Value: 01h, 00h for Function #1  
 Access: Read Only  
 Size: 8 bits

Bit	Description
7:0	<b>Interrupt Pin:</b> As a single function device, the IGD (Integrated GFX Device) specifies INTA# as its interrupt pin. 01h=INTA#. For Function #1, this register is set to 00h.

### 3.11.18. MINGNT – Minimum Grant Register - Device #2

Address Offset: 3Eh  
 Default Value: 00h  
 Access: Read Only  
 Size: 8 bits

Bit	Description
7:0	<b>Minimum Grant Value:</b> The IGD does not burst as a PCI compliant master.

### 3.11.19. MAXLAT – Maximum Latency Register - Device #2

Address Offset: 3Fh  
 Default Value: 00h  
 Access: Read Only  
 Size: 8 bits

Bit	Description
7:0	<b>Maximum Latency Value:</b> Bits[7:0]=00h. The IGD has no specific requirements for how often it needs to access the PCI bus.



### 3.11.20. PMCAP – Power Management Capabilities Register - Device #2

Address Offset: D2h D3h  
 Default Value: 0221h  
 Access: Read Only  
 Size: 16 bits

Bit	Description
15:11	<b>PME Support:</b> This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10:6	<b>Reserved</b>
5	<b>Device Specific Initialization (DSI):</b> Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	<b>Auxiliary Power Source:</b> Hardwired to 0.
3	<b>PME Clock:</b> Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	<b>Version:</b> Hardwired to 001b to indicate there are 4 bytes of power management registers implemented.

### 3.11.21. PMCS – Power Management Control/Status Register - Device #2

Address Offset: D4h D5h  
 Default Value: 0000h  
 Access: Read/Write, Read Only  
 Size: 16 bits

Bit	Description										
15	<b>PME_Status RO:</b> This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).										
14:9	<b>Reserved</b>										
8	<b>PME_En RO:</b> This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.										
7:2	<b>Reserved</b>										
1:0	<p><b>PowerState R/W:</b> This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values.</p> <table border="0"> <thead> <tr> <th>Bits[1:0]</th> <th>Power State</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>D0 Default</td> </tr> <tr> <td>01</td> <td>D1</td> </tr> <tr> <td>10</td> <td>D2 Not Supported</td> </tr> <tr> <td>11</td> <td>D3</td> </tr> </tbody> </table>	Bits[1:0]	Power State	00	D0 Default	01	D1	10	D2 Not Supported	11	D3
Bits[1:0]	Power State										
00	D0 Default										
01	D1										
10	D2 Not Supported										
11	D3										



## 4. Intel 852GM/852GMV GMCH System Address Map

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A system based on the GMCH supports 4 GB of addressable System Memory space and 64 kB+3B of addressable I/O space. The I/O and System Memory spaces are divided by system configuration software into regions. The System Memory ranges are useful either as System Memory or as specialized System Memory, while the I/O regions are used solely to control the operation of devices in the system.

When the GMCH receives a write request whose address targets an invalid space, the data is ignored. For reads, the GMCH responds by returning all zeros on the requesting interface.

### 4.1. System Memory Address Ranges

The GMCH provides a maximum System Memory of 1-GB. The GMCH does not remap APIC memory space and does not limit DDR SDRAM space in hardware. **It is the BIOS or system designer's responsibility to limit System Memory population so that adequate PCI High BIOS and APIC memory space can be allocated.** Figure 4 and Figure 5 represent System Memory address map in a simplified form and provide details on mapping specific System Memory regions as defined and supported by the GMCH.



Figure 4. Simplified View of System Address Map

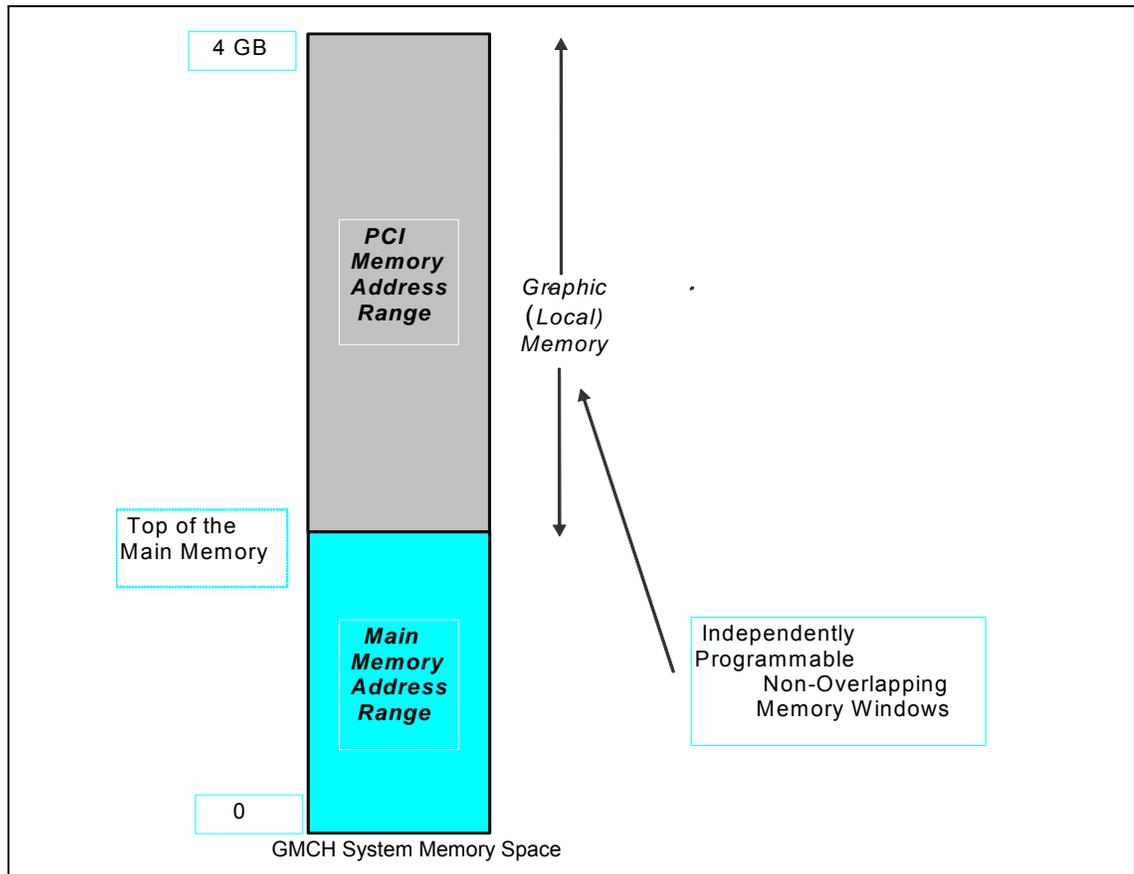
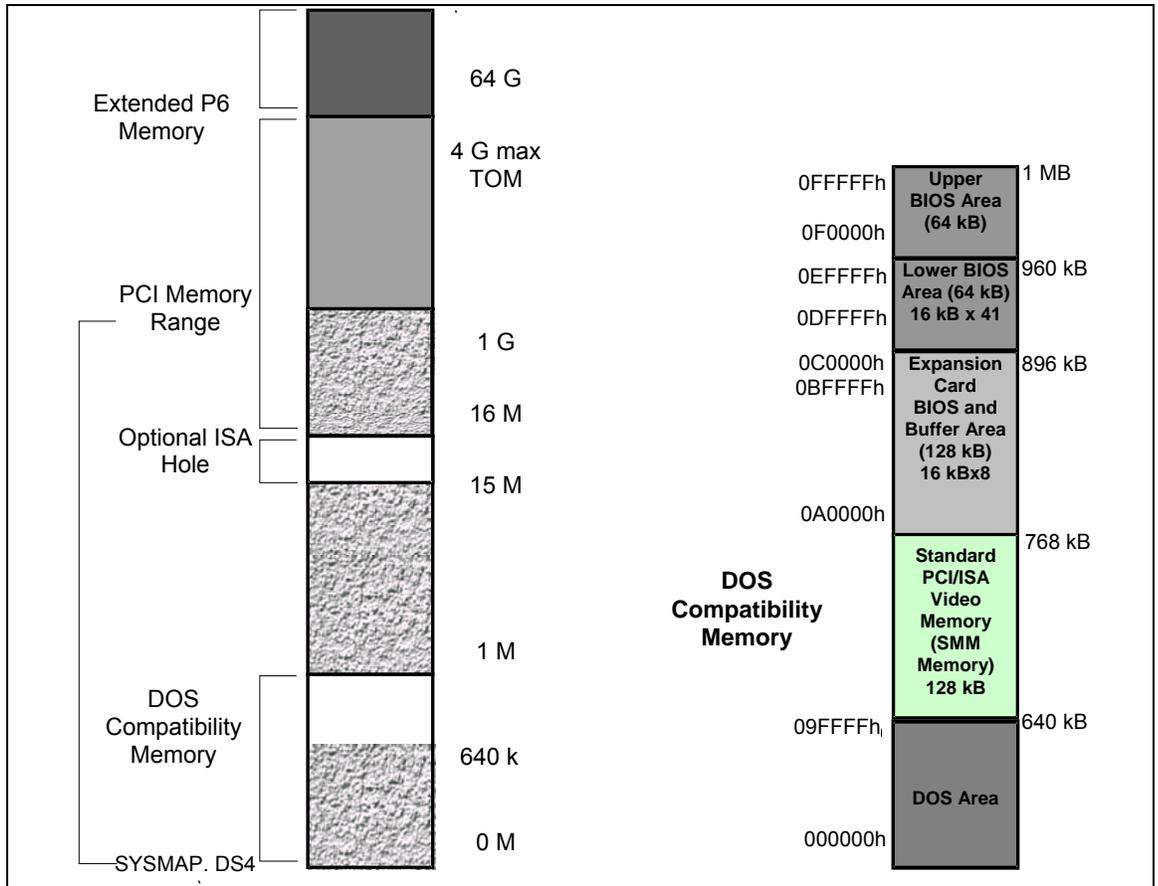


Figure 5. Detailed View of System Address Map



## 4.2. Compatibility Area

This area is divided into the following address regions:

- 0 - 640 kB DOS Area
- 640 – 768 kB Video Buffer Area
- 768 - 896 kB in 16-kB sections (total of 8 sections) - Expansion Area
- 896 –960 kB in 16-kB sections (total of 4 sections) - Extended System BIOS Area
- 960 kB - 1 MB System Memory (BIOS Area) - System BIOS Area

There are 16 System Memory segments in the compatibility area. Thirteen of the System Memory ranges can be enabled or disabled independently for both read and write cycles.



Table 23. System Memory Segments and Their Attributes

System Memory Segments	Attributes	Comments
000000H - 09FFFFH	Fixed - always mapped to main DDR SDRAM	0 to 640 kB – DOS Region
0A0000H - 0BFFFFH	Mapped to Hub Interface or IGD - configurable as SMM space	Video Buffer (physical DDR SDRAM configurable as SMM space)
0C0000H - 0C3FFFH	WE RE	Add-on BIOS
0C4000H - 0C7FFFH	WE RE	Add-on BIOS
0C8000H - 0CBFFFH	WE RE	Add-on BIOS
0CC000H - 0CFFFFH	WE RE	Add-on BIOS
0D0000H - 0D3FFFH	WE RE	Add-on BIOS
0D4000H - 0D7FFFH	WE RE	Add-on BIOS
0D8000H - 0DBFFFH	WE RE	Add-on BIOS
0DC000H - 0DFFFFH	WE RE	Add-on BIOS
0E0000H - 0E3FFFH	WE RE	BIOS Extension
0E4000H - 0E7FFFH	WE RE	BIOS Extension
0E8000H - 0EBFFFH	WE RE	BIOS Extension
0EC000H - 0EFFFFH	WE RE	BIOS Extension
0F0000H - 0FFFFFFH	WE RE	BIOS Area

### DOS Area (00000h-9FFFFh)

The DOS area is 640-kB in size and is always mapped to the main System Memory controlled by the GMCH.

### Legacy VGA Ranges (A0000h-BFFFFh)

The legacy 128-kB VGA memory range A0000h-BFFFFh (Frame Buffer) can be mapped to IGD (Device #2) and to the Hub Interface depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the GMCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The GMCH always positively decodes internally mapped devices, namely the IGD. Subsequent decoding of regions mapped to the Hub Interface depends on the Legacy VGA configurations bits (VGA Enable and MDAP). This region is also the default for SMM space.

### Compatible SMRAM Address Range (A0000h-BFFFFh)

When compatible SMM space is enabled, SMM-mode CPU accesses to this range are routed to physical DDR SDRAM at this address. Non-SMM-mode CPU accesses to this range are considered to be to the video buffer area as described above. Hub Interface originated cycles to enabled SMM space are not allowed and are considered to be to the video buffer area.

### **Monochrome Adapter (MDA) Range (B0000h - B7FFFh)**

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD and the Hub Interface (depending on configuration bits). Since the monochrome adapter may be mapped to anyone of these devices, the GMCH must decode cycles in the MDA range and forward them either to IGD or to Hub Interface. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the System Memory range B0000h to B7FFFh, the GMCH decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, and 3BFh and forwards them to the either the IGD or the Hub Interface.

### **Expansion Area (C0000h-DFFFFh)**

This 128-kByte ISA Expansion region is divided into eight 16-kByte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through GMCH and are subtractively decoded to ISA space. System Memory that is disabled is not remapped.

### **Extended System BIOS Area (E0000h-EFFFFh)**

This 64-kByte area is divided into four 16-kByte segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DDR SDRAM or to Hub Interface. Typically, this area is used for RAM or ROM. System Memory segments that are disabled are not remapped elsewhere.

### **System BIOS Area (F0000h-FFFFFFh)**

This area is a single 64-kByte segment. This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to Hub Interface. By manipulating the Read/Write attributes, the GMCH can “shadow” BIOS into the main DDR SDRAM. When disabled, this segment is not remapped.

## **4.3. Extended System Memory Area**

This System Memory area covers 100000h (1 MB) to FFFFFFFFh (4 GB-1) address range and it is divided into the following regions:

- Main System Memory from 1 MByte to the Top of System Memory; maximum 512 MB.

- PCI Memory space from the Top of System Memory to 4 GB with two specific ranges.

- APIC Configuration Space from FEC0\_0000h (4 GB-20 MB) to FECF\_FFFFh and FEE0\_0000h to FEEF\_FFFFh

- High BIOS area from 4 GByte to 4 GByte - 2 MB



## 4.4. Main System Memory Address Range (0010\_0000h to Top of Main Memory)

The address range from 1 MB to the top of main system memory is mapped to main DDR SDRAM address range controlled by the GMCH. The Top of Memory (TOM) is limited to 512-MB DDR SDRAM. The GMCH will forward all accesses to addresses within this range to the DDR SDRAM unless a hole in this range is created using the fixed hole as controlled by the FDHC register. Accesses within this hole are forwarded to Hub interface.

The GMCH provides a maximum DDR SDRAM address decode space of 4 GB. The GMCH does not remap APIC memory space. The GMCH does not limit DDR SDRAM address space in hardware.

### 4.4.1. 15 MB-16 MB Window

A hole can be created at 15 MB-16 MB as controlled by the fixed hole enable (FDHC register) in Device 0 space. Accesses within this hole are forwarded to the Hub Interface. The range of physical DDR SDRAM disabled by opening the hole is not remapped to the Top of the memory – that physical DDR SDRAM space is not accessible. This 15 MB-16 MB hole is an optionally enabled ISA hole. Video accelerators originally used this hole. Validation and customer SV teams also use it for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15-16 hole.

### 4.4.2. Pre-allocated System Memory

Voids of physical addresses that are not accessible as general System Memory and reside within System Memory address range (< TOM) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of BIOS to properly initialize these regions.** The number of UMA options has been extended. Allocation is at a fixed address in terms of rigid positioning of UMA System Memory →TOM-TSEG-UMA(size), but it is mapped at any available address by a PCI allocation algorithm. GMADR and MMADR are requested through BARs.

The following table details the location and attributes of the regions.

**Table 24. Pre-allocated System Memory**

System Memory Segments	Attributes	Comments
00000000H - 03E7FFFFH	R/W	Available System Memory 62.5 MB
03E80000H - 03F7FFFFH	R/W	Pre-allocated Graphics VGA memory. 1-MB (or 4/8/16/32- MB) when IGD is enabled.
03F80000H - 03FFFFFFH	SMM Mode Only - CPU Reads	TSEG Address Range
03F80000H - 03FFFFFFH	SMM Mode Only - CPU Reads	TSEG Pre-allocated System Memory

#### 4.4.2.1. Extended SMRAM Address Range (HSEG and TSEG)

The HSEG and TSEG SMM transaction address spaces reside in this extended System Memory area.

#### 4.4.2.2. HSEG

SMM mode CPU accesses to enabled HSEG are remapped to 000A0000h-000BFFFFh. Non-SMM mode CPU accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM mode Write Back cycles that are remapped to SMM space to maintain cache coherency. Hub Interface originated cycles to enabled SMM space are not allowed. Physical DDR SDRAM behind the HSEG transaction address is not remapped and is not accessible.

#### 4.4.2.3. TSEG

TSEG is 1-MB in size and is at the top of physical System Memory. SMM mode CPU accesses to enabled TSEG access the physical DDR SDRAM at the same address. Non-SMM mode CPU accesses to enabled TSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode Write Back cycles that are directed to the physical SMM space to maintain cache coherency. Hub Interface originated cycles that enable SMM space are not allowed.

The size of the SMRAM space is determined by the USMM value in the SMRAM register. When the extended SMRAM space is enabled, non-SMM CPU accesses and all other accesses in this range are forwarded to the Hub Interface. When SMM is enabled the amount of System Memory available to the system is equal to the amount of physical DDR SDRAM minus the value in the TSEG register.

#### 4.4.2.4. Intel Dynamic Video Memory Technology (DVMT)

The IGD supports DVMT in a non-graphics System Memory configuration. DVMT is a mechanism that manages System Memory and the internal graphics device for optimal graphics performance. DVMT-enabled software drivers, working with the memory arbiter and the operating system, utilize the System Memory to support 2D graphics and 3D applications. DVMT dynamically responds to application requirements by allocating the proper amount of display and texturing memory.

#### 4.4.2.5. PCI Memory Address Range (Top of Main System Memory to 4 GB)

The address range from the top of main DDR SDRAM to 4-GB (top of physical System Memory space supported by the GMCH) is normally mapped via the Hub Interface to PCI.

As an internal graphics configuration, there are two exceptions to this rule.

1. The first exception is addresses decoded to the Graphics Memory Range. One per function in device #2.
2. The second exception is addresses decoded to the System Memory Mapped Range of the Internal Graphics Device. One per function in device #2. Both exception cases are forwarded to the Internal Graphics Device.

There are two sub-ranges within the PCI Memory address range defined as APIC Configuration Space and High BIOS Address Range. As an Internal Graphics Device, the Graphics Memory Range and the Memory Mapped Range of the Internal Graphics Device **MUST NOT** overlap with these two ranges. These ranges are described in detail in the following paragraphs.



#### 4.4.2.6. APIC Configuration Space (FEC0\_0000h -FECF\_FFFFh, FEE0\_0000h-FEEF\_FFFFh)

This range is reserved for APIC configuration space that includes the default I/O APIC configuration space. The default Local APIC configuration space is FEE0\_0000h to FEEF\_0FFFh.

CPU accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the CPU. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each CPU should be relocated to the FEC0\_0000h (4 GB-20 MB) to FECF\_FFFFh range so that one MTRR can be programmed to 64-kB for the Local and I/O APICs. The I/O APIC(s) usually resides in the ICH4-M portion of the chip-set or as a stand-alone component(s).

I/O APIC units will be located beginning at the default address FEC0\_0000h. The first I/O APIC will be located at FEC0\_0000h. Each I/O APIC unit is located at FEC0\_x000h where *x* is I/O APIC unit number 0 through F(hex). This address range will be normally mapped to Hub Interface.

The address range between the APIC configuration space and the High BIOS (FED0\_0000h to FFDF\_FFFFh) is always mapped to the Hub Interface.

#### 4.4.2.7. High BIOS Area (FFE0\_0000h -FFFF\_FFFFh)

The top 2-MB of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. CPU begins execution from the High BIOS after reset. This region is mapped to Hub Interface so that the upper subset of this region aliases to 16 MB to 256-kB range. The actual address space required for the BIOS is less than 2 MB but the minimum CPU MTRR range for this region is 2-MB so that full 2-MB must be considered.

### 4.4.3. System Management Mode (SMM) Memory Range

The GMCH supports the use of main System Memory as System Management RAM (SMM RAM) enabling the use of System Management Mode. The GMCH supports three SMM options: Compatible SMRAM (C\_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a System Memory area that is available for the SMI handler's and code and data storage. This System Memory resource is normally hidden from the system OS so that the processor has immediate access to this System Memory space upon entry to SMM. The GMCH provides three SMRAM options:

Below 1-MByte option that supports compatible SMI handlers.

Above 1-MByte option that allows new SMI handlers to execute with write-back cacheable SMRAM.

Above 1-MByte solutions require changes to compatible SMRAM handlers code to properly execute above 1-MByte.

**Note:** Hub Interface is not allowed to access the SMM space.

### 4.4.3.1. SMM Space Restrictions

If any of the following conditions are violated the results of SMM accesses are unpredictable and may cause the system to hang:

1. The Compatible SMM space **must not** be set-up as cacheable.
2. High or TSEG SMM transaction address space **must not** overlap address space assigned to DDR SDRAM or to any “PCI” devices (including Hub Interface and graphics devices). This is a BIOS responsibility.
3. Both D\_OPEN and D\_CLOSE **must not** be set to 1 at the same time.
4. When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available . This is a BIOS responsibility.

### 4.4.3.2. SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DDR SDRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the CPU to access SMM space. DDR SDRAM SMM space is defined as the range of physical DDR SDRAM locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High, and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DDR SDRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DDR SDRAM SMM space is a different address range. Note that the High DDR SDRAM space is the same as the Compatible Transaction Address space. The table below describes three unique address ranges:

1. Compatible Transaction Address (Adr C)
2. High Transaction Address (Adr H)
3. TSEG Transaction Address (Adr T)

These abbreviations are used later in Table 25.

**Table 25. SMM Space Transaction Handling**

SMM Space Enabled	Transaction Address Space (Adr)	DRAM Space (DRAM)
Compatible (C)	A0000h to BFFFFh	A0000h to BFFFFh
High (H)	0FEDA0000h to 0FEDBFFFFh	A0000h to BFFFFh
TSEG (T)	(TOM-TSEG_SZ) to TOM	(TOM-TSEG_SZ) to TOM

### 4.4.4. System Memory Shadowing

Any block of System Memory that can be designated as read-only or write-only can be “shadowed” into GMCH DDR SDRAM. Typically this is done to allow ROM code to execute more rapidly out of main DDR SDRAM. ROM is used as a read-only during the copy process while DDR SDRAM at the same time is designated write-only. After copying, the DDR SDRAM is designated read-only so that ROM is shadowed. CPU bus transactions are routed accordingly.

### 4.4.5. I/O Address Space

The GMCH does not support the existence of any other I/O devices beside itself on the CPU bus. The GMCH generates Hub Interface or PCI bus cycles for all CPU I/O accesses that it does not claim. Within



the host bridge the GMCH contains two internal registers in the CPU I/O space, Configuration Address Register (CONFIG\_ADDRESS) and the Configuration Data Register (CONFIG\_DATA). These locations are used to implement configuration space access mechanism and as described in the Configuration register section.

The CPU allows 64kB +3B to be addressed within the I/O space. The GMCH propagates the CPU I/O address without any translation on to the destination bus and therefore provides addressability for 64 k+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when CPU bus A16# address signal is asserted. A16# is asserted on the CPU bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. A16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) is consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics IO decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the Hub Interface. The GMCH will not post I/O write cycles to IDE.

#### 4.4.6. GMCH Decode Rules and Cross-Bridge Address Mapping

The address map described above applies globally to accesses arriving on any of the three interfaces i.e. Host bus, IGD, and Hub Interface.

#### 4.4.7. Hub Interface Decode Rules

The GMCH accepts accesses from Hub Interface to the following address ranges:

- All memory read and write accesses to Main DDR SDRAM including PAM region (except SMM space)
- All memory read/write accesses to the Graphics Aperture (DRAM) defined by APBASE and APSIZE.
- Memory writes to VGA range.

All memory reads from the Hub Interface A that are targeted > 4-GB System Memory range will be terminated with Master Abort completion, and all memory writes (>4-GB) from the Hub Interface will be ignored.

Hub Interface System Memory accesses that fall elsewhere within the System Memory range are considered invalid and will be remapped to System Memory address 0h, snooped on the host bus, and dispatched to DDR SDRAM. Reads will return all 1's with Master Abort completion. Writes will have BE's deasserted and will terminate with Master Abort if completion is required. I/O cycles will not be accepted. They are terminated with Master Abort completion packets.



#### 4.4.7.1. Hub Interface Accesses to GMCH that Cross Device Boundaries

Hublink accesses are limited to 256-bytes but have no restrictions on crossing address boundaries. A single Hublink request may therefore span device boundaries (DDR SDRAM) or cross from valid addresses to invalid addresses (or vice versa). The GMCH does not support transactions that cross device boundaries. For reads and for writes requiring completion, the GMCH will provide separate completion status for each naturally aligned 32 -or 64 -byte block. If the starting address of a transaction hits a valid address, the portion of a request that hits that target device (DDR SDRAM) will complete normally. The remaining portion of the access that crosses a device boundary (targets a different device than that of the starting address) or hits an invalid address will be remapped to System Memory address 0h, snooped on the host bus, and dispatched to DDR SDRAM. Reads will return all 1's with Master Abort completion. Writes will have BE's deasserted and will terminate with Master Abort if completion is required.

If the starting address of a transaction hits an invalid address the entire transaction will be remapped to System Memory address 0h, snooped on the host bus, and dispatched to DDR SDRAM. Reads will return all 1's with Master Abort completion. Writes will have BE's deasserted and will terminate with Master Abort if completion is required.



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## 5. Functional Description

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### 5.1. Host Interface Overview

The GMCH Processor System Bus uses source synchronous transfer for the address and data signals. The address signals are double pumped and two addresses can be generated every bus clock. At 100-MHz bus frequency, the two address signals run at 200-MT/s for a maximum address queue rate of 50-M addresses/sec. The data is quad pumped and an entire 64B cache line can be transferred in two bus clocks. At 100-MHz bus frequency, the data signals run at 400 MHz for a maximum bandwidth of 3.2-GB/s. The 852GM/852GMV GMCH has In-Order Queue to support outstanding pipelined address requests on the host bus.

### 5.2. Dynamic Bus Inversion

The GMCH supports Dynamic Bus Inversion (DBI) when driving and receiving data from the Host Bus. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the power consumption of the GMCH. DINV[3:0] indicates if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

**Table 26. Relation of DBI Bits to Data Bits**

DINV[3:0]	Data Bits
DINV[0]#	HD[15:0]#
DINV[1]#	HD[31:16]#
DINV[2]#	HD[47:32]#
DINV[3]#	HD[63:48]#

Whenever the CPU or the GMCH drives data, each 16-bit segment is analyzed. If more than eight of the 16 signals would normally be driven low on the bus the corresponding DINV# signal will be asserted and the data will be inverted prior to being driven on the bus. Whenever the CPU or the GMCH receives data it monitors DINV[3:0]# to determine if the corresponding data segment should be inverted.

#### 5.2.1. System Bus Interrupt Delivery

Each processor supports System Bus interrupt delivery. It does not support the APIC serial bus interrupt delivery mechanism. Interrupt related messages are encoded on the System Bus as “Interrupt Message Transactions”. In a GMCH platform, System Bus interrupts may originate from the processor on the System Bus, or from a downstream device on Hub Interface.

In a GMCH platform, the ICH4-M contains IOxAPICs and its interrupts are generated as upstream Hub Interface Memory Writes. Furthermore, PCI 2.2 defines MSI’s (Message Signaled Interrupts) that are also in the form of Memory Writes. A PCI 2.2 device may generate an interrupt as an MSI cycle on its PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC, which in turn generates an interrupt as an upstream Hub Interface Memory Write. Alternatively the MSI may be directed directly to the System bus. The target of an MSI is dependent on



the address of the interrupt Memory Write. The GMCH forwards inbound Hub Interface Memory Writes to address 0FEEEx\_xxxxh, to the System bus as “Interrupt Message Transactions”.

## 5.2.2. Upstream Interrupt Messages

The GMCH accepts message based interrupts from its Hub Interface and forwards them to the System bus as Interrupt Message Transactions. The interrupt messages presented to the GMCH are in the form of Memory Writes to address 0FEEEx\_xxxxh. At the Hub Interface the Memory Write interrupt message is treated like any other Memory Write; it is either posted into the inbound data buffer (if space is available) or retried (if data buffer space is not immediately available). Once posted, the Memory Write from the Hub Interface, to address 0FEEEx\_xxxxh, is decoded as a cycle that needs to be propagated by the GMCH to the System bus as an Interrupt Message Transaction.

## 5.3. System Memory Interface

### 5.3.1. DDR SDRAM Interface Overview

The GMCH supports DDR SDRAM at 200/266-MHz and includes the following support:

- Up to 1-GB of PC1600/PC2100 DDR SDRAM (Intel 852GM/852GMV GMCH)
- PC1600/2100 unbuffered 200-pin DDR SDRAM SO-DIMMs
- Maximum of two SO-DIMMs, single-sided and/or double-sided

The 2-bank select lines SBA[1:0] and the 13 Address lines SMA[12:0] allow the GMCH to support 64-bit wide SO-DIMMs using 128-Mb, 256-Mb, and 512-Mb DDR SDRAM technology. While address lines SMA[9:0] determine the starting address for a burst, burst length can only be 4. Four chip selects SCS[3:0]# lines allow a maximum of two rows of single-sided DDR SDRAM SO-DIMMs and four rows of double-sided DDR SDRAM SO-DIMMs.

The GMCH main System Memory controller targets CAS latencies of 2 and 2.5 for DDR SDRAM. The GMCH provides refresh functionality with a programmable rate (normal DDR SDRAM rate is 1 refresh/15.6 s). For write operations of less than a full cache line, GMCH will perform a cache-line read and into the write buffer and perform byte-wise write-merging in the write buffer.

### 5.3.2. System Memory Organization and Configuration

#### 5.3.2.1. Configuration Mechanism for SO-DIMMs

Detection of the type of DDR SDRAM installed on the SO-DIMM is supported via Serial Presence Detect mechanism as defined in the JEDEC 200-pin SO-DIMM specification.

Before any cycles to the System Memory interface can be supported, the GMCH DDR SDRAM registers must be initialized. The GMCH must be configured for operation with the installed System Memory types. Detection of System Memory type and size is done via the System Management Bus (SMB) interface on the ICH4-M. This two-wire bus is used to extract the DDR SDRAM type and size information from the Serial Presence Detect port on the DDR SDRAM SO-DIMMs. DDR SDRAM SO-DIMMs contain a 5-pin Serial Presence Detect interface, including SCL (serial clock), SDA (serial data) and SA[2:0]. Devices on the SMBus have a 7-bit address. For the DDR SDRAM SO-DIMMs, the upper four bits are fixed at 1010. The lower three bits are strapped on the SA[2:0] pins. SCL and SDA are connected directly to the System Management Bus on the ICH4-M. Thus data is read from the Serial

Presence Detect port on the SO-DIMMs via a series of I/O cycles to the south bridge. The BIOS needs to determine the size and type of System Memory used for each of the rows of System Memory in order to properly configure the GMCH System Memory interface.

For SMBus Configuration and Access of the Serial Presence Detect Ports, refer to the Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet (order number: 252337) for more detail.

### 5.3.2.2. System Memory Register Programming

This section provides an overview of how the required information for programming the DDR SDRAM registers is obtained from the Serial Presence Detect ports on the SO-DIMMs. The Serial Presence Detect ports are used to determine Refresh Rate, MA and MD Buffer Strength, Row Type (on a row by row basis), DDR SDRAM Timings, Row Sizes and Row Page Sizes. The following table lists a subset of the data available through the on board Serial Presence Detect ROM on each SO-DIMM.

**Table 27. Data Bytes on SO-DIMM Used for Programming DRAM Registers**

Byte	Function
2	System Memory Type (DDR SDRAM)
3	Number of Row Addresses, not counting Bank Addresses
4	Number of Column Addresses
5	Number of SO-DIMM banks
11	No ECC
12	Refresh Rate/Type
17	Number Banks on each Device

The above table is only a subset of the defined SPD bytes on the SO-DIMMs. These bytes collectively provide enough data for programming the GMCH DDR SDRAM registers.

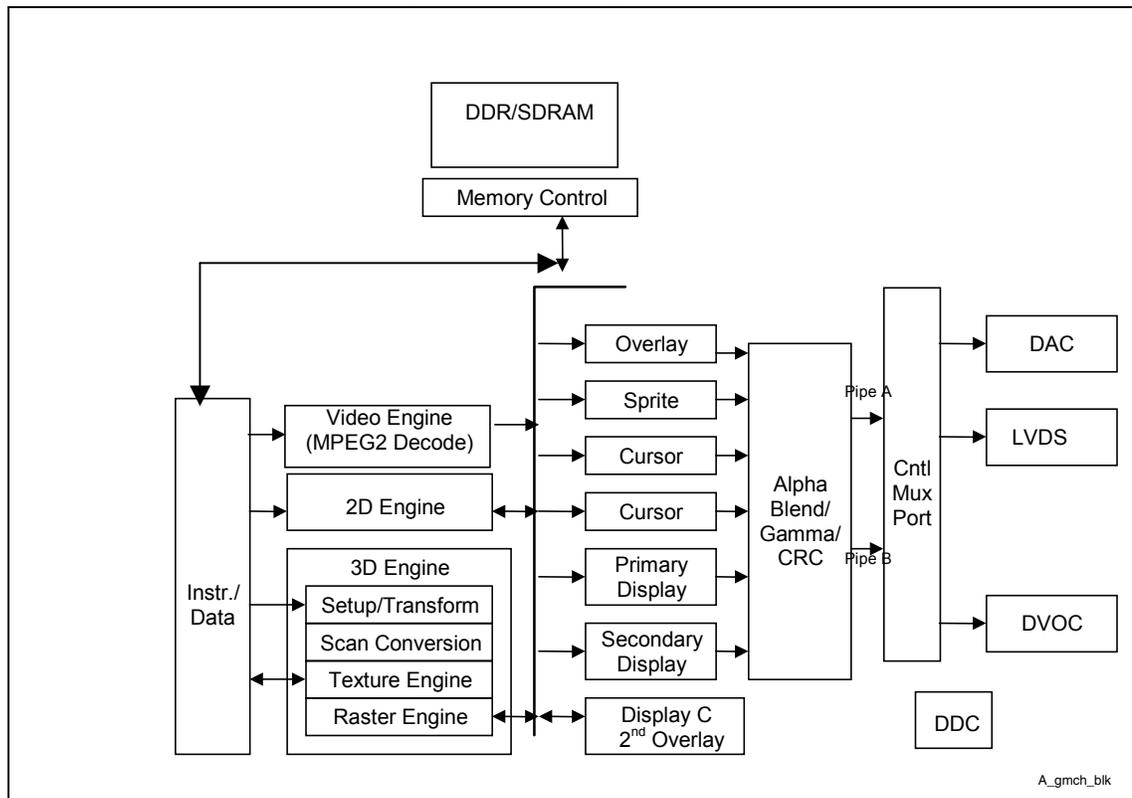
### 5.3.3. DDR SDRAM Performance Description

The overall System Memory performance is controlled by the DDR SDRAM timing register, pipelining depth used in GMCH, System Memory speed grade and the type of DDR SDRAM used in the system. Besides this, the exact performance in a system is also dependent on the total System Memory supported, external buffering and System Memory array layout. The most important contribution to overall performance by the System Memory controller is to minimize the latency required to initiate and complete requests to System Memory, and to support the highest possible bandwidth (full streaming, quick turn-arounds). One measure of performance is the total flight time to complete a cache line request. A true discussion of performance really involves the entire chipset, not just the System Memory controller.

## 5.4. Integrated Graphics Overview

The GMCH provides a highly integrated graphics accelerator and PCI set while allowing a flexible Integrated System Graphics solution.

Figure 6. Intel 852GM/852GMV GMCH Graphics Block Diagram



High bandwidth access to data is provided through the System Memory port. The GMCH uses a tiling architecture to minimize page miss latencies and thus maximize effective rendering bandwidth.

### 5.4.1. 3D/2D Instruction Processing

The GMCH contains an extensive set of instructions that control various functions including 3D rendering, BLT operations, display, MPEG decode acceleration, and overlay. The 3D instructions set 3D pipeline states and control the processing functions. The 2D instructions provide an efficient method for invoking BLT operations.

## 5.4.2. 3D Engine

The 3D engine of the GMCH has been designed with a deeply pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive. The GMCH supports the following:

- Perspective-correct Texture Mapping,
- Multitextures
- Embossed and Dot-Product Bump-Mapping
- Cubic Environment Maps
- Bilinear, Trilinear, and Anisotropic MIP mapped filtering
- Gouraud shading
- Alpha-blending
- Per-Vertex and Per- Pixel Fog
- Z/W Buffering

These features are independently controlled via a set of 3D instructions. The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the Setup Engine, Scan Converter, Texture Pipeline, and Raster Pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rendering instructions containing 3D primitive vertex data.

### 5.4.2.1. Setup Engine

The GMCH 3D setup engine takes the input data associated with each vertex of a 3D primitive and computes the various parameters required for scan conversion. In formatting this data, the GMCH maintains sub-pixel accuracy. The per-vertex data is converted into gradients that can be used to interpolate the data at any pixel within a polygon (colors, alpha, Z or W depth, fog, and texture coordinates). The pixels covered by a polygon are identified and per-pixel texture addresses are calculated.

### 5.4.2.2. Viewport Transform and Perspective Divide

A 3D-geometry pipeline typically involves transformation of vertices from model space to clipping space followed by clip test and clipping. Lighting can be performed during the transformation or at any other point in the pipeline. After clipping, the next stage involves perspective divide followed by transformation to the viewport or screen space. The GMCH can support Viewport Transform and Perspective Divide portion of the 3D geometry pipeline in hardware.

### 5.4.2.3. 3D Primitives and Data Formats Support

The 3D primitives rendered by the GMCH are points, lines, discrete triangles, line strips, triangle strips, triangle fans, and polygons. In addition to this, the GMCH supports DirectX's\* Flexible Vertex Format\* (FVF), which enables the application to specify a variable length parameter list, obviating the need for sending unused information to the hardware. Strips, Fans, and Indexed Vertices as well as FVF improves delivered vertex rate to the setup engine significantly.



#### 5.4.2.4. Pixel Accurate Fast Scissoring and Clipping Operation

The GMCH supports clipping to a scissoring rectangle within the drawing window. The GMCH clipping and scissoring in hardware reduce the need for software to process polygons, and thus improves performance. During the setup stage, the GMCH clips polygons to the drawing window. The scissor rectangle accelerates the clipping process by allowing the driver to clip to a bigger region than the hardware renders to. The scissor rectangle is pixel accurate, and independent of line and point width. The GMCH supports a single scissor box rectangle.

#### 5.4.2.5. Backface Culling

As part of the setup, the GMCH can discard polygons from further processing, if they are either facing away from or towards the user's viewpoint. This operation, referred to as "Back Face Culling" is accomplished based on the "clockwise" or "counter-clockwise" orientation of the vertices on a primitive. This can be enabled or disabled by the driver.

#### 5.4.2.6. Scan Converter

The Scan Converter takes the vertex and edge information is used to identify all pixels that are affected by features being rendered. It works on a per-polygon basis, and one polygon may be entering the pipeline while calculations finish on another.

#### 5.4.2.7. Texture Engine

The GMCH allows an image pattern, or video to be placed on the surface of a 3D polygon. The texture engine performs texture color or chromakey matching texture filtering (an-isotropic, tri-linear, and bilinear), and YUV to RGB conversion.

As texture sizes increase beyond the bounds of graphics memory, executing textures from graphics memory becomes impractical. Every rendering pass would require copying each and every texture in a scene from System Memory to graphics memory, then using the texture, and finally overwriting the local memory copy of the texture by copying the next texture into graphics memory. The GMCH, using Intel's Direct Memory Execution model, simplifies this process by rendering each scene using the texture located in System Memory. The GMCH includes a cache controller to avoid frequent memory fetches of recently used texture data.

#### 5.4.2.8. Perspective Correct Texture Support

A textured polygon is generated by mapping a 2D texture pattern onto each pixel of the polygon. A texture map is like wallpaper pasted onto the polygon. Since polygons are rendered in perspective, it is important that texture be mapped in perspective as well. Without perspective correction, texture is distorted when an object recedes into the distance. Perspective correction involves a compute-intensive "per-pixel-divide" operation on each pixel. Perspective correction is necessary for realistic 3D graphics.

#### 5.4.2.9. Texture Decompression

As the textures' average size gets larger with higher color depth and multiple textures become the norm, it becomes increasingly important to provide support for compressed textures.

DirectX\* supports Texture Compression/Decompression to reduce the bandwidth required to deliver textures. The GMCH supports several compressed texture formats (DirectX: DXT1, DXT2, DXT3, DXT4, DXT5) and OpenGL FXT1 formats.

#### 5.4.2.10. Texture Chromakey

Chromakey is a method for removing a specific color or range of colors from a texture map before it is applied to an object. For “nearest” texture filter modes, removing a color simply makes those portions of the object transparent (the previous contents of the back buffer show through). For “linear” texture filtering modes, the texture filter is modified if only the non-nearest neighbor texels match the key (range).

Chromakeying can be performed for both paletted and non-paletted textures, and removes texels that fall within a specified color range. The Chromakey mode refers to testing the ARGB or YUV components to see if they fall between high and low state variable values. If the color of a texel contribution is in this range and chromakey is enabled, then this contribution is removed from the resulting pixel color.

#### 5.4.2.11. Anti-Aliasing

Aliasing is one of the artifacts that degrade image quality. In its simplest manifestation, aliasing causes the jagged staircase effects on sloped lines and polygon edges. Another artifact is the moiré patterns, which occur as a result of the fact that there is very small number of pixels available on screen to contain the data of a high-resolution texture map.

Full Scene Anti-Aliasing uses super-sampling, which means that the image is rendered internally at a higher resolution than it is displayed on screen. The GMCH can render internally at 1600x1200 and then this image is down-sampled (via a Bilinear filter) to the screen resolution of 640x480 and 800x600. Full Scene Anti-aliasing removes jaggies at the edges as well as moiré patterns. The GMCH renders the super-sampled image up to 2K x 2K pixel dimensions. The GMCH then reads it as a texture and bilinear filters it to the final resolution.

#### 5.4.2.12. Texture Map Filtering

Many texture-mapping modes are supported. Perspective correct mapping is always performed. As the map is fitted across the polygon, the map can be tiled, mirrored in either the U or V directions, or mapped up to the end of the texture and no longer placed on the object (this is known as clamp mode). The way a texture is combined with other object attributes is also definable.

The GMCH supports up to 12 Levels-of-Detail (LODs) ranging in size from 2048x2048 to 1x1 texels. (A texel is defined as a texture map element.) Included in the texture processor is a texture cache, which provides efficient MIP-mapping.

The GMCH supports 7 types of texture filtering:

Nearest (also known as Point Filtering): Texel with coordinates nearest to the desired pixel is used. (This is used if only one LOD is present.)

Linear (also known as Bilinear Filtering): A weighted average of a 2x2 area of texels surrounding the desired pixel is used. (This is used if only one LOD is present.)

Nearest MIP Nearest (also known as Point Filtering): This is used if many LODs are present. The nearest LOD is chosen and the texel with coordinates nearest to the desired pixel are used.

Linear MIP Nearest (Bilinear MIP Mapping): This is used if many LODs are present. The nearest LOD is chosen and a weighted average of a 2x2 area of texels surrounding the desired pixel is used (four texels). This is also referred to as Bilinear MIP Mapping.

Nearest MIP Linear (Point MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and within each LOD the texel with coordinates nearest to the desired pixel are selected. The Final texture value is generated by linear interpolation between the two texels selected from each of the MIP Maps.



**Linear MIP Linear (Trilinear MIP Mapping):** This is used if many LODs are present. Two appropriate LODs are selected and a weighted average of a 2x2 area of texels surrounding the desired pixel in each MIP Map is generated (four texels per MIP Map). The Final texture value is generated by linear interpolation between the two texels generated for each of the MIP Maps. Trilinear MIP Mapping is used minimize the visibility of LOD transitions across the polygon.

**Anisotropic MIP Nearest (Anisotropic Filtering):** This filter can be used when textured object pixels map back to significantly non-square regions of the texture (e.g., when the texture is scaled in one screen direction than the other screen direction).

Both DirectX and OGL (Rev.1.1) allow support for all these filtering modes.

#### **5.4.2.13. Multiple Texture Composition**

The GMCH also performs multiple texture composition. This allows the combination of two or greater MIP maps to produce a new one with new LODs and texture attributes in a single or iterated pass. The setup engine supports up to four texture map coordinates in as single pass. The GMCH allows up to two Bilinear MIP Maps or a single Trilinear MIP Map to be composited in a single pass. Greater than two Bilinear MIP Maps or more than one Trilinear MIP Map would require multiple passes. The actual blending or composition of the MIP Maps is done in the raster engine. The texture engine provides the required texels including blending information.

Flexible vertex format support allows multi-texturing because it makes it possible to pass more than one texture in the vertex structure.

#### **5.4.2.14. Cubic Environment Mapping**

Environment maps allow applications to render scenes with complex lighting and reflections while significantly decreasing CPU load. There are several methods to generate environment maps such as spherical, circular and cubic. The GMCH supports cubic reflection mapping over spherical and circular since it is the best choice to provide real-time environment mapping for complex lighting and reflections.

Cubic Mapping supports a texture map for each of the 6 cube faces. These can be generated by pointing a camera with a 90-degree field-of-view in the appropriate direction. Per-vertex vectors (normal, reflection or refraction) are interpolated across the polygon and the intersection of these vectors with the cube texture faces are calculated. Texel values are then read from the intersection point on the appropriate face and filtered accordingly.

#### **5.4.2.15. Bump Mapping**

The GMCH only supports embossed and dot product bump mapping, not environment bump mapping.

### **5.4.3. Raster Engine**

The Raster Engine is where the color data such as fogging, specular RGB, texture map blending, etc. is processed. The final color of the pixel is calculated and the RGB value combined with the corresponding components resulting from the Texture Engine. These textured pixels are modified by the specular and fog parameters. These specular highlighted, fogged, textured pixels are color blended with the existing values in the frame buffer. In parallel, stencil, alpha, and depth buffer tests are conducted which will determine whether the Frame and Depth Buffers will be updated with the new pixel values.



#### **5.4.3.1. Texture Map Blending**

Multiple Textures can be blended together in an iterative process and applied to a primitive. The GMCH allows up to four distinct or shared texture coordinates and texture maps to be specified onto the same polygon. Also, the GMCH supports a texture coordinate set to access multiple texture maps. State variables in multiple textures are bound to texture coordinates, texture map or texture blending.

#### **5.4.3.2. Combining Intrinsic and Specular Color Components**

The GMCH allows an independently specified and interpolated “specular RGB” attribute to be added to the post-texture blended pixel color. This feature provides a full RGB specular highlight to be applied to a textured surface, permitting a high quality reflective colored lighting effect not available in devices, which apply texture after the lighting components have been combined. If specular-add state variable is disabled, only the resultant colors from the map blending are used. If this state variable is enabled, the specular RGB color is added to the RGB values from the output of the map blending.

### 5.4.3.3. Color Shading Modes

The Raster Engine supports the flat and Gouraud shading modes. These shading modes are programmed by the appropriate state variables issued through the command stream.

Flat shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue), Specular (R, G, B), Fog, and Alpha to the pixel, where each vertex color has the same value. The setup engine substitutes one of the vertex's attribute values for the other two vertices attribute values thereby creating the correct flat shading terms. This condition is set up by the appropriate state variables issued prior to rendering the primitive.

Gouraud shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue), Specular (RGB), Fog, and Alpha to the pixel, where each vertex color has a different value. All the attributes can be selected independently to one of the shading mode by setting the appropriate value state variables.

### 5.4.3.4. Color Dithering

Color Dithering in the GMCH helps to hide color quantization errors for 16-bit color buffers. Color Dithering takes advantage of the human eye's propensity to "average" the colors in a small area. Input color, alpha, and fog components are converted from 8-bit components to 5-bit or 6-bit component by dithering. Dithering is performed on blended textured pixels. In 32-bit mode, dithering is not performed.

### 5.4.3.5. Vertex and Per Pixel Fogging

Fogging is used to create atmospheric effects such as low visibility conditions in flight simulator-type games. It adds another level of realism to computer-generated scenes. Fog can be used for depth cueing or hiding distant objects. With fog, distant objects can be rendered with fewer details (less polygons), thereby improving the rendering speed or frame rate. Fog is simulated by attenuating the color of an object with the fog color as a function of distance, and the greater the distance, the higher the density (lower visibility for distant objects). There are two ways to implement the fogging technique: per-vertex (linear) fogging and per-pixel (non-linear) fogging. The per-vertex method interpolates the fog value at the vertices of a polygon to determine the fog factor at each pixel within the polygon. This method provides realistic fogging as long as the polygons are small. With large polygons (such as a ground plane depicting an airport runway), the per-vertex technique results in unnatural fogging.

The GMCH supports both types of fog operations, vertex and per pixel or table fog. If fog is disabled, the incoming color intensities are passed unchanged to the destination blend unit. If fog is enabled, the incoming pixel color is blended with the fog color based on a fog coefficient on a per pixel basis using the following equation before sending to the destination blend unit.

### 5.4.3.6. Alpha Blending

Alpha Blending in the GMCH adds the material property of transparency or opacity to an object. Alpha blending combines a source pixel color and alpha component with a destination pixel color and alpha component. For example, this is so that a glass surface on top (source) of a red surface (destination) would allow much of the red base color to show through.

Blending allows the source and destination color values to be multiplied by programmable factors and then combined via a programmable blend function. The combined and independent selection of factors and blend functions for color and alpha is supported.

#### 5.4.3.7. Color Buffer Formats: (Destination Alpha)

The Raster Engine supports 8-bit, 16-bit, and 32-bit Color Buffer Formats. The 8-bit format is used to support planar YUV420 format, which is used only in Motion Compensation and Arithmetic Stretch format. The bit format of Color and Z is allowed to mix.

The GMCH can support an 8-bit destination alpha in 32-bit mode. Destination alpha is supported in 16-bit mode in 1555 or 4444 format. The Intel 852GM/852GMV GMCH does not support general 3D rendering to 8-bit surfaces. 8-bit destinations are supported for operations on planar YUV surfaces (e.g., stretch Blts) where each 8-bit color component is written in a separate pass. The GMCH also supports a mode where both U and V planar surfaces can be operated on simultaneously.

The frame buffer of the GMCH contains at least two hardware buffers - the Front Buffer (display buffer) and the Back Buffer (rendering buffer). While the back buffer may actually coincide with (or be part of) the visible display surface, a separate (screen or window-sized) back buffer is typically used to permit double-buffered drawing. That is, the image being drawn is not visible until the scene is complete and the back buffer made visible or copied to the front buffer via a 2D BLT operation. Rendering to one buffer and displaying from the other buffer removes image tearing artifacts. Additionally, more than two back buffers (e.g., triple-buffering) can be supported.

#### 5.4.3.8. Depth Buffer

The Raster Engine is able to read and write from this buffer and use the data in per fragment operations that determine resultant color and depth value of the pixel for the fragment are to be updated or not.

Typical applications for entertainment or visual simulations with exterior scenes require far/near ratios of 1000 to 10000. At 1000, 98% of the range is spent on the first 2% of the depth. This can cause hidden surface artifacts in distant objects, especially when using 16-bit depth buffers. A 24-bit Z-buffer provides 16 million Z-values as opposed to only 64 k with a 16-bit Z-buffer. With lower Z-resolution, two distant overlapping objects may be assigned the same Z-value. As a result, the rendering hardware may have a problem resolving the order of the objects, and the object in the back may appear through the object in the front.

By contrast, when w (or eye-relative z) is used, the buffer bits can be more evenly allocated between the near and far clip planes in world space. The key benefit is that the ratio of far and near is no longer an issue, and allows applications to support a maximum range of miles, yet still get reasonably accurate depth buffering within inches of the eye point. The selection of depth buffer size is relatively independent of the color buffer. A 16-bit Z/W or 24-bit Z/W buffer can be selected with a 16-bit color buffer. Z buffer is not supported in 8-bit mode.

#### 5.4.3.9. Stencil Buffer

The Raster Engine provides 8-bit stencil buffer storage in 32-bit mode and the ability to perform stencil testing. Stencil testing controls 3D drawing on a per pixel basis and conditionally eliminates a pixel on the outcome of a comparison between a stencil reference value and the value in the stencil buffer at the location of the source pixel being processed. They are typically used in multipass algorithms to achieve special effects, such as decals, outlining, shadows, and constructive solid geometry rendering.

One of three possible stencil operations is performed when stencil testing is enabled. The stencil operation specifies how the stencil buffer is modified when a fragment passes or fails the stencil test. The selection of the stencil operation to be performed is based upon the result of the stencil test and the depth test. A stencil write mask is also included that controls the writing of particular bits into the stencil buffer. It selects between the destination value and the updated value on a per-bit basis. The mask is 8-bit wide.



### 5.4.3.10. Projective Textures

The GMCH supports two simultaneous projective textures at full rate processing. These textures require three floating-point texture coordinates to be included in the FVF format. Projective textures enable special effects such as projecting spot light textures obliquely onto walls, etc.

### 5.4.4. 2D Engine

The GMCH provides an extensive set of 2D instructions and 2D HW acceleration for block transfers of data (BLTs). The BLT engine provides the ability to copy a source block of data to a destination and perform operations (e.g., ROP1, ROP2, and ROP3) on the data using a pattern, and/or another destination. The Stretch BLT engine is used to move source data to a destination that need not be the same size, with source transparency. Performing these common tasks in hardware reduces CPU load, and thus improves performance.

#### 5.4.4.1. 256-Bit Pattern Fill and BLT Engine

Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft\* Windows\*. The GMCH BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between System Memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between System Memory locations
- Data Alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between System Memory locations. Data to be transferred can consist of regions of System Memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8-bits, 16-bits, or 32-bits per pixel.

The GMCH BLT engine has the ability to expand monochrome data into a color depth of 8-bits, 16-bits, or 32-bits. BLTs can be either opaque or transparent. Opaque transfers, move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source System Memory location, the GMCH can specify which area in System Memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.

The GMCH has instructions to invoke BLT operations, permitting software to set up instruction buffers and use batch processing as described in the Instruction Processing Section. The GMCH can perform hardware clipping during BLTs.

#### 5.4.4.2. Alpha Stretch BLT

The stretch BLT function can stretch source data in the X and Y directions to a destination larger or smaller than the source. Stretch BLT functionality expands a region of System Memory into a larger or smaller region using replication and interpolation. The stretch BLT function also provides format conversion and data alignment.

## 5.4.5. Planes and Engines

The GMCH display can be functionally delineated into Planes and Engines (Pipes and Ports). A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces, which are rectangular System Memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

A pipe consists of a set of planes that will be combined and a timing generator. A port is the destination for the result of the pipe. Therefore, planes are associated with pipes and pipes are associated with ports.

### 5.4.5.1. Dual Pipe Independent Display Functionality

The display consists of two display pipes, A and B. Pipes have a set of planes that are assigned to them as sources. The analog display port may only use Pipe A or Pipe B, the DVO C port may use either Pipe A or Pipe B, and the LFP LVDS interface may only use Pipe B. This limits the resolutions available on a digital display when an analog CRT is active.

**Table 28. Dual Display Usage Model (Intel 852GM/852GMV GMCH)**

Display Pipe A	Display Pipe B
CRT	LVDS
DVO C	CRT
CRT	DVO C
DVO C	LVDS
CRT/DVO C	LVDS

## 5.4.6. Hardware Cursor Plane

The GMCH supports two hardware cursors. The cursor plane is one of the simplest display planes. With a few exceptions, has a fixed size of 64 x 64 and a fixed Z-order (top). In legacy modes, cursor can cause the display data below it to be inverted. In the alpha blend mode, true color cursor data can be alpha blended into the display stream. It can be assigned to either display pipe A or display pipe B and dynamically flipped from one to the other when both are running.

### 5.4.6.1. Cursor Color Formats

Color data can be in an indexed format or a true color format. Indexed data uses the entries in the four-entry cursor palette to convert the two-bit index to a true color format before being passed to the blenders. The index can optionally specify that a cursor pixel be transparent or cause an inversion of the pixel value below it or one of two colors from the cursor palette. Blending of YUV or RGB data is only supported with planes that have data of the same format.

### 5.4.6.2. Popup Plane (Second Cursor)

The popup plane is used for control functions in mobile applications. Only the hardware cursor has a higher Z-order precedence over the hardware icon. In standard modes (non-VGA) either cursor A or cursor B can be used as a Popup Icon. For VGA modes, 32-bpp data format is not supported.

### 5.4.6.3. **Popup Color Formats**

Source color data for the popup is in an indexed format. Indexed data uses the entries in the four-entry cursor palette to convert the two-bit index to a true color format before being passed to the blenders. Blending of color data is only supported with data of the same format.

### 5.4.7. **Overlay Plane**

The overlay engine provides a method of merging either video capture data (from an external Video Capture device) or data delivered by the CPU, with the graphics data on the screen.

#### 5.4.7.1. **Multiple Overlays (Display C)**

A single overlay plane and scalar is implemented. This overlay plane can be connected to the primary display, secondary display or in bypass mode. In the default mode, it appears on the primary display. The overlay may be displayed in a multi-monitor scenario for single-pipe simultaneous displays only. Picture-in-Picture feature is supported via software through the arithmetic stretch blitter.

#### 5.4.7.2. **Source/Destination Color/Chroma-keying**

Overlay source/destination chroma-keying enables blending of the overlay with the underlying graphics background. Destination color-/chroma-keying can be used to handle occluded portions of the overlay window on a pixel-by-pixel basis that is actually an underlay. Destination color keying supports a specific color (8-bit or 15-bit) mode as well as 32-bit alpha blending.

Source color/chroma-keying is used to handle transparency based on the overlay window on a pixel-by-pixel basis. This is used when “blue screening” an image to overlay the image on a new background later.

#### 5.4.7.3. **Gamma Correction**

To compensate for overlay color intensity loss, the overlay engine supports independent gamma correction. This allows the overlay data to be converted to linear data or corrected for the display device when not blending.

#### 5.4.7.4. **YUV to RGB Conversion**

The format conversion can be bypassed in the case of RGB source data.

#### 5.4.7.5. **Color Control**

Color control provides a method of changing the color characteristics of the pixel data. It is applied to the data while in YUV format and uses input parameters such as brightness, saturation, hue (tint) and contrast. This feature is supplied for the overlay only and works in YUV formats only.

#### 5.4.7.6. **Dynamic Bob and Weave**

Interlaced data that originates from a video camera creates two fields that are temporally offset by 1/60 of a second. There are several schemes to de-interlace the video stream: line replication, vertical filtering, field merging, and vertical temporal filtering. Field merging takes lines from the previous field and inserts them into the current field to construct the frame – this is known as Weaving. This is the best solution for images with little motion; however, showing a frame that consists of the two fields will have

serration or feathering of moving edges when there is motion in the scene. Vertical filtering or “Bob” interpolates adjacent lines rather replicating the nearest neighbor. This is the best solution for images with motion however, it will have reduced spatial resolution in areas that have no motion and introduce jaggies. In absence of any other de-interlacing, these form the baseline and are supported by the GMCH.

## 5.4.8. Video Functionality

The GMCH supports MPEG-2 decoding hardware, sub-picture support and DTV all format decode.

### 5.4.8.1. MPEG-2 Decoding

The GMCH MPEG2 Decoding supports Hardware Motion Compensation (HWMC). The GMCH can accelerate video decoding for the following video coding standards:

- MPEG-2 support

- MPEG-1: Full feature support

- H.263 support

- MPEG-4: Only supports some features in the simple profile.

The GMCH HWMC interface is optimized for Microsoft's\* VA API. Hardware Video Acceleration API (HVA) is a generic DirectDraw and DirectShow interface supported in Windows 2000 and Windows 98 Millennium to provide video decoding acceleration. Direct VA is the open standard implementation of HVA, which is natively supported by the GMCH hardware.

### 5.4.8.2. Hardware Motion Compensation

The Hardware Motion Compensation (HWMC) process consists of reconstructing a new picture by predicting (either forward, backward, or bi-directional) the resulting pixel colors from one or more reference pictures. The GMCH receives the video stream and implements Motion Compensation and subsequent steps in hardware. Performing Motion Compensation in hardware reduces the processor demand of software-based MPEG-2 decoding, and thus improves system performance.

### 5.4.8.3. Sub-picture Support

Sub-picture is used for two purposes: Subtitles for movie captions, which are superimposed on a main picture, and for Menus to provide some visual operation environments for the user.

DVD allows movie subtitles to be recorded as Sub-pictures. On a DVD disc, it is called “Subtitle” because it has been prepared for storing captions. Since the disc can have a maximum of 32 tracks for Subtitles, they can be used for various applications, for example, as Subtitles in different languages.

There are two kinds of Menus, the System Menus and other In-Title Menus. First, the System Menus are displayed and operated at startup of or during the playback of the disc or from the stop state. Second, In-Title menus can be programmed as a combination of Sub-picture and Highlight commands to be displayed during playback of the disc.

The GMCH supports sub-picture for DVD and DBS by mixing the two video streams via alpha blending. Unlike color keying, alpha blending provides a softer effect and each pixel that is displayed is a composite between the two video stream pixels. The GMCH can utilize four methods when dealing with sub-pictures. This flexibility means that the GMCH can work with all sub-picture formats.



## 5.5. Display Interface

The GMCH has three dedicated display ports: the analog port, the LFP LVDS interface, and Digital display port, DVOC. DVOC can support TV-out encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device. The data that is sent out the display ports are selected from one of the two possible sources, display pipe A or display pipe B, except for the LVDS port which can only be driven on Pipe B.

The GMCH's digital display port is capable of driving a 165-MHz pixel clock on a single DVO port.

### 5.5.1. Analog Display Port Characteristics

The analog display port provides an RGB signal output along with an HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector.

#### 5.5.1.1. Integrated RAMDAC

The display function contains a 350-MHz integrated 24-bit RAM-based Digital-to-Analog Converter (RAMDAC) that transforms up to 1600X1200 digital pixels (Intel 852GM/852GMV GMCH) at a maximum refresh rate of 85 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.

#### 5.5.1.2. DDC (Display Data Channel)

DDC is defined by VESA. It allows communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 1 and 2 is implemented.

## 5.5.2. Digital Display Interface

### 5.5.2.1. Dedicated LVDS Interface

The GMCH has a dedicated ANSI/TIA/EIA –644-1995 Specification compliant dual channel LFP LVDS interface that can support TFT panel resolutions up to SXGA+ with a maximum pixel format of 18 bpp (with SSC supported frequency range from 25-MHz to 112-MHz (single channel/dual channel).

The display pipe selected by the LVDS display port is programmed with the panel timing parameters that are determined by installed panel specifications or read from an onboard EDID ROM. The programmed timing values are then “locked” into the registers to prevent unwanted corruption of the values. From that point on, the display modes are changed by selecting a different source size for that pipe, programming the VGA registers, or selecting a source size and enabling the VGA. The timing signals will remain stable and active through mode changes. These mode changes include VGA to VGA, VGA to HiRes, HiRes to VGA, and HiRes to HiRes.

The transmitter can operate in a variety of modes and supports several data formats. The serializer supports 6-bit or 8-bit color and single or dual channel operating modes. The display stream from the display pipe is sent to the LVDS transmitter port at the dot clock frequency, which is determined by the panel timing requirements. The output of LVDS is running at a fixed multiple of the dot clock frequency, which is determined by the mode of operation; single or dual channel.

Depending on configuration and mode, a single channel can take 18-bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) and output them on three differential data pair outputs; or 24 bits of RGB plus 3 bits of timing control output on four differential data pair outputs. A dual channel interface converts 36 bits or 48 bits of color information plus the 3 bits of timing control and outputs it on six or eight sets of differential data outputs.

This display port is normally used in conjunction with the pipe functions of panel scaling and a 6-bit to 8-bit dither. This display port is also used in conjunction with the panel power sequencing and additional associated functions.

When enabled, the LVDS constant current drivers consume significant power. Individual pairs or sets of pairs can be selected to be powered down when not used. When disabled, individual or sets of pairs will enter a low power state. When the port is disabled all pairs enters a low power mode. The panel power sequencing can be set to override the selected power state of the drivers during power sequencing. For more details on using the GMCH's LFP LVDS interface for TFT Panel support, please refer to the *Common Panel Interface Specification, Rev 1.5* for details on:

- CPIS Supported Resolutions
- CPIS DC/AC Specifications
- CPIS Pin Lists and Connectors
- CPIS EDID Table Outline
- CPIS Reference EDID Formats (XGA at 60-Hz Refresh Rate)
- Sample CPIS EDID DTD's (Primary Resolution at 60-Hz Refresh Rate)
- Video Serialization Formats
- References and External Standards

### 5.5.2.2. LVDS Interface Signals

LVDS for flat panel is compatible with the ANSI/TIA/EIA-644 specification. This is an electrical standard only defining driver output characteristics and receiver input characteristics. There are two LVDS transmitter channels (channel A and channel B) in the LVDS interface. Each channel consists of four data pairs and a clock pair. The interface consists of a total of ten differential signal pairs of which eight are data and two are clocks. The phase locked transmit clock is transmitted in parallel with the data being sent out over the data pairs and over the LVDS clock pair.

Each channel supports transmit clock frequency ranges from 25-MHz to 112-MHz, which provides a throughput of up to 784-Mbps on each data output and up to 112-MP/s on the input. When using both channels, they each operate at the same frequency each carrying a portion of the data. The maximum pixel rate is increased to 224-MP/s but may be limited to less than that due to restrictions elsewhere in the circuit.

The LVDS Port Enable bit enables or disables the entire LVDS interface. When the port is disabled, it will be in a low power state. Once the port is enabled, individual driver pairs will be disabled based on the operating mode. Disabled drivers can be powered down for reduced power consumption or optionally fixed to forced 0's output.

### 5.5.2.3. LVDS Pair States

The LVDS pairs can be put into one of the following five states: powered down tri-state, powered down Zero Volts, common mode, send zeros, or active. When in the active state, several data formats are supported. When in powered down state, the circuit enters a low power state and drives out 0 V or tri-states on both the output pins for the entire channel. The common mode tri-state is both pins of the pair



set to the common mode voltage. When in the send zeros state, the circuit is powered up but sends only zero for the pixel color data regardless what the actual data is with the clock lines and timing signals sending the normal clock and timing data.

#### 5.5.2.4. Single Channel versus Dual Channel Mode

Both single channel and dual channel modes are available to allow interfacing to either single or dual channel panel interfaces. This LVDS port can operate in single channel or dual channel mode. Dual channel mode uses twice the number of LVDS pairs and transfers the pixel data at twice the rate of the single channel. In general, one channel will be used for even pixels and the other for odd pixel data. The first pixel of the line is determined by the display enable going active and that pixel will be sent out channel A. All horizontal timings for active, sync, and blank will be limited to be on two pixel boundaries in the two channel modes.

#### 5.5.2.5. LVDS Channel Skew

When in dual channel mode, the two channels must meet the panel requirements with respect to the inter channel skew.

#### 5.5.2.6. LVDS PLL

The Display PLL is used to synthesize the clocks that control transmission of the data across the LVDS interface. The three operations that are controlled are the pixel rate, the load rate, and the IO shift rate. These are synchronized to each other and have specific ratios based on single channel or dual channel mode. If the pixel clock is considered the 1x rate, a 7x or 3.5x speed IO\_shift clock needed for the high-speed, serial outputs setting the data rate of the transmitters. The load clock will have either a 1x or .5x ratio to the pixel clock.

#### 5.5.2.7. SSC Support

The GMCH is designed to tolerate 0.5%, 1.0%, and 2.5% down/center spread at a modulation rate from 30-50kHz triangle. An external SSC clock synthesizer can be used to provide the 48/66-MHz reference clock into the GMCH Pipe B PLL.

#### 5.5.2.8. Panel Power Sequencing

This section provides details for the power sequence timing relationship of the panel power, the backlight enable and the LVDS data timing delivery. In order to meet the panel power timing specification requirements, two signals, PANELVDDEN and PANELBKLTEN are provided to control the timing sequencing function of the panel and the backlight power supplies.

##### 5.5.2.8.1. Panel Power Sequence States

A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state and the LVDS clock and data lines are all managed by an internal power sequencer.

A requested power-up sequence is only allowed to begin after the power cycle delay time requirement T4 is met.

Figure 7. Panel Power Sequencing

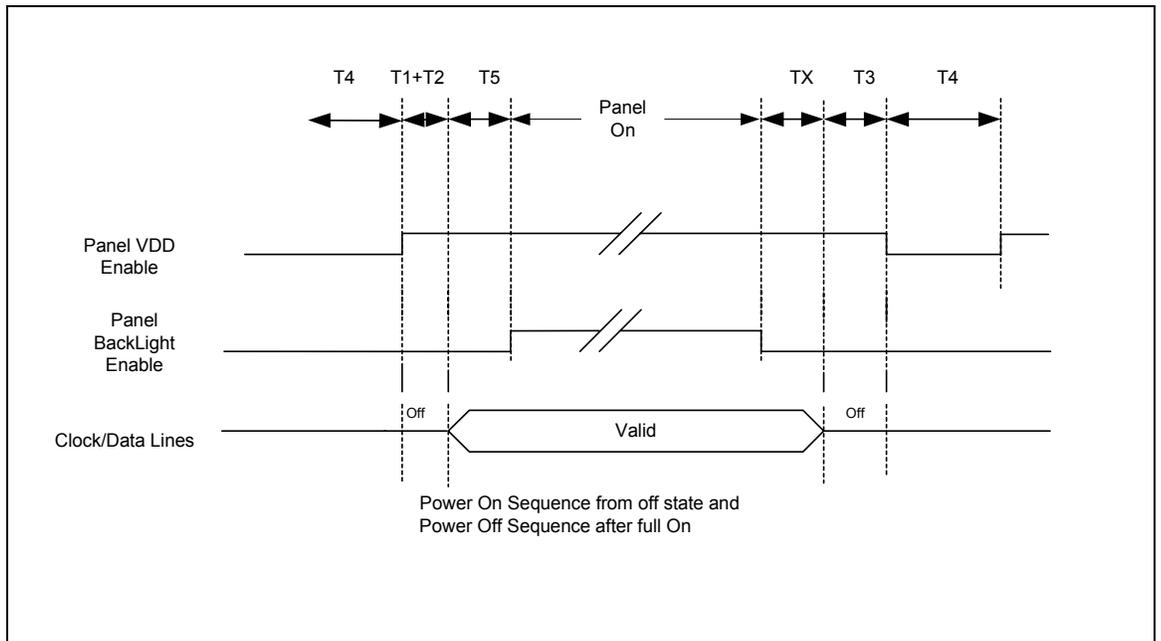


Table 29. Panel Power Sequencing Timing Parameters

Name	Panel Power Sequence Timing Parameters		
	Spec Name	From	To
T1+T2	<b>Vdd On to LVDS Active</b> Panel Vdd must be on for a minimum time before the LVDS data stream is enabled.	.1 Vdd	LVDS Active
T5	<b>Backlight</b> LVDS data must be enabled for a minimum time before the backlight is turned on.	LVDS Active	Backlight on
TX	<b>Backlight State</b> Backlight must be disabled for a minimum time before the LVDS data stream is stopped.	Backlight Off	LVDS off
T3	<b>LVDS State</b> Data must be off for a minimum time before the panel VDD is turned off.	LVDS Off	Start power off
T4	<b>Power cycle Delay</b> When panel VDD is turned from On to Off, a minimum wait must be satisfied before the panel VDD is enabled again.	Power Off	Power On Sequence Start

### 5.5.2.9. Back Light Inverter Control

The GMCH offers integrated PWM for TFT panel Backlight Inverter control. Other methods of control are specified in the *Common Panel Interface Specification*, Version 1.5.

PWM – based Backlight Brightness Control

SMBus-based Backlight Brightness Control

DBL (Display Brightness Link) –to- VDL (Video Data Link) Power Sequencing

### 5.5.2.10. Digital Video Output Port

The GMCH has the capability to support additional digital display devices (e.g. TMDS transmitter, LVDS transmitter or TV-out encoder) through its digital video output port. DVOC can deliver a 165-MHz dot clock on its 12-bit interface.

The digital display port consists of a digital data bus, VSYNC, HSYNC, and BLANK# signals. The data bus can operate only in a 12-bit mode. Embedded sync information or HSYNC and VSYNC signals can optionally provide the basic timing information to the external device and the BLANK# signal indicates which clock cycles contain valid data. The BLANK# signal can be optionally selected to include the border area of the timing. The VSYNC and HSYNC signals can be disabled when embedded sync information is to be used or to support DPMS. Optionally a STALL signal can cause the next line of data to not be sent until the STALL signal is removed. Optionally the FIELD pin can indicate to the overlay which field is currently being displayed at the display device.

## 6. *Power and Thermal Management*

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The Intel 852GM/852GMV GMCH platform is intended to be compliant with the following specifications and technologies:

APM Rev 1.2

PCI Power Management Rev 1.0

PC'99, Rev 1.0, PC'99A, and PC'01, Rev 1.0

ACPI 1.0b and 2.0 support

ACPI S0, S1-M, S3, S4, S5, C0, C1, C2, C3 states

Internal Graphics Adapter D0, D1, D3 (Hot/Cold)

Enhanced Intel SpeedStep® Technology

On Die Thermal Sensor, enabling core and System Memory write thermal throttling for prevention of catastrophic thermal conditions

External Thermal Sensor Input pin

Enabling SO-DIMM thermal throttling

C4 compatible (C4 = Deeper sleep) is same as C3 from the GMCH perspective, but from platform perspective, CPU voltage is reduced during C3 and S1-M entry to minimum to maintain state)

The GMCH also reduces I/O power dynamically, by disabling sense amps on input buffers, as well as tristating output buffers when possible



## 6.1. General Description of Supported CPU States

**C0 (Full On):** This is the only state that runs software. All clocks are running, STPCLK is deasserted, and the processor core is active. The processor can service snoops and maintain cache coherency in this state.

**C1 (Auto Halt):** The first level of power reduction occurs when the processor executes an Auto-Halt instruction. This stops the execution of the instruction stream and reduces the processor's power consumption. The processor can service snoops and maintain cache coherency in this state.

**C2 (Stop Grant):** To enter this low power state, STPCLK is asserted. The processor can still service snoops and maintain cache coherency in this state.

**C3 (Sleep or Deep Sleep):** In these states the processor clock is stopped. The GMCH assumes that no Hub Interface cycles (except special cycles) will occur while the GMCH is in this state. The processor cannot snoop its caches to maintain coherency while in the C3 state. The GMCH will transition from the C0 state to the C3 state when software reads the Level 3 Register. This is an ACPI defined register but BIOS or APM (via BIOS) can use this facility when entering a low power state. The Host Clock PLL within the GMCH can be programmed to be shut off for increased power savings and the GMCH uses the DPSLP signal input for this purpose.

**C4 (Deeper Sleep):** The C4 state appears to the GMCH as identical to the C3 state, but in this state the processor core voltage is lowered. There are no internal events in GMCH for the C4 state that differ from the C3 state (this state is not supported for Intel Celeron M processor and mobile Intel Celeron processor).

## 6.2. General Description of ACPI States

Internal Graphics Adapter:

D0 Full on, display active

D1 Low power state, low latency recovery. No display, System Memory retained

D3 Hot - All state lost other than PCI config. System Memory lost (optionally)

D3 Cold - Power off

CPU:

C0 Full On

C1 Auto Halt

C2 DesktopStop Clock. Clk to CPU still running. Clock stopped to CPU core.

C3 Deep Sleep. Clock to CPU stopped.

C4 Deeper Sleep. Same as C3 with reduced voltage on the CPU.

System States

- G0/S0 Full On

- G1/S1-M Power On Suspend (POS). System Context Preserved

- G1/S2 Not supported.

- G1/S3 Suspend to RAM (STR). Power and context lost to chipset.

- G1/S4 Suspend to Disk (STD). All power lost (except wakeup on ICH4-M)

- G2/S5 Hard off. Total reboot.

### 6.3. Enhanced Intel SpeedStep Technology Overview

With Enhanced Intel SpeedStep Technology the processor core voltage changes and allows true CPU core frequency changes versus only clock throttling.

*Note:* Enhanced Intel Speed Step technology is not supported for Intel Celeron M processor, mobile Intel Celeron processor and Intel Celeron D processor on 90 nm process and in the 478-pin package.

**Table 30. Enhanced Intel SpeedStep Technology Overview**

<b>CPU</b>	Mobile Intel Pentium 4 Processor-M
<b>Benefit Over Non-power Managed CPU</b>	Additional lower voltages and frequencies
<b>Transition Prompt</b>	OS based on CPU load demand, thermal control, or user event based
<b>CPU Availability</b>	CPU unavailability can be restricted to ~250 $\mu$ s (CPU dependent) by s/w

### 6.4. Internal Thermal Sensor

This section describes the new on-die thermal sensor capability. The thermal sensor functions are provided below:

**Catastrophic Trip Point:** This trip point is programmed through the BIOS during initialization. This trip point is set at the temperature at which the GMCH should be shut down immediately with minimal software support. The settings for this are lockable.

**High Temperature Trip Point:** This trip point is nominally 14°C below the Catastrophic Trip Point. The BIOS can be programmed to provide an interrupt when it is crossed in either direction. Upon the trip event, hardware throttling may be enabled when the temperature is exceeded.

#### 6.4.1. Hardware Throttling

The Hot trip points' crossings events may be used to trigger throttling without intervention by software.

System Memory write throttling may be enabled on Hot trip points. The HTC register selects whether it is Catastrophic or both that enable throttling. System Memory write throttling registers in Device #0 configuration space determine whether throttling is enabled at all.

#### 6.4.2. Register Locking

TCO contains a lock bit that locks the catastrophic programming interface, including TCO, TCTS, and two bits in TSCR that could disable the sensor or alter the trip point. HTC has a lock bit for the hardware throttling settings.



### 6.4.3. Hysteresis Operation

Hysteresis provides a small amount of positive feedback to the thermal sensor circuit to prevent a trip point from flipping back and forth rapidly when the temperature is right at the trip point.

## 6.5. External Thermal Sensor Input

An external thermal sensor with a serial interface may be placed next to DDR SDRAM SO-DIMM (or any other appropriate platform location), or a remote Thermal Diode may be placed next to the SO-DIMM (or any other appropriate platform location) and connected to the external Thermal sensor. Intel advises that the external Thermal sensor contains some form of hysteresis, since none is provided by the GMCH hardware.

The external sensor can be connected to the ICH4-M via the SMBus Interface to allow programming and setup by BIOS software over the serial interface. The external sensor's output should include an Active-Low Open-Drain signal indicating an Over-Temp condition, which remains asserted for as long as the Over-Temp Condition exists, and deasserts when temperature has returned to within normal operating range. This external sensor output will be connected to the GMCH input (EXTTS\_0) and will trigger a preset interrupt and/or read-throttle on a level-sensitive basis.

Additional external thermal sensor's outputs, for multiple sensors, can be wire-ORed together allow signaling from multiple sensors located physically separately. Software can, if necessary, distinguish which SO-DIMM(s) is the source of the over-temp through the serial interface. However, since the SO-DIMM(s) will be located on the same System Memory Bus Data lines, any GMCH-based Read Throttle will apply equally.

**Note:** The use of external sensors that include an internal pull-up resistor on the open-drain thermal trip output is discouraged. However, it may be possible depending on the size of the pull-up and the voltage of the sensor. Please refer to the platform design guide for more information.

### 6.5.1. Usage

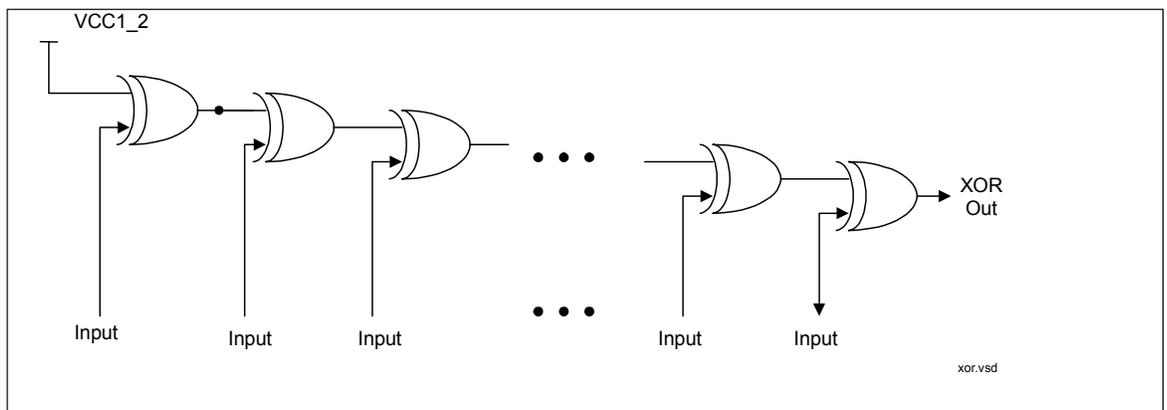
External Sensor(s) Used for Dynamic Temperature Feedback Control in production releases:

Sensor on SO-DIMMs, which can be used to dynamically control read throttling.

## 7. Testability

In the Intel 852GM/852GMV GMCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates, each with one input pin connected to it. The XOR Chain test mode is used by product engineers during manufacturing and OEMs during board level connectivity tests. The main purpose of this test mode is to detect connectivity shorts between adjacent pins and to check proper bonding between I/O pads and I/O pins.

**Figure 8. XOR-Tree Chain**



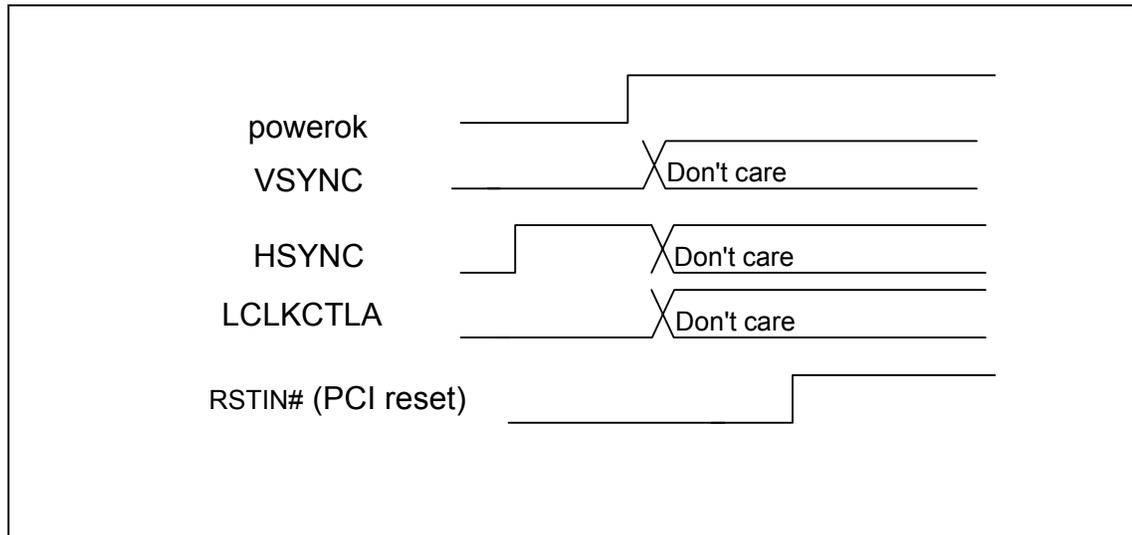
The algorithm used for in-circuit test is as follows:

1. Drive all input pins to an initial logic level 1. Observe the output corresponding to scan chain being tested.
2. Toggle pins one at a time starting from the first pin in the chain, continuing to the last pin, from its initial logic level to the opposite logic level. Observe the output changes with each pin toggle.

### 7.1. XOR Test Mode Entry

Please refer to XOR Chain Test Mode Entry Events Diagram in Figure 9.

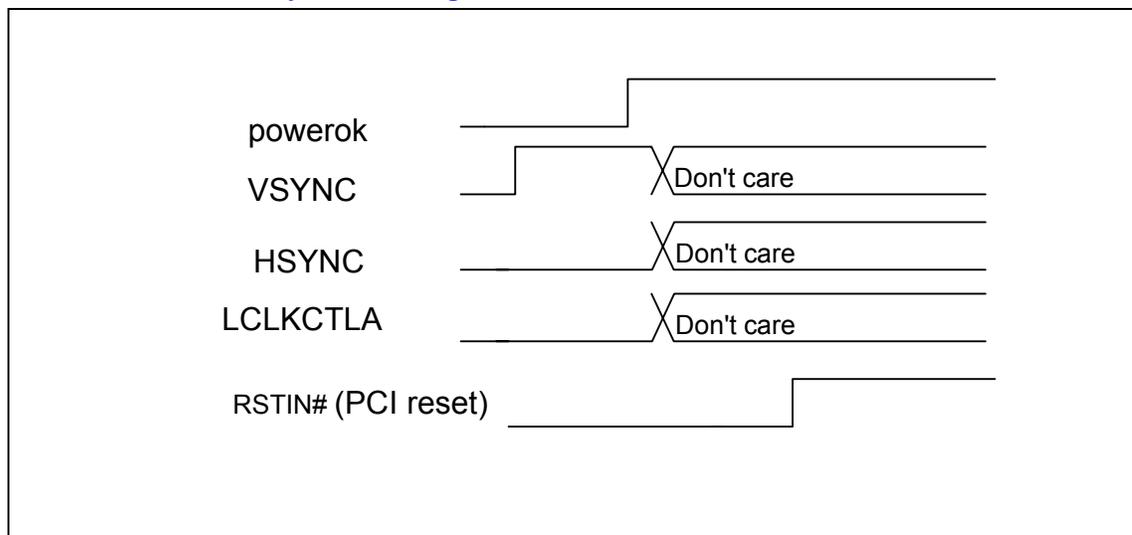
**Figure 9. XOR Chain Test Mode Entry Events Diagram**



**Note:** HSYNC and LCLKCTLA = XOR Chain Test Mode Activation; No clock is required for XOR Chain Test Mode. A minimum of 50 ns PWROK assertion prior to RSTIN# assertion is recommended. A minimum of 10 ns VSYNC/HSYNC/LCLKCTLA assertion prior to PWROK assertion is recommended.

Please refer to ALLZ Test Mode Entry Events Diagram in Figure 10.

**Figure 10. ALLZ Test Mode Entry Events Diagram**



**NOTE:** VSYNC and LCLKCTLA = ALL Z Test Mode Activation; No clock is required for ALLZ Test Mode Activation. A minimum of 50 ns PWROK assertion prior to RSTIN# assertion is recommended. A minimum of 10 ns VSYNC/HSYNC/LCLKCTLA assertion prior to PWROK assertion is recommended.

## 7.2. XOR Chain Differential Pairs

Table 31 provides differential signals in the XOR chains that must be treated as pairs. Pin1 and Pin2 as shown below need to drive to the opposite value always.

**Table 31. Differential Signals in the XOR Chains**

Pin1	Pin2	XOR Chain
DVOCCLK#	DVOCCLK	DVO XOR 2
HLSTB#	HLSTB	HUB XOR

## 7.3. XOR Chain Exclusion List

See Table 32 for a list of pins that are not included in the XOR chains (excluding all VCC/VSS/VTT).

**Note:** Connectivity column is used to identify what need to be driven on that particular pin during XOR chain test mode.

**Table 32. XOR Chain Exclusion List of Pins**

Item#	IN/OUT	Ball	Pin/VHDL	I/O Type	Voltage	Connectivity
1	IN	Y3	GCLKIN	PLL CLK	3.3	0
2	-	W1	HLVREF	Analog	1/3 VCCHL	0.4
3	-	T2	HLRCOMP	Analog	N/A	N/A
4	-	U2	PSWING	Analog	N/A	N/A
5	-	F1	GVREF	Analog	1/2 VCCDVO	0.75
6	-	D1	DVORCOMP	Analog	N/A	N/A
7	IN	J11	PWROK	CMOS	3.3	N/A
8	IN	B7	DREFCLK	PLL CLK	3.3	0
9	-	E8	REFSET	Analog	N/A	N/A
10	-	C9	BLUE	Analog	N/A	N/A
11	-	D9	BLUE#	Analog	N/A	N/A
12	-	C8	GREEN	Analog	N/A	N/A
13	-	D8	GREEN#	Analog	N/A	N/A
14	-	A7	RED	Analog	N/A	N/A
15	-	A8	RED#	Analog	N/A	N/A
16	-	D12	LVREFH	Analog	1.1	1.1
17	-	A10	LIBG	Analog	N/A	N/A
18	-	B12	LVBG	Analog	N/A	N/A
19	-	F12	LVREFL	Analog	1.1	1.1
20	IN	B17	DREFSSCLK	PLL CLK	3.3	0
21	-	J17	HDVREF[2]	Analog	2/3 VTTLF	1.0



Item#	IN/OUT	Ball	Pin/VHDL	I/O Type	Voltage	Connectivity
22	-	B20	HXRCOMP	Analog	N/A	N/A
23	-	B18	HXSWING	Analog	N/A	N/A
24	-	J21	HDVREF[1]	Analog	2/3 VTTLF	1.0
25	IN	AD29	BCLK#	Diff	0.7	0
26	IN	AE29	BCLK	Diff	0.7	0.7
27	-	K21	HDVREF[0]	Analog	2/3 VTTLF	1.0
28	-	Y28	HCCVREF	Analog	2/3 VTTLF	1.0
29	-	Y22	HAVREF	Analog	2/3 VTTLF	1.0
30	-	H28	HYRCOMP	Analog	N/A	N/A
31	-	K28	HYSWING	Analog	N/A	N/A
32	IN	D28	RSTIN#	CMOS	3.3	N/A
33	-	AJ24	SMVREF_0	Analog	1/2 VCCSM	1.25
34	-	AB1	SMRCOMP	Analog	N/A	N/A

## 7.4. XOR Chain Connectivity/Ordering

The following tables contain the ordering for all of the Intel 852GM/852GMV GMCH XOR chains and pin to ball mapping information:

Table 33. XOR Mapping

XOR Chain DVO 1					
XOR Out	DVO IN/OUT	Ball	Pin/VHDL	I/O Type	Voltage
		OUT	AB5	SMA[12]	SSTL_2
1	INOUT	T6	RSVD	DVO	1.5
2	INOUT	T5	RSVD	DVO	1.5
3	INOUT	T7	MDDCDATA	DVO	1.5
4	INOUT	R3	RSVD	DVO	1.5
5	INOUT	R4	RSVD	DVO	1.5
6	INOUT	R6	RSVD	DVO	1.5
7	INOUT	R5	RSVD	DVO	1.5
8	INOUT	P2	RSVD	DVO	1.5
9	INOUT	P4	RSVD	DVO	1.5
10	INOUT	P3	RSVD	DVO	1.5
11	INOUT	P6	RSVD	N/A	N/A
12	INOUT	P5	RSVD	N/A	N/A
13	INOUT	N2	RSVD	N/A	N/A
14	INOUT	N3	RSVD	N/A	N/A
15	INOUT	M1	RSVD	N/A	N/A
16	INOUT	N5	RSVD	N/A	N/A
17	INOUT	M2	RSVD	N/A	N/A
18	INOUT	M5	RSVD	N/A	N/A
19	INOUT	M3	DVOBCCLKINT	DVO	1.5
20	INOUT	L2	RSVD	N/A	N/A
21	INOUT	P7	MDDCCLK	DVO	1.5
22	INOUT	N6	MI2CDATA	DVO	1.5
23	INOUT	M6	MDVIDATA	DVO	1.5
24	INOUT	N7	MDVICLK	DVO	1.5
25	INOUT	L7	DVODETECT	DVO	1.5
26	INOUT	K7	MI2CCLK	DVO	1.5
27	OUT	B2	RSVD	N/A	N/A
28	IN	B3	RSVD	N/A	N/A
XOR Chain DVO 2					
XOR Out	DVO IN/OUT	Ball	Pin/VHDL	I/O Type	Voltage
	OUT	AD5	SMA[11]	SSTL_2	2.5
1	INOUT	L3	DVOCBLANK#	DVO	1.5



2	INOUT	K1	DVOCDC[1]	DVO	1.5
3	INOUT	L4	RSVD	DVO	N/A
4	INOUT	L5	DVOCVSYNC	DVO	1.5
5	INOUT	K2	DVOCDC[3]	DVO	1.5
6	INOUT	K5	DVOCDC[0]	DVO	1.5
7	INOUT	K3	DVOCDC[2]	DVO	1.5
8	INOUT	J2	DVOCCLK#	DVO	1.5
9	INOUT	J3	DVOCCLK	DVO	1.5
10	INOUT	H2	DVOCDC[6]	DVO	1.5
11	INOUT	J5	DVOCDC[5]	DVO	1.5
12	INOUT	H1	DVOCDC[7]	DVO	1.5
13	INOUT	J6	DVOCDC[4]	DVO	1.5
14	INOUT	K6	DVOCCHSYNC	DVO	1.5
15	INOUT	H4	DVOCDC[9]	DVO	1.5
16	INOUT	H3	DVOCDC[8]	DVO	1.5
17	INOUT	H5	DVOCFLDSTL	DVO	1.5
18	INOUT	H6	DVOCDC[10]	DVO	1.5
19	INOUT	G2	DVOCBCINT#	DVO	1.5
20	INOUT	G3	DVOCDC[11]	DVO	1.5
21	IN	D2	RSVD	N/A	N/A
22	IN	D3	RSVD	N/A	N/A
23	IN	F4	ADDID[5]	DVO	1.5
24	IN	F5	ADDID[1]	DVO	1.5
25	IN	F6	ADDID[7]	DVO	1.5
26	IN	E2	ADDID[3]	DVO	1.5
27	IN	E5	ADDID[0]	DVO	1.5
28	IN	F3	RSVD	N/A	N/A
29	IN	F2	RSVD	N/A	N/A
30	OUT	C2	RSVD	N/A	N/A
31	IN	E3	ADDID[2]	DVO	1.5
32	OUT	C3	GST[1]	DVO	1.5
33	OUT	C4	GST[0]	DVO	1.5
34	IN	G5	ADDID[4]	DVO	1.5
35	IN	G6	ADDID[6]	DVO	1.5
36	IN	D5	DPMS	DVO	1.5

XOR Chain FSB 1					
XOR Out	IN/OUT	Ball	Pin	I/O Type	Voltage
		OUT	AC19	SMA[10]	SSTL_2
1	INOUT	D16	HD[62]#	GTL+	1.5
2	INOUT	C16	HD[60]#	GTL+	1.5
3	INOUT	G16	HD[58]#	GTL+	1.5
4	INOUT	C17	HD[55]#	GTL+	1.5
5	INOUT	E17	HD[61]#	GTL+	1.5
6	INOUT	E16	HD[59]#	GTL+	1.5
7	INOUT	F17	HD[56]#	GTL+	1.5
8	INOUT	B19	HD[57]#	GTL+	1.5
9	INOUT	E18	HDSTBP[3]#	GTL+	1.5
10	INOUT	D18	HDSTBN[3]#	GTL+	1.5
11	INOUT	C18	HD[63]#	GTL+	1.5
12	INOUT	G17	HD[51]#	GTL+	1.5
13	INOUT	C19	HD[54]#	GTL+	1.5
14	INOUT	D20	HD[52]#	GTL+	1.5
15	INOUT	E20	HD[50]#	GTL+	1.5
16	INOUT	E19	HD[49]#	GTL+	1.5
17	INOUT	G19	DINV[3]#	GTL+	1.5
18	INOUT	F19	HD[53]#	GTL+	1.5
19	INOUT	G18	HD[48]#	GTL+	1.5
20	INOUT	B21	HD[32]#	GTL+	1.5
21	INOUT	C20	HD[46]#	GTL+	1.5
22	INOUT	C23	HD[35]#	GTL+	1.5
23	INOUT	B23	HD[43]#	GTL+	1.5
24	INOUT	B22	HD[42]#	GTL+	1.5
25	INOUT	B25	DINV[2]#	GTL+	1.5
26	INOUT	D22	HD[36]#	GTL+	1.5
27	INOUT	C24	HD[34]#	GTL+	1.5
28	INOUT	C21	HD[47]#	GTL+	1.5
29	INOUT	E21	HDSTBP[2]#	GTL+	1.5
30	INOUT	E22	HDSTBN[2]#	GTL+	1.5
31	INOUT	D24	HD[39]#	GTL+	1.5
32	INOUT	C25	HD[37]#	GTL+	1.5
33	INOUT	F21	HD[45]#	GTL+	1.5
34	INOUT	E24	HD[38]#	GTL+	1.5

35	INOUT	E23	HD[41]#	GTL+	1.5
36	INOUT	G21	HD[33]#	GTL+	1.5
37	INOUT	F23	HD[44]#	GTL+	1.5
38	INOUT	G20	HD[40]#	GTL+	1.5
39	OUT	M27	RS[2]#	GTL+	1.5
40	OUT	P28	BPRI#	GTL+	1.5
41	OUT	AA22	DPWR#	GTL+	1.5
42	INOUT	AA26	HADSTB[1]#	GTL+	1.5
<b>XOR Chain FSB 2</b>					
XOR Out	IN/OUT	Ball	Pin	I/O Type	Voltage
	OUT	AC5	SMA[9]	SSTL_2	2.5
1	INOUT	E25	DINV[1]#	GTL+	1.5
2	INOUT	B26	HD[26]#	GTL+	1.5
3	INOUT	C26	HD[28]#	GTL+	1.5
4	INOUT	B27	HD[18]#	GTL+	1.5
5	INOUT	B28	HD[31]#	GTL+	1.5
6	INOUT	G23	HD[30]#	GTL+	1.5
7	INOUT	E26	HD[9]#	GTL+	1.5
8	INOUT	D26	HDSTBP[1]#	GTL+	1.5
9	INOUT	C27	HDSTBN[1]#	GTL+	1.5
10	INOUT	G22	HD[27]#	GTL+	1.5
11	INOUT	G24	HD[24]#	GTL+	1.5
12	INOUT	C28	HD[25]#	GTL+	1.5
13	INOUT	E27	HD[20]#	GTL+	1.5
14	INOUT	F2	HD[17]#	GTL+	1.5
15	INOUT	D27	HD[23]#	GTL+	1.5
16	INOUT	G25	HD[21]#	GTL+	1.5
17	INOUT	F25	HD[16]#	GTL+	1.5
18	INOUT	H23	HD[19]#	GTL+	1.5
19	INOUT	F28	HD[22]#	GTL+	1.5
20	INOUT	K23	HD[11]#	GTL+	1.5
21	INOUT	J23	HD[14]#	GTL+	1.5
22	INOUT	H25	HD[10]#	GTL+	1.5
23	INOUT	G27	HD[12]#	GTL+	1.5
24	INOUT	K22	HD[0]#	GTL+	1.5
25	INOUT	H26	HD[15]#	GTL+	1.5
26	INOUT	G28	HD[5]#	GTL+	1.5
27	INOUT	H27	HD[1]#	GTL+	1.5

28	INOUT	J24	HD[9]#	GTL+	1.5
29	INOUT	L23	HD[7]#	GTL+	1.5
30	INOUT	K25	HD[2]#	GTL+	1.5
31	INOUT	K27	HDSTBP[0]#	GTL+	1.5
32	INOUT	J28	HDSTBN[0]#	GTL+	1.5
33	INOUT	J25	DINV[0]#	GTL+	1.5
34	INOUT	K26	HD[13]#	GTL+	1.5
35	INOUT	L24	HD[3]#	GTL+	1.5
36	INOUT	L25	HD[8]#	GTL+	1.5
37	INOUT	L27	HD[6]#	GTL+	1.5
38	INOUT	J27	HD[4]#	GTL+	1.5
39	OUT	M28	DEFER#	GTL+	1.5
40	OUT	N23	RS[0]#	GTL+	1.5
41	OUT	P26	RS[1]#	GTL+	1.5
42	INOUT	T26	HADSTB[0]#	GTL+	1.5

**XOR Chain FSB 3**

XOR Out	IN/OUT	Ball	Pin	I/O Type	Voltage
		OUT	AC6	SMA[8]	SSTL_2
1	OUT	F15	CPURST#	GTL+	1.5
2	IN	Y23	DPSLP#	CMOS	1.5
3	INOUT	N27	HIT#	GTL+	1.5
4	INOUT	N28	HITM#	GTL+	1.5
5	INOUT	N25	BNR#	GTL+	1.5
6	INOUT	N24	DRDY#	GTL+	1.5
7	IN	P27	HLOCK#	GTL+	1.5
8	INOUT	M23	BREQ0#	GTL+	1.5
9	OUT	M25	HTRDY#	GTL+	1.5
10	INOUT	M26	DBSY#	GTL+	1.5
11	INOUT	L28	ADS#	GTL+	1.5
12	INOUT	R28	HREQ[0]#	GTL+	1.5
13	INOUT	P25	HREQ[1]#	GTL+	1.5
14	INOUT	T28	HA[5]#	GTL+	1.5
15	INOUT	R27	HA[6]#	GTL+	1.5
16	INOUT	R23	HREQ[2]#	GTL+	1.5
17	INOUT	R24	HA[9]#	GTL+	1.5
18	INOUT	T27	HA[13]#	GTL+	1.5
19	INOUT	U28	HA[10]#	GTL+	1.5



20	INOUT	P23	HA[3]#	GTL+	1.5
21	INOUT	T25	HA[4]#	GTL+	1.5
22	INOUT	R25	HREQ[3]#	GTL+	1.5
23	INOUT	V27	HA[14]#	GTL+	1.5
24	INOUT	U27	HA[12]#	GTL+	1.5
25	INOUT	V28	HA[11]#	GTL+	1.5
26	INOUT	T23	HREQ[4]#	GTL+	1.5
27	INOUT	U24	HA[8]#	GTL+	1.5
28	INOUT	U23	HA[7]#	GTL+	1.5
29	INOUT	V26	HA[16]#	GTL+	1.5
30	INOUT	U25	HA[15]#	GTL+	1.5
31	INOUT	V25	HA[18]#	GTL+	1.5
32	INOUT	Y26	HA[30]#	GTL+	1.5
33	INOUT	W28	HA[28]#	GTL+	1.5
34	INOUT	W25	HA[20]#	GTL+	1.5
35	INOUT	V23	HA[19]#	GTL+	1.5
36	INOUT	W27	HA[25]#	GTL+	1.5
37	INOUT	Y25	HA[21]	GTL+	1.5
38	INOUT	W24	HA[23]#	GTL+	1.5
39	INOUT	Y27	HA[26]#	GTL+	1.5
40	INOUT	Y24	HA[17]#	GTL+	1.5
41	INOUT	AA27	HA[22]#	GTL+	1.5
42	INOUT	W23	HA[24]#	GTL+	1.5
43	INOUT	AB28	HA[31]#	GTL+	1.5
44	INOUT	AB27	HA[29]#	GTL+	1.5
45	INOUT	AA28	HA[27]	GTL+	1.5

**XOR Chain GPIO**

XOR Out	IN/OUT	Ball	Pin	I/O Type	Voltage
		OUT	AD7	SMA[7]	SSTL_2
1	OUT	G8	PANELBKLTCTL	CMOS	3.3
2	OUT	F8	PANELBKLTEN	CMOS	3.3
3	OUT	C6	LCLKCTLB	CMOS	3.3
4	IN	D6	EXTTS_0	CMOS	3.3
5	OUT	F7	AGPBUSY#	CMOS	3.3
6	IN	D7	RSVD	N/A	N/A
7	INOUT	C5	DDCPDATA	CMOS	3.3
8	INOUT	B4	DDCPCLK	CMOS	3.3
9	OUT	H10	HSYNC	CMOS	3.3



10	OUT	A5	PANELVDDEN	CMOS	3.3
11	INOUT	B6	DDCACLK	CMOS	3.3
12	OUT	J9	VSYNC	CMOS	3.3
13	INOUT	G9	DDCADATA	CMOS	3.3
14	OUT	H9	LCLKCTLA	CMOS	3.3

**XOR Chain HUB**

XOR Out	IN/OUT	Ball	Pin	I/O Type	Voltage
	OUT	AD8	SMA[6]	SSTL_2	2.5
1	INOUT	W2	HL[4]	HL1.5	1.2
2	INOUT	W6	HL[5]	HL1.5	1.2
3	INOUT	W7	HL[7]	HL1.5	1.2
4	INOUT	V6	HL[6]	HL1.5	1.2
5	INOUT	W3	HLSTB	HL1.5	1.2
6	INOUT	V2	HLSTB#	HL1.5	1.2
7	IN	V5	HI[9]	HL1.5	1.2
8	INOUT	V4	HL[10]	HL1.5	1.2
9	INOUT	V3	HL[3]	HL1.5	1.2
10	INOUT	U4	HL[1]	HL1.5	1.2
11	INOUT	U3	HL[2]	HL1.5	1.2
12	INOUT	U7	HL[0]	HL1.5	1.2
13	OUT	T3	HL[8]	HL1.5	1.2

**XOR Chain LVDS**

XOR Out	IN/OUT	Ball	Pin	I/O Type	Voltage
	OUT	AD17	SMA[3]	SSTL_2	2.5
1	INOUT	F10	ICLKBP	LVDS	1.5
2	INOUT	E10	ICLKBM	LVDS	1.5
3	INOUT	G10	IYBP[3]	LVDS	1.5
4	INOUT	G11	IYBM[3]	LVDS	1.5
5	INOUT	G12	IYBP[0]	LVDS	1.5
6	INOUT	H12	IYBM[0]	LVDS	1.5
7	INOUT	E11	IYBP[1]	LVDS	1.5
8	INOUT	E12	IYBM[1]	LVDS	1.5
9	INOUT	C11	IYBP[2]	LVDS	1.5
10	INOUT	C12	IYBM[2]	LVDS	1.5
11	INOUT	E13	ICLKAP	LVDS	1.5
12	INOUT	D14	ICLKAM	LVDS	1.5
13	INOUT	B13	IYAP[3]	LVDS	1.5



14	INOUT	C13	IYAM[3]	LVDS	1.5
15	INOUT	F14	IYAP[0]	LVDS	1.5
16	INOUT	G14	IYAM[0]	LVDS	1.5
17	INOUT	C14	IYAP[2]	LVDS	1.5
18	INOUT	C15	IYAM[2]	LVDS	1.5
19	INOUT	E14	IYAP[1]	LVDS	1.5
20	INOUT	E15	IYAM[1]	LVDS	1.5
<b>XOR Chain SM1</b>					
XOR Out	DDR SDRAM IN/OUT	Ball	Pin	I/O Type	Voltage
	OUT	AD23	SCS[0]#	SSTL_2	2.5
1	INOUT	AE27	SDQ[62]	SSTL_2	2.5
2	INOUT	AD27	SDQ[63]	SSTL_2	2.5
3	INOUT	AF26	SDQ[61]	SSTL_2	2.5
4	INOUT	AG26	SDQ[60]	SSTL_2	2.5
5	OUT	AC25	SCS[3]#	SSTL_2	2.5
6	OUT	AD24	SDM[6]	SSTL_2	2.5
7	INOUT	AH24	SDQS[6]	SSTL_2	2.5
8	OUT	AD25	SWE#	SSTL_2	2.5
9	OUT	AC18	SMA[0]	SSTL_2	2.5
10	INOUT	AH17	SDQS[4]	SSTL_2	2.5
11	OUT	AD19	SDM[4]	SSTL_2	2.5
12	CLK	AC26	SCK[1]	SSTL_2	2.5
13	CLK	AB23	SCK[4]	SSTL_2	2.5
14	CLK	AA3	SCK[5]	SSTL_2	2.5
15	CLK	AC2	SCK[3]	SSTL_2	2.5
16	CLK	AB2	SCK[0]	SSTL_2	2.5
17	CLK	AC3	SCK[2]	SSTL_2	2.5
18	OUT	AH15	SDM[8]	SSTL_2	2.5
19	INOUT	AF17	RSVD	N/A	N/A
20	INOUT	AF16	RSVD	N/A	N/A
21	INOUT	AG16	RSVD	N/A	N/A
22	INOUT	AE15	RSVD	N/A	N/A
23	INOUT	AH14	RSVD	N/A	N/A
24	INOUT	AE17	RSVD	N/A	N/A
25	INOUT	AD15	SDQS[8]	SSTL_2	2.5
26	INOUT	AE14	RSVD	N/A	N/A
27	INUT	AG14	RSVD	N/A	N/A

28	INOUT	AH8	SDQS[2]	SSTL_2	2.5
29	OUT	AE9	SDM[2]	SSTL_2	2.5
30	OUT	AC7	SCKE[0]	SSTL_2	2.5
31	INOUT	AG2	SDQS[0]	SSTL_2	2.5
32	OUT	AE5	SDM[0]	SSTL_2	2.5

**XOR Chain SM2**

XOR Out	DDR SDRAM IN/OUT	Ball	Pin	I/O Type	Voltage
		OUT	AD26	SCS[1]#	SSTL_2
1	INOUT	AF28	SDQ[59]	SSTL_2	2.5
2	INOUT	AG28	SDQ[58]	SSTL_2	2.5
3	INOUT	AH27	SDQS[7]	SSTL_2	2.5
4	OUT	AH28	SDM[7]	SSTL_2	2.5
5	INOUT	AE26	SDQ[57]	SSTL_2	2.5
6	INOUT	AH26	SDQ[56]	SSTL_2	2.5
7	INOUT	AH25	SDQ[51]	SSTL_2	2.5
8	INOUT	AG25	SDQ[55]	SSTL_2	2.5
9	INOUT	AF25	SDQ[54]	SSTL_2	2.5
10	INOUT	AE24	SDQ[50]	SSTL_2	2.5
11	INOUT	AH23	SDQ[49]	SSTL_2	2.5
12	INOUT	AF23	SDQ[53]	SSTL_2	2.5
13	INOUT	AE23	SDQ[48]	SSTL_2	2.5
14	INOUT	AG23	SDQ[52]	SSTL_2	2.5
15	INOUT	AE21	SDQS[5]	SSTL_2	2.5
16	OUT	AD21	SDM[5]	SSTL_2	2.5
17	OUT	AD20	SBA[1]	SSTL_2	2.5
18	OUT	AD22	SBA[0]	SSTL_2	2.5
19	OUT	AC21	SRAS#	SSTL_2	2.5
20	OUT	AC15	RCVENOUT#	SSTL_2	2.5
21	INOUT	AC16	RCVENIN#	SSTL_2	2.5
22	CLK	AB24	SCK[4]#	SSTL_2	2.5
23	CLK	AB25	SCK[1]#	SSTL_2	2.5
24	CLK	AB4	SCK[5]#	SSTL_2	2.5
25	CLK	AA2	SCK[0]#	SSTL_2	2.5
26	CLK	AD2	SCK[3]#	SSTL_2	2.5
27	CLK	AD4	SCK[2]#	SSTL_2	2.5
28	OUT	AD10	SMAB[5]	SSTL_2	2.5
29	OUT	AD14	SMA[1]	SSTL_2	2.5



30	OUT	AD16	SMAB[1]	SSTL_2	2.5
31	OUT	AD13	SMA[2]	SSTL_2	2.5
32	OUT	AF11	SMAB[4]	SSTL_2	2.5
33	OUT	AC12	SMAB[2]	SSTL_2	2.5
34	OUT	AC13	SMA[5]	SSTL_2	2.5
35	INOUT	AE12	SDQS[3]	SSTL_2	2.5
36	OUT	AH12	SDM[3]	SSTL_2	2.5
37	OUT	AD11	SMA[4]	SSTL_2	2.5
38	OUT	AC10	SCKE[3]	SSTL_2	2.5
39	OUT	AE6	SDM[1]	SSTL_2	2.5
40	INOUT	AH5	SDQS[1]	SSTL_2	2.5
41	OUT	AC9	SCKE[2]	SSTL_2	2.5
42	OUT	AB7	SCKE[1]	SSTL_2	2.5
<b>XOR Chain SM 3</b>					
<b>XOR Out</b>	<b>DDR SDRAM IN/OUT</b>	<b>Ball</b>	<b>Pin</b>	<b>I/O Type</b>	<b>Voltage</b>
	OUT	AC22	SCS[2]#	SSTL_2	2.5
1	OUT	AC24	SCAS#	SSTL_2	2.5
2	INOUT	AG22	SDQ[47]	SSTL_2	2.5
3	INOUT	AH22	SDQ[43]	SSTL_2	2.5
4	INOUT	AF22	SDQ[42]	SSTL_2	2.5
5	INOUT	AG20	SDQ[41]	SSTL_2	2.5
6	INOUT	AF20	SDQ[44]	SSTL_2	2.5
7	INOUT	AH21	SDQ[46]	SSTL_2	2.5
8	INOUT	AH19	SDQ[45]	SSTL_2	2.5
9	INOUT	AH20	SDQ[40]	SSTL_2	2.5
10	INOUT	AH16	SDQ[32]	SSTL_2	2.5
11	INOUT	AD18	SDQ[36]	SSTL_2	2.5
12	INOUT	AG19	SDQ[39]	SSTL_2	2.5
13	INOUT	AH18	SDQ[38]	SSTL_2	2.5
14	INOUT	AF19	SDQ[34]	SSTL_2	2.5
15	INOUT	AE18	SDQ[37]	SSTL_2	2.5
16	INOUT	AG17	SDQ[33]	SSTL_2	2.5
17	INOUT	AE20	SDQ[35]	SSTL_2	2.5
18	INOUT	AG13	SDQ[26]	SSTL_2	2.5
19	INOUT	AF14	SDQ[27]	SSTL_2	2.5
20	INOUT	AF13	SDQ[30]	SSTL_2	2.5
21	INOUT	AH13	SDQ[31]	SSTL_2	2.5

22	INOUT	AD12	SDQ[29]	SSTL_2	2.5
23	INOUT	AH10	SDQ[24]	SSTL_2	2.5
24	INOUT	AH11	SDQ[25]	SSTL_2	2.5
25	INOUT	AG11	SDQ[28]	SSTL_2	2.5
26	INOUT	AF10	SDQ[22]	SSTL_2	2.5
27	INOUT	AE11	SDQ[23]	SSTL_2	2.5
28	INOUT	AG10	SDQ[19]	SSTL_2	2.5
29	INOUT	AF8	SDQ[16]	SSTL_2	2.5
30	INOUT	AH9	SDQ[18]	SSTL_2	2.5
31	INOUT	AD9	SDQ[21]	SSTL_2	2.5
32	INOUT	AH7	SDQ[20]	SSTL_2	2.5
33	INOUT	AG8	SDQ[17]	SSTL_2	2.5
34	INOUT	AF7	SDQ[14]	SSTL_2	2.5
35	INOUT	AG7	SDQ[10]	SSTL_2	2.5
36	INOUT	AE8	SDQ[11]	SSTL_2	2.5
37	INOUT	AH6	SDQ[15]	SSTL_2	2.5
38	INOUT	AF5	SDQ[12]	SSTL_2	2.5
39	INOUT	AD6	SDQ[8]	SSTL_2	2.5
40	INOUT	AH4	SDQ[13]	SSTL_2	2.5
41	INOUT	AG5	SDQ[9]	SSTL_2	2.5
42	INOUT	AH2	SDQ[3]	SSTL_2	2.5
43	INOUT	AF4	SDQ[2]	SSTL_2	2.5
44	INOUT	AG4	SDQ[6]	SSTL_2	2.5
45	INOUT	AH3	SDQ[7]	SSTL_2	2.5
46	INOUT	AF2	SDQ[0]	SSTL_2	2.5
47	INOUT	AD3	SDQ[4]	SSTL_2	2.5
48	INOUT	AE3	SDQ[1]	SSTL_2	2.5
49	INOUT	AE2	SDQ[5]	SSTL_2	2.5

## 7.4.1. VCC/VSS Voltage Groups

Table 34. Voltage Levels and Ball Out for Voltage Groups

Name	Voltage Level	Ball out
VCC	1.2	H14,J15,N14,N16,P13,P15,P17,R14,R16,T13,T15, T17,U14,U16,W21,AA15,AA17,AA19
VCCADAC	1.5	A9,B9
VCCDVO	1.5	E1,E4,E6,H7,J1,J4,J8,K9,L8,M4,M8,M9,N1,N8,P9,R8
VCCASM	1.2	AD1,AF1
VCCDLVDS	1.5	B14,B15,G13,J13
VCCGPIO	3.3	A3,A4
VCCHL	1.2	U6,U8,V1,V7,V9,W5,W8,Y1
VCCQSM	2.5	AJ6,AJ8
VCCSM	2.5	Y4,Y7,Y9,AA6,AA8,AA11,AA13,AB3,AB6,AB8,AB10, AB12,AB14,AB16,AB18,AB20,AB22,AC1,AC29,AF3, AF6,AF9,AF12,AF15,AF18,AF21,AF24,AF27,AF29, AG1,AG29,AJ5,AJ9,AJ13,AJ17,AJ21,AJ25
VCCTXLVDS	2.5	A12,B10,D10,F9
VTTHF	1.5	A22,A24,H29,M29,V29
VTTLF	1.5	A18,A20,A26,F29,G15,H16,H18,H20,H22,J19,K29,L21, M22,N21,P22,R21,T22,U21,V22,Y29,AB29
VSS	0	A13,A17,A19,A21,A23,A25,A27,B5,B24,C1,C7,C10,C22,C29, D4,D11,D13,D15,D17,D19,D21,D23,D25,D28,E7,E9,E28,E29, F11,F13,F16,F18,F20,F22,F24,F27,G1,G4,G7,G26,G29,H8,H11, H13,H15,H17,H19,H21,H24,J7,J10,J12,J14,J16,J18,J20,J22,J26, J29,K4,K8,K24,L1,L6,L9,L22,L26,L29,M7,M21,M24,N4,N9,N13, N15,N17,N22,N26,N29,P8,P14,P16,P21,P24,R2,R7,R9,R13,R15, R17,R22,R26,T4,T8,T9,T14,T16,T21,T24,U1,U5,U9,U13,U15, U17,U22,U26,U29,V8,V21,V24,W4,W9,W22,W26,W29,Y5,Y6, Y8,Y21,AA1,AA4,AA7,AA10,AA12,AA14,AA16,AA18,AA20, AA21,AA23,AA24,AA25,AA29,AB9,AB11,AB13,AB15,AB17, AB19,AB21,AB26,AC4,AC8,AC11,AC14,AC17,AC20,AC23, AC27,AC28,AE1,AE4,AE7,AE10,AE13,AE16,AE19,AE22,AE25, AE28,AG3,AG6,AG9,AG12,AG15,AG18,AG21,AG24,AG27,AJ1, AJ3,AJ7,AJ10,AJ11,AJ12,AJ18,AJ20,AJ23,AJ26,AJ27

## 8. Intel 852GM/852GMV GMCH Strap Pins

### 8.1. Strapping Configuration

Table 35. Strapping Signals and Configuration

Pin Name	Strap Description	Configuration	I/F Type	Buffer Type
HSYNC	XOR Chain Test	Low = Normal Ops (Default) High = XOR Test On	GPIO	OUT
VSYNC	ALL Z Test	Low = Normal Ops (Default) High = AllZ Test On	GPIO	OUT
LCLKCTLB	VTT Voltage Select	High = Mobile Intel Pentium 4 Processor-M/ Mobile Intel Celeron processor/Intel Celeron M processor/Intel Celeron D processor on 90 nm process and in the 478-pin package	GPIO	OUT
DVODETECT	*DVO Select (If DVODETECT=0 during Reset, ADDID[7:0] is latched to the ADDID Register)	Low = DVO (Default) High = Reserved	DVO	BI
GST[1]	* Clock Config: Bit_1	Please refer to Device #0 Function #3 (HPLLCC Register) for proper GST[1:0] settings	DVO	Out: 0) Before CPURST#, there is internal pull-down 1) Just out of CPURST#: These pins are Hi-Z
GST[0]	* Clock Config: Bit_0			2) C3: these pins are Hi-Z 3) S1-M: these pins are Hi-Z 4) Internal GFX D1/D3: these pins are Hi-Z 5) S3: these pins are Power down 6) S4/S5: these pins are Power down
*	External pull-ups/downs will be required on the board to enable the non-default state of the straps.			



**NOTE:** All strap signals are sampled with respect to the leading edge of the Intel 852GM/852GMV GMCH PWROK In signal.

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# 9. Ballout and Package Information

Figure 11. Intel 852GM/852GMV GMCH Ballout Diagram (Top View)

	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
AJ	NC	NC	VSS	VSS	VCCSM	SMVREF_0	VSS	SMVSW_NGL	VCCSM	VSS	SMVSW_NGH	VSS	VCCSM				VCCSM	VSS	VSS	VSS	VCCSM	VCCSM	VSS	VCCSM	VCCSM	NC	VSS	NC
AH	NC	SDM[7]	SDQS[7]	SDQ[56]	SDQ[55]	SDQS[6]	SDQ[48]	SDQ[43]	SDQ[46]	SDQ[40]	SDQ[45]	SDQ[38]	SDQS[4]	SDQ[32]	SDM[8]	SDQ[68]	SDQ[31]	SDM[3]	SDQ[25]	SDQ[24]	SDQ[18]	SDQS[2]	SDQ[20]	SDQ[15]	SDQS[1]	SDQ[13]	SDQ[7]	SDQ[3]
AG	VCCSM	SDQ[58]	VSS	SDQ[60]	SDQ[55]	VSS	SDQ[52]	SDQ[47]	VSS	SDQ[41]	SDQ[39]	VSS	SDQ[33]	SDQ[67]	VSS	SDQ[64]	SDQ[26]	VSS	SDQ[28]	SDQ[19]	VSS	SDQ[17]	SDQ[10]	VSS	SDQ[9]	SDQ[8]	VSS	SDQS[0]
AF	VCCSM	SDQ[59]	VCCSM	SDQ[61]	SDQ[54]	VCCSM	SDQ[53]	SDQ[42]	VCCSM	SDQ[44]	SDQ[34]	VCCSM	SDQ[71]	SDQ[70]	VCCSM	SDQ[27]	SDQ[30]	VCCSM	SMAB[4]	SDQ[22]	VCCSM	SDQ[16]	SDQ[14]	VCCSM	SDQ[12]	SDQ[2]	VCCSM	SDQ[0]
AE	BCLK	VSS	SDQ[62]	SDQ[57]	VSS	SDQ[50]	SDQ[48]	VSS	SDQS[5]	SDQ[35]	VSS	SDQ[37]	SDQ[66]	VSS	SDQ[69]	SDQ[65]	VSS	SDQS[3]	SDQ[23]	VSS	SDM[2]	SDQ[11]	VSS	SDM[1]	SDM[0]	VSS	SDQ[1]	SDQ[5]
AD	BCLK#	RSTIN#	SDQ[63]	SCS[1]#	SWE#	SDM[6]	SCS[0]#	SBA[0]	SDM[5]	SBA[1]	SDM[4]	SDQ[36]	SMA[3]	SMA[1]	SMA[2]	SDQ[29]	SMA[4]	SMA[5]	SDQ[21]	SMA[6]	SMA[7]	SDQ[8]	SMA[11]	SCK[2]#	SDQ[4]	SCK[3]#		
AC	VCCSM	VSS	VSS	SCK[1]	SCS[3]#	SCAS#	VSS	SCS[2]#	SRAS#	VSS	SMA[10]	SMA[0]	VSS	RCVEN_N#	RCVEN_OUT	VSS	SMA[5]	SMAB[2]	VSS	SCKE[3]	SCKE[2]	VSS	SCKE[0]	SMA[8]	SMA[9]	VSS	SCK[2]	SCK[3]
AB	VTTLF	HA[31]#	HA[29]#	VSS	SCK[1]#	SCK[4]#	SCK[4]	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	SCKE[1]	VCCSM	SMA[12]	SCK[5]#	VCCSM	SCK[0]
AA	VSS	HA[27]#	HA[22]#	HADSTB[1]#	VSS	VSS	VSS	DPWR#	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCCSM	VSS	VCCSM	VSS	NC	VCCSM	VSS	VCCSM	RSVD	VSS	SCK[5]	SCK[0]#
Y	VTTLF	HCCVREF	HA[26]#	HA[30]#	HA[21]#	HA[17]#	DPPLP#	HAVREF	VSS												VCCSM	VSS	VCCSM	VSS	VSS	VCCSM	GLCKIN	VCCAGFLL
W	VSS	HA[28]#	HA[25]#	VSS	HA[20]#	HA[23]#	HA[24]#	VSS	VCC												VSS	VCCHL	HL[7]	HL[5]	VCCHL	VSS	HLSTB	HL[4]
V	VTTHF	HA[11]#	HA[14]#	HA[16]#	HA[18]#	VSS	HA[19]#	VTTLF	VSS												VCCHL	VSS	VCCHL	HL[6]	HL[9]	HL[10]	HL[3]	HLSTB#
U	VSS	HA[10]#	HA[12]#	VSS	HA[15]#	HA[8]#	HA[7]#	VSS	VTTLF				VSS	VCC	VSS	VCC	VSS				VSS	VCCHL	HL[0]	VCCHL	VSS	HL[1]	HL[2]	PSWING
T		HA[5]#	HA[13]#	HADSTB[0]#	HA[4]#	VSS	HREQ[4]#	VTTLF	VSS				VCC	VSS	VCC	VSS	VCC				VSS	VSS	MDDCCATA	RSVD	RSVD	VSS	HL[8]	HLRCCOMP
R		HREQ[0]#	HA[6]#	VSS	HREQ[3]#	HA[9]#	HREQ[2]#	VSS	VTTLF				VSS	VCC	VSS	VCC	VSS				VSS	VCCDV0	VSS	RSVD	RSVD	RSVD	RSVD	VSS
P		BPR#	HLOCK#	RS[1]#	HREQ[1]#	VSS	HA[3]#	VTTLF	VSS				VCC	VSS	VCC	VSS	VCC				VCCDV0	VSS	MDDCLK	RSVD	RSVD	RSVD	RSVD	RSVD
N	VSS	HITM#	HIT#	VSS	BNR#	DRDY#	RS[0]#	VSS	VTTLF				VSS	VCC	VSS	VCC	VSS				VSS	VCCDV0	MDVICLK	M2CDA TA	RSVD	VSS	RSVD	RSVD
M	VTTHF	DEFER#	RS[2]#	DBSY#	HTRDY#	VSS	BREQ0#	VTTLF	VSS												VCCDV0	VCCDV0	VSS	MDVIDA TA	RSVD	VCCDV0	DOBOCLKINT	RSVD
L	VSS	ADS#	HD[6]#	VSS	HD[8]#	HD[3]#	HD[7]#	VSS	VTTLF												VSS	VCCDV0	DVODECT	VSS	DVOCYNC	RSVD	DVOCBLANK#	RSVD
K	VTTLF	HYSWING	HDSTBP[0]#	HD[13]#	HD[2]#	VSS	HD[11]#	HD[0]#	HDVREF[0]												VCCDV0	VSS	M2CCLK	DVOCHSYNC	DVOCDA[0]	VSS	DVOCDA[2]	DVOCDA[3]
J	VSS	HDSTB[0]#	HD[4]#	VSS	DINV[0]#	HD[9]#	HD[14]#	VSS	HDVREF[1]	VSS	VTTLF	VSS	HDVREF[2]	VSS	VCC	VSS	VCCDLVDS	VSS	PWRCK	VSS	VSYN	VCCDV0	VSS	DVOCDA[4]	DVOCDA[5]	VCCDV0	DVOCCLK	DVOCCLK#
H	VTTHF	HYRCOMP	HD[1]#	HD[15]#	HD[10]#	VSS	HD[19]#	VTTLF	VSS	VTTLF	VSS	VTTLF	VSS	VTTLF	VSS	VCC	VSS	IBM[0]	VSS	HSYN	LCLKCTLA	VSS	VCCDV0	DVOCDA[10]	DVOCFLDSTL	DVOCDA[9]	DVOCDA[8]	DVOCDA[6]
G	VSS	HD[5]#	HD[12]#	VSS	HD[21]#	HD[24]#	HD[30]#	HD[27]#	HD[33]#	HD[40]#	DINV[3]#	HD[48]#	HD[51]#	HD[58]#	VTTLF	IYAM[0]	VCCDLVDS	IBP[0]	IBM[3]	IBP[3]	DDCADA TA	PANELB KLCTCL	VSS	ADDID[6]	ADDID[4]	VSS	DVOCDA[11]	DVOCB NTR#
F	VTTLF	HD[22]#	VSS	HD[17]#	HD[16]#	VSS	HD[44]#	VSS	HD[45]#	VSS	HD[53]#	VSS	HD[56]#	VSS	CPURST#	IYAP[0]	VSS	RSVD	VSS	ICLKBP	VCCTXLVDS	PANELB KLTEN	AGPBUS Y#	ADDID[7]	ADDID[1]	ADDID[5]	RSVD	RSVD
E	VSS	VSS	HD[20]#	HD[29]#	DINV[1]#	HD[38]#	HD[41]#	HDSTB[2]#	HDSTBP[2]#	HD[50]#	HD[49]#	HDSTBP[3]#	HD[61]#	HD[59]#	IYAM[1]	IYAP[1]	ICLKAP	IBM[1]	IBP[1]	ICLKBM	VSS	REFSET	VSS	VCCDV0	ADDID[0]	VCCDV0	ADDID[2]	ADDID[3]
D	VCCAHP LL	VSS	HD[23]#	HDSTBP[1]#	VSS	HD[39]#	VSS	HD[36]#	VSS	HD[52]#	VSS	HDSTB[3]#	VSS	HD[62]#	VSS	ICLKAM	VSS	RSVD	VSS	VCCTXLVDS	BLUE#	GREEN#	RSVD	EXTSL_0	DPMS	VSS	RSVD	RSVD
C	VSS	HD[25]#	HDSTB[1]#	HD[28]#	HD[37]#	HD[34]#	HD[35]#	VSS	HD[47]#	HD[46]#	HD[54]#	HD[63]#	HD[55]#	HD[60]#	IYAM[2]	IYAP[2]	IYAM[3]	IBM[2]	IBP[2]	VSS	BLUE	GREEN	VSS	LCLKCTLB	DDCPDA TA	GST[0]	GST[1]	RSVD
B	NC	HD[31]#	HD[18]#	HD[26]#	DINV[2]#	VSS	HD[43]#	HD[42]#	HD[32]#	HXRCCOMP	HD[57]#	HXSWING	DREFSS CLK	VCCADP LLB	VCCDLVDS	VCCDLVDS	IYAP[3]	RSVD	VSSALVDS	VCCTXLVDS	VCCADAC	VSSADAC	DREFCLK	DDCCLK	VSS	DDCPCLK	RSVD	RSVD
A	NC	NC	VSS	VTTLF	VSS	VTTHF	VSS	VTTHF	VSS	VTTLF	VSS	VTTLF	VSS				VSS	VCCTXLVDS	VCCALVDS	LIB	VCCADAC	RED#	RED	VCCADFLA	PANELVDEN	VCCGPI0	VCCGPI0	NC



Table 36. Ballout Table

Row	Column	Signal Name
E	5	ADDID[0]
F	5	ADDID[1]
E	3	ADDID[2]
E	2	ADDID[3]
G	5	ADDID[4]
F	4	ADDID[5]
G	6	ADDID[6]
F	6	ADDID[7]
L	28	ADS#
F	7	AGPBUSY#
AE	29	BCLK
AD	29	BCLK#
C	9	BLUE
D	9	BLUE#
N	25	BNR#
P	28	BPRI#
M	23	BREQ0#
F	15	CPURST#
M	26	DBSY#
B	6	DDCACLK
G	9	DDCADATA
B	4	DDCPCLK
C	5	DDCPDATA
M	28	DEFER#
J	25	DINV[0]#
E	25	DINV[1]#
B	25	DINV[2]#
G	19	DINV[3]#
D	5	DPMS
Y	23	DPSLP#
N	24	DRDY#
B	7	DREFCLK
B	17	DREFSCLK
L	2	DVOBBLANK#

Row	Column	Signal Name
M	3	DVOBCCLKINT
G	2	DVOBCINTR#
P	3	RSVD
P	4	RSVD
R	3	RSVD
R	5	RSVD
M	1	RSVD
M	5	RSVD
R	6	RSVD
R	4	RSVD
P	6	RSVD
P	5	RSVD
N	5	RSVD
P	2	RSVD
N	2	RSVD
N	3	RSVD
M	2	RSVD
T	6	RSVD
T	5	RSVD
L	7	DVODETECT
D	1	DVORCOMP
D	6	EXTTS_0
Y	3	GCLKIN
C	8	GREEN
D	8	GREEN#
F	1	GVREF
U	28	HA[10]#
V	28	HA[11]#
U	27	HA[12]#
T	27	HA[13]#
V	27	HA[14]#
U	25	HA[15]#
V	26	HA[16]#
Y	24	HA[17]#
V	25	HA[18]#

Row	Column	Signal Name
V	23	HA[19]#
W	25	HA[20]#
Y	25	HA[21]#
AA	27	HA[22]#
W	24	HA[23]#
W	23	HA[24]#
W	27	HA[25]#
Y	27	HA[26]#
AA	28	HA[27]#
W	28	HA[28]#
AB	27	HA[29]#
P	23	HA[3]#
Y	26	HA[30]#
AB	28	HA[31]#
T	25	HA[4]#
T	28	HA[5]#
R	27	HA[6]#
U	23	HA[7]#
U	24	HA[8]#
R	24	HA[9]#
T	26	HADSTB[0]#
AA	26	HADSTB[1]#
Y	22	HAVREF
Y	28	HCCVREF
K	22	HD[0]#
H	27	HD[1]#
H	25	HD[10]#
K	23	HD[11]#
G	27	HD[12]#
K	26	HD[13]#
J	23	HD[14]#
H	26	HD[15]#
F	25	HD[16]#
F	26	HD[17]#
B	27	HD[18]#
H	23	HD[19]#



Row	Column	Signal Name
K	25	HD[2]#
E	27	HD[20]#
G	25	HD[21]#
F	28	HD[22]#
D	27	HD[23]#
G	24	HD[24]#
C	28	HD[25]#
B	26	HD[26]#
G	22	HD[27]#
C	26	HD[28]#
E	26	HD[29]#
L	24	HD[3]#
G	23	HD[30]#
B	28	HD[31]#
B	21	HD[32]#
G	21	HD[33]#
C	24	HD[34]#
C	23	HD[35]#
D	22	HD[36]#
C	25	HD[37]#
E	24	HD[38]#
D	24	HD[39]#
J	27	HD[4]#
G	20	HD[40]#
E	23	HD[41]#
B	22	HD[42]#
B	23	HD[43]#
F	23	HD[44]#
F	21	HD[45]#
C	20	HD[46]#
C	21	HD[47]#
G	18	HD[48]#
E	19	HD[49]#
G	28	HD[5]#
E	20	HD[50]#

Row	Column	Signal Name
G	17	HD[51]#
D	20	HD[52]#
F	19	HD[53]#
C	19	HD[54]#
C	17	HD[55]#
F	17	HD[56]#
B	19	HD[57]#
G	16	HD[58]#
E	16	HD[59]#
L	27	HD[6]#
C	16	HD[60]#
E	17	HD[61]#
D	16	HD[62]#
C	18	HD[63]#
L	23	HD[7]#
L	25	HD[8]#
J	24	HD[9]#
J	28	HDSTBN[0]#
C	27	HDSTBN[1]#
E	22	HDSTBN[2]#
D	18	HDSTBN[3]#
K	27	HDSTBP[0]#
D	26	HDSTBP[1]#
E	21	HDSTBP[2]#
E	18	HDSTBP[3]#
K	21	HDVREF[0]
J	21	HDVREF[1]
J	17	HDVREF[2]
N	27	HIT#
N	28	HITM#
U	7	HL[0]
U	4	HL[1]
V	4	HL[10]
U	3	HL[2]
V	3	HL[3]

Row	Column	Signal Name
W	2	HL[4]
W	6	HL[5]
V	6	HL[6]
W	7	HL[7]
T	3	HL[8]
V	5	HL[9]
P	27	HLOCK#
T	2	HLRCOMP
W	3	HLSTB
V	2	HLSTB#
W	1	HLVREF
R	28	HREQ[0]#
P	25	HREQ[1]#
R	23	HREQ[2]#
R	25	HREQ[3]#
T	23	HREQ[4]#
H	10	HSYNC
M	25	HTRDY#
B	20	HXRCOMP
B	18	HXSWING
H	28	HYRCOMP
K	28	HYSWING
D	14	ICLKAM
E	13	ICLKAP
E	10	ICLKBM
F	10	ICLKBP
G	14	IYAM[0]
E	15	IYAM[1]
C	15	IYAM[2]
C	13	IYAM[3]
F	14	IYAP[0]
E	14	IYAP[1]
C	14	IYAP[2]
B	13	IYAP[3]
H	12	IYBM[0]



Row	Column	Signal Name
E	12	IYBM[1]
C	12	IYBM[2]
G	11	IYBM[3]
G	12	IYBP[0]
E	11	IYBP[1]
C	11	IYBP[2]
G	10	IYBP[3]
H	9	LCLKCTLA
C	6	LCLKCTLB
A	10	LIBG
P	7	MDDCCLK
T	7	MDDCDATA
N	7	MDVICLK
M	6	MDVIDATA
K	7	MI2CCLK
N	6	MI2CDATA
AJ	29	NC
AH	29	NC
B	29	NC
A	29	NC
AJ	28	NC
A	28	NC
AA	9	NC
AJ	4	NC
AJ	2	NC
A	2	NC
AH	1	NC
B	1	NC
G	8	PANELBKLTCTL
F	8	PANELBKLTEN
A	5	PANELVDDEN
U	2	PSWING
J	11	PWROK
AC	16	RCVENIN#
AC	15	RCVENOUT
A	7	RED

Row	Column	Signal Name
A	8	RED#
E	8	REFSET
N	23	RS[0]#
P	26	RS[1]#
M	27	RS[2]#
AD	28	RSTIN#
AA	22	DPWR#
L	3	DVOCBLANK#
J	3	DVOCCLK
J	2	DVOCCLK#
K	5	DVOC[0]
K	1	DVOC[1]
H	6	DVOC[10]
G	3	DVOC[11]
K	3	DVOC[2]
K	2	DVOC[3]
J	6	DVOC[4]
J	5	DVOC[5]
H	2	DVOC[6]
H	1	DVOC[7]
H	3	DVOC[8]
H	4	DVOC[9]
H	5	DVOCFLDSTL
K	6	DVOCHSYNC
L	5	DVOCVSYNC
F	12	RSVD
D	12	RSVD
B	12	RSVD
AA	5	RSVD
L	4	RSVD
C	4	GST[0]
F	3	RSVD
D	3	RSVD
C	3	GST[1]
B	3	RSVD
F	2	RSVD

Row	Column	Signal Name
D	2	RSVD
C	2	RSVD
B	2	RSVD
D	7	RSVD
AD	22	SBA[0]
AD	20	SBA[1]
AC	24	SCAS#
AB	2	SCK[0]
AA	2	SCK[0]#
AC	26	SCK[1]
AB	25	SCK[1]#
AC	3	SCK[2]
AD	4	SCK[2]#
AC	2	SCK[3]
AD	2	SCK[3]#
AB	23	SCK[4]
AB	24	SCK[4]#
AA	3	SCK[5]
AB	4	SCK[5]#
AC	7	SCKE[0]
AB	7	SCKE[1]
AC	9	SCKE[2]
AC	10	SCKE[3]
AD	23	SCS[0]#
AD	26	SCS[1]#
AC	22	SCS[2]#
AC	25	SCS[3]#
AE	5	SDM[0]
AE	6	SDM[1]
AE	9	SDM[2]
AH	12	SDM[3]
AD	19	SDM[4]
AD	21	SDM[5]
AD	24	SDM[6]
AH	28	SDM[7]
AH	15	SDM[8]



Row	Column	Signal Name
AF	2	SDQ[0]
AE	3	SDQ[1]
AG	7	SDQ[10]
AE	8	SDQ[11]
AF	5	SDQ[12]
AH	4	SDQ[13]
AF	7	SDQ[14]
AH	6	SDQ[15]
AF	8	SDQ[16]
AG	8	SDQ[17]
AH	9	SDQ[18]
AG	10	SDQ[19]
AF	4	SDQ[2]
AH	7	SDQ[20]
AD	9	SDQ[21]
AF	10	SDQ[22]
AE	11	SDQ[23]
AH	10	SDQ[24]
AH	11	SDQ[25]
AG	13	SDQ[26]
AF	14	SDQ[27]
AG	11	SDQ[28]
AD	12	SDQ[29]
AH	2	SDQ[3]
AF	13	SDQ[30]
AH	13	SDQ[31]
AH	16	SDQ[32]
AG	17	SDQ[33]
AF	19	SDQ[34]
AE	20	SDQ[35]
AD	18	SDQ[36]
AE	18	SDQ[37]
AH	18	SDQ[38]
AG	19	SDQ[39]
AD	3	SDQ[4]

Row	Column	Signal Name
AH	20	SDQ[40]
AG	20	SDQ[41]
AF	22	SDQ[42]
AH	22	SDQ[43]
AF	20	SDQ[44]
AH	19	SDQ[45]
AH	21	SDQ[46]
AG	22	SDQ[47]
AE	23	SDQ[48]
AH	23	SDQ[49]
AE	2	SDQ[5]
AE	24	SDQ[50]
AH	25	SDQ[51]
AG	23	SDQ[52]
AF	23	SDQ[53]
AF	25	SDQ[54]
AG	25	SDQ[55]
AH	26	SDQ[56]
AE	26	SDQ[57]
AG	28	SDQ[58]
AF	28	SDQ[59]
AG	4	SDQ[6]
AG	26	SDQ[60]
AF	26	SDQ[61]
AE	27	SDQ[62]
AD	27	SDQ[63]
AG	14	SDQ[64]
AE	14	SDQ[65]
AE	17	SDQ[66]
AG	16	SDQ[67]
AH	14	SDQ[68]
AE	15	SDQ[69]
AH	3	SDQ[7]
AF	16	SDQ[70]
AF	17	SDQ[71]

Row	Column	Signal Name
AD	6	SDQ[8]
AG	5	SDQ[9]
AG	2	SDQS[0]
AH	5	SDQS[1]
AH	8	SDQS[2]
AE	12	SDQS[3]
AH	17	SDQS[4]
AE	21	SDQS[5]
AH	24	SDQS[6]
AH	27	SDQS[7]
AD	15	SDQS[8]
AC	18	SMA[0]
AD	14	SMA[1]
AC	19	SMA[10]
AD	5	SMA[11]
AB	5	SMA[12]
AD	13	SMA[2]
AD	17	SMA[3]
AD	11	SMA[4]
AC	13	SMA[5]
AD	8	SMA[6]
AD	7	SMA[7]
AC	6	SMA[8]
AC	5	SMA[9]
AD	16	SMAB[1]
AC	12	SMAB[2]
AF	11	SMAB[4]
AD	10	SMAB[5]
AB	1	SMRCOMP
AJ	24	SMVREF_0
AJ	19	SMVSWINGH
AJ	22	SMVSWINGL
AC	21	SRAS#
AD	25	SWE#
W	21	VCC



Row	Column	Signal Name
AA	19	VCC
AA	17	VCC
T	17	VCC
P	17	VCC
U	16	VCC
R	16	VCC
N	16	VCC
AA	15	VCC
T	15	VCC
P	15	VCC
J	15	VCC
U	14	VCC
R	14	VCC
N	14	VCC
H	14	VCC
T	13	VCC
P	13	VCC
B	9	VCCADAC
A	9	VCCADAC
A	6	VCCADPLLA
B	16	VCCADPLLB
Y	2	VCCAGPLL
D	29	VCCAHPLL
A	11	VCCALVDS
AF	1	VCCASM
AD	1	VCCASM
B	15	VCCDLVDS
B	14	VCCDLVDS
J	13	VCCDLVDS
G	13	VCCDLVDS
P	9	VCCDVO
M	9	VCCDVO
K	9	VCCDVO
R	8	VCCDVO
N	8	VCCDVO
M	8	VCCDVO

Row	Column	Signal Name
L	8	VCCDVO
J	8	VCCDVO
H	7	VCCDVO
E	6	VCCDVO
M	4	VCCDVO
J	4	VCCDVO
E	4	VCCDVO
N	1	VCCDVO
J	1	VCCDVO
E	1	VCCDVO
A	4	VCCGPIO
A	3	VCCGPIO
V	9	VCCHL
W	8	VCCHL
U	8	VCCHL
V	7	VCCHL
U	6	VCCHL
W	5	VCCHL
Y	1	VCCHL
V	1	VCCHL
AJ	8	VCCQSM
AJ	6	VCCQSM
AG	29	VCCSM
AF	29	VCCSM
AC	29	VCCSM
AF	27	VCCSM
AJ	25	VCCSM
AF	24	VCCSM
AB	22	VCCSM
AJ	21	VCCSM
AF	21	VCCSM
AB	20	VCCSM
AF	18	VCCSM
AB	18	VCCSM
AJ	17	VCCSM
AB	16	VCCSM

Row	Column	Signal Name
AF	15	VCCSM
AB	14	VCCSM
AJ	13	VCCSM
AA	13	VCCSM
AF	12	VCCSM
AB	12	VCCSM
AA	11	VCCSM
AB	10	VCCSM
AJ	9	VCCSM
AF	9	VCCSM
Y	9	VCCSM
AB	8	VCCSM
AA	8	VCCSM
Y	7	VCCSM
AF	6	VCCSM
AB	6	VCCSM
AA	6	VCCSM
AJ	5	VCCSM
Y	4	VCCSM
AF	3	VCCSM
AB	3	VCCSM
AG	1	VCCSM
AC	1	VCCSM
A	12	VCCTXLVDS
D	10	VCCTXLVDS
B	10	VCCTXLVDS
F	9	VCCTXLVDS
AA	29	VSS
W	29	VSS
U	29	VSS
N	29	VSS
L	29	VSS
J	29	VSS
G	29	VSS
E	29	VSS
C	29	VSS



Row	Column	Signal Name
AE	28	VSS
AC	28	VSS
E	28	VSS
D	28	VSS
AJ	27	VSS
AG	27	VSS
AC	27	VSS
F	27	VSS
A	27	VSS
AJ	26	VSS
AB	26	VSS
W	26	VSS
U	26	VSS
R	26	VSS
N	26	VSS
L	26	VSS
J	26	VSS
G	26	VSS
AE	25	VSS
AA	25	VSS
D	25	VSS
A	25	VSS
AG	24	VSS
AA	24	VSS
V	24	VSS
T	24	VSS
P	24	VSS
M	24	VSS
K	24	VSS
H	24	VSS
F	24	VSS
B	24	VSS
AJ	23	VSS
AC	23	VSS
AA	23	VSS

Row	Column	Signal Name
D	23	VSS
A	23	VSS
AE	22	VSS
W	22	VSS
U	22	VSS
R	22	VSS
N	22	VSS
L	22	VSS
J	22	VSS
F	22	VSS
C	22	VSS
AG	21	VSS
AB	21	VSS
AA	21	VSS
Y	21	VSS
V	21	VSS
T	21	VSS
P	21	VSS
M	21	VSS
H	21	VSS
D	21	VSS
A	21	VSS
AJ	20	VSS
AC	20	VSS
AA	20	VSS
J	20	VSS
F	20	VSS
AE	19	VSS
AB	19	VSS
H	19	VSS
D	19	VSS
A	19	VSS
AJ	18	VSS
AG	18	VSS
AA	18	VSS

Row	Column	Signal Name
J	18	VSS
F	18	VSS
AC	17	VSS
AB	17	VSS
U	17	VSS
R	17	VSS
N	17	VSS
H	17	VSS
D	17	VSS
A	17	VSS
AE	16	VSS
AA	16	VSS
T	16	VSS
P	16	VSS
J	16	VSS
F	16	VSS
AG	15	VSS
AB	15	VSS
U	15	VSS
R	15	VSS
N	15	VSS
H	15	VSS
D	15	VSS
AC	14	VSS
AA	14	VSS
T	14	VSS
P	14	VSS
J	14	VSS
AE	13	VSS
AB	13	VSS
U	13	VSS
R	13	VSS
N	13	VSS
H	13	VSS
F	13	VSS



Row	Column	Signal Name
D	13	VSS
A	13	VSS
AJ	12	VSS
AG	12	VSS
AA	12	VSS
J	12	VSS
AJ	11	VSS
AC	11	VSS
AB	11	VSS
H	11	VSS
F	11	VSS
D	11	VSS
AJ	10	VSS
AE	10	VSS
AA	10	VSS
J	10	VSS
C	10	VSS
AG	9	VSS
AB	9	VSS
W	9	VSS
U	9	VSS
T	9	VSS
R	9	VSS
N	9	VSS
L	9	VSS
E	9	VSS
AC	8	VSS
Y	8	VSS
V	8	VSS
T	8	VSS
P	8	VSS
K	8	VSS
H	8	VSS

Row	Column	Signal Name
AJ	7	VSS
AE	7	VSS
AA	7	VSS
R	7	VSS
M	7	VSS
J	7	VSS
G	7	VSS
E	7	VSS
C	7	VSS
AG	6	VSS
Y	6	VSS
L	6	VSS
Y	5	VSS
U	5	VSS
B	5	VSS
AE	4	VSS
AC	4	VSS
AA	4	VSS
W	4	VSS
T	4	VSS
N	4	VSS
K	4	VSS
G	4	VSS
D	4	VSS
AJ	3	VSS
AG	3	VSS
R	2	VSS
AJ	1	VSS
AE	1	VSS
AA	1	VSS
U	1	VSS
L	1	VSS
G	1	VSS

Row	Column	Signal Name
C	1	VSS
B	8	VSSADAC
B	11	VSSALVDS
J	9	VSYNCR
V	29	VTTHF
M	29	VTTHF
H	29	VTTHF
A	24	VTTHF
A	22	VTTHF
AB	29	VTTTLF
Y	29	VTTTLF
K	29	VTTTLF
F	29	VTTTLF
A	26	VTTTLF
V	22	VTTTLF
T	22	VTTTLF
P	22	VTTTLF
M	22	VTTTLF
H	22	VTTTLF
U	21	VTTTLF
R	21	VTTTLF
N	21	VTTTLF
L	21	VTTTLF
H	20	VTTTLF
A	20	VTTTLF
J	19	VTTTLF
H	18	VTTTLF
A	18	VTTTLF
H	16	VTTTLF
G	15	VTTTLF

## 9.1. Package Mechanical Information

The following figures provide detail on the package information and dimensions of the Intel 852GM/852GMV GMCH. The Intel 852GM/852GMV GMCH comes in a Micro-FCBGA package, which is similar to the mobile processors. The package consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keepout area, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

**Figure 12. Intel 852GM/852GMV GMCH Micro-FCBGA Package Dimensions (Top View)**

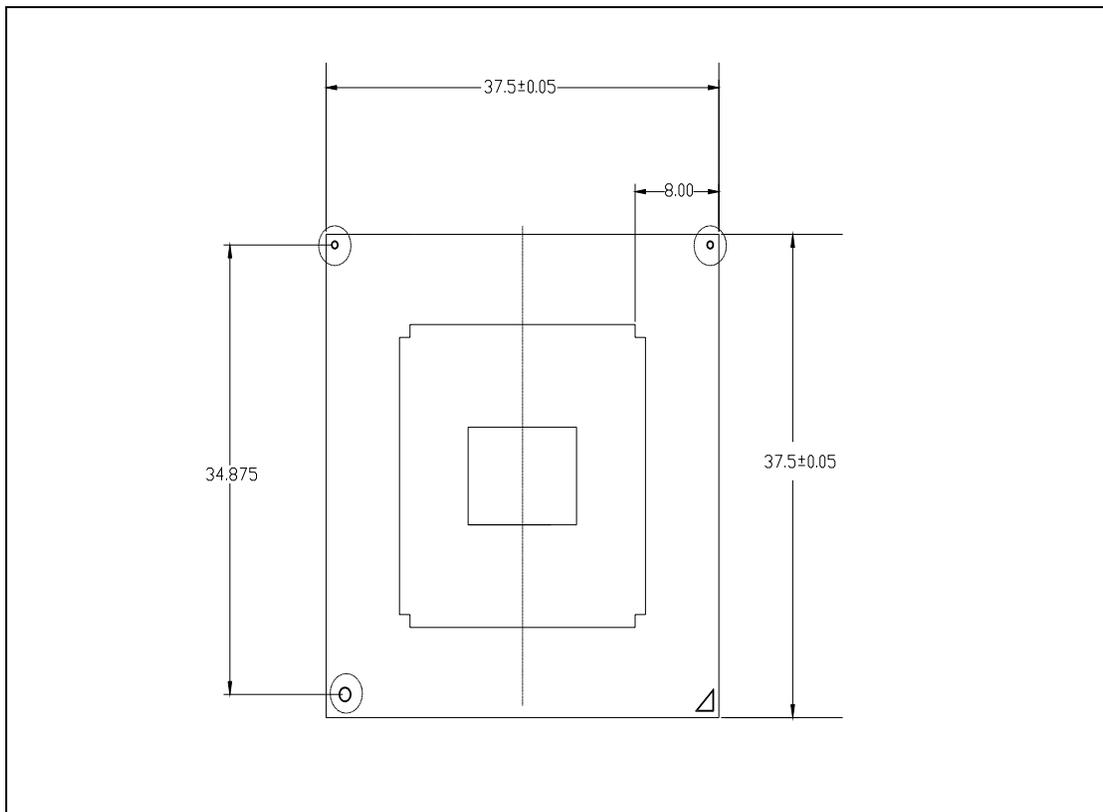




Figure 13. Intel 852GM/852GMV GMCH Micro-FCBGA Package Dimensions (Side View)

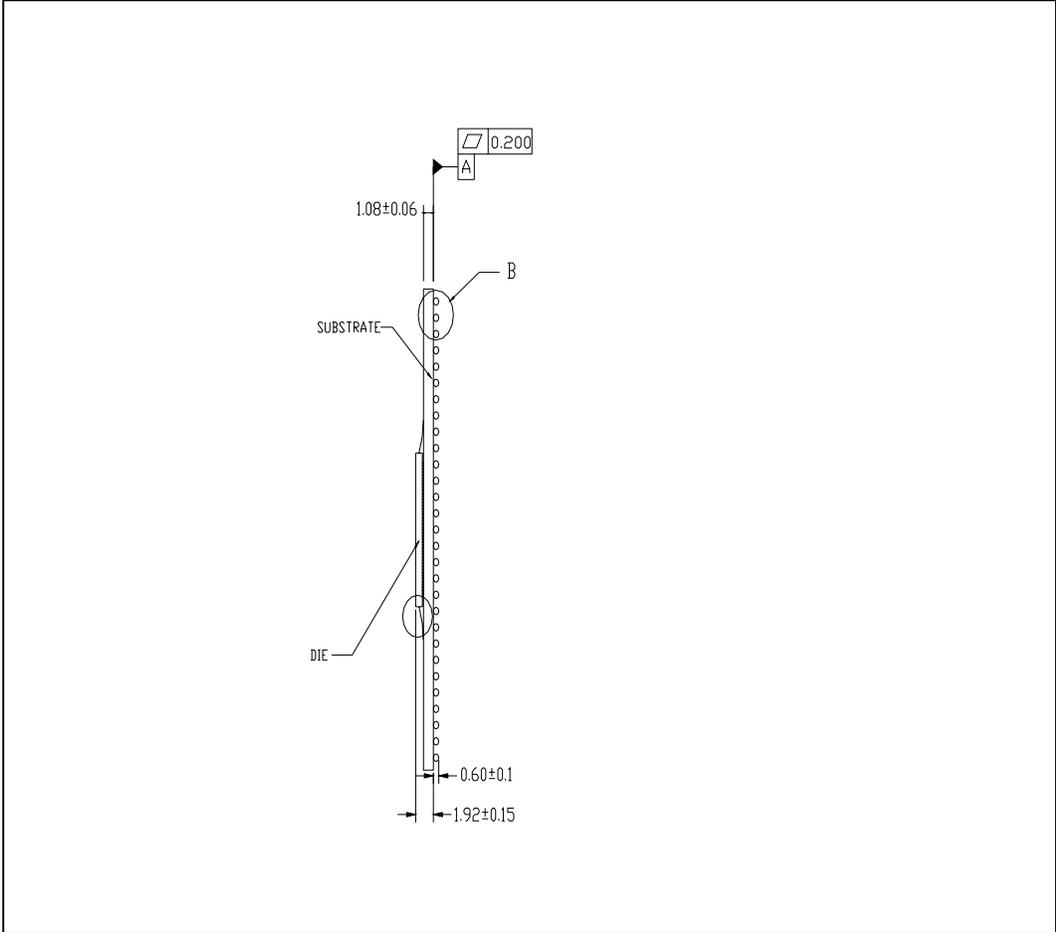
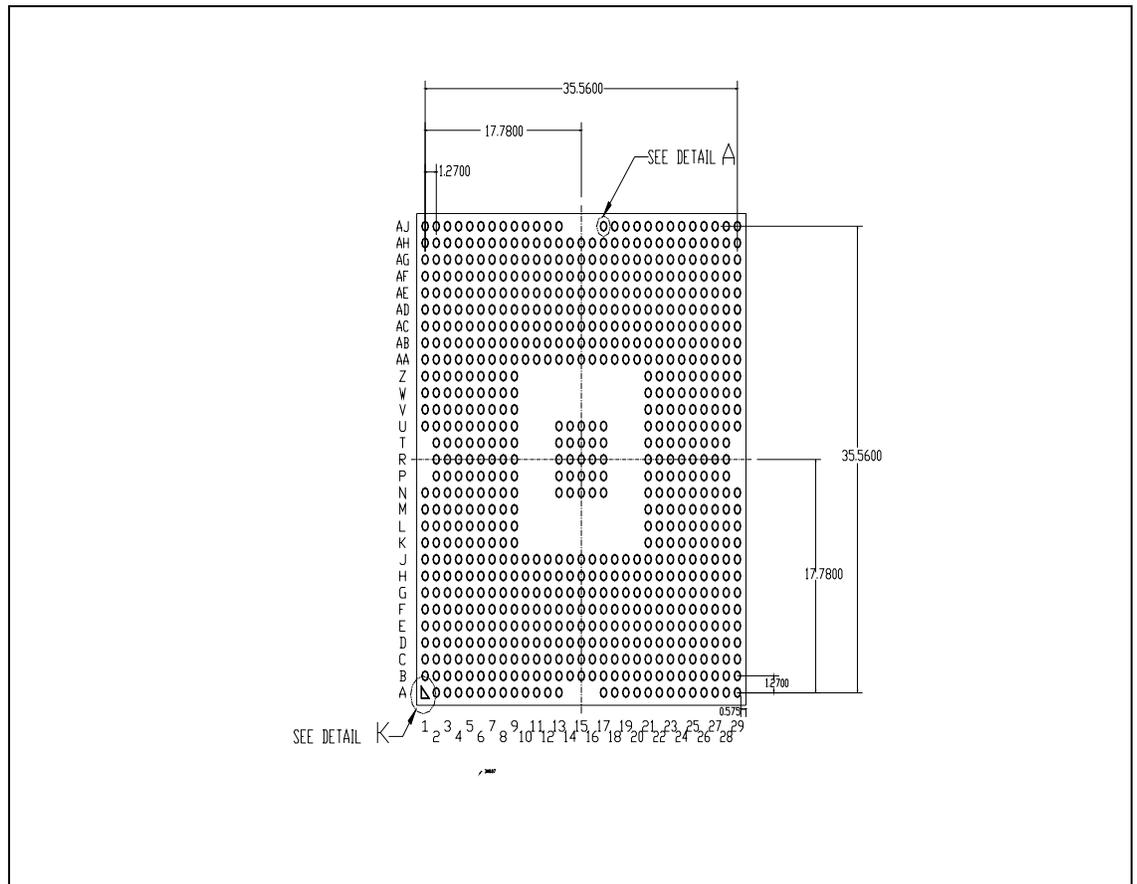


Figure 14. Intel 852GM/852GMV GMCH Micro-FCBGA Package Dimensions (Bottom View)





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