ABHiQV

for B65555 & B69000

(Fab. Revision C)

HiQVideo™ Series ABHiQV Daughtercard (Fab. Rev. C) User's Guide

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Revision History

Revision	Date	By	Comment
0.1	9/15/97	RG/lnc	Internal draft (first Frame document)
1.0	10/22/97	RG/lnc	Initial Release
1.1	6/22/98	RG/lnc	Amended to highlight B65555 and B69000 Delete reference to 65560 Fab Rev. C

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HiQVideo™ Series ABHiQV Daughtercard (Fab. Rev. C) PCB Design Documentation

1.0 Product Description

The ABHiQV daughtercard is capable of being used with the B65555 and B69000 graphics controllers. The B65555 is designed to be used with EDO DRAM whereas the B69000 has 2MB of SDRAM embedded within the controller and does not use external DRAM components. Both combinations of controller and memory can be accommodated by the ABHiQV daughtercard.

The design kits for these products in the PCI bus environment all use a common board known as the DKHIQV-PCI Board. The ABHiQV daughtercard containing HiQVideo Controller is installed onto the DKHiQV-PCI board to complete the design kit. This User's Guide describes the ABHiQV (Fab. Rev. C) daughtercard.

2.0 Daughtercard Features

- Works with the DKHiQV-PCI DK board
- EDO memory support
- On-board 3.3V 64Kx8 DIP-socketed BIOS
- 8-position DIP switch used to latch configuration bits at power-on
- All voltage sources are 3.3V
- Supports test mode control for the B69000
- Support for two external oscillators for MCLK and DCLK
- Filtered memory power
- On-card test points
- Reset strapping option for AA6 (see Table 7)

3.0 Installation

3.1 General Overview of the Setup Process

The ABHiQV daughtercard is normally shipped with a VGA BIOS EPROM already installed (U2; refer to Figure 1). This BIOS has been programmed to support a limited set of resolutions and is intended primarily to allow a CRT monitor to display the system status as the system boots up.

To set the VGA BIOS and drivers for a specific flat panel, the user must use the CHIPS BIOS Modification Program (BMP) to configure the VGA BIOS (usually a RAM-loadable BIOS) to match the specifications of the panel. Refer to the corresponding CHIPS BIOS and driver user's manual for details of how to use the BMP. There is no need to remove or modify the pre-installed VGA BIOS EPROM when using a RAM-loadable BIOS.

It should be verified that the DK board works correctly with a CRT interface using the pre-installed VGA BIOS ROM before attempting to install a flat panel.

3.2 Installation Procedure

1. Unpack the ABHiQV (Fab Rev. C) daughtercard and visually inspect for any damage that may have occurred during shipping.
2. Read this ABHiQV (Fab Rev. C) daughtercard User’s Guide to become familiar with the board operations.
3. Read the DKHiQV-PCI User’s Guide to become familiar with the board operations.
4. Read the MM6555x (Fab. Rev. C) Multimedia Daughtercard User’s Guide to become familiar with board operations.
5. Read the datasheet applicable to the graphics controller being used.
6. Verify the appropriate settings for the DKHiQV-PCI board and the ABHiQV (Fab Rev. C) daughtercard as shown in tables one through six. Refer to Figures 1and 3 for jumper locations.
   Caution: Check to ensure all voltage sources are set to 3.3V (consult the DKHiQV-PCI schematics).
   Note: For TV-out and multimedia settings, refer to Tables 5 and 6.
7. Plug the ABHiQV (Fab Rev. C) daughtercard onto the DKHiQV-PCI board. The connectors/header in the ABHiQV daughtercard is composed of eight 2X16 header-socket-type pins (P1).
8. Power down the host system and plug the DKHiQV-PCI board into an available PCI slot on the motherboard.
9. Connect the monitor to the 15-pin VGA connector. The default configuration of the DK board is for CRT display.
10. Turn on the system and observe the sign-on message. The sign-on message does not appear, turn off the system and follow the instructions in the troubleshooting section.
11. Load the proper driver, BIOS and utilities to activate the ABHiQV daughtercard.

Table 1: DKHiQV-PCI (Rev. A) Board Configuration Settings For B69000, TV Out And Multimedia Disabled

Note: Refer to Figure 3 for jumper locations.

Jumper	Function*	State**	Jumper	Function*	State**
W1	sh.2, STANDBY	off	W33	sh.4, BVCC55X	2-3
W2	sh.5, TV out	off	W34	sh.4, XVCC55X	2-3
W3	sh.2, 14MHz	off	W35	sh.4, 3VMAIN	1-2
W4	sh.5, TV out	1-2	W36	sh.2, CVCC	1-2
W5	sh.2, TV out	1-2	W37	sh.5, M/PCLK	2-3
W6	sh.5, TV out	off	W38	sh.5, Panel V_{DD}	2-3
W7	sh.5, DDC pull up	2-3	W39	sh.5, VEESAFE by R82	off
W8	sh.2, TV out	off	W40	sh.2, int #	on
W9	sh.2, GVCC	2-3	JP1	sh.5, CRTdrive	off
W10	sh.3, PCI	on	JP2	sh.5, CRTdrive	off
W11	sh.3, PCI	off	JP3	sh.5, CRTdrive	off
W12	sh.5, VEESAFE	off	JP4	sh.5, Panel VCC	off
W13	sh.5, VEESAFE	off	JP5	sh.2, I2C	All off
W14	sh.5, VEESAFE	on	JP6	sh.2, I2C	All off
W15	sh.5,VDDSAFE	on	JP7	sh.2, DDC	1-2 & 3-4
W16	sh.5,VDDSAFE	off	JP8	sh.2, DDC	All off
W17	sh.5,VDDSAFE	off	JP9	sh.2, GPIO	All off
W18	sh.5, +12SAVE	off	JP10	sh.2, GPIO	1-4 & 2-3
W19	sh.5, +12SAVE	on	JP11	sh.2, GPIO	1-4 & 2-3
W20	sh.5, +12SAVE	off	JP12	sh.2, GPIO	3-4
W21	sh.5, VEESAFE	all off	JP13	sh.2, CSYNC/HSYNC	off
W23	sh.4, 3VREG2	off	JP15	sh.2, P34	on
W24	sh.4, PVCC/SVCC	2-3	JP16	sh.2, P35	on
W25	sh.4, PVCC/SVCC	2-3	JP17	sh.2, P32	on
W26	sh.4, OCSVCC	1-2	JP18	sh.2, P30	on
W27	sh.4, AVCC55X	2-3	JP19	sh.2, P33	on
W28	sh.4, IVCC55X	2-3	JP20	sh.2, P31	on
W29	sh.4, IVCC55X	2-3	R59	sh.5, VEESAFE	Note (1)
W30	sh.4, DVCC55X	2-3	R75	sh.4, 3VREG2	Note (2)
W31	sh.4, MVCC55X	2-3	R76	sh.4, 3VMAIN	Note (3)
W32	sh.4, RAMVCC	2-3	R82	sh. 5, VEESAFE	Note (4)

Notes: ***Schematic reference and functional category
****'on' - jumper plug is installed
'off' - jumper plug is not installed
1. Set potentiometer R59 for panel requirements.
2. Set potentiometer R75 for 3.3V on W24, pin 3.
3. Set potentiometer R76 for 3.3V on W25, pin 3.
4. Set potentiometer R82 for panel requirements.

Table 2: ABHiQV (Fab. Rev. C) Daughtercard Configuration Settings for B69000, TV Out And Multimedia Disabled

Note: Refer to Figure 1 for jumper locations.

Jumper	Function*	State**
W1	sh.1, EXT CLK	off
W2	sh.1, BVCC55X	off
W3	sh.1, ACTI/ENABLK	off
W4	sh.1, TMD 0	off
W5	sh.1, TMD1	off
W6	sh.2, MVCC55X	1-2
Switch Position	**Function***	**State****
S1[1]	sh.1, CFG 15	off
S1[2]	sh.1, PID 3	off
S1[3]	sh.1, PID 2	off
S1[4]	sh.1, PID 1	off
S1[5]	sh.1, PID 0	off
S1[6]	sh.1, PCI	off
S1[7]	sh.1, CLK - TST	off
S1[8]	sh.1, CFG 9	off

Notes: ***** Schematic reference and functional category
****** 'on' - jumper plug is installed
'off' - jumper plug is not installed

Table 3: DKHiQV-PCI board (Rev. A) Configuration Settings for B65555, TV out and multimedia disabled

Note: Refer to Figure 3 for jumper locations**.**

Jumper	Function*	State**	Jumper	Function*	State**
W1	sh.2, STANDBY	off	W33	sh.4, BVCC55X	2-3
W2	sh.5, TV out	off	W34	sh.4, XVCC55X	2-3
W3	sh.2, 14MHz	off	W35	sh.4, 3VMAIN	1-2
W4	sh.5, TV out	1-2	W36	sh.2, CVCC	1-2
W5	sh.2, TV out	1-2	W37	sh.5, M/PCLK	2-3
W6	sh.5, TV out	off	W38	sh.5, Panel V_{DD}	2-3
W7	sh.5, DDC pull up	2-3	W39	sh.5, VEESAFE by R82	off
W8	sh.2, TV out	off	W40	sh.2, interrupt	on
W9	sh.2, GVCC	2-3	JP1	sh.5, CRTdrive	off
W10	sh.3, PCI	on	JP2	sh.5, CRTdrive	off
W11	sh.3, PCI	off	JP3	sh.5, CRTdrive	off
W12	sh.5, VEESAFE	off	JP4	sh.5, Panel V_{CC}	off
W13	sh.5, VEESAFE	off	JP5	sh.2, I2C	All off
W14	sh.5, VEESAFE	on	JP6	sh.2, I2C	All off
W15	sh.5,VDDSAFE	on	JP7	sh.2, DDC	1-2 & 3-4
W16	sh.5,VDDSAFE	off	JP8	sh.2, DDC	All off
W17	sh.5,VDDSAFE	off	JP9	sh.2, GPIO	All off
W18	sh.5, +12SAVE	off	JP10	sh.2, GPIO	1-4 & 2-3
W19	sh.5, +12SAVE	on	JP11	sh.2, GPIO	1-4 & 2-3
W20	sh.5, +12SAVE	off	JP12	sh.2, GPIO	3-4
W21	sh.5, VEESAFE	All off	JP13	sh.2, CSYNC/HSYNC	off
W23	sh.4, 3VREG2	off	JP15	sh.2, P34	on
W24	sh.4, PVCC/SVCC	2-3	JP16	sh.2, P35	on
W25	sh.4, PVCC/SVCC	2-3	JP17	sh.2, P32	on
W26	sh.4, OCSVCC	1-2	JP18	sh.2, P30	on
W27	sh.4, AVCC55X	2-3	JP19	sh.2, P33	on
W28	sh.4, IVCC55X	2-3	JP20	sh.2, P31	on
W29	sh.4, IVCC55X	2-3	R59	sh.5, VEESAFE	Note (1)
W30	sh.4, DVCC55X	2-3	R75	sh.4, 3VREG2	Note (2)
W31	sh.4, MVCC55X	2-3	R76	sh.4, 3VMAIN	Note (3)
W32	sh.4, RAMVCC	2-3	R82	sh. 5, VEESAFE	Note (4)

Notes: *****Schematic reference and functional category

******'on' - jumper plug is installed
'off' - jumper plug is not installed

1. Set potentiometer R59 for panel requirements.
2. Set potentiometer R75 for 3.3V on W24, pin 3.
3. Set potentiometer R76 for 3.3V on W25, pin 3.
4. Set potentiometer R82 for panel requirements.

Table 4: ABHiQV (Fab. Rev. C) Daughtercard Configuration Settings for B65555, TV out and Multimedia Disabled

Note: Refer to Figure 1 for jumper locations

Jumper	Function*	State**
W1	sh.1, EXT CLK	off
W2	sh.1, BVCC55X	off
W3	sh.1, ACTI/ENABLK	off
W4	sh.1, TMD 0	off
W5	sh.1, TMD1	off
W6	sh.2, MVCC55X	2-3
Switch Position	**Function***	**State****
S1[1]	sh.1, CFG 15	off
S1[2]	sh.1, PID 3	off
S1[3]	sh.1, PID 2	off
S1[4]	sh.1, PID 1	off
S1[5]	sh.1, PID 0	off
S1[6]	sh.1, PCI	off
S1[7]	sh.1, CLK - TST	off
S1[8]	sh.1, CFG 9	off

Notes: ***Schematic reference and functional category
****'on' - jumper plug is installed
'off' - jumper plug is not installed

Table 5: DKHiQV-PCI Jumper configuration settings for TV-out Enabled on B69000 and B65555

Note: Refer to Figure 3 for jumper locations.

Jumper	NTSC[2] Function*	State**	Jumper	PAL[1,2] Function*	State**
W2	sh. 5, TV OUT	off	W2	sh.5, TV OUT	Off
W4	sh.5, TV OUT	1-2	W4	sh.5, TV OUT	2-3
W5	sh.2, TV OUT, disable CRT	off	W5	sh.5, TV OUT, disable CRT	Off
W6	sh.5, TV OUT, NTSC	off	W6	sh.5, TV OUT, PAL	On
W8	sh.2, TV OUT, TSYNC	off	W8	sh.2, TV OUT, TSYNC	Off
JP1	sh.5, TV OUT	On	JP1	sh.5, TV OUT	On
JP2	sh.5, TV OUT	On	JP2	sh.5, TV OUT	On
JP3	sh.5, TV OUT	On	JP3	sh.5, TV OUT	On
JP13	sh.2, CSYNC/HSYNC	On	JP13	sh.2, CSYNC/HSYNC	On

Notes: ***Schematic reference and functional category
******'on' - jumper plug is installed
'off - jumper plug is not installed

1. For PAL, U1/U4 on DKHiQV-PCI DK board must be replaced with a 17.7344 MHz crystal oscillator.
2. Using BMP utility, change RAM BIOS to enable TV through GPIO0 and enable output composite sync in NTSC/PAL.

Table 6: DKHiQV-PCI Jumper configuration settings for Multimedia Enabled on B69000 and B65555

Note: Refer to Figure 3 for jumper locations.

Jumper	Function*	State**
JP5	sh.2, I2C	1-2, 3-4
JP6	sh.2, I2C	All off
JP7	sh.2, DDC	1-2, 3-4
JP8	sh.2, DDC	All off
JP9	sh.2, GPIO	2-3
JP10	sh.2, GPIO	1-4
JP11	sh.2, GPIO	1-4, 2-3
JP12	sh.2, GPIO	off

Notes: ***Schematic reference and functional category
******'on' - jumper plug is installed
'off' - jumper plug is not installed

4.0 ABHiQV (Fab Rev. C) Configuration Components

Figure 1 shows the location of the components used to configure the ABHiQV (Fab Rev. CFab Rev. C) daughtercard.

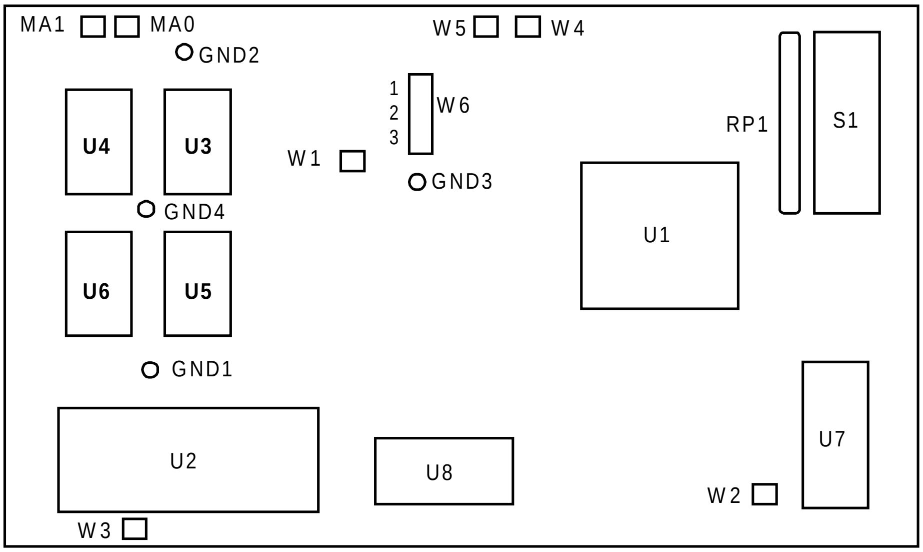

Figure 1 Component Location (front view)

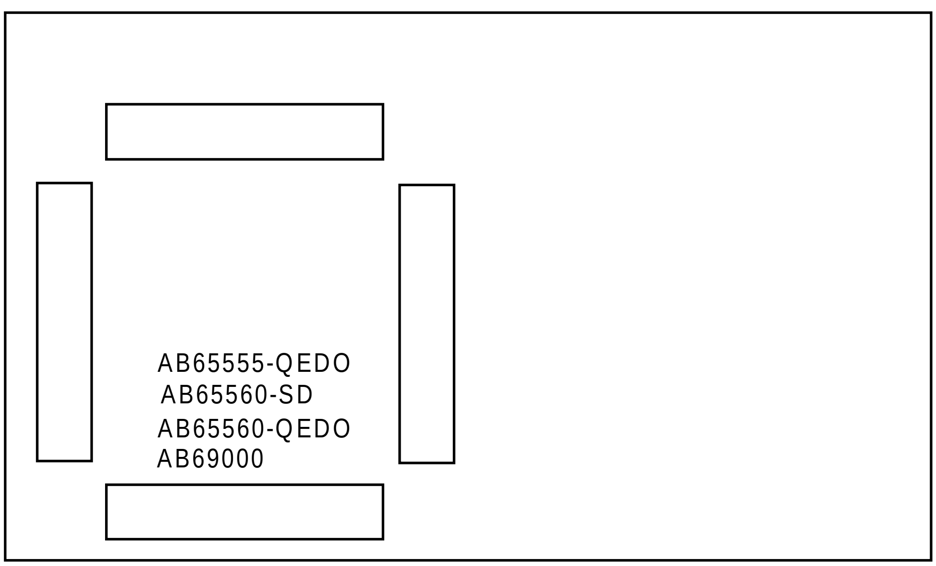

Figure 2 Component Location (Rear View)

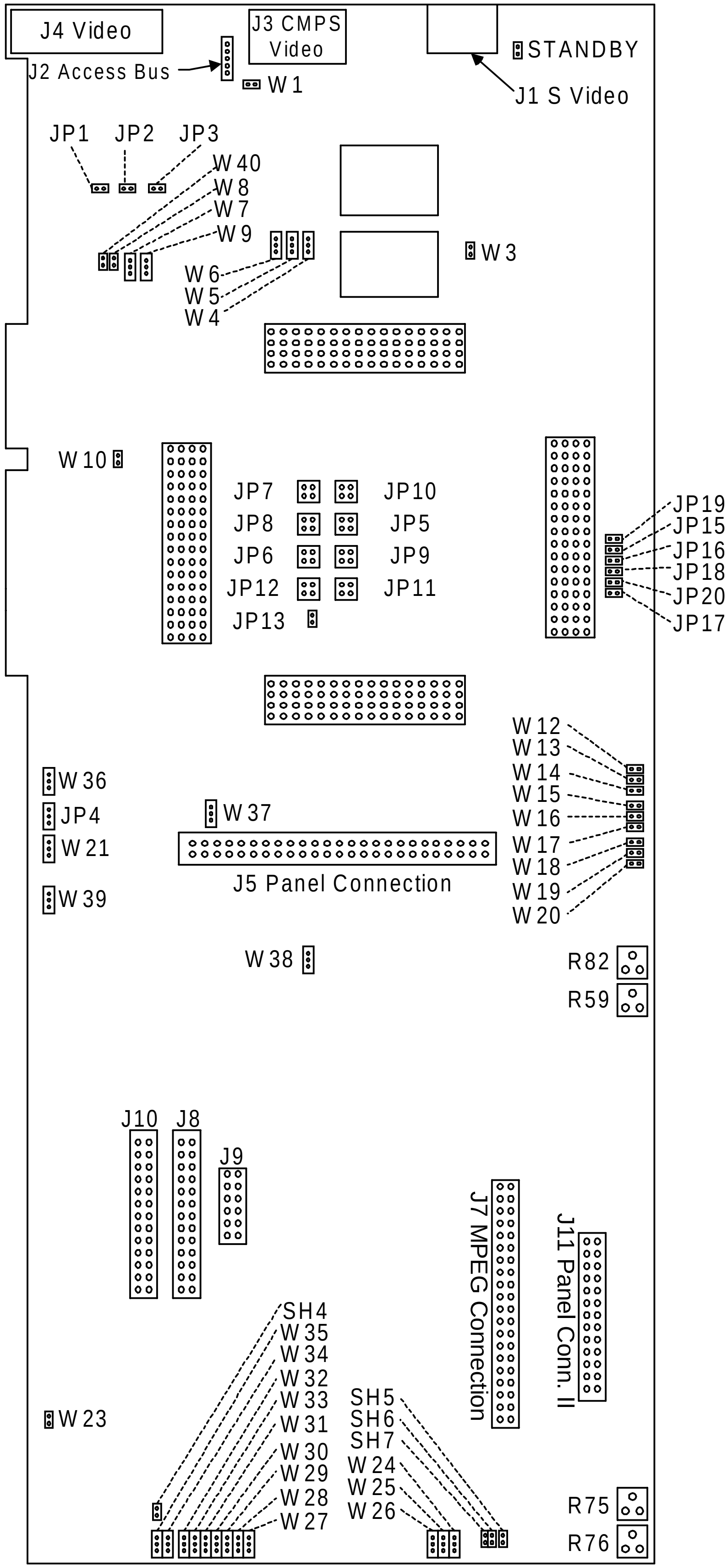

Figure 3 DKHiQV-PCI (Rev. A) Board Jumper Location

4.1 Configuration Switch (S1) and Jumpers (W1 and W3)

The ABHiQV provides one on-board Dip Switch S1 and two jumpers W1 and W2 for various configuration settings.

There are three configuration bits (CFG7,4,1) which are latched from AA7,4,1 on reset. CFG7,4,1 are written into the HiQVideo™ controller extended register XR70[7:0].

Four additional configuration bits, CGF14:11 are latched into XR71[6:3] from MAD[6:3] on reset. The software reserves these configuration bits for input of panel IDs. They correspond to DIP switch S1 positions 5:2 on the ABHiQV daughtercard.

All CFG pins have internal weak pull up and may be pulled down by 4.7k resistors on the daughtercard if the DIP switches are set to ON. Table 7 summarizes all the CFG bits and corresponding DIP switches and jumpers W1 and W3.

Table 7: Configuration Settings

Bits	Latched From	Name	Purpose	XR Bits	Daughtercard DIP Switch Position and Defaults
CFG0	AA0	Reserved		XR70[0]	
CFG1	AA1	PCI	VGA I/O Decoding Enable/ Disable on PCI bus	XR70[1]	S1[6]: open
CFG2	AA2	Reserved		XR70[2]	
CFG3	AA3	Reserved		XR70[3]	
CFG4	AA4	Ext. CLK	External OSC for MCLK and DCLK	XR70[4]	W1: open
CFG5	AA5	Reserved		XR70[5]	
CFG6	AA6	Reserved	ACTI/ENABKL	XR70[6]	W3: open
CFG7	AA7	CLK-TST	Internal clock test mode disable	XR70[7]	S1[7]: open
CFG8	AA8	Reserved		XR71[0]	
CFG10	MA 2	Reserved		XR71[2]	
CFG11	MA 3	PID0	Panel Type	XR71[3]	S1[5]: open
CFG12	MA 4	PID1	Panel Type	XR71[4]	S1[4]: open
CFG13	MA 5	PID2	Panel Type	XR71[5]	S1[3]: open
CFG14	MA 6	PID3	Panel Type	XR71[6]	S1[2]: open

Refer to the applicable databook for additional configuration options.

4.2 Top Assembly Check Boxes

The bottom side of the board is silk-screened with a list of possible 'top assemblies' for which the AB-HiQV daughtercard can be built. The list is the same as shown below (four possible top assembly versions). The intent is that when the daughtercard is built, a check mark will be placed in the box next to the appropriate top assembly version. For example, if a B65555 chip and EDO DRAM are soldered onto the board, the "AB65555-QEDO" box will have a check mark placed in it.

The complete list of possible usages of the ABHiQV daughtercard is as follows:

AB65555-QEDO	(B65555 with PQFP EDO DRAM*)
AB69000	(B69000 with no external DRAM)

* 'QEDO' refers to EDO DRAM in the PQFP package footprint.

4.3 W1 Jumper

Jumper W1 provides a convenient reset strapping option for AA4 (see Table 7):

W1 closed	External OSC for MCLK and DCLK option set low at reset
W1 open	External OSC for MCLK and DCLK option set high at reset

4.4 W2 Jumper

Jumper W2 governs the source of the external oscillator supply voltage:

W2 closed	BVCC55X supplies voltage for external oscillator for MCLK and DCLK
W2 open	no supply voltage for external oscillator

4.5 W3 Jumper

Jumper W3 provides a convenient reset strapping option for AA6 (see Table 7):

W3 open	ACTI/ENABKL option set high at reset
W3 closed	ACTI/ENABKL option set low at reset

4.6 W4 and W5 Test Configuration Jumpers

Jumpers W4 and W5 control the test mode inputs on the B69000:

W4	TMD0	(open for normal operation)
W5	TMD1	(open for normal operation)

4.7 W6 Jumper

Jumper W6 selects filtered MVCC for B69000 memory power. On non-B69000 daughtercards this filter is used for the SDRAM/EDO chips. The jumper allows the filter to be used for the internal memory power of the B69000 instead of external memory, since the memory is internal in the case of the B69000:

W6 = 1 - 2 MVCC55X for B69000 is a filtered version of RAMVCC on the DKHiQV-PCI DK board
W6 = 2 - 3 MVCC55X for non-B69000 is directly from MVCC55X on the DKHiQV-PCI DK board

4.8 Miscellaneous

The daughtercard provides support for the MA0 and MA1 on-card test points.

5.0 DKHiQV-PCI DK Board Configuration Components

Figure 3 shows the location of the components used to configure the DKHiQV-PCI board. Refer to the DKHiQV-PCI user's guide for detailed operation.

6.0 Operation

The HiQVideo LCD/CRT controllers (B65555 & B69000) provide low power, high performance and minimal component video subsystem solutions. The DKHiQV-PCI and ABHiQV evaluation boards are video adapter cards that implement the HiQVideo controller for PC bus operation. Since the B65555 & B69000 are 3.3V technology, the default setting for all VCC jumpers is the 3.3V setting. In addition, the user may check for the power-down operation of the HiQVideo controller using a jumper (W1) on the DK board.

6.1 Memory Interface

The ABHiQV daughtercard is designed to support 256K x 32 EDO memory in the 100 pin PQFP mechanical package. Stuffing of various different ones of the resistors is used as a means of accommodating the few differences in pin assignment. See Tables 8-9 for EDO DRAM.

Table 8: Memory Interface Configuration

EDO CONFIGURATION	
R1	NC
R2	NC
R9	C
R14	NC
R15	NC
R16	NC
R17	NC
R18	C
R19	NC

Note: 'C' is connected and 'NC' is not connected.

The user can set the display memory type through XR41[0,1], memory size through XR42[2] and the DRAM data bus width through XR43[4,5] for the B65555. The table below show the possible configurations:

Table 9: EDO Memory Configuration Types for B65555

EDO				
SIZE	BANDWIDTH	ORGANIZATION	Qty. needed	Modules
2 MB	64-bit (single bank)	256Kx32	2	U3, U5
4 MB	64-bit (dual bank)	256Kx32	4	U3, U4, U5, U6

Note: XR41 = 01h for EDO memory, XR42 = 00h for 256-wide column and XR43 = 10h for 64-bit interface.

6.2 STN-DD Buffer

Dual-drive LCD panels require video data alternating between two separate locations in memory. In addition, a dual-drive panel requires data from both locations simultaneously. These operations require a frame storage area, called a 'STN-DD buffer'. The embedded STN-DD buffer may be enabled by setting FR1A[0]=1.

6.3 Clock

The ABHiQV daughtercard provides two on-board oscillators U7 and U8. These external oscillators can be used to provides DCLK and MCLK through pins TCLK and TDI respectively. By default, the graphics controller's internal synthesizers are used to generate the clock for DCLK and MCLK. The option of choosing external oscillators vs. internal clocks may be controlled by XRCF[1,2]=0,0. The default state of these bits reflects the state of pin AA4 (W1) during reset. It is recommended to leave W1 open and use XRCF register to select the external oscillators. The purpose of W1 is related to testing and verification. See XRCF register in the applicable databook for more detail. The value of the DCLK oscillator is up to the user to determine since it is based on panel resolution and other factors. Although oscillators of frequencies other than 14.318MHz may be used for MCLK, this is not recommended.

6.4 Utilities and Drivers

The SETCLK utility included in the utilities diskette independently programs MCLK and DCLK of the HiQVideo™ controller. The diskette normally shipped with the daughtercard also provides other utilities such as MODETEST. The MODETEST utility runs all the standard VGA modes and super VGA modes. The driver diskettes normally shipped with the daughtercard contain display drivers for various PC-based operating systems including WIN95 and WinNT. These drivers are downloadable from CHIPS' BBS, from which the utilities can also be obtained -- please contact your CHIPS representative for more information. These drivers are accompanied by text files to help you install them.

7.0 Troubleshooting

1. Check that the ABHiQV daughtercard and DKHiQV-PCI main board are properly connected together.
2. Ensure that 3.3V is set on DKHiQV-PCI main board.
3. Verify that all other parts of the computer system are functioning properly by testing a known working VGA board with the system.
4. Make sure the combination of the DKHiQV-PCI main board and ABHiQV daughtercard works before attaching the 65550 Multimedia daughtercard.
5. If the 65550 Multimedia Daughtercard still does not work with DKHiQV-PCI, contact your CHIPS representative.

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