Synertek.

SY6845E
CRT Controller

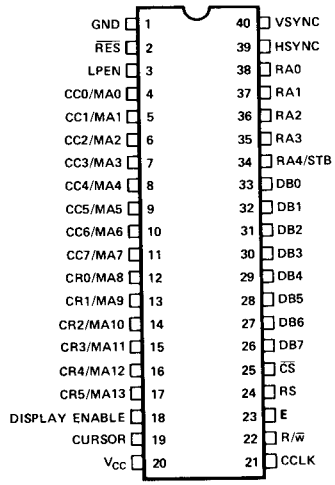
Features

- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required.
- Pin-compatible with MC6845R.
- Row/Column or straight-binary addressing for Video Display RAM.
- Video Display RAM may be configured as part of microprocessor memory field or independently slaved to 6845
- Internal status register.
- 3.7 MHz Character Clock
- Transparent Address Mode

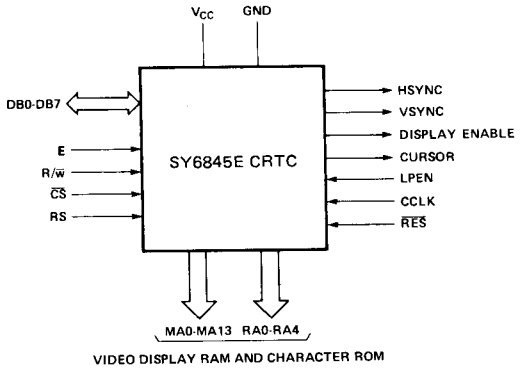
Description

The SY6845E is a CRT Controller intended to provide capability for interfacing any 8 or 16 bit microprocessor family to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

Pin Configuration



Interface Diagram



VIDEO DISPLAY RAM AND CHARACTER ROM

MICRO-PROCESSORS

Absolute Maximum Ratings*

Supply Voltage, V_{CC}	-0.3V to +7.0V
Input/Output Voltage, V_{IN}	-0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

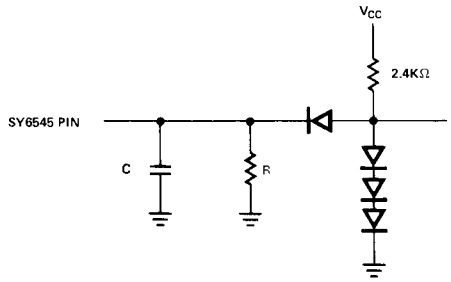
Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0–70° C, unless otherwise noted)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
I_{IN}	Input Leakage (ϕ2, R/W, RES, CS, RS, LPEN, CCLK)	—		2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	—		±10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = −205μA (DB0-DB7) I_{LOAD} = −100μA (all others)	2.4		—	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	—		0.4	V
P_D	Power Dissipation	—	325	650	mW
C_{IN}	Input Capacitance ϕ2, R/W, RES, CS, RS, LPEN, CCLK DB0-DB7	 — —		 10.0 12.5	 pF pF
C_{OUT}	Output Capacitance	—		10.0	pF

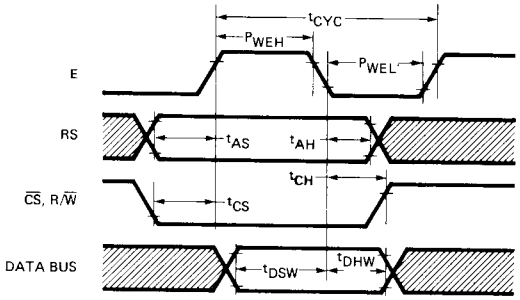
Test Load



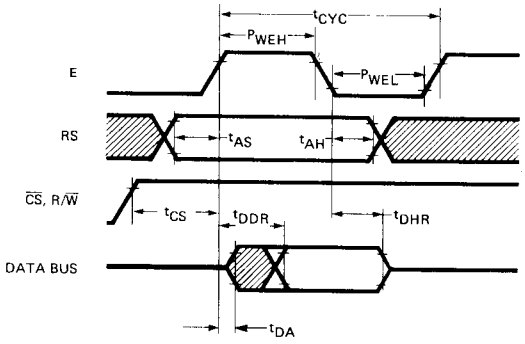
R = 11KΩ FOR DB_0-DB_7
R = 24KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR D_0-D_7
C = 30 pF ALL OTHER OUTPUTS

MPU Bus Interface Characteristics

WRITE CYCLE



READ CYCLE



Write Timing Characteristics (V_{CC} = 5.0V ±5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristic	SY6845E		SY6845EA		SY6845EB		SY6845EC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	0.33	—	0.25	—	μs
P_{WEH}	E Pulse Width, High	440	—	200	—	150	—	115	—	ns
P_{WEL}	E Pulse Width, Low	420	—	190	—	140	—	100	—	ns
t_{AS}	Address Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{AH}	Address Hold Time	0	—	0	—	0	—	0	—	ns
t_{CS}	R/W, CS Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{CH}	R/W, CS Hold Time	0	—	0	—	0	—	0	—	ns
t_{DSW}	Data Bus Set-Up Time	165	—	60	—	60	—	60	—	ns
t_{DHW}	Data Bus Hold Time	10	—	10	—	10	—	10	—	ns

(t_r and t_f = 10 to 30 ns)

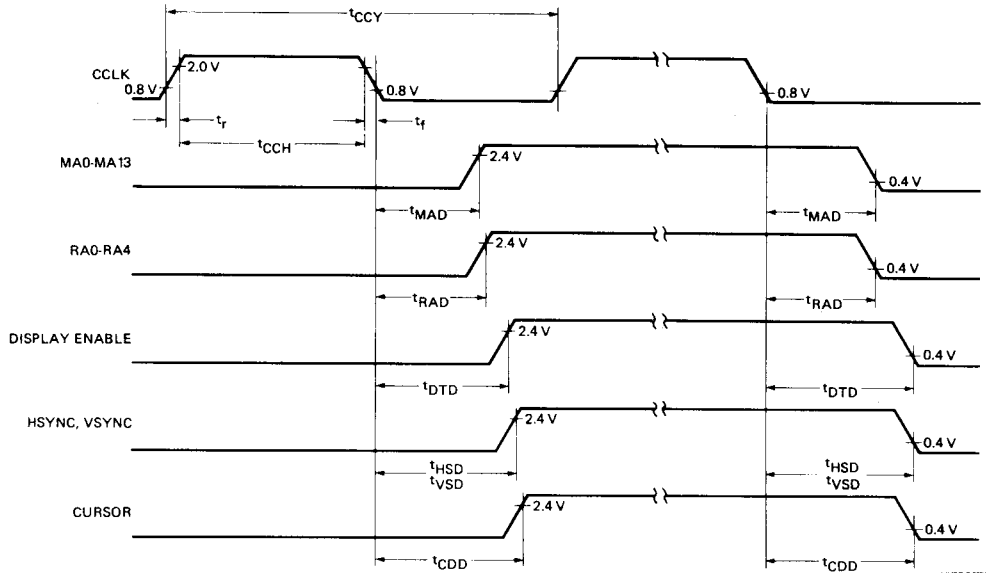
Read Timing Characteristics (V_{CC} = 5.0V ±5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristic	SY6845E		SY6845EA		SY6845EB		SY6845EC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	0.33	—	0.25	—	μs
P_{WEH}	ϕ2 Pulse Width, High	440	—	200	—	150	—	115	—	ns
P_{WEL}	ϕ2 Pulse Width, Low	420	—	190	—	140	—	100	—	ns
t_{AS}	Address Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{AH}	Address Hold Time	0	—	0	—	0	—	0	—	ns
t_{CS}	R/W, CS Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{DDR}	Read Access Time (Valid Data)	—	290	—	150	—	100	—	85	ns
t_{DHR}	Read Hold Time	10	—	10	—	10	—	10	—	ns
t_{DA}	Data Bus Active Time (Invalid Data)	20	60	20	60	20	60	20	60	ns
t_{TAD}	MA0–MA13 Switching Delay (Refer to Figure Trans. Addressing)	100 typ.	160	100 typ.	160	90 typ.	130	60 typ.	95	ns

(t_r and t_f = 10 to 30 ns)

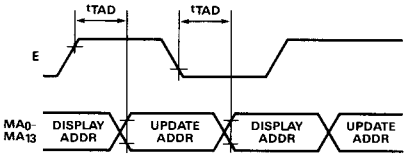
MICRO-PROCESSORS

Memory and Video Interface Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

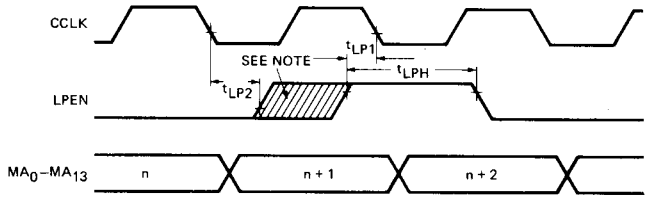


Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CCH}	Minimum Clock Pulse Width, High	130			ns
t_{CCY}	Clock Frequency			3.7	MHz
t_r, t_f	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	250	ns
t_{HSD}	Horizontal Sync Delay Time		160	250	ns
t_{VSD}	Vertical Sync Delay Time		160	250	ns
t_{CDD}	Cursor Display Timing Delay Time		160	250	ns

Transparent Addressing (Φ1/Φ2 Interleaving)



Light Pen Strobe Timing



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

Symbol	Characteristic	SY6845E		SY6845EA		SY6845EB		SY6845EC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Strobe Width	100	—	100	—	100	—	100	—	ns
t_{LP1}	LPEN to CCLK Delay	—	120	—	120	—	120	—	120	ns
t_{LP2}	CCLK to LPEN Delay	—	0	—	0	—	0	—	0	ns

t_r and t_f = 20ns (max.)

MPU Interface Signal Description

E (Enable)

The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the SY6845. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the SY6845 to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6845; a low on the R/$\overline{W}$ pin allows a write to the SY6845.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The SY6845 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6845. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

Video Interface Signal Description

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the SY6845 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

Memory Address Signal Description

MA0-MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

- Binary
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.
- Row/Column
  In this mode, MA0-MA7 function as column addresses CC0-CC7, and MA8-MA13, as row addresses CR0-CR5. In this case, the software may handle addresses in terms of row and column locations, but additional

address compression circuits are needed to convert CC0–CC7 and CR0–CR5 into a memory-efficient binary scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the SY6845 is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video Display RAM update address is gated on to the address lines, MA0–MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the SY6845 with only a small amount of external circuitry.

Description of Internal Registers

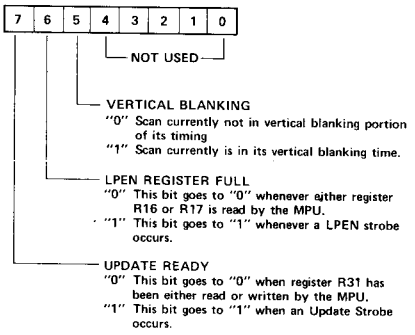
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various SY6845 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct SY6845 data transfers to and from the system MPU. Its contents is the number of the desired register (0–31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This 3-bit register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

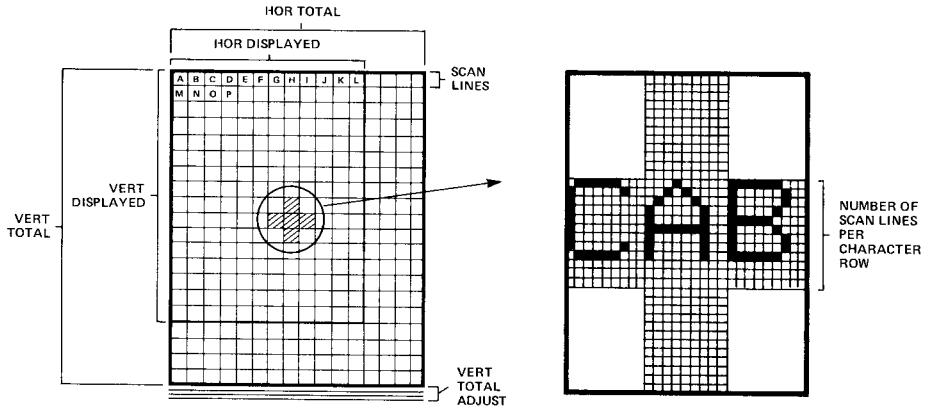


Figure 1. Video Display Format

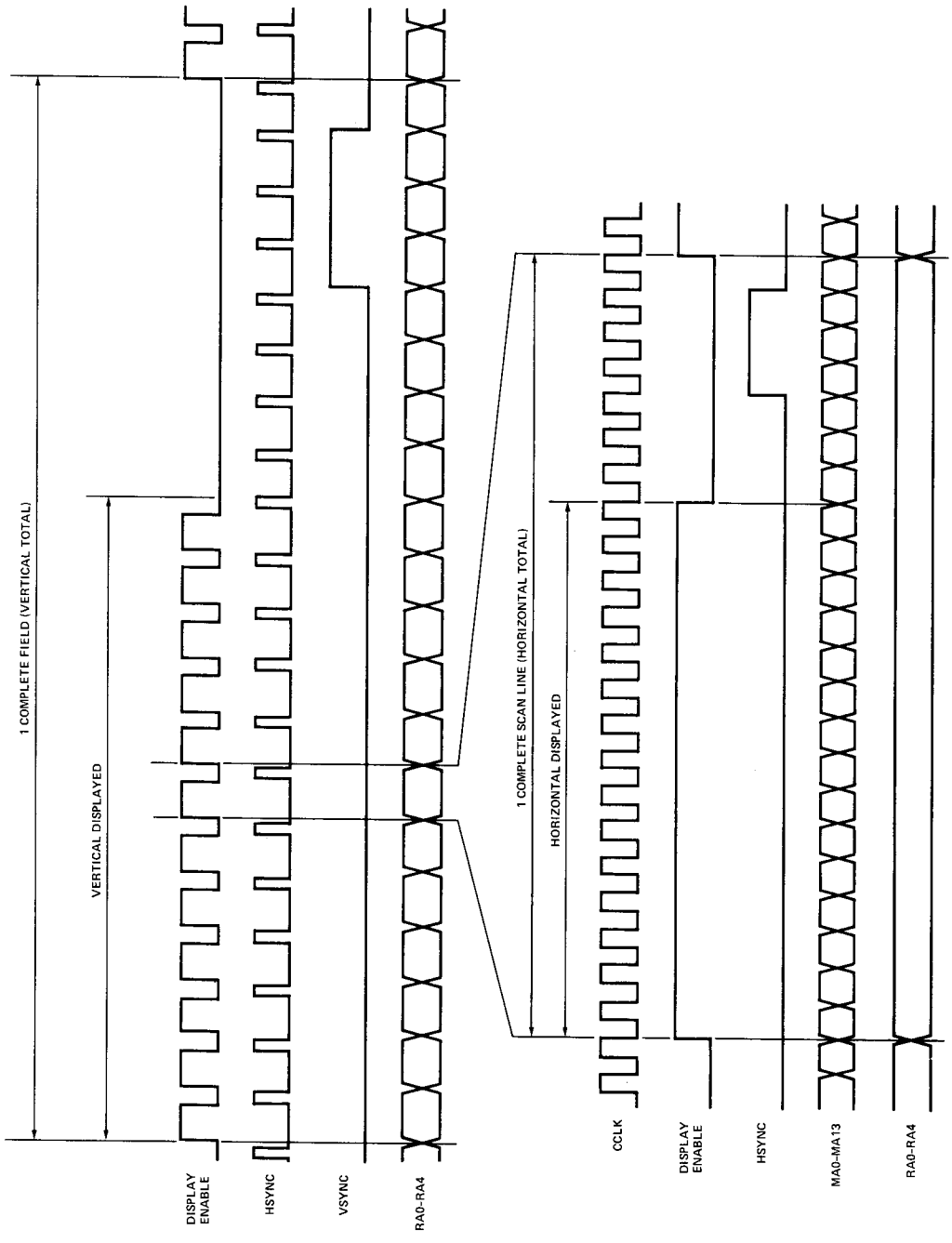
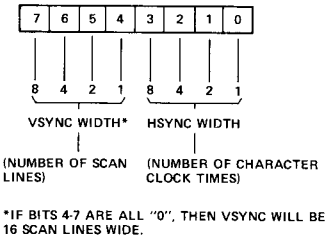


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Control of these parameters allows the SY6845 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

$\overline{CS}$	RS	Address Reg. 4	3	2	1	0	Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Reg.	Reg. No.		√				A_4	A_3	A_2	A_1	A_0
0	0	–	–	–	–	–	–	Status Reg.		√		U	L	V					
0	1	0	0	0	0	0	R0	Horiz. Total	# Charac. -1		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz. Displayed	= Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz. Sync Position	= Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	= Scan Lines and = Char. Times		√	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	= Charac. Row -1		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert. Total Adjust	= Scan Lines		√				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert. Displayed	= Charac. Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert. Sync Position	= Charac. Rows		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√	U_1	U_0	C	D	T	RC	I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	= Scan Lines -1		√				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)	Row		√			●	●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)	Col		√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)	Row	√	√			●	●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)	Col	√	√	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√				●	●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●
0	1	1	0	0	1	0	R18	Update Location (H)			√			●	●	●	●	●	●
0	1	1	0	0	1	1	R19	Update Location (L)			√	●	●	●	●	●	●	●	●
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: ● Designates binary bit

▨ Designates unused bit. Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = "1" which operates likewise.

Figure 3. Internal Register Summary

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

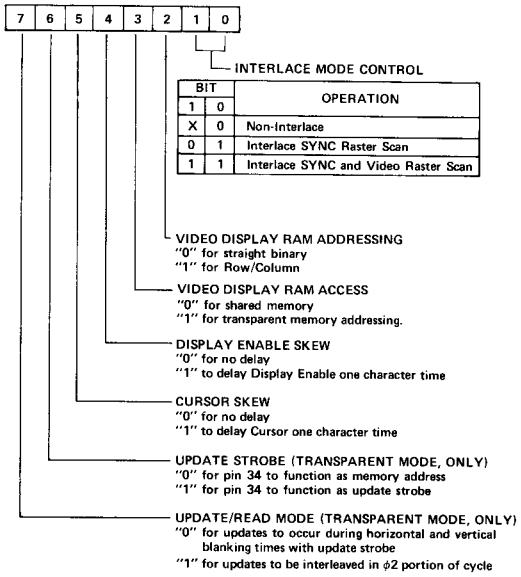
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the SY6845 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT 6	BIT 5	CURSOR MODE
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16x field rate (fast)
1	1	Blink at 32x field rate (slow)

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the SY6845 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

Description of Operation

Register Formats

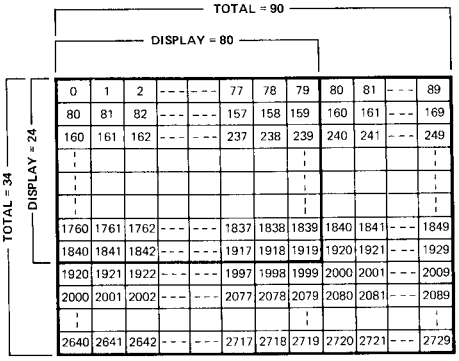
Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

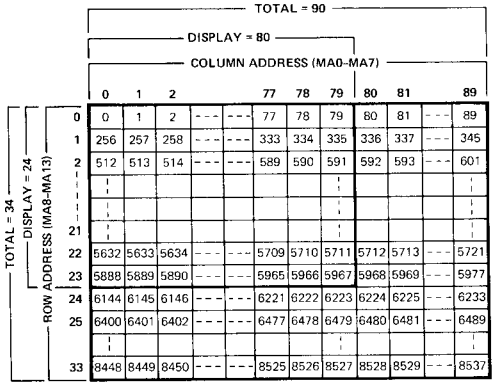
Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.



STRAIGHT BINARY ADDRESSING SEQUENCE



ROW/COLUMN ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

Video Display RAM Addressing

There are two modes of addressing for the video display memory:

1. Shared Memory
   In this mode the memory is shared between the MPU address bus and the SY6845 address bus. For this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the SY6845 must have access to the video display RAM and the contention circuits must resolve this multiple access requirement. Figure 5 illustrates the system configuration.
2. Transparent Memory Addressing
   For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the SY6845. All MPU accesses are made via the SY6845 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

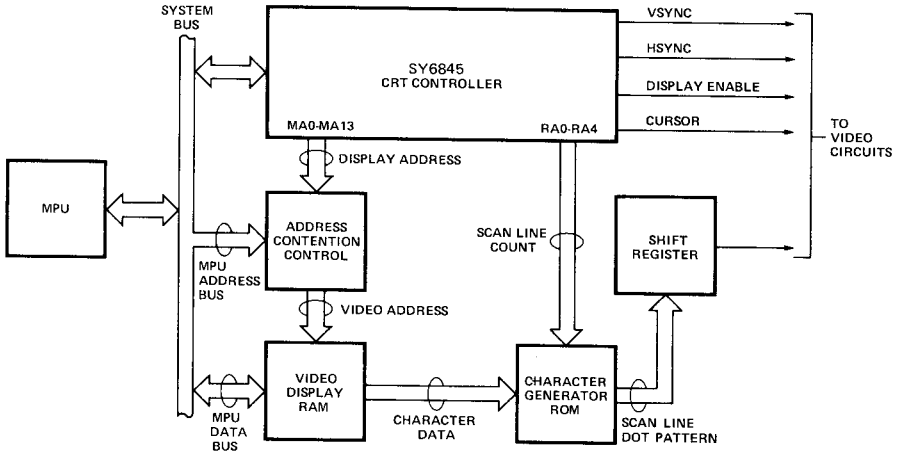


Figure 5. Shared Memory System Configuration

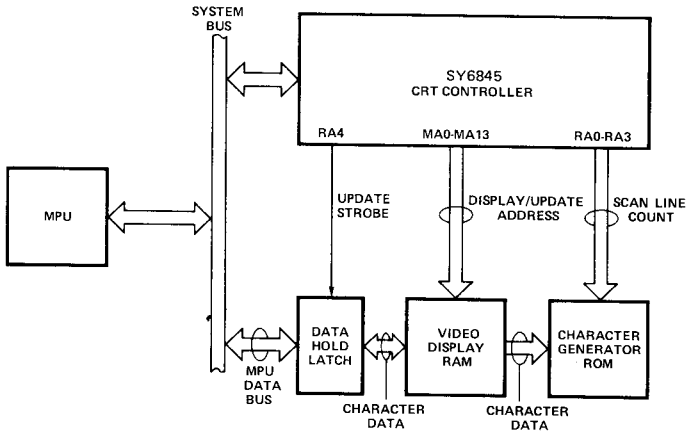


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch needed for Horizontal/Vertical Blanking updates, only).

MICRO-PROCESSORS

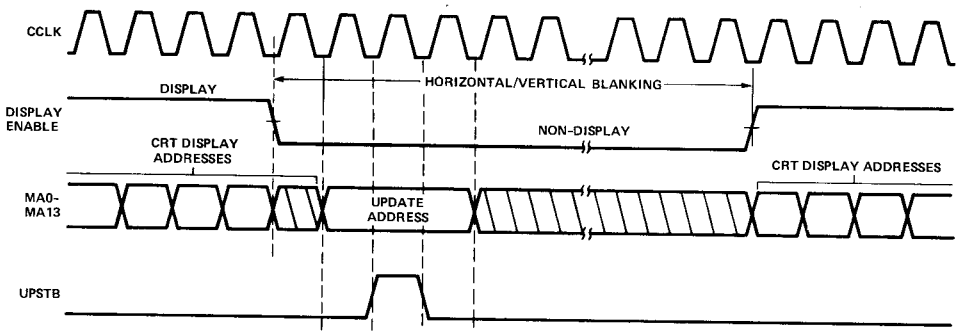


Figure 9. Retrace Update Timings

Interlace Modes

There are three raster-scan display modes (see Figure 10).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace-Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 11 and is the only difference in the SY6845 operation in this mode.

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlace-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered.

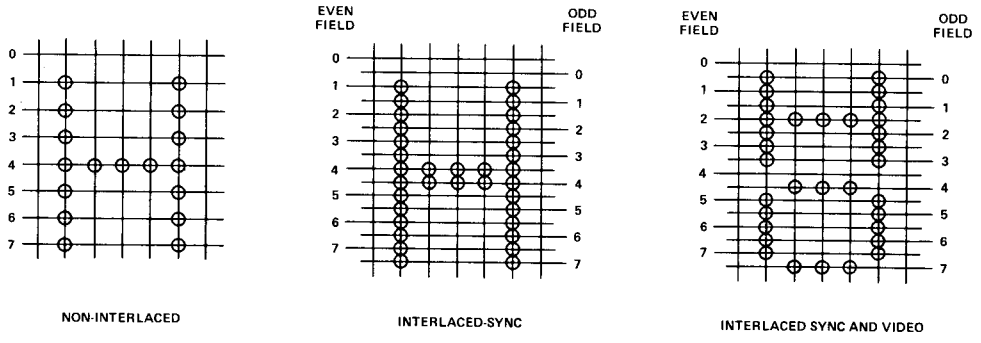
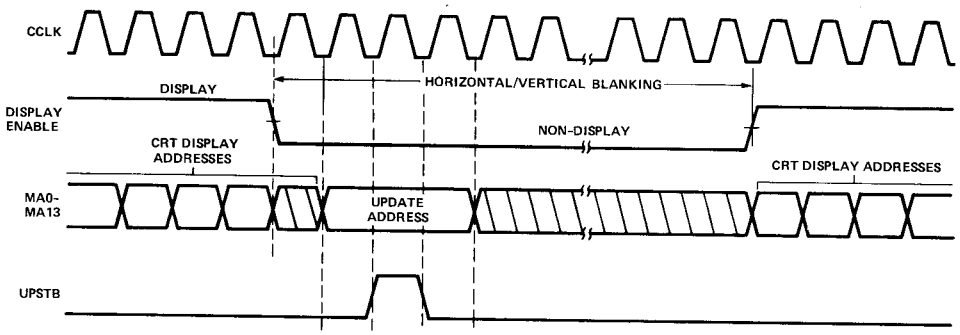


Figure 10. Comparison of Display Modes.



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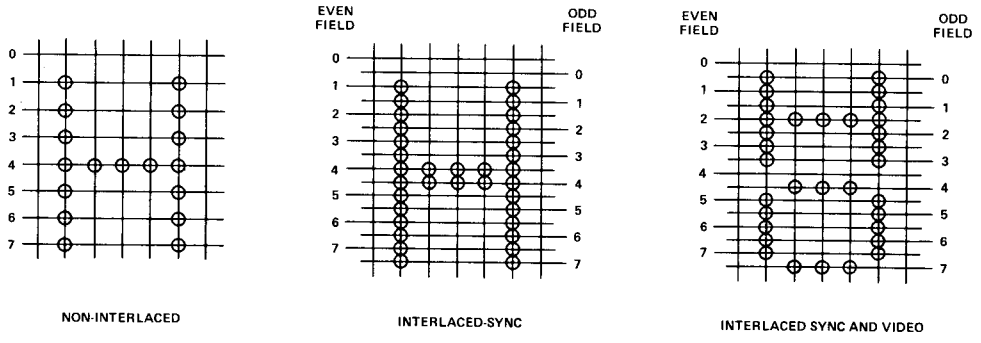

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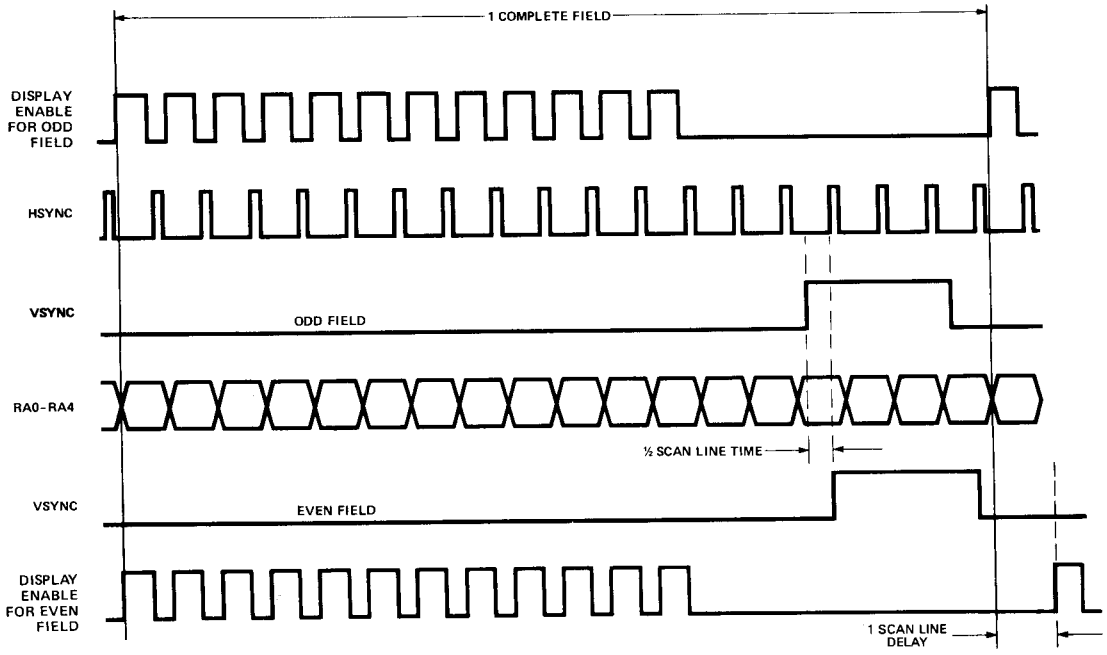

Figure 11. Interlace Sync Mode and Interlace Sync & Video Mode Timing

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effect of the delays.

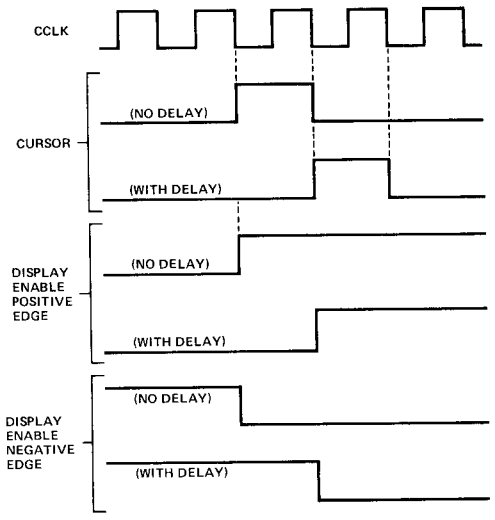

Figure 12. Cursor and Display Enable Skew

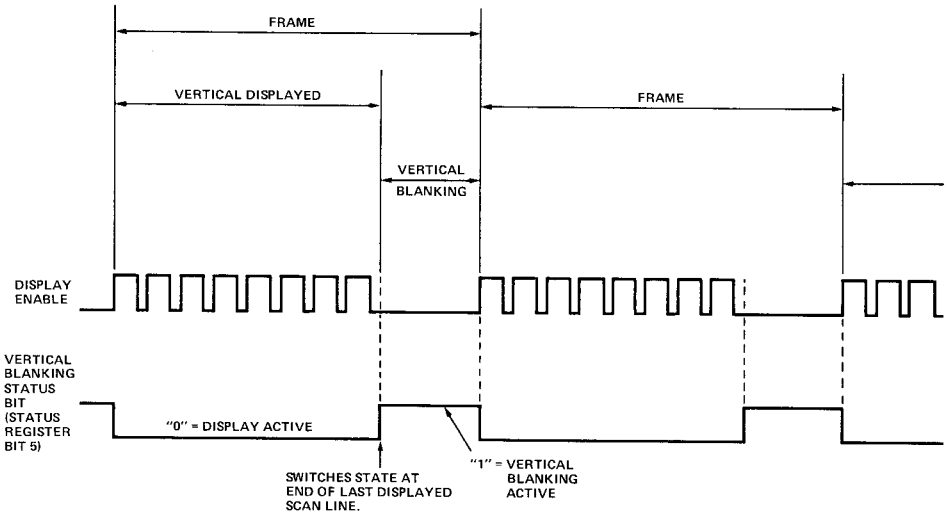

Figure 13. Operation of Vertical Blanking Status Bit

Package Availability

40 Pin Molded DIP

Ordering Information

Part Number	Package	CPU Clock Rate
SYP6845E	Molded DIP	1 MHz
SYP6845EA	Molded DIP	2 MHz
SYP6845EB	Molded DIP	3 MHz

Detailed help in Application Notes 7 and 8 available from Synertek sales offices.

MICRO-PROCESSORS

CRTC Register Comparison

NON-INTERLACE

REGISTER	SY6845R	MC6845R HD6845R	HD6845S	SY6545-1	SY6845E
R0 HORIZONTAL TOT	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R1 HORIZONTAL DISP	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R2 HORIZONTAL SYNC	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R3 HORIZONTAL AND VERT SYNC WIDTH	HORIZONTAL	HORIZONTAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL
R4 VERTICAL TOT	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R5 VERTICAL TOT ADJ	ANY VALUE	ANY VALUE	ANY VALUE	ANY VALUE EXCEPT R5 = (R9H) • X	ANY VALUE
R6 VERTICAL DISP	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4
R7 VERTICAL SYNC POS	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL-1
R8 MODE REG BITS 0 AND 1	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT
BITS 2	–	–	–	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING
BITS 3	–	–	–	SHARED OR TRANSPARENT ADDR	SHARED OR TRANSPARENT ADDR
BITS 4	–	–	DISPEN SKEW	DISPEN SKEW	DISPEN SKEW
BITS 5	–	–	DISPEN SKEW	CURSOR SKEW	CURSOR SKEW
BITS 6	–	–	CURSOR SKEW	RA4/UPSTB	RA4/UPSTB
BITS 7	–	–	CURSOR SKEW	TRANSPARENT MODE SELECT	TRANSPARENT MODE SELECT
R9 SCAN LINES	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R10 CURSOR START	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R11 CURSOR END	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R12/R13 DISP ADDR	WRITE ONLY	WRITE ONLY	READ/WRITE	WRITE ONLY	WRITE ONLY
R14/R15 CURSOR POS	READ/WRITE	WRITE ONLY	READ/WRITE	READ/WRITE	READ/WRITE
R16/R17 LPEN REG	READ ONLY	READ ONLY	READ ONLY	READ ONLY	READ ONLY
R18/R19 UPDATE ADDR REG	N/A	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
R31 DUMMY REG	N/A	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
STATUS REG	YES	NO	NO	YES	YES
INTERLACE SYNC					
R0	TOT-1 = ODD OR EVEN	TOT-1 = ODD	TOT-1 = ODD	TOT-1 = ODD	TOT-1 = ODD OR EVEN
INTERLACE SYNC AND VIDEO					
R4 VERTICAL	TOT-1	TOT-1	TOT-1	TOT/2-1	TOT-1
R6 VERT DISP	TOT	TOT/2	TOT	TOT/2	TOT
R7 VERT SYNC	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL/2	ACTUAL-1
R9 SCAN LINES	TOT-1 ODD/EVEN	TOT-1 ONLY EVEN	TOT-2 ODD/EVEN	TOT-1 ODD/EVEN	TOT-1 ODD/EVEN
R10 CURSOR START R11 CURSOR END	ODD/EVEN ODD/EVEN	BOTH ODD OR BOTH EVEN	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN
CCLK	2.5 MHz	2.5 MHz	3.7 MHz	2.5 MHz	3.7 MHz