

APPENDIX B

External Interfaces

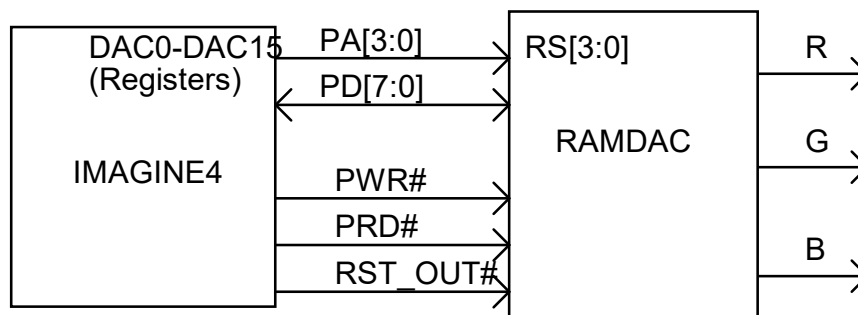
Appendix B: Peripheral Devices Interface

B.1 External RAMDAC

In addition to the 128 bit Display Buffer interface, IMAGINE 128 provides an additional 8 bit interface. The following devices can reside on the Interface:

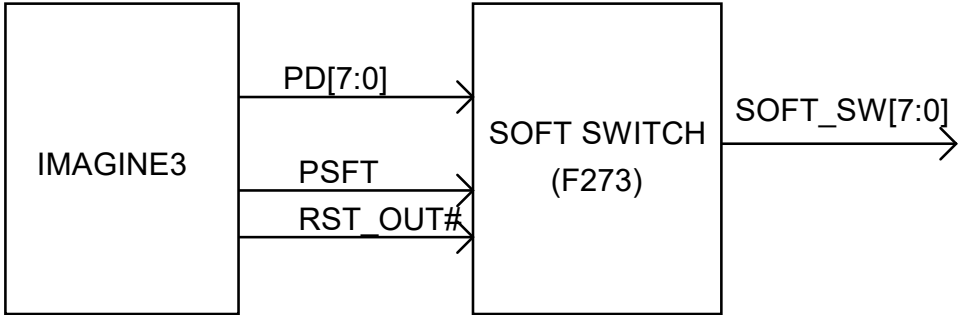
Device	Width	Function
RAM DAC	8	Output Stage
Soft Switches	8	Miscellaneous board functions (clock gen, LED)
PROM	8	VGA BIOS

This interface provides direct support for a high performance RAM DAC such as the IBM526. If the RAMDAC is VGA compatible, I/O locations x3C6, x3C7, x3C8, and x3C9 can be mapped to the RAMDAC. See the section on VGA DAC shadowing for more information. In high performance modes, up to sixteen RAMDAC registers are mapped into IMAGINE 128 memory space. If more than sixteen registers are required an external soft switch may be connected to the highest order register select line on the RAMDAC. The address and data lines for the DAC are supplied from the Peripheral Devices Interface. The RAMDAC data port is assumed to always be eight bits. The read and write control are provided from dedicated control pins. A typical RAMDAC connection is shown below. DAC wait states may be added via the DWS field in the CONFIG2 register.



B.2 Soft Switches

Up to 8 bits of external soft switch registers may be connected directly to the Peripheral Devices data bus (PD). The soft switches can be used to provide control for other board devices such as a frequency synthesizer, status indicator (LED), or any other device that requires software accessible control. The soft switch register is an I/O mapped device. The soft switch register is shadowed to an internal register that may be read at any time. On reset, the internal as well as external soft switch registers are initialized to 0.



B.3 EPROM

IMAGINE 128 can support an EPROM interface. To enable EPROM decode at boot, CP[29] needs to be strapped to a 1. The intended purpose of the EPROM is to provide the VGA BIOS if a VGA mode is enabled. The EPROM is mapped into PCI memory space by the EPROM Base Address Register in PCI configuration space. The amount of PCI memory space allocated to the EPROM is 64KB. When an EPROM read access is detected, IMAGINE 128 will return an entire dword of data regardless of the state of the byte enables. Flash EPROM may also be used. In this case, single byte writes to the EPROM are supported. EPROM wait states may be added via the EWS field in CONFIG2.

To connect an EPROM to IMAGINE 128, an F373 latch must be used to construct the full EPROM address. The latch is controlled by the PCS# signal which is also the chip select for the EPROM. One F373 latch along with the unlatched address provides a large enough address to access 64KB of EPROM. The OE and WE pins of the EPROM are connected as shown below.

