CHAPTER 9 ELECTRICAL DATA

9.1 DC SPECIFICATIONS

9.1.1 TA = 0° C TO 70° C, VDD = 5V +/- 5%, VSS = 0V

Symbol	Parameter	Min	Max	Unit	Condition	Notes
Voh	Output High Voltage	2.4		V	Ioh = 400 uA	
Vol	Output Low Voltage		0.4	V	Iol = 24 mA	1,2
Vol	Output Low Voltage		0.4	V	Iol = 8 mA	3
Vol	Output Low Voltage		0.4	V	Iol = 4 mA	4
Vol	Output Low Voltage		0.4	V	Iol = 2 mA	5
Vih	Input High Voltage	2	VCC+0.5	V	TTL	6
Vil	Input Low Voltage	-0.5	0.8	V	TTL	6
Vis	Schmitt Input Voltage	2.4	VCC+0.5	V	Schmitt	6
Vic	CMOS Input Voltage	3.8	VCC+0.5	V	CMOS	6
ILI	Input Leakage Current	-10	10	uA		
OLI	Output Leakage Current	-10	10	uA		
ICC	Operating Supply Current typical normal operation		350	mA		8
CI	Input Capacitance		8	pF		
CO	Output Capacitance		8	pF		
CIO	I/O Capacitance		8	pF		

9.1.2 TA = 0° C TO 70° C, VDD = 3.3V +/- 0.3V, VSS = 0V

Symbol	Parameter	Min	Max	Unit	Condition	Notes
Voh	Output High Voltage	2.4		V	Ioh = 400 uA	
Vol	Output Low Voltage		0.4	V	Iol = 24 mA	1,2
Vol	Output Low Voltage		0.4	V	Iol = 8 mA	3
Vol	Output Low Voltage		0.4	V	Iol = 4 mA	4
Vol	Output Low Voltage		0.4	V	Iol = 2 mA	5
Vih	Input High Voltage	2	VCC+0.3	V	TTL	6
Vil	Input Low Voltage	-0.3	0.8	V	TTL	7
Vis	Schmitt Input Voltage	2.4	VCC+0.5	V	Schmitt	6
Vic	CMOS Input Voltage	3.8	VCC+0.5	V	CMOS	6
ILI	Input Leakage Current	-3	3	uA		
OLI	Output Leakage Current	-3	3	uA		
ICC	Operating Supply Current typical normal operation		350	mA		8
CI	Input Capacitance		8	pF		
CO	Output Capacitance		8	pF		
CIO	I/O Capacitance		8	pF		

Notes: Other than Monitor interface, there are no DC requirements on the outputs. The other interfaces only have AC requirements.

1. Output Current (Iol) Capabilities:
   16mA: AD[31:0], BEN#[3:0]
2. Open Drain Outputs:
   16mA: CINT#
3. 8mA: HSYNC, VSYNC, RASL#, CASL#/WEL#, MA[7:0], CASU#/WEU#/MA[8], RASH#/MA[9], PAR, REQ#, SD[31:16], C/BE[3:0], FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, DCLK, PTSEL/BLANK#, IMD[15:0]
4. 4mA: P[23:16], SCL, SDA, SCL2, SDA2, WEA#/CASA#, WEB#/CASB#, WEC#/CASC#, WED#/CASD#, WEE#/CASE#, WEF#/CASF#, WEG#/CASG#, WEH#/CASH#
5. 2mA: ARD#, AWR#, BD[7:0], ARS[1:0], MD[63:0], ARLT1#, ARLT0#, ROMENL#/ARLT#, BLANK#, DE, MSW, TPD[23:0], DOTCLK
6. Input Structures:
   TTL: All inputs
   TTL w/pull-ups: ESYNC, EPDATA, EPCLK
7. Vil(min) = 1.5V AC (pulse width ≤ 5nS)
8. Normal operating ICC measured at 1024x768 @75Hz.

9.2 AC SPECIFICATIONS

All AC Timing Diagrams are strictly to show relative timing from one signal to the next. These diagrams are not necessarily logically correct or complete. For better understanding of logical cycles for PCI bus, please refer to the respective specifications.

The AC values are preliminary and subject to change.

9.2.1 PCI BUS TIMING

RESET TIMING

No	Symbol	Parameter	Min (MCLK)	Max (MCLK)	Load (pF)	Notes
RES1	tRESET#L	RESET# Low Time	1			
RES2	tMDV	MD Valid from RESET# Rising Edge		32		
RES3	tMDVH	MD Valid Hold Time	5			

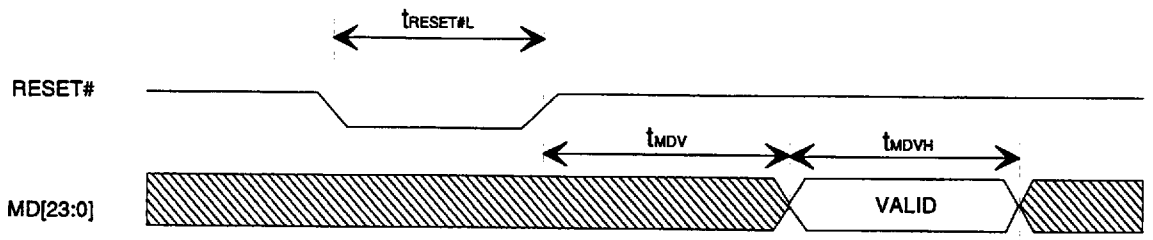


Figure 9.1 - Reset Timing

PCI BUS CLOCK REQUIREMENT

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI1	tPCKP	PCI Bus Clock Period	30			
PCI2	tPCKL	PCI Bus Clock Low Time	12			
PCI3	tPCKH	PCI Bus Clock High Time	12			

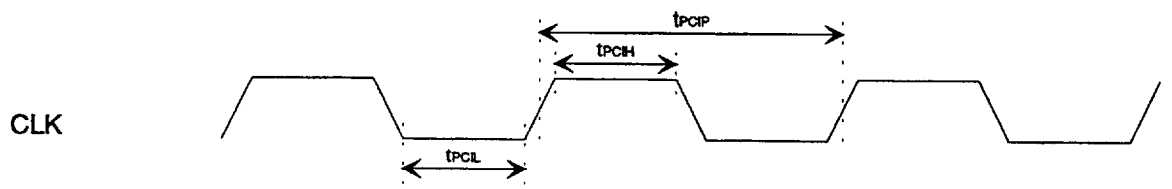


Figure 9.2 - PCI Bus Clock Requirement

PCI BUS TIMING (READ OPERATION)

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI4	tSPCI	Input Setup Time to CLK	7			
PCI5	tHPCI	Input Hold Time to CLK	0			
PCI6	tPPCI	Output Propagation Delay from CLK	2	11	0/50	1

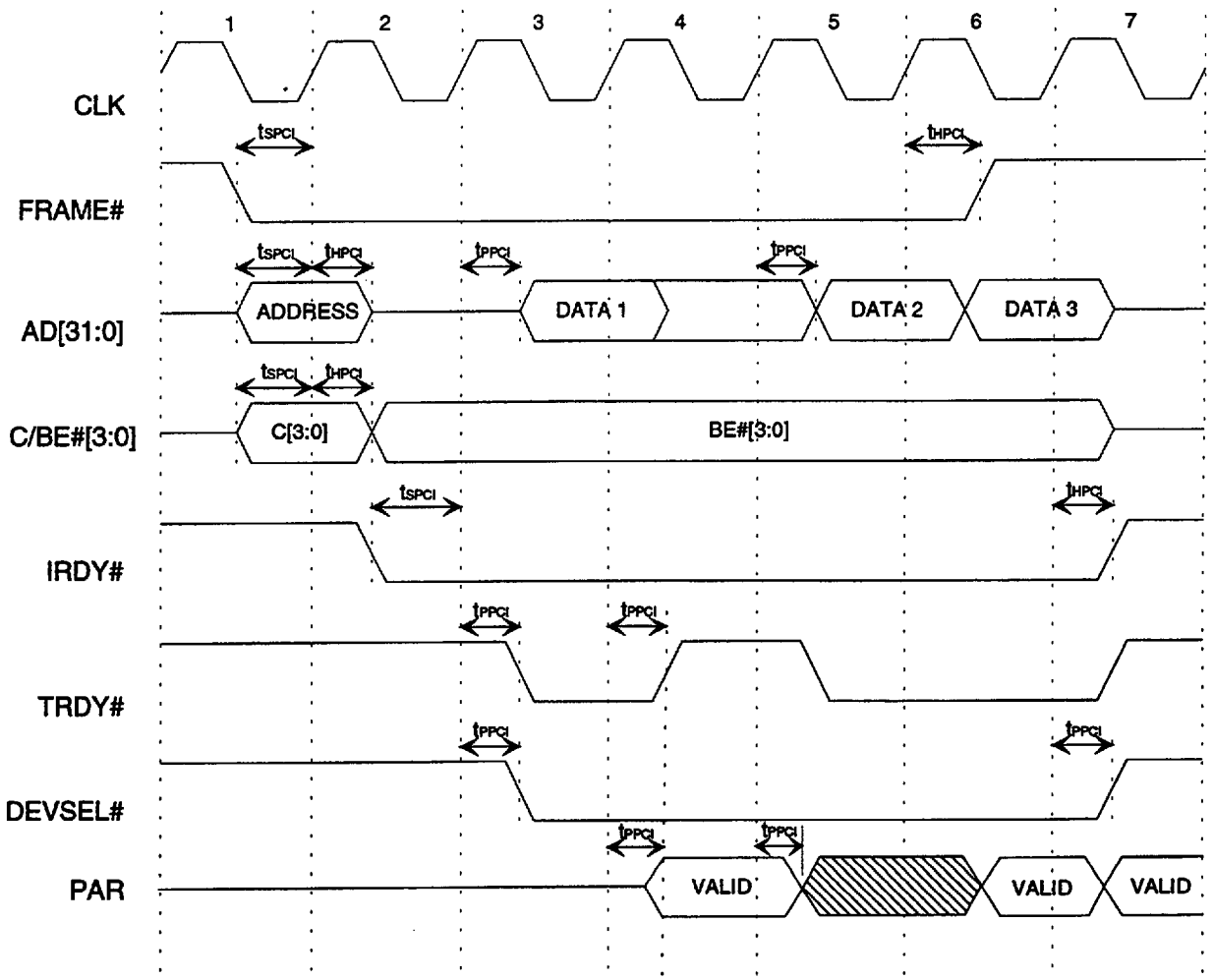


***Figure 9.3** - PCI Bus Timing (Read Operation)*

Note: Minimum timing is when load=0pF, and maximum timing is when load=50pF.

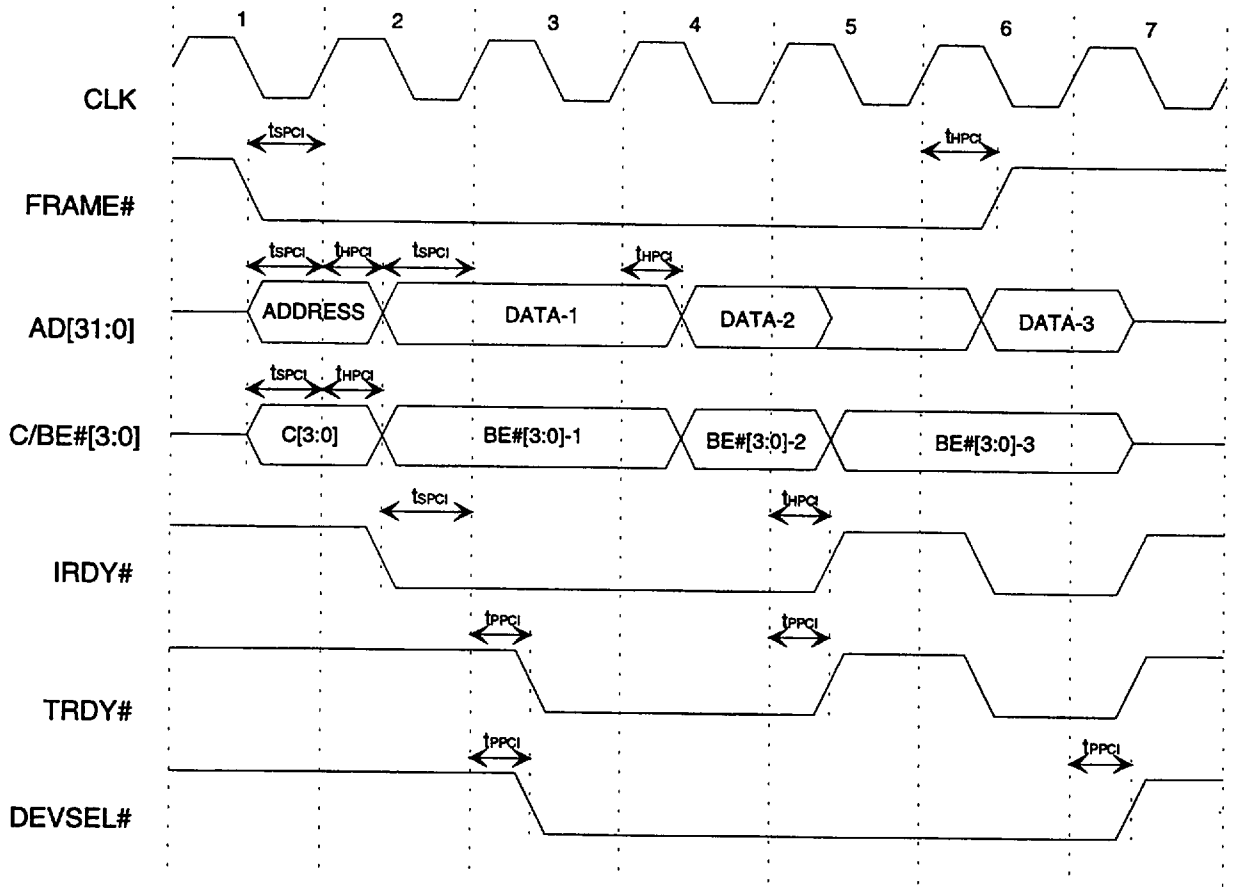


***Figure 9.4** - PCI Bus Timing (Write Operation)*

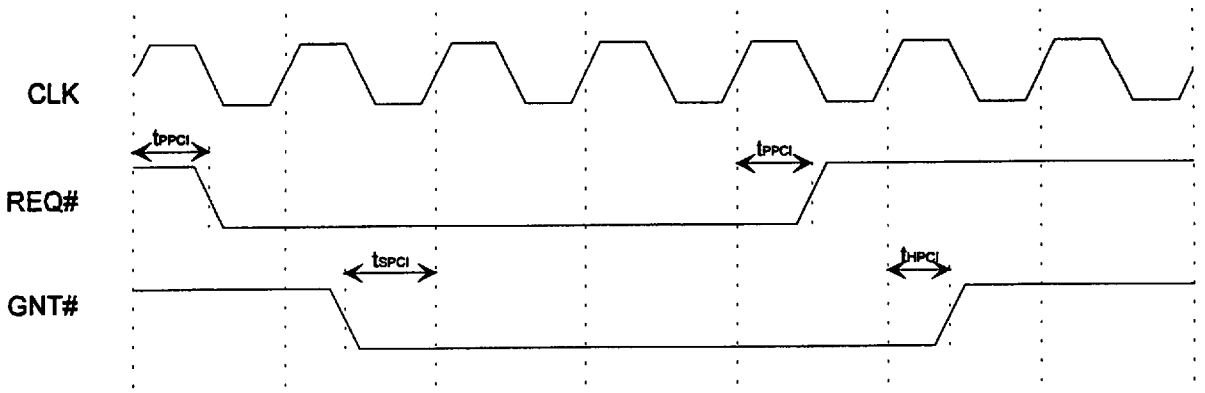


***Figure 9.5** - PCI Bus Master Request Timing*

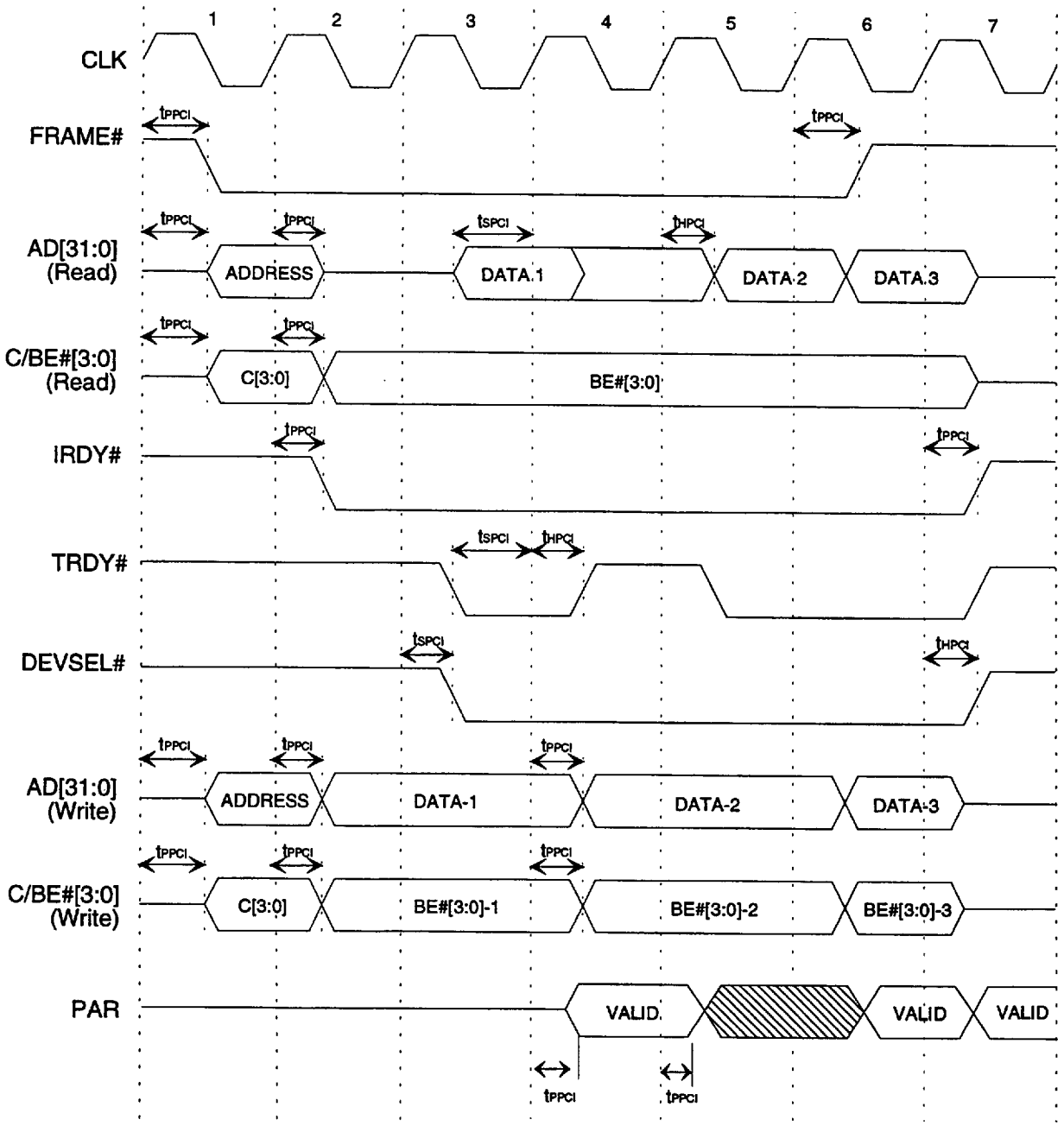


***Figure 9.6** - PCI Bus Master Read/Write Timing*

PCI AND AUXBUS ROM READ TIMING

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI4	tSPCI	Input Setup Time to CLK	7			
PCI5	tHPCI	Input Hold Time to CLK	0			
PCI6	tPPCI	Output Propagation Delay from CLK	2	11	0/50	1
PCI7	tROMENL	ROMENL# Delay from CLK		25	50	
	tROMA	ROM Data Valid from RA[14:0] (AD[30:16])		120	50	2
	tROME	ROM Data Valid from ROMENL#		60	50	2
	tROMO	ROM Data Float from ROMENL#		55	50	2
	tARLT#	ARLT1# & ARLT2# Delay from CLK		25	50	
	tCLKBD	BD Data Delay from CLK		30	50	

Note: Minimum timing is when load=0pF, and maximum timing is when load=50pF. These parameters are for reference only. They can be used to choose the appropriate EPROM speed. These requirements are based on the bus clock being 33 MHz.

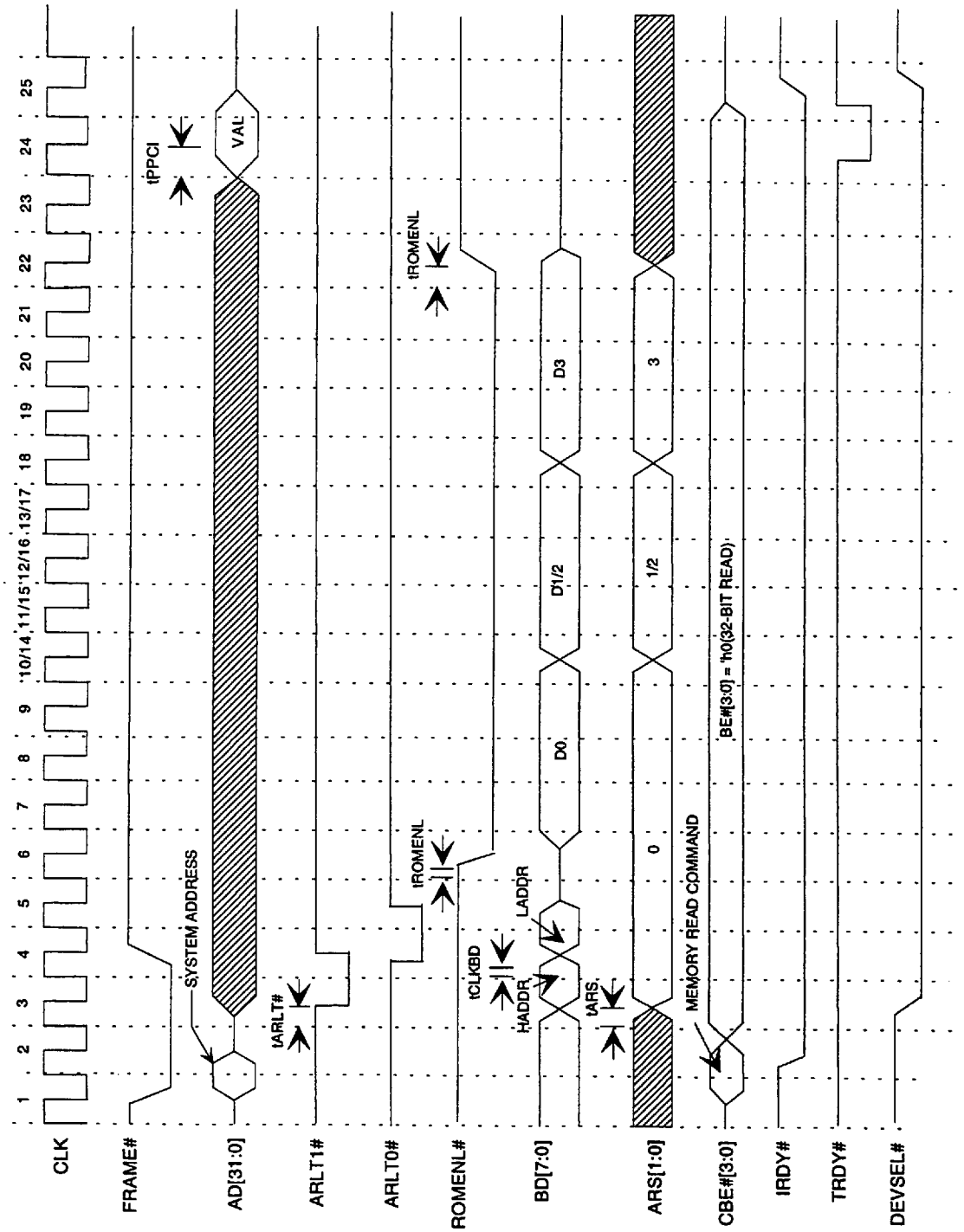


Figure 9.7 - PCI and AuxBus ROM Read Timing

PCI &AUXBUS TIMING

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI4	tSPCI	Input Setup Time to CLK	7			
PCI5	tHPCI	Input Hold Time to CLK	0			
PCI6	tPPCI	Output Propagation Delay from CLK	2	11	0/50	1
PCI8	tARS	ARS[1:0] Delay from CLK		25	50	
PCI9	tADC	Auxiliary Command Delay from CLK		25	50	
PCI10	tBDAD	BD[7:0] Valid to AD[31:0] Valid		40	50	
PCI11	tADBD	AD[31:0] Valid to BD[7:0] Valid		40	50	
PCI12	tHADC	BD[7:0] Valid Hold from AWR# Inactive	10		50	
	tRLQS	BD[7:0] Setup from CLK	7		50	2

Notes:

1. Minimum timing is when load=0pF, and maximum timing is when load=50pF.
2. This parameter is for reference only. They can be used to choose the appropriate AuxBus I/O speed. These requirements are based on the bus clock being 33 MHz.

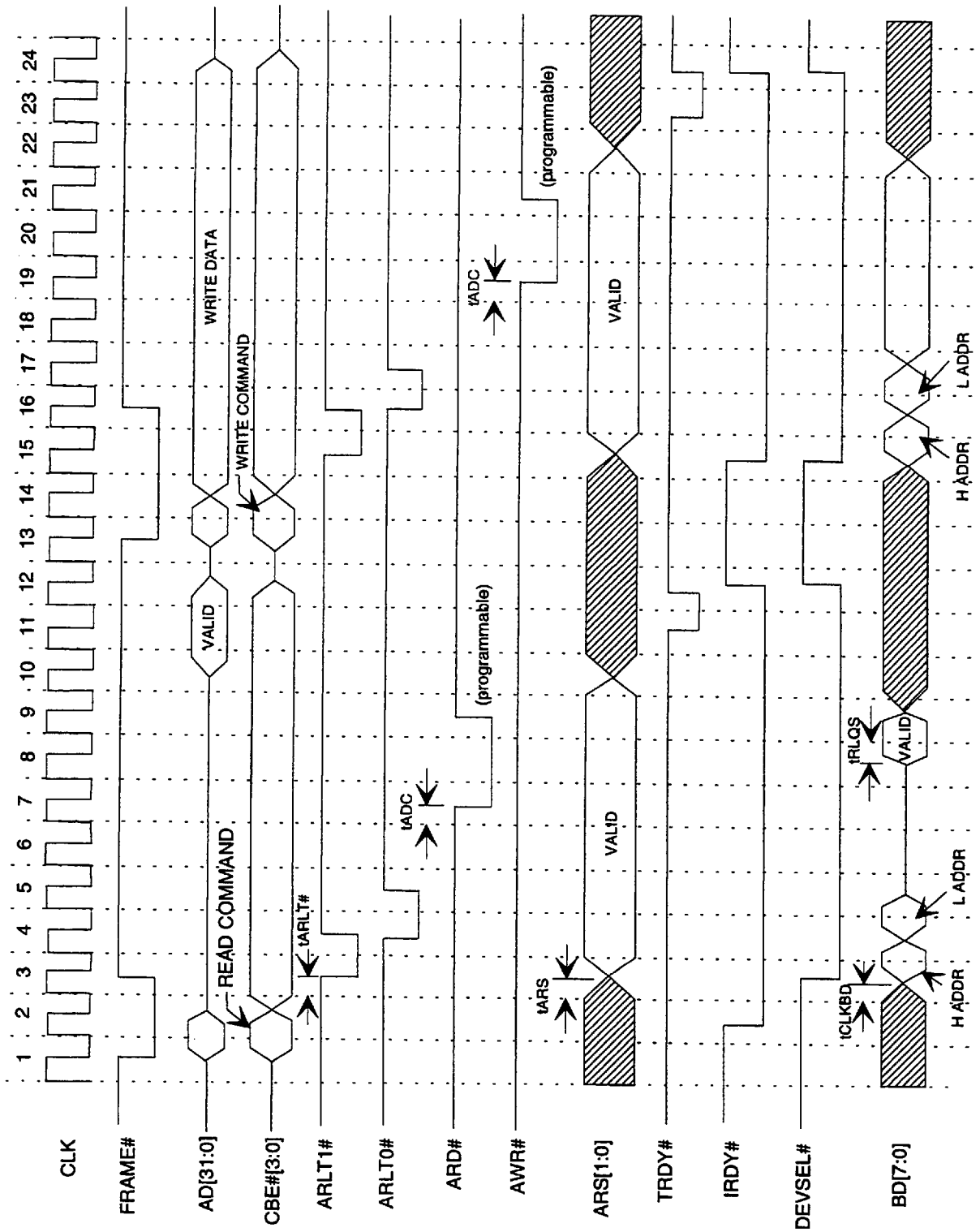


***Figure 9.8** - PCI & AuxBus Timing*

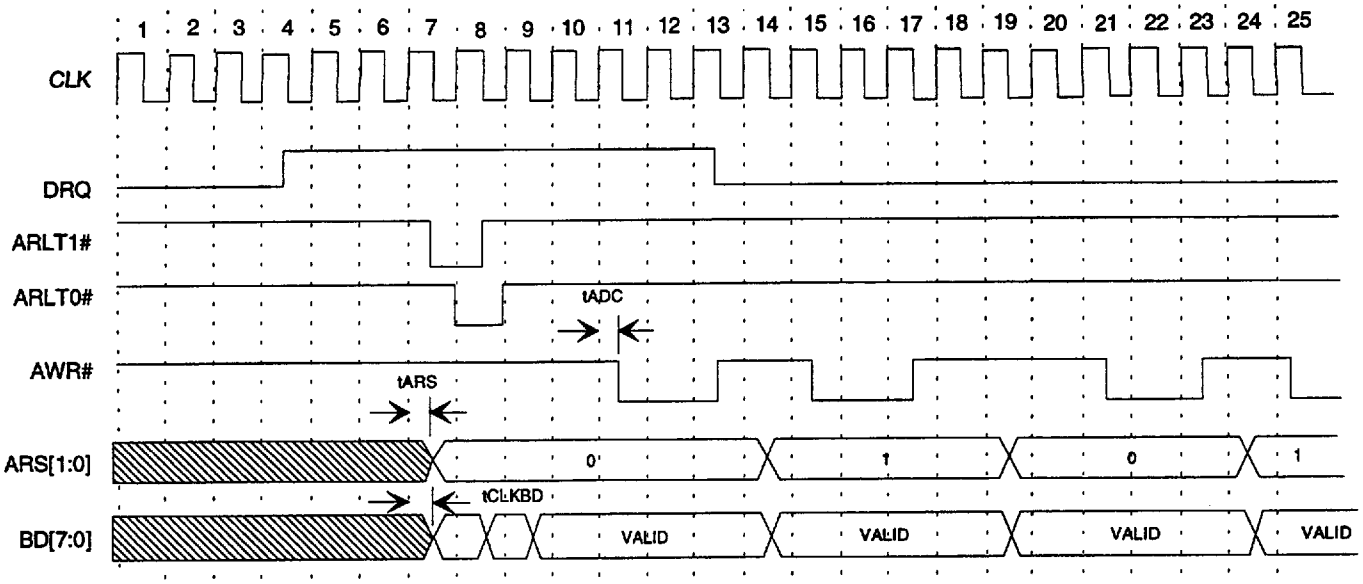


***Figure 9.9** - DMA Transfer on AuxBus*

INTERRUPT TIMING

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
INT1	tINT	CINT# Valid from Rising Edge of EINT#		40	50	

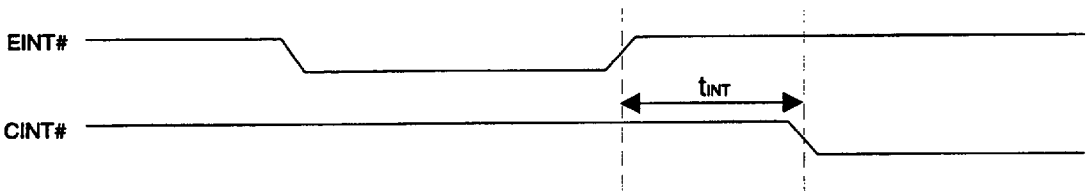


***Figure 9.10** - Interrupt Timing*

9.2.2 MEMORY INTERFACE TIMING

MEMORY CLOCK REQUIREMENT

No.	Symbol	Parameter	Min	Max	Units	Notes
M1	tMP	Memory Clock Period	12.5	25	ns	1
M1	tMP	Memory Clock Frequency	40	80	MHz	

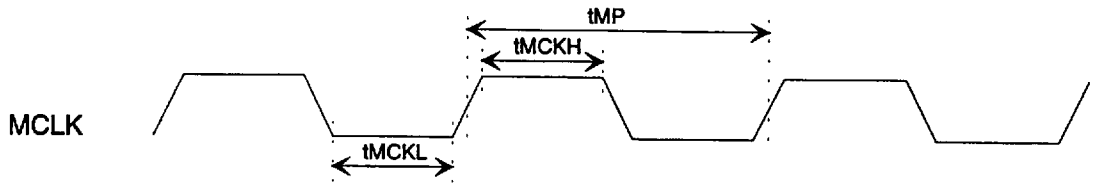


Figure 9.11 *- Memory Clock Requirement*

MEMORY INTERFACE TIMING

No.	Symbol	Parameter	Min (tMP)	Max (tMP)	Tol. (ns)	Load (pF)	Notes
	tRC	Random Rd/Wr Cycle time	5	-			1
	tPC	EDO or Fast Page Mode Cycle Time	1	-			1
	tRAC	Access Time From RAS#	3	4			1
	tCAC	Access Time From CAS#	1	1			1
	tAA	Access Time From Col. Addr. (MA)	2	-			1
	tCPA	Access Time From CAS# Precharge	1.5	2			1
	tOFF	Output Buffer Turn-off Delay ***	1	1			1
M4	tRP	RAS# Precharge Time	2	5		100	
M5	tRAS	RAS# Pulse Width	3	-		100	2
M6	tRSH	RAS# Hold Referenced to CAS#	1	1		100	
M7	tCSH	CAS# Hold Referenced to RAS#	3	-		100	

No.	Symbol	Parameter	Min (tMP)	Max (tMP)	Tol. (ns)	Load (pF)	Notes
M8	tCAS	CASx# Pulse Width	0.5	0.5		100	
M9	tCP	CASx# Precharge Time	0.5	0.5		100	
M10	tRCD	RASx# to CAS# Delay Time	1	4		100	
M11	tRAD	RASx# to Column Address Delay Time	1	4		100	
M12	tASR	Row Address Setup Time	0.5	1		100	
M13	tRAH	Row Address Hold Time	1	1		100	
M14	tASC	Column Address Setup Time	0.5	1		100	
M15	tCAH	Column Address Hold Time	0.5	0.5		100	
M16	tAR	Column Address Hold Ref. to RASx#	3	4		100	2
M17	tRAL	Column Address to RAS# Lead Time	1	1		100	
M18	tWCH	WExx# Hold Ref. to CASx#	0.5	0.5		100	
M19	tWCR	WExx# Hold Ref. to RASx#	3	4		100	
M20	tWP	WExx# Pulse Width	1	1		100	
M21	tRWL	WExx# to RAS# Lead Time	1	1		100	2
M22	tCWL	WExx# to CAS# Lead Time	0.5	1		100	
M23	tWCS	WExx# Setup to CASx#	0	0.5		100	
M24	tDS	MD Setup to CASx#	0	0.5		100	
M25	tDH	MD Hold to CASx#	0.5	-		100	
M26	tDHR	MD Hold Ref. to RASx#	3	4		100	
M27	tCSR	CAS# Setup to RASx# (Ref. Cycle)	0.5	1		100	3
M28	tCHR	CAS# Hold to RASx# (Ref. Cycle)	1	3		100	3

Notes:

1. These parameters are for reference only.
2. The maximum specified is for maximum programmable for a single cycle, it is not the absolute maximum.
3. These parameters are for CAS-before-RAS refresh only.

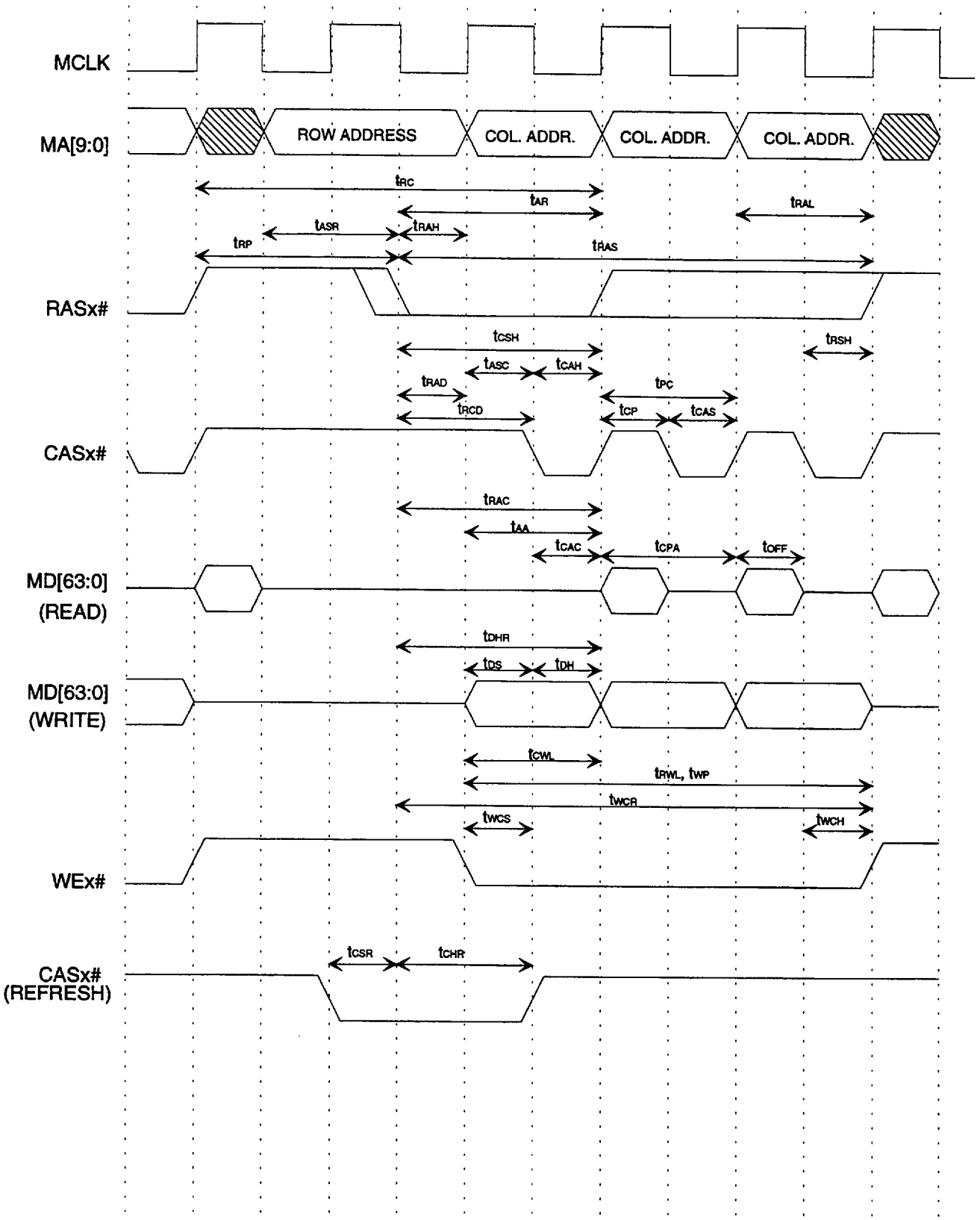


***Figure 9.12** - Memory Interface Timing*

SGRAM MEMORY INTERFACE TIMING

Symbol	Parameter	Min (tMP)	Max (tMP)	Notes
tAC	Access time from CLK		1	
tAH	Address Hold Time	0.5		
tAS	Address Setup Time	0.5		
tCH	Csn, Rasn, Casn, Wen, Dqm Hold Time	0.2		
tCS	Csn, Rasn, Casn, Wen, Dqm Setup Time	0.5		
tDH	Data-in Hold Time	0.2		
tDS	Data-in Setup Time	0.2		
tHZ	Dataout - high impedance time	0.5	1	
tLZ	Dataout - low impedance time	0.5		
tMTC	LOAD MODE Register	2		
tOH	Data-out hold timed	0.5		
tRAS	Active to Precharge period	6		
tRC	Auto Refresh and Active to Active Period	10		
tRCD	Active to Read/Write delay	3		
tRP	Precharge command period	3		
tRRD	Active bank A to Active bank B command period	3		

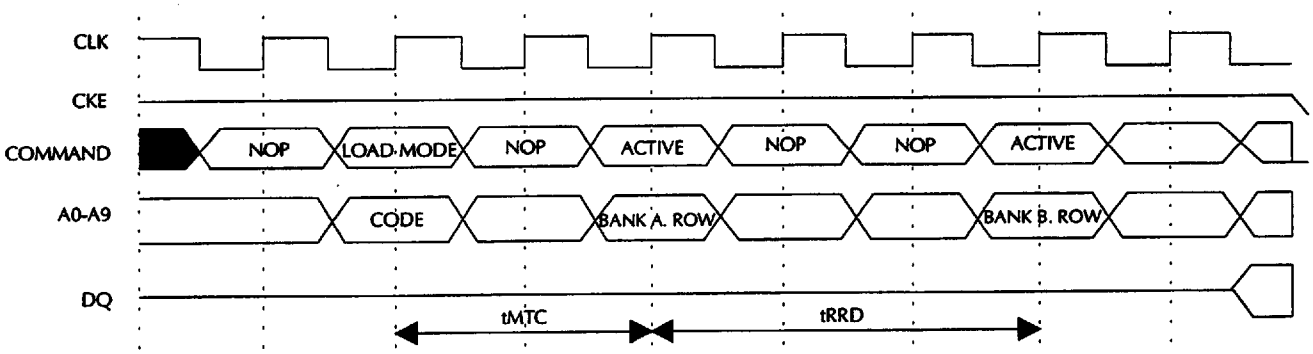


***Figure 9.13** - SGRAM Timing*

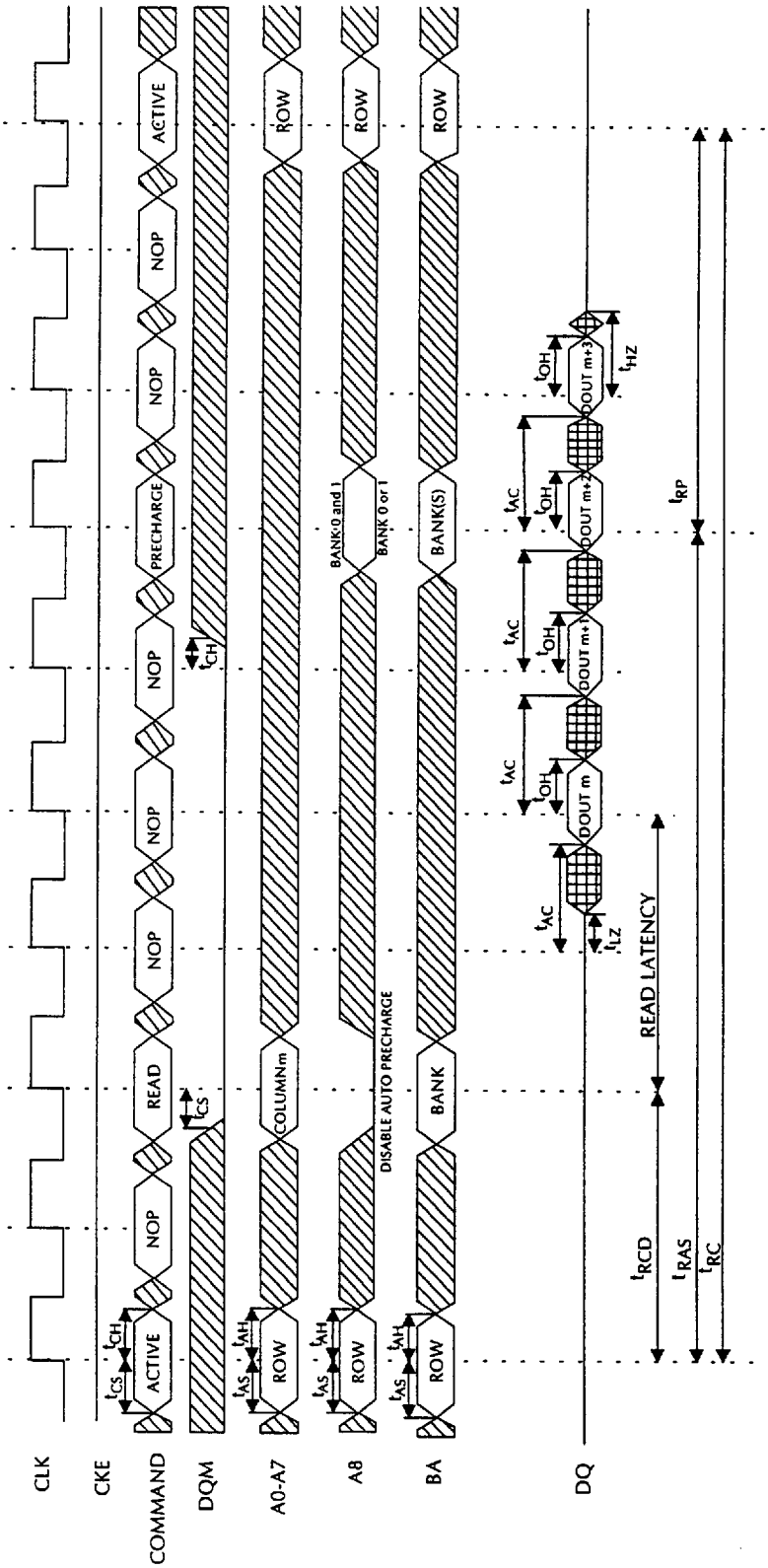


***Figure 9.14** - SGRAM Timing*

9.2.3 MEDIABUS TIMING

MEDIABUS TIMING

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pf)	Notes
MM1	tMCKP	MediaBus Clock Period (16-bit mode)	66			
MM2	tMCKL	MediaBus Clock Low Time (16-bit mode)	10			
MM3	tMCKH	MediaBus Clock High Time (16-bit mode)	10			
MM4	tMMS	MediaBus Input Setup to IMCLK	4			
MM5	tMMH	MediaBus Input Hold to IMCLK	4			
MM6	tMMD	MediaBus Clock to Output Delay		15		

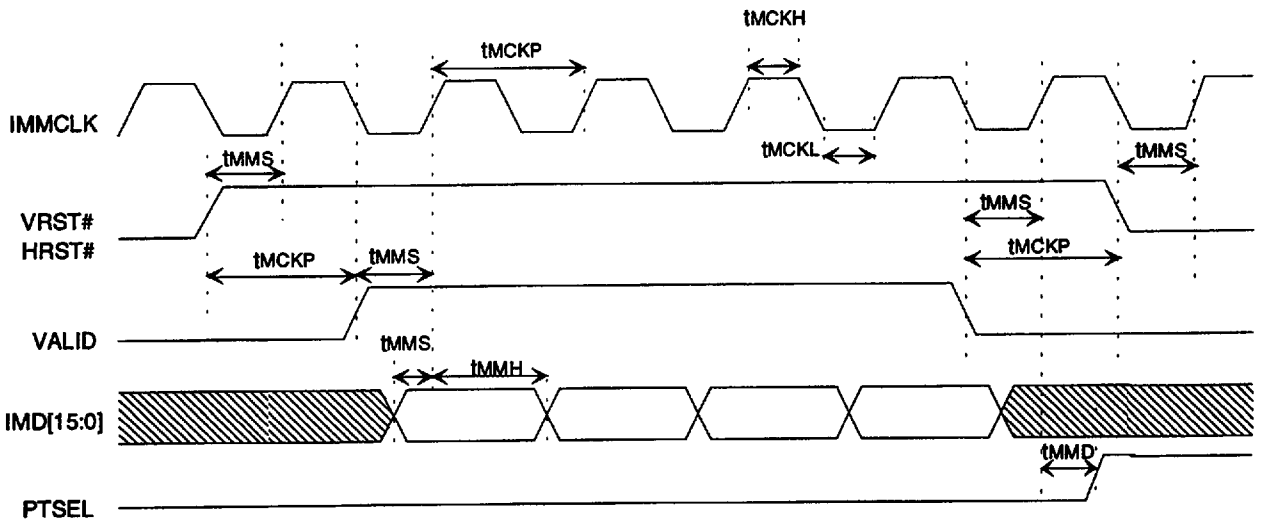


***Figure 9.15** - 16-bit MediaBus Timing*

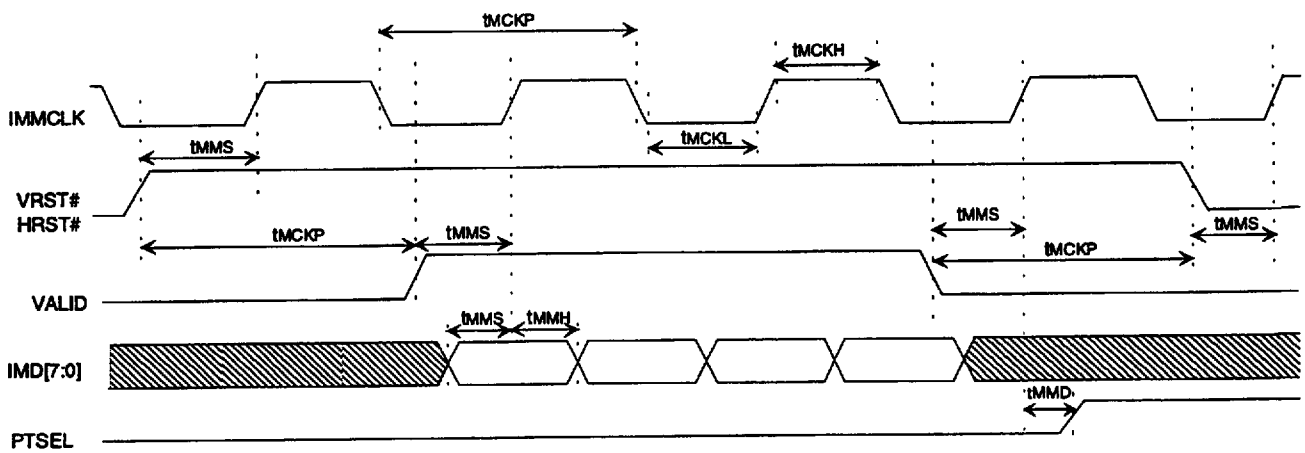


***Figure 9.16** - 8-bit MediaBus Timing*

PIXEL DATA TEST TIMING

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PDT1	tPDTCKP	Pixel Data Test Clock Period	35		50	
PDT2	tPDTS	Pixel Data Test Data Setup		8	50	
PDT3	tPDTH	Pixel Data Test Data Hold		8	50	

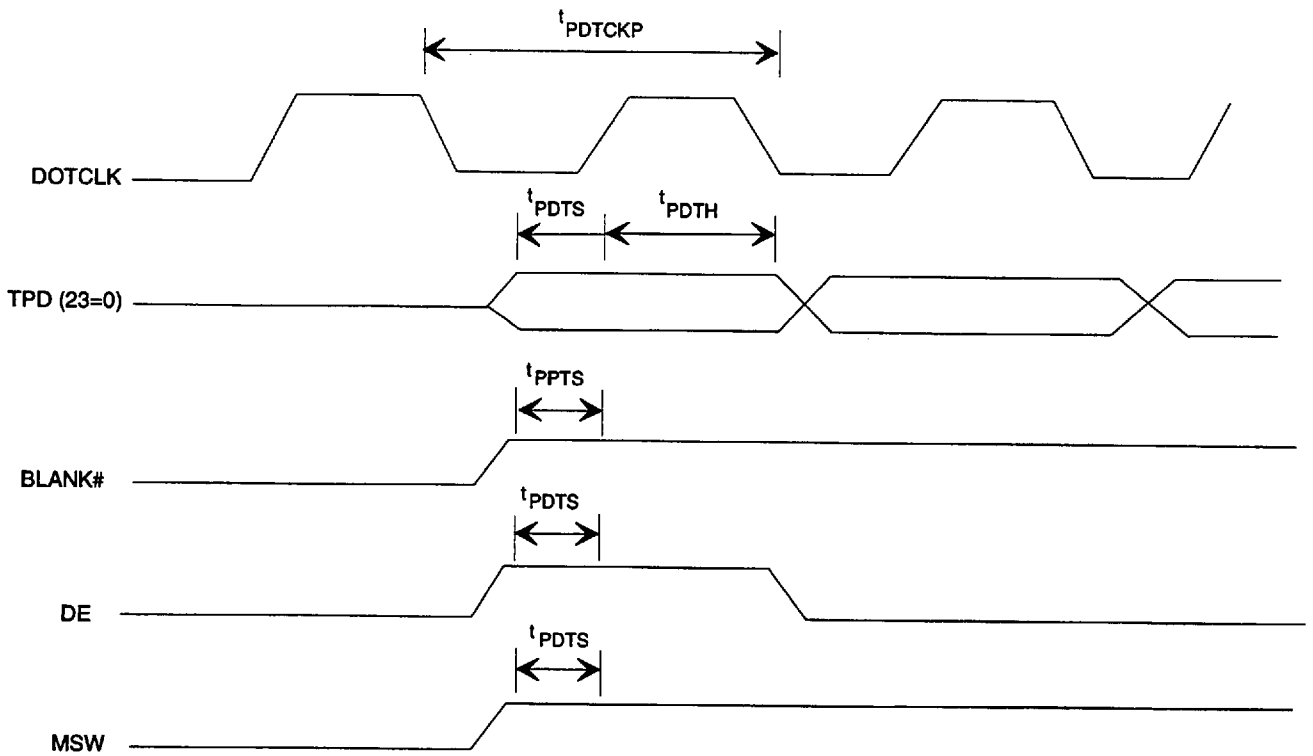


Figure 9.17- Pixel Data Test Timing

FEATURE CONNECTOR TIMING

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
FC1	tFCD	Feature Connector Signals Delay from Clock		7	100	
FC2	tFCS	Feature Connector Signals Setup	5			
FC3	tFCH	Feature Connector Signals Hold	10			

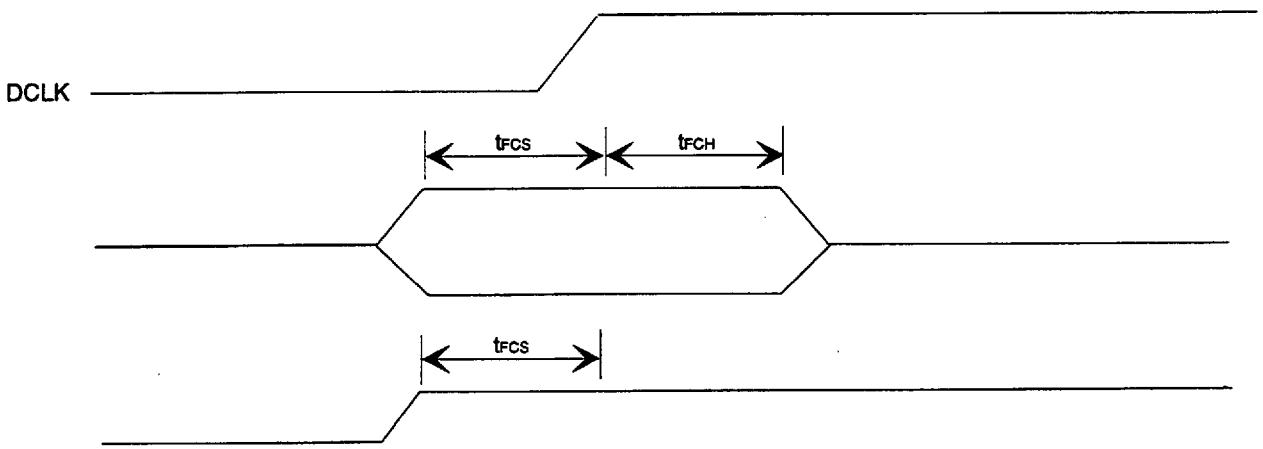


***Figure 9.18** - Feature Connector Input Timing*

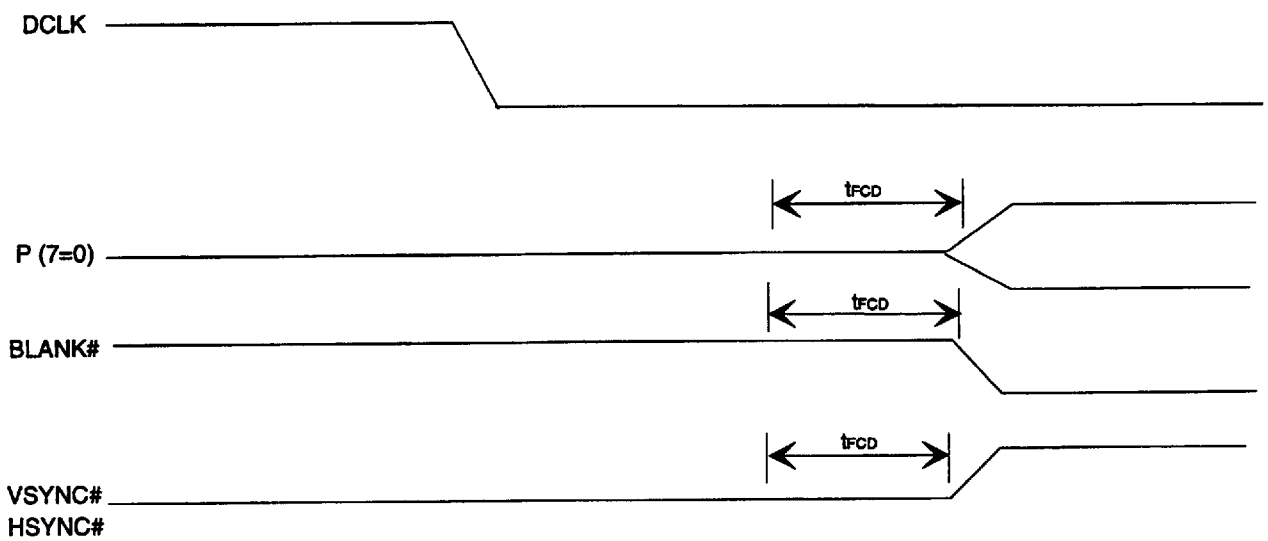
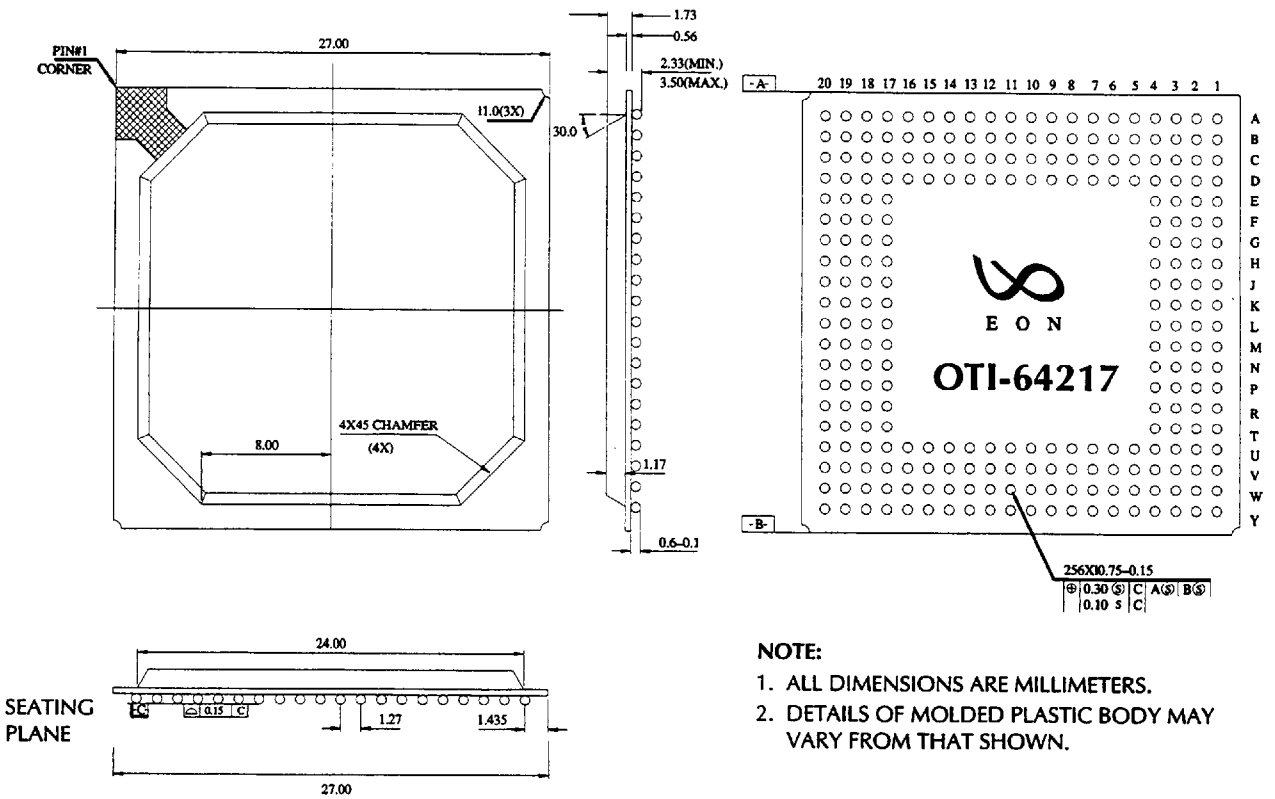


***Figure 9.19** - Feature Connector Output Timing*

CHAPTER 11 PACKAGE DIMENSIONS

The OTI-64217 is packaged in a 256-pin BGA.



NOTE:

1. ALL DIMENSIONS ARE MILLIMETERS.
2. DETAILS OF MOLDED PLASTIC BODY MAY VARY FROM THAT SHOWN.