SM107

Mobile Multimedia

Companion Chip

Databook

Version 1.00

Silicon Motion®, Inc.

SM107 MMCC Databook

Chip Versions

This document is applicable to the SM107 family, all revisions.

Notice

Silicon Motion®, Inc. has made best efforts to ensure that the information contained in this document is accurate and reliable. However, the information is subject to change without notice. No responsibility is assumed by Silicon Motion, Inc. for the use of this information, nor for infringements of patents or other rights of third parties.

Copyright Notice

Revision Record

Version Number	Date	Note
1.00	10/25/07	First release.

Contents

Figures

Tables

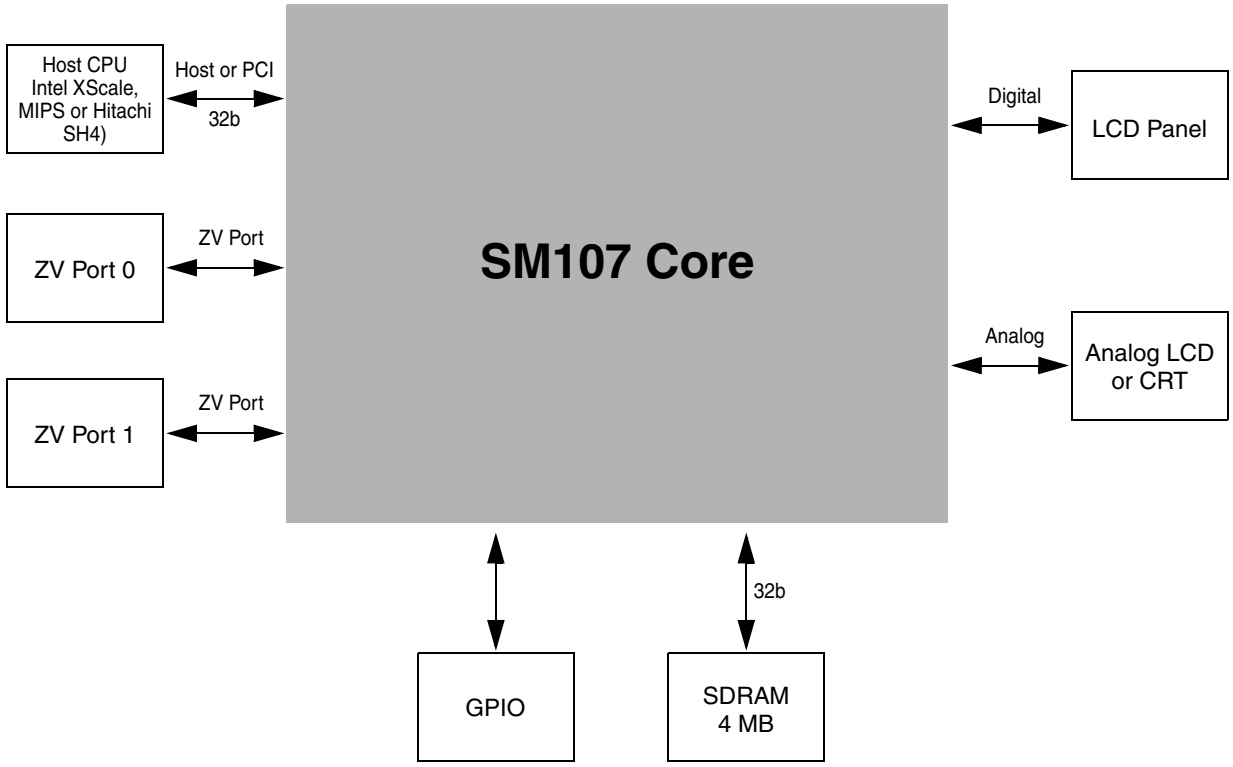
1 Introduction

Overview

The SM107 is a Mobile Multimedia Companion Chip (MMCC™) device, packaged in a 208-pin BGA. Designed to complement needs for the embedded industry, it provides video and 2D capability. To help reduce system costs, it supports a wide variety of I/O, including analog RGB and digital LCD Panel interfaces, two Zoom Video interfaces, and Pulse Width Modulation (PWM). There are additional GPIO bits that can be used to interface to external devices as well.

The 2D engine includes a front-end color space conversion with 4:1 and 1:8 scaling support. The video engine supports two different video outputs (Dual Monitor), at 8-bit, 16-bit, or 32-bit per pixel and a 3-color hardware cursor per video output. The LCD panel video pipe supports a back-end YUV color space conversion with 4:1 and $1:2^{12}$ scaling. A Zoom Video (ZV) port is also included to interface to external circuitry for MPEG decode or TV input.

Figure 1-1: System Block Diagram



Typical System Block Diagram

The SM107 supports a variety of interfaces to the Host CPU. For systems with a PCI™ bus, the SM107 may be attached directly to the PCI bus. For systems with the Intel XScale, Hitachi SH4 or NEC MIPS V_R4122/4131 CPU, the SM107 could connect through a 32-bit SRAM-like memory interface directly to the CPU. The PCI bus interface and the memory interface use many of the same I/O pins, so their use is mutually exclusive.

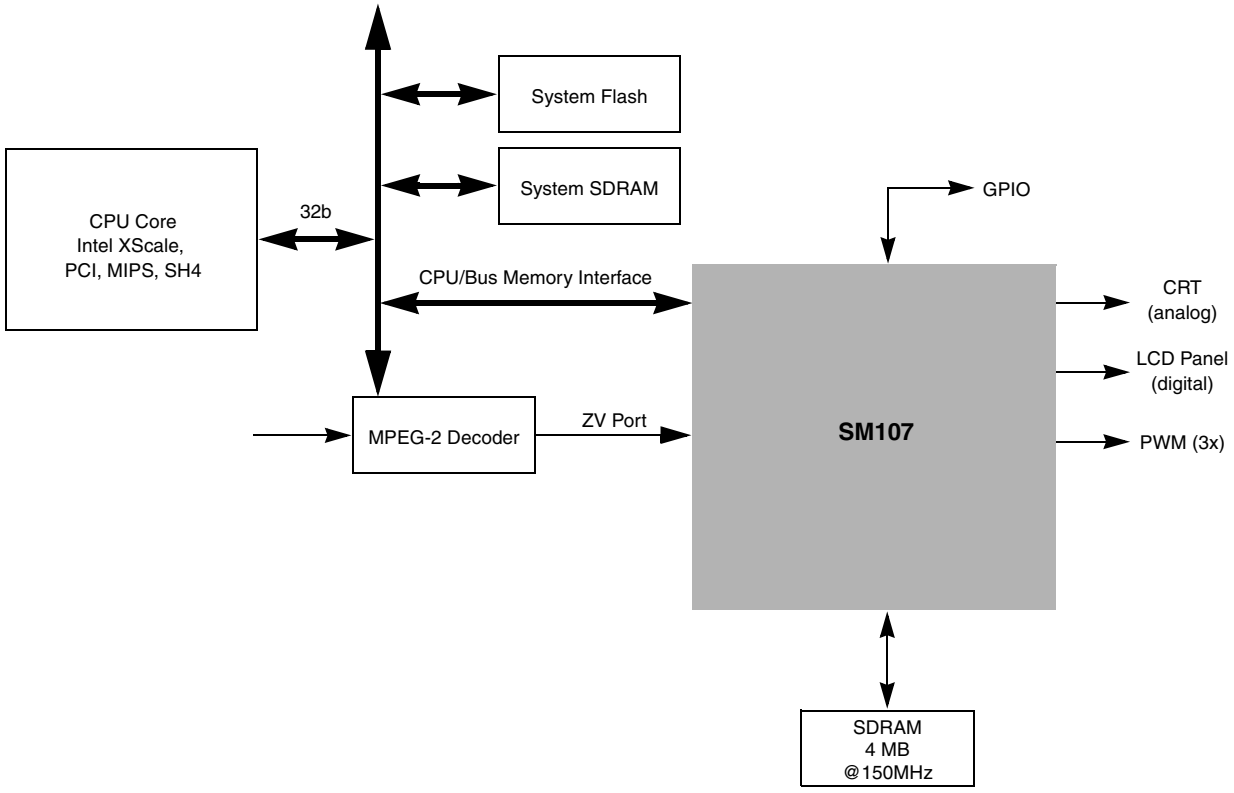
The SM107 supports the following host interface and memory configurations:

Table 1-1: SM107 Supported Host Interfaces and Memory Configurations

Memory Type / Interface	Host Interface (PCI *or* memory)	Frame Memory Interface
UMA_{LOCAL} or Frame	32-bit	32-bit

Figure 1-2 shows a possible system configuration with the SM107 connected through a CPU SRAM-like memory interface.

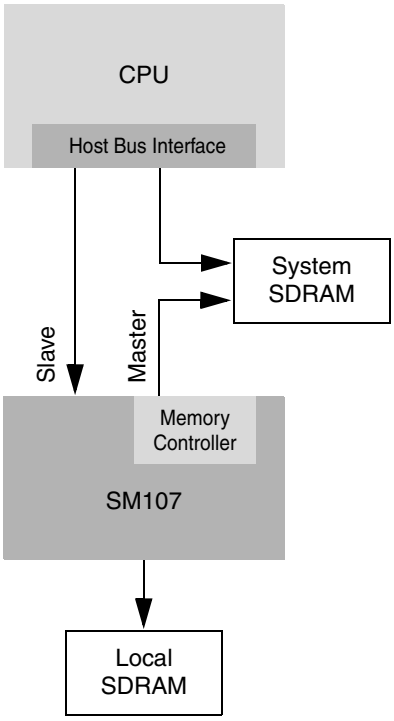
Figure 1-2: Example System Diagram



UMA Architectures

The configuration shown in Figure 1-3 uses dedicated memories for the system and SM107. The System SDRAM contains the system memory and the local SDRAM contains the frame buffer. The SM107 acts as a slave on the Host Bus Interface of the CPU. It controls the local SDRAM. The SM107 can also access the system SDRAM by acquiring the bus and act as a master.

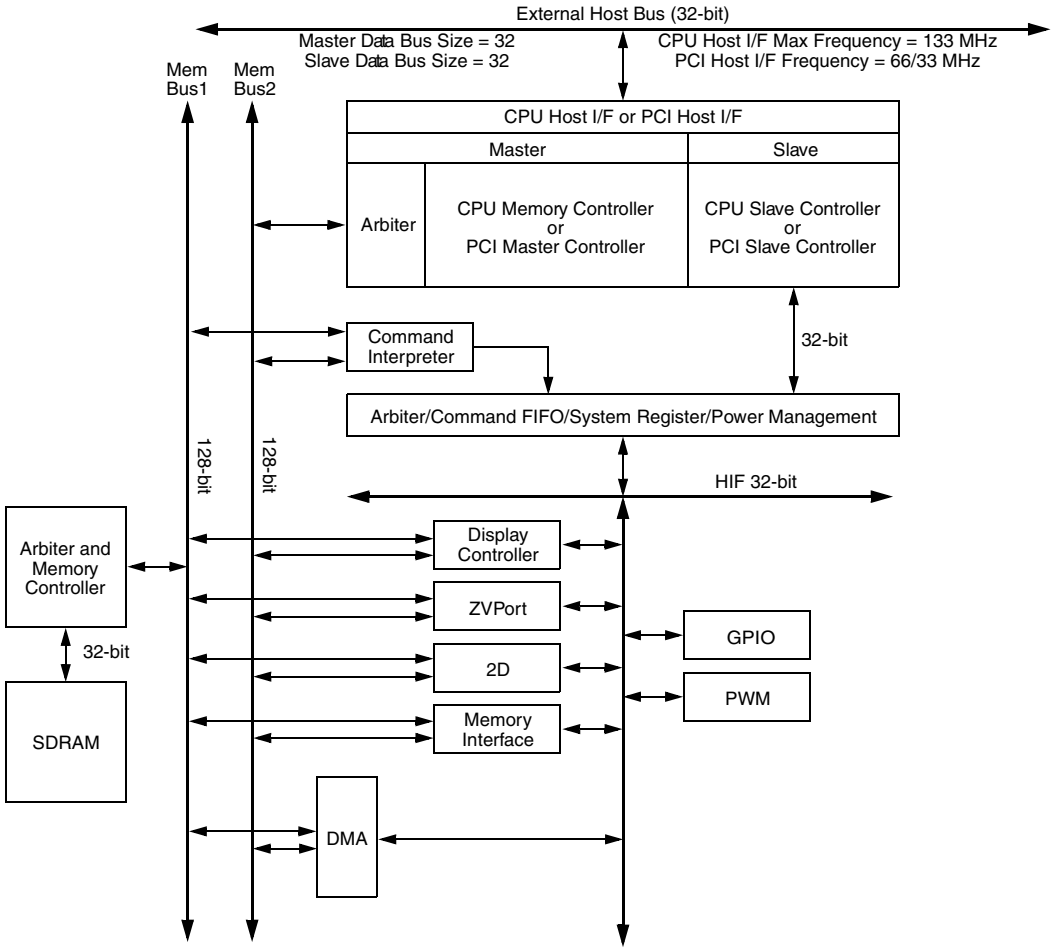
Figure 1-3: System Configurations



Internal Block Description

As can be seen from Figure 1-4, the SM107 uses three major buses for internal communication. The HIF bus (32 bits wide) is used to read and write internal registers. A 128-bit wide data bus (MEM BUS2) is also provided to move data into and out of the Host CPU interface. A second 128-bit wide bus (MEM BUS1) is used to transfer data to and from the SM107's local memory.

Figure 1-4: Internal Block Diagram



Host CPU Memory or PCI Interface

The SM107 supports two mutually exclusive modes of interfacing with the host CPU. The first option is to configure the SM107 as a memory-mapped device located off the host system's CPU to memory interface. In this case, the SM107 supports a 32-bit interface for commands/status and a 32-bit interface for data transfer. With a typical Intel XScale processor interface, this allows for a peak bandwidth of 400 MB/s.

For UMA designs, the SM107 supports an 8x32-bit memory cache at the host interface.

The second configuration option is to use the SM107 as a PCI device on a PCI bus. In this mode, the SM107 supports PCI-1X and 2X for a maximum bus throughput of 266 MB/s.

The following sections summarize the interface connections between the SM107 and a host CPU or PCI bus. See the *SM107 MMCC Design Guide* for more information.

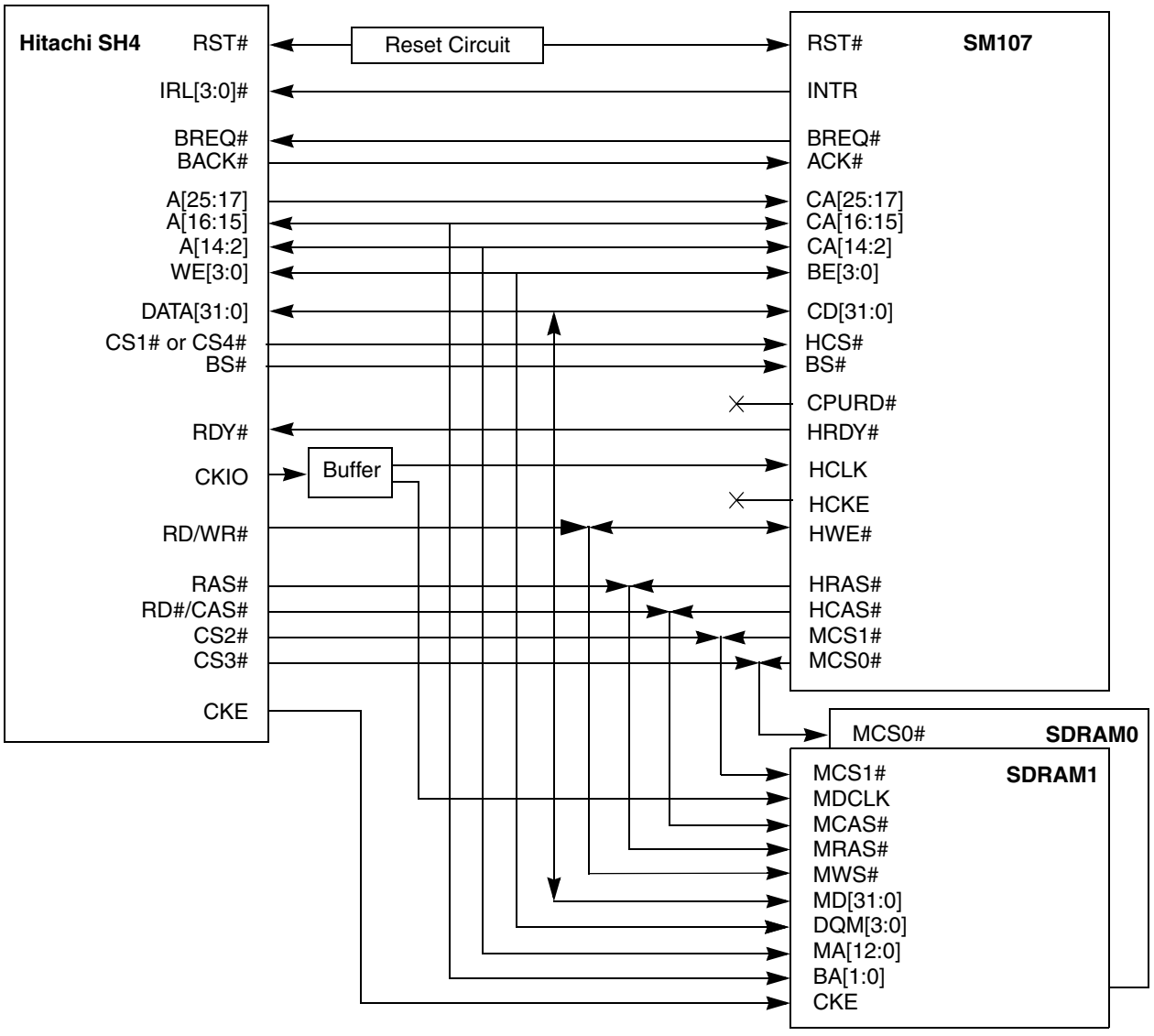
Hitachi SH4

When the SM107 is interfaced to the Hitachi SH4 host bus, it can run in two different host interface modes:

1. In Master mode: SDRAM mode.
2. In Slave mode: Byte Control SRAM mode.

Figure 1-5 shows a typical system-level hookup between the SM107 device and the Hitachi SH4.

Figure 1-5: Hitachi SH4 to the SM107 Bus Interface



Design Notes:

1. During the SM107 Bus Master mode, because the SH4 always drives the SDRAM clock, the timing for the SDRAM signals being driven by the SM107 (CAS#, RAS#, WE#, data, etc.) must reference the memory MDCLK input and meet the memory specifications.

2. In the SM107 Slave mode, the SH4 CPU drives RD/WR# (WE#) for the SM107 and SDRAM. In Bus Master mode, the SM107 drives this line.

3. The SH4 supports up to 64 MB with each chip select. Depending on the memory size and configuration, address [14:12] can be used for the bank address or the memory address. The design shown in Figure 1-5 supports two groups of 64MB memory.
4. The SM107 works as a byte-enable SRAM with the SH4. The SH4 supports byte-enable SRAM only with CS1 or CS4.
5. The SH4 can be programmed for 4-level or 16-level interrupts. The SM107 interrupt output can be connected to one of the 4-level interrupt inputs, depending on the system and software designs. To connect to a 16-level interrupt, an external circuit is required.
6. For a discussion of clock buffering, see the *SM107 MMCC Design Guide*.

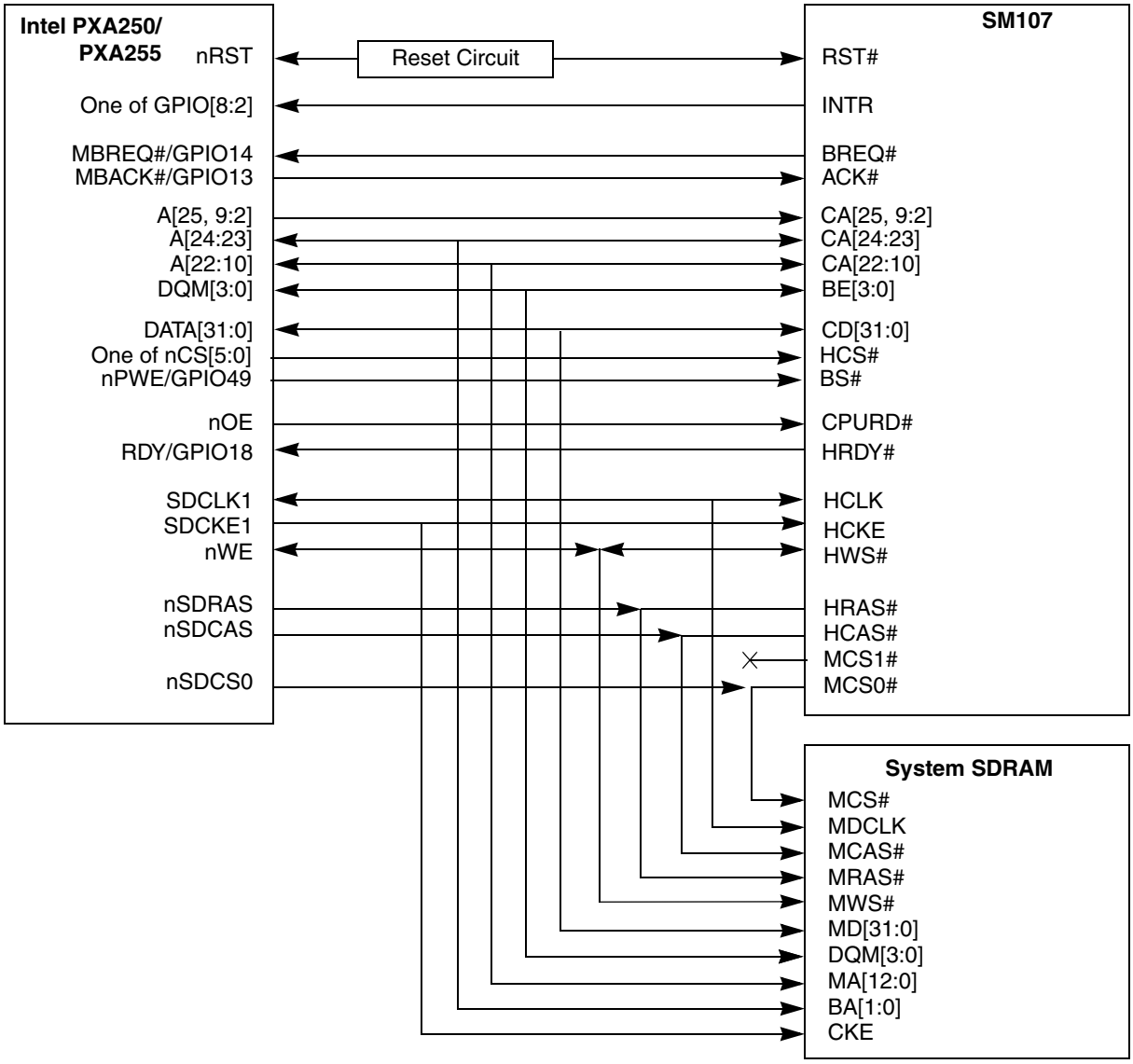
XScale

When the SM107 is interfaced to the XScale host bus, it can run in two different host interface modes:

1. In Master mode: SDRAM mode.
2. In Slave mode: SRAM-like Variable Latency I/O mode.

Figure 1-6 shows a typical system-level hookup between the SM107 device and the PXA250 or PXA255 processor.

Figure 1-6: Intel XScale (PXA250/255) to the SM107 Bus Interface



Design Notes:

1. In Bus Master mode, the SM107 drives the clock to SDRAM, and the CPU must 3-state the clock line. In Slave mode, the CPU drives the clock to both the SM107 and SDRAM.
2. The XScale processor only has one 3-stateable SDRAM CS line. Thus the SM107 can support only one group of SDRAMs in Bus Master mode.
3. According to the XScale specification, SDRAM must use SDCLK2 or SDCLK1. The variable latency I/O must use either SDCLK0 (synchronous) or no clock. Because the SM107 has to drive the SDRAM clock on the same line, SDCLK1 is used.
4. According to the XScale specification, the variable latency I/O device can use one of nCS[5:0] as the chip select.
5. The XScale processor does have a dedicated interrupt input. Use one of GPIO[8:2] and configure the selection as an interrupt via software.

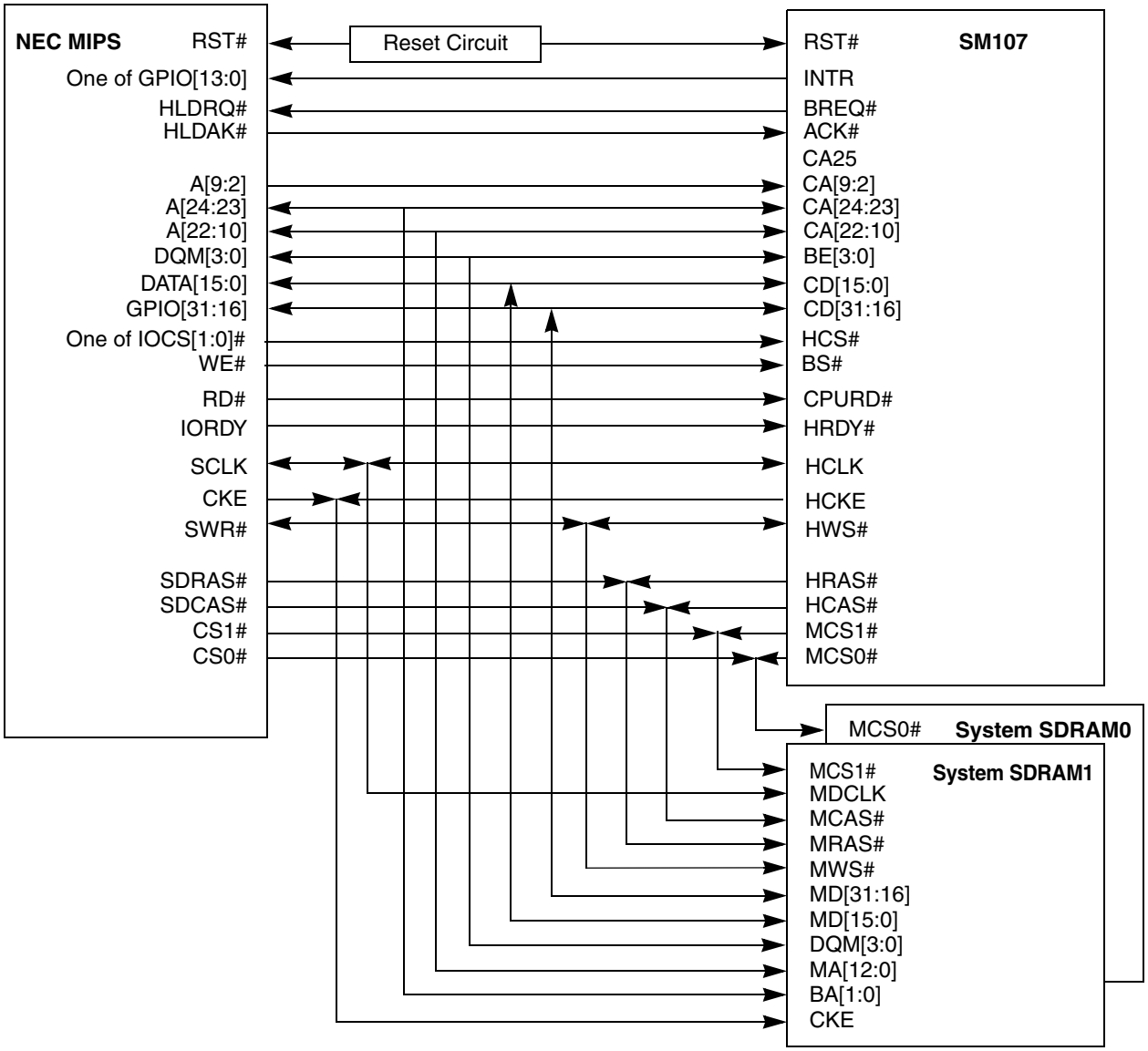
NEC V_R4122/4131 MIPS

When the SM107 is interfaced to the NEC V_R4122/31 MIPS host bus, it can run in two different host interface modes:

1. In Master mode: SDRAM mode.
2. In Slave mode: LCD Controller mode.

Figure 1-7 shows a typical system-level hookup between the SM107 device and the NEC V_R4122/31 MIPS processor.

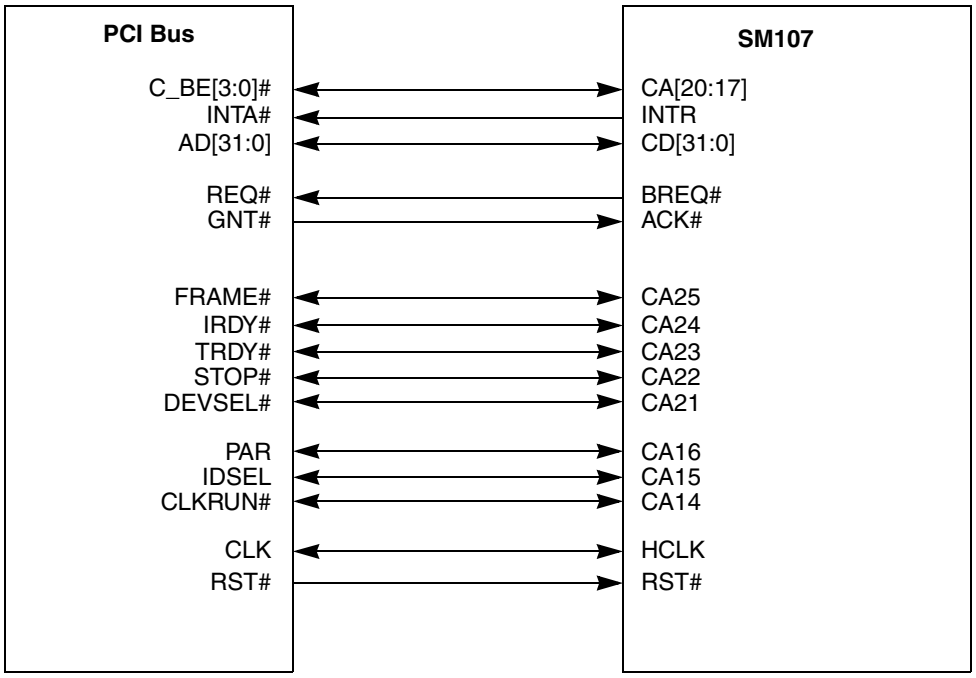
Figure 1-7: NEC MIPS to the SM107 Bus Interface



PCI Bus

Figure 1-8 shows a typical system-level hookup between the SM107 device and the PCI bus.

Figure 1-8: PCI Bus Interconnection



Command Interpreter / Command List Processor

This module is provided as an aid to the graphics controller and is used to move data from system memory to the graphics engine, executing a "Command List" placed in the shared memory. The Command Interpreter is capable of making decisions (such as a branch to another part of memory) and wait for events or conditions inside other modules.

Zoom Video Port

The SM107 includes two Zoom Video (ZV) ports to allow the use of external MPEG decoders for DVD playback, external TV tuners, and other sources. This interface supports the YUV 4:2:2, YUV 4:2:2 with byte swap and RGB 5:6:5 data formats. It also supports ITU656-8 bit.

The standard ZV port uses an 8-bit interface at 72 MHz. However, if desired, an extra 8 bits in the GPIO interface may be used to interface to ICs that only support a 16-bit ZV interface or uses the extra 8 bits for the second ZV port input. The pins used for the ZV interface are designated GPIO pins. See the *SM107 MMCC Design Guide* for more information.

Note that the ZV input to video display path is as follows: ZV port → capture → frame buffer → video scalar → display. The capture portion supports a 1:1 or 2:1 reducing. In addition, the video scalar allows arbitrary scaling from 1:1 to 4:1 on shrinking and 1:1 to $1:2^{12}$ on expansion; however, the quality of the expansion is degraded beyond 1:8. This will easily allow 4:3 and 16:9 conversion, full screen PAL, and picture-in-picture.

See Chapter 8 for more information about the ZV Port registers. See the *SM107 MMCC Design Guide* for more information about interfacing the SM107 to external sources.

2D Engine

The SM107 provides industry-leading 2D acceleration through the combination of an optimized 128-bit 2D drawing engine and a high bandwidth link to local frame memory. The 2D engine also contains a command interpreter (an enhanced DMA engine) that can intelligently fetch operands out of the frame buffer at up to 600MB/s. The command interpreter can conditionally branch to another location in memory, wait for status from another module, etc. as it fetches and interprets commands.

The 2D drawing engine also contains a color space conversion unit. The color space conversion unit allows for direct translation from many YUV formats into RGB. The 2D drawing engine also contains a bi-linear scalar, which supports 4:1 shrink and $1:2^{16}$ stretch.

As noted previously, the SM107 supports frame memory in UMA, and local 32-bit modes. With 32 bits of SDRAM running at 144 MHz, the SM107's DMA engine has 600MB/s of memory bandwidth to use for fetching 2D operands and data. (The UMA solution's performance is dependent on the host system's topology.) This high memory bandwidth allows the 2D engine to run at full speed without costly waits or pipeline stalls from the frame buffer.

The 2D drawing engine understands the following commands:

1. BitBlt (from system/local memory to system/local memory) with 256 raster operations. Pattern is selectable between 8x8 monochrome pattern, 8x8 color pattern or another surface located in either system or local memory.
2. Transparent BitBlt with the same capabilities as the previous command, but only the source or destination can be transparent (either ColorKey or ChromaKey).
3. Alpha BitBlt with a constant alpha value.
4. Rotation BitBlt for any block size. This feature allows high speeds conversion between landscape and portrait display without the need for special software drivers. (90° , 180° , 270° .)
5. YUV to 16-bit/32-bit RGB Blt conversion with $1:2^{16}$ stretch or 4:1 shrink to provide high speeds video in common format.
6. Auto-wrapping for smooth scrolling support for navigational or other data.
7. Support for tiled memory to optimize performance for 2D operations and rotation.

As noted previously, the 2D Drawing Engine has a 112 MHz clock and a 128-bit wide memory access path. With 8-bpp colors, the 2D engine can process 2400M pixels/s, and with 16-bpp the 2D engine can process 1200M pixels/s.

See Chapter 4 for more information about the 2D Drawing Engine.

Performance

By using a UMA architecture, the number of operations required by the graphics driver is less because there is no need to transfer data between host bitmaps and device bitmaps – they are the same in a UMA architecture.

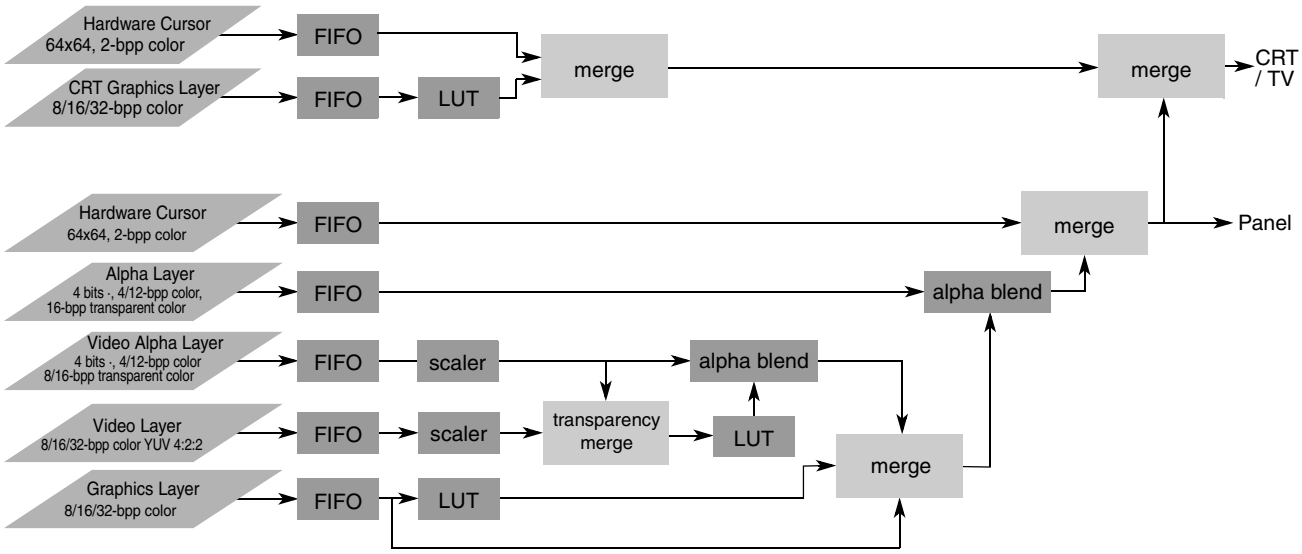
Also, both the Command Interpreter and the Color Space Conversion with Scaling will reduce the CPU utilization considerably – in the order of a 50% reduction. The reason behind this reduction is that the CPU does not have to convert the YUV color space into a RGB color space and the CPU does not have to wait until the drawing engine is finished.

Also, a sophisticated Command Interpreter algorithm can reduce the number of operations by looking into the command list for instructions still to be scheduled and combine certain instructions into one instruction.

Video Display Layers

As shown in Figure 1-9, the SM107 supports seven layers of display frames (2x hardware cursor, primary graphics, video, video alpha, alpha, and secondary graphics). (See Chapter 5 for more information about the Display Controller.)

Figure 1-9: Video Layers and Data Processing



Layer #7: Secondary Hardware Cursor

To display a cursor on the analog output for multi-monitor function.

- One single 64x64 pixel cursor 2-bpp color [1:0] (00 = transparent, 01 = color0, 10 = color1, 11 = color2), is mapped into a 32-bit RGB 8:8:8 color map.

Layer #6: Secondary Graphics

To display text or drawings on the analog output (CRT) for multi-monitor function.

- 8-bpp (index into RGB 8:8:8 lookup table).
- 16-bpp RGB 5:6:5.
- 32-bpp RGB 8:8:8.

Layer #5: Primary Hardware Cursor

To display a cursor on the digital output.

- One single 64x64 pixel cursor 2-bpp color [1:0] (00 = transparent, 01 = color0, 10 = color1, 11 = color2), is mapped into a 32-bit RGB 8:8:8 color map.

Layer #4: Alpha

To alpha-blend and/or color-key an image on top of the Primary Graphics and Video layer outputs.

- 16-bpp (4-bit alpha, 4-bit Red, 4-bit Green, 4-bit Blue) or RGB 5:6:5.
- 16-bit transparency register (with 16-bit RGB 5:6:5 mode); if a color matches the register's value it is transparent.

- 4-bit planar blending register (in 16-bit RGB 5:6:5 mode only) to blend all pixels on the plane (that are non-transparent) to one planar alpha value.

Layer #3: Video Alpha

To alpha-blend and/or color-key an image on top of the Video layer output.

- Supports bi-linear scale up or down.
- 8-bpp (4-bit alpha, 4-bit index color), or 8-bit index (index into RGB 8:8:8 lookup table).
- 16-bpp (4-bit alpha, 4-bit Red, 4-bit Green, 4-bit Blue) or RGB 5:6:5.
- 8-bit transparency register (with 8-bit index), or 16-bit transparency register (with 16-bit RGB 5:6:5 mode); if a color matches the register's value it is transparent.
- 4-bit planar blending register (in 16-bit RGB 5:6:5 mode only) to blend all pixels on the plane (that are non-transparent) to one planar alpha value.

Layer #2: Video

To overlay video image or graphics on top of Primary Graphics layer.

- Supports bi-linear scale up or down.
- 8-bit index (index into RGB 8:8:8 lookup table).
- 16-bpp RGB 5:6:5 or YUV 4:2:2.
- 32-bpp RGB 8:8:8.

Layer #1: Primary Graphics

To display text or drawings on the primary output (LCD panel).

- Support smooth scrolling and auto-wrapping.
- 8-bit index (index into RGB 8:8:8 lookup table).
- 16-bpp RGB 5:6:5.
- 32-bpp RGB 8:8:8.
- 8-bit (with 8-bit index), 16-bit (with 16-bit RGB 5:6:5), or 32-bit (with 32-bit RGB 8:8:8) color key register. If the color value matches the register's value, the color is transparent and the pixel from the Primary Video layer is shown instead.

Terminology

Some definitions of terms used above:

bpp – bits per pixel.

RGB – Red, Green, Blue.

RGB 5:6:5 – 16-bit color mode, where Red has 5 bits, Green has 6 bits, and Blue has 5 bits.

RGB 8:8:8 – 32-bit color mode, where Red has 8 bits, Green has 8 bits, and Blue has 8 bits. The upper 8 bits are unused.

Alpha – A means of blending two layers together. The fundamental equation is (α * *c*) + (1 - α) * (original pixel), where *c* is the 4-bit color that points into the 18-bit lookup table. In practical terms, 4-bit alpha blending means that for two given display layers, one layer is dominant (e.g. video layer) and the other layer (e.g. video alpha) has 16 levels of transparency from 100% to 0% that may be applied to the colors in that layer.

LUT – Lookup table; a means to map an 8-bit color index into a 24-bit color space, thus a smaller number of simultaneous colors (8-bit) but with a wide range of colors (24-bit) to choose from.

Display Resolution

The SM107 supports display resolutions up to 1280 x 1024. 16:9 formats in this range (e.g. 800 x 480, 1024 x 600, and 1280 x 768) are supported. Note that there are trade-offs between the maximum resolution, the number of active video layers, and the frame memory choice.

Dual Display

The SM107 supports Dual Display, i.e. two different displays of the same or different resolutions.

As shown in Figure 1-9, only the panel pipe supports the video and alpha planes. However, since these planes fetch data from the frame buffer memory as well, there might not be enough bandwidth to enable the video and alpha planes in Dual Display mode.

In order to display video on the panel pipe in Dual Display mode and on the CRT pipe in any mode, the 2D Engine's Color Space Conversion and Stretching functionality should be used.

LCD Panel

The SM107's LCD logic block drives an 18-bit or 24-bit TFT panel directly. Eight-bit and 12-bit CSTN panels are also supported, and a dithering engine supports them to an effective 18-bit resolution. The maximum supported panel size is 1280 x 1024. Panel power sequencing is through software control.

Figure 1-10 shows a typical interface between the SM107 and a 24-bit TFT panel. Note the following with regards to this interface:

1. The timings of VDEN, FPEN, and BIAS are fully controlled by software.
2. The TFT panel does not use Vbias. The BIAS control used here controls the On/Off switch of the backlights. Program its timing so backlight is on after 12V is applied to the inverter.
3. The SM107 provides three PWM signals that can be used to control brightness.
4. To support a 24-bit TFT panel, use pins GPIO[63:58]. The pins are then limited to use as digital 8-bit TV data out and 8- or 16-bit video capture.

See the *SM107 MMCC Design Guide* for information about interfacing to LCD displays.

Figure 1-10: Typical 24-bit TFT Panel Interface

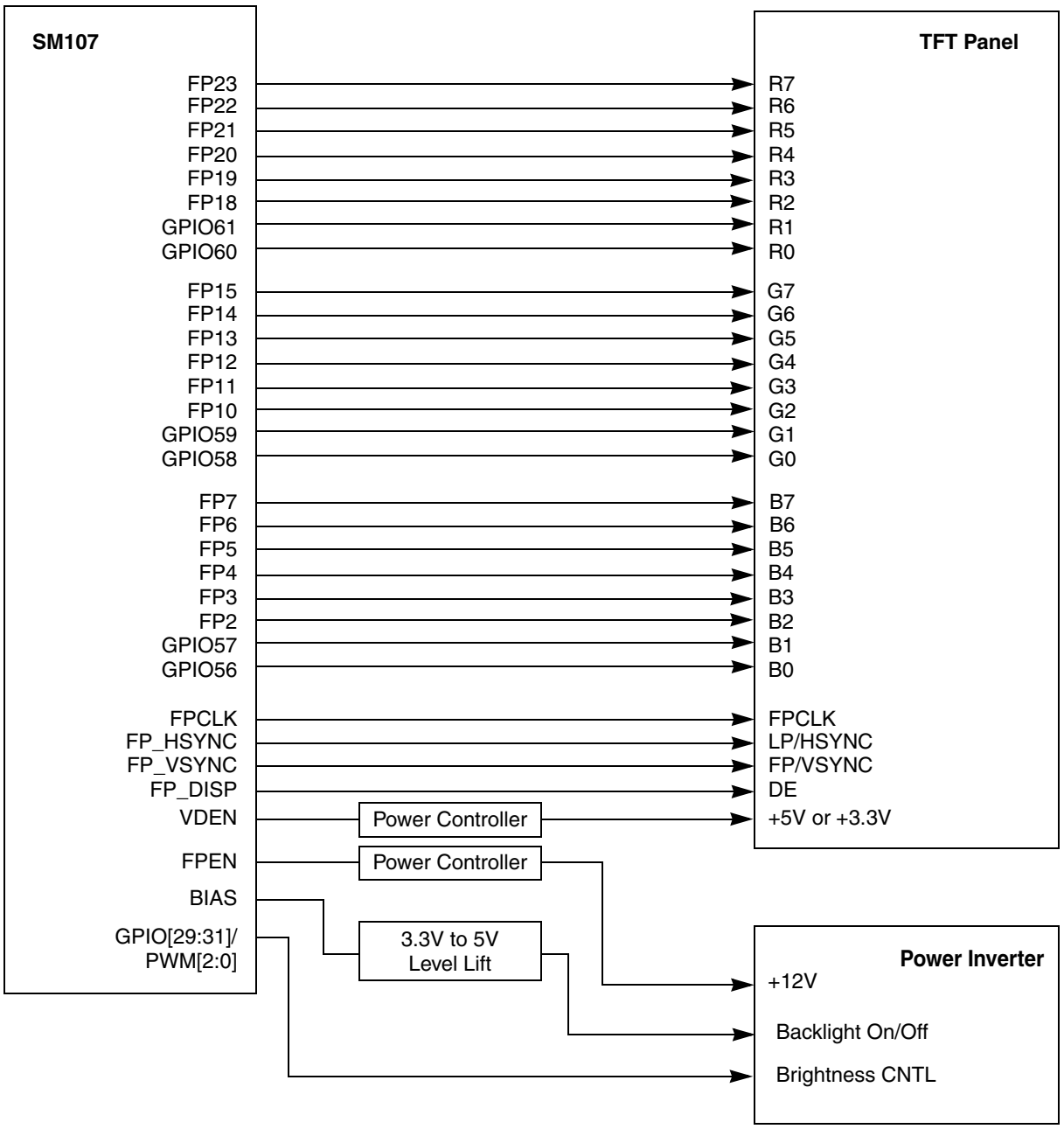


Figure 1-11 shows a typical interface between the SM107 and an 18-bit TFT panel.

Figure 1-11: Typical 18-bit TFT Panel Interface

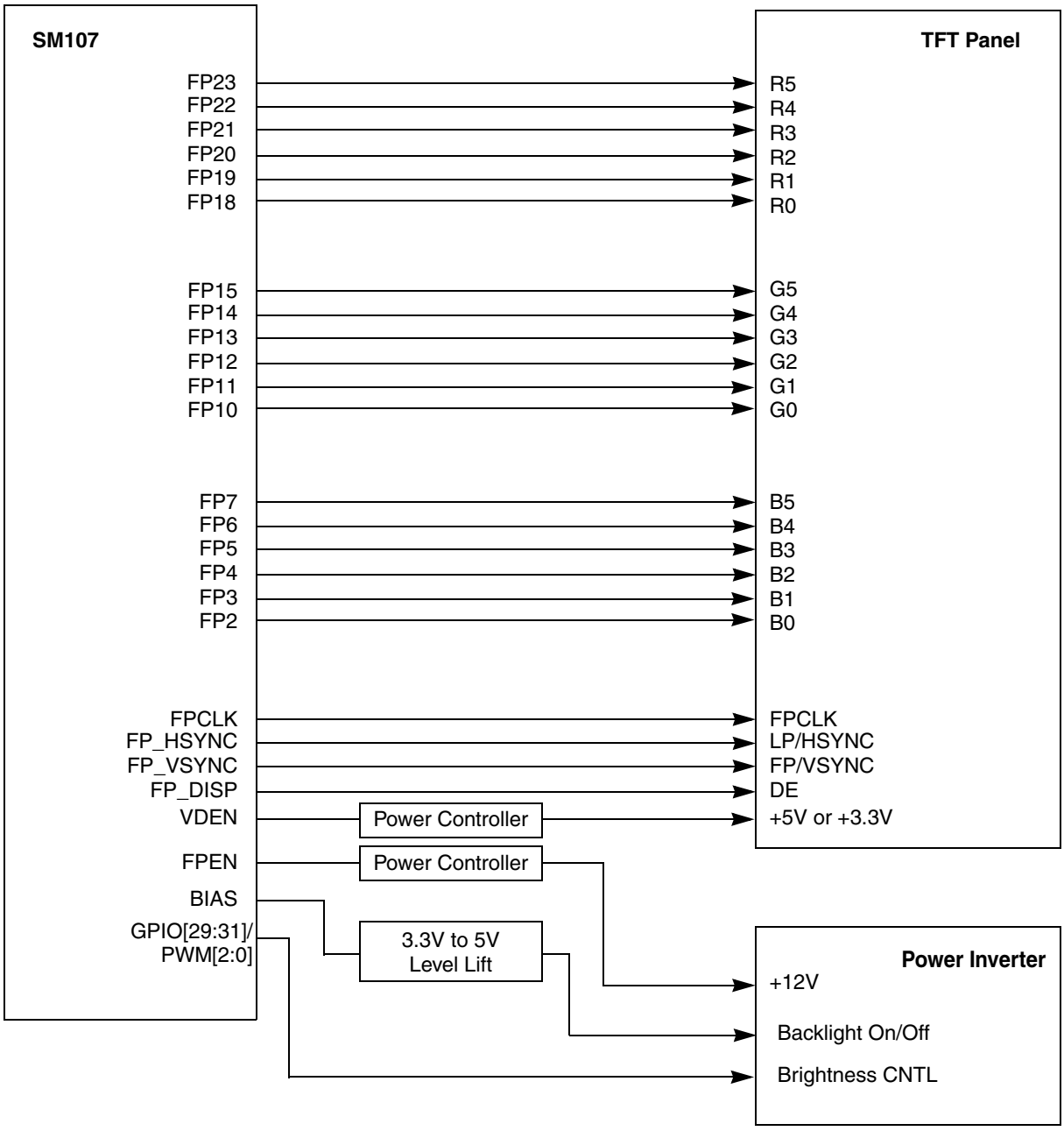


Figure 1-12 shows a typical interface between the SM107 and a 24-bit LVDS transmitter.

Figure 1-12: Typical 24-bit LVDS Interface (DS90C385)

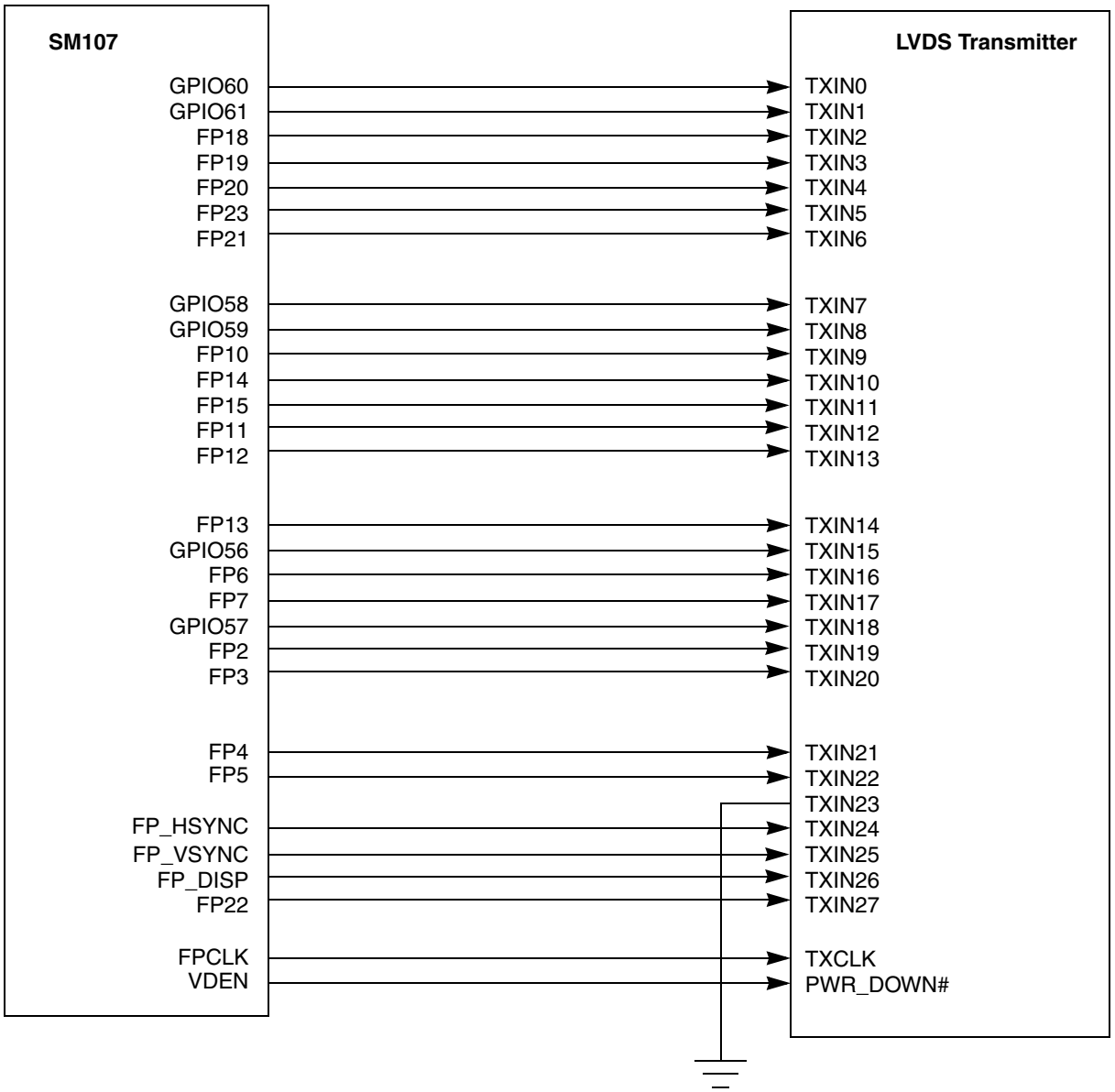


Table 1-2 compares the display data between the TFT panel, LVDS, and digital out.

Table 1-2: SM107 Display Data

	TFT Panel		LVDS	Digital Out[1]		CTSN (8 bit)			CTSN (12 bit)
	24-bit TFT[2]	18-bit TFT	DS90C385	1st Clock	2nd Clock	1st Clock	2nd Clock	3rd Clock	
GPIO63				G2	R4				
GPIO62				G1	R3				
FP23	R7	R5	TXIN5						R0
FP22	R6	R4	TXIN27						G0
FP21	R5	R3	TXIN6						B0
FP20	R4	R2	TXIN4						R1
FP19	R3	R1	TXIN3			R0	B2	G5	G1
FP18	R2	R0	TXIN2			G0	R3	B5	B1
GPIO61	R1		TXIN1	G0	R2				
GPIO60	R0		TXIN0	B4	R1				
FP15	G7	G5	TXIN11			B0	G3	R6	R2
FP14	G6	G4	TXIN10			R1	B3	G6	G2
FP13	G5	G3	TXIN14			G1	R4	B6	B2
FP12	G4	G2	TXIN13			B1	G4	R7	R3
FP11	G3	G1	TXIN12			R2	B4	G7	G3
FP10	G2	G0	TXIN9			G2	R5	B7	B3
GPIO59	G1		TXIN8	B3	R0				
GPIO58	G0		TXIN7	B2	G5				
FP7	B7	B5	TXIN17						
FP6	B6	B4	TXIN16						
FP5	B5	B3	TXIN22						
FP4	B4	B2	TXIN21						
FP3	B3	B1	TXIN20						
FP2	B2	B0	TXIN19						
GPIO57	B1		TXIN18	B1	G4				
GPIO56	B0		TXIN15	B0	G3				
GPIO55				2X Pixel Clock					

1. For Digital Out, program bit 25 of the Miscellaneous Control Register at offset 0x4 to 0 and bits [31:23] of the GPIO63:32 Control Register at offset 0xC to 0x1FF.
2. For 24-bit TFT, program bit 25 of the Miscellaneous Control Register at offset 0x4 to 1 and bits [29:24] of the GPIO[63:32] Control Register at offset 0xC to 0x3F.

Analog RGB (Analog LCD or CRT)

The analog RGB block contains a 24-bit DAC (RGB 8:8:8) to drive an external analog RGB interface. The 200 MHz DAC easily supports the maximum resolution of 1280 x 1024. See the *SM107 MMCC Design Guide* for information about interfacing the SM107 to analog RGB devices.

Internal Memory

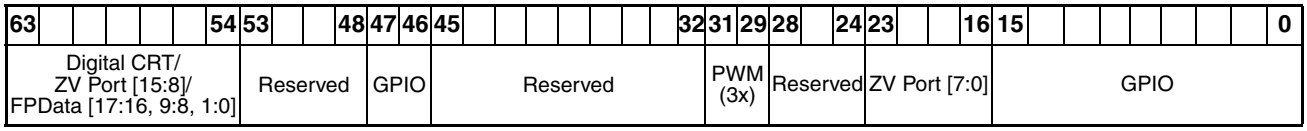
For designs using frame buffers, the SM107 allows the use of 4MB SDRAM internal to the SM107 MCB package. This allows minimal footprint impact to the system design as well as minimizing the layout and electrical constraints associated with using external SDRAM.

See the *SM107 MMCC Design Guide* for information about interfacing the SM107 to local memory.

GPIO

The SM107 provides 39 bits of GPIO. Figure 1-13 shows the layout of these bits.

Figure 1-13: GPIO Layout



The 24-bit TFT panel interface, 16-bit ZV port interface, and 8-bit Digital CRT interface are multiplexed. Four configurations can be supported with GPIO[63:56]:

- Configuration 1: 24-bit TFT panel interface and 8-bit ZV port interface
- Configuration 2: 18-bit TFT panel interface and 16-bit ZV port interface
- 18-bit TFT panel interface, 8-bit ZV port interface and 8-bit Digital CRT interface
- 18-bit TFT panel interface, two 8-bit ZV port interfaces

Table 1-3 shows the function summary for pins GPIO[63:55].

Table 1-3: Function Summary, GPIO[63:55]

GPIO	16-Bit ZV Port	Second ZV Port	Digital CRT	FP Data
55		ZVCLK	CLOCK	
56	ZV8	ZV0	DCRT0	FP0
57	ZV9	ZV1	DCRT1	FP1
58	ZV10	ZV2	DCRT2	FP8
59	ZV11	ZV3	DCRT3	FP9
60	ZV12	ZV4	DCRT4	FP16
61	ZV13	ZV5	DCRT5	FP17
62	ZV14	ZV6	DCRT6	
63	ZV15	ZV7	DCRT7	

The following sections define the special features of the GPIO.

ZV Port

Most ZV-compatible ICs support an 8-bit wide ZV port. The SM107 includes this functionality using GPIO pins 16:23. However, some ICs may only support a 16-bit ZV interface. To support these ICs, GPIO bits 56:63 may be used to add the extra 8 bits to the ZV interface.

Note: The upper 8 bits (bits 56:63) are multiplexed with the Digital CRT and Flat Panel Data [17:16,9:8,1:0].

PWM Interface

Three independent PWM outputs (bits 29:31 of GPIO) are provided for generic use. Each output has its own control register. Two PWMs have each three independently selectable frequencies. The third PWM has three selectable frequency multiples that are synchronized to the Video Sync signal.

Digital TV Encoder Interface

The SM107 supports an 8-bit digital RGB output (bits 55:63 of GPIO) to hook up to external TV encoders.

Note: These bits are multiplexed with ZV Port [15:8] and Flat Panel Data [17:16, 9:8, 1:0].

Strap Pins

GPIO pins 0 through 4, 7, 29, and 31 control the power-on configuration for the SM107 according to Table 1-4.

Table 1-4: GPIO Strap Pins

Pin	Default Strapping	Description
GPIO0	Pulled-down	Bus selection: 0: Host Bus. 1: PCI.
GPIO[2:1]	Pulled-down	Host Bus selection: 00: Hitachi SH3/SH4 host bus. 01: Intel XScale PXA250/PXA255 host bus. 11: NEC MIPS V_R4122/V_R4131 host bus.
GPIO3	Pulled-down	Clock select: 0: Internal PLL. 1: External test clock.
GPIO4	Pulled-down	Ready polarity for Hitachi SH series CPU: 0: Active low. 1: Active high.
GPIO7	Pulled-down	Clock divider reset control: 0: Do not reset clock divider. 1: Reset clock divider.
GPIO31, GPIO29	Pulled-down	XScale Host Clock Input Source 00: From internal clock generated by internal PLL. 01: From HCLK pin. 1x: From GPIO30 pin.

Flat Panel Data

The SM107 supports a native 18-bit panel interface, which can be extended to 24-bit by using GPIO bits 55-60. See the section entitled “Video Layers and Data Processing” on page 11 for a detailed list of how the 24-bit panel interface is connected.

Note: These bits are multiplexed with Digital TV Encoder and ZV Port [15:0].

DMA Controller

The SM107 supports a DMA controller that can move data from one memory bus to another. DMA1 is used to transfer data between or within memory buses.

Interrupt Controller

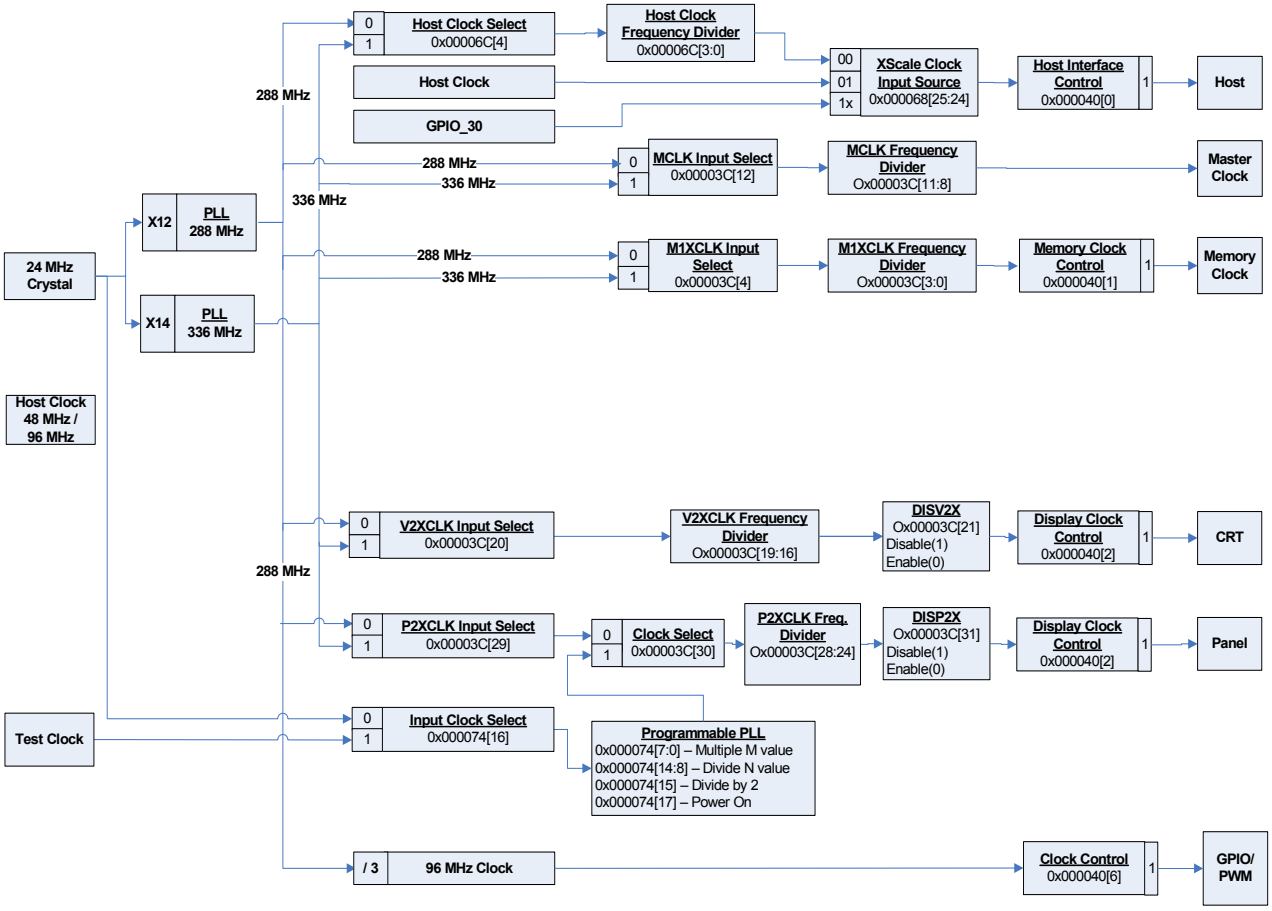
Because the SM107 has only one interrupt to the host bus, all internal interrupts are shared without priority.

One interrupt status register specifies which module(s) generated the interrupts and the software drivers are responsible for clearing the interrupt at the source. The Host Interrupt remains asserted as long as there is any bit set in the System Interrupt Status register.

Clock Control

The SM107 has one oscillator input and two external clock inputs. Figure 1-14 shows the clock tree for the SM107.

Figure 1-14: Clock Tree



Power Management

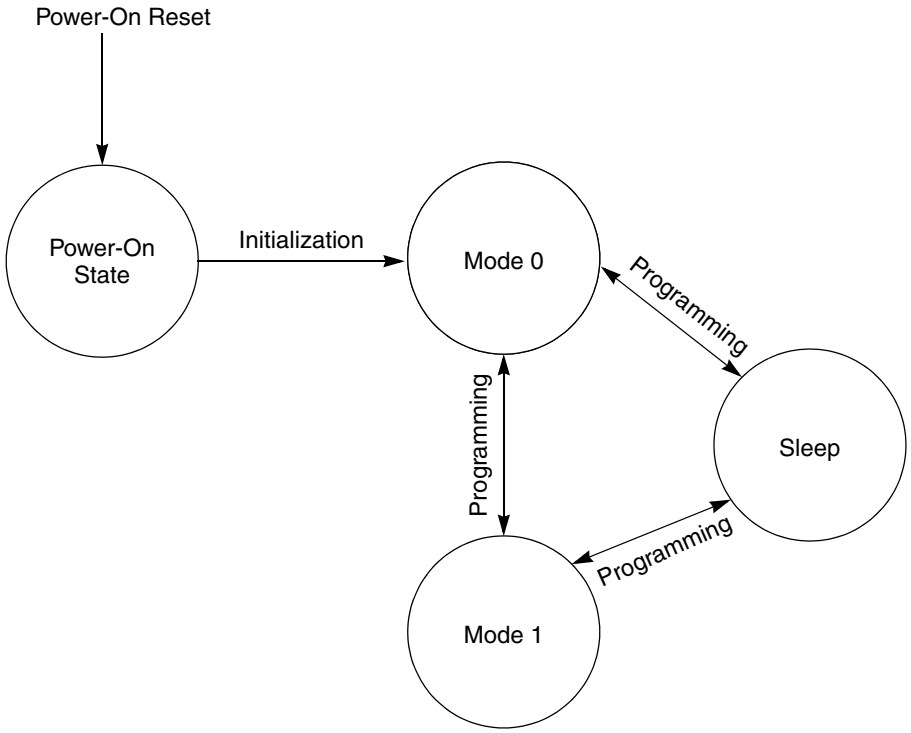
Figure 1-15 shows the possible power states the SM107 supports.

During power-on reset, the SM107 comes up in a predefined state with all I/O turned off, and running the lowest possible clock. The software is responsible for programming the Mode 0 power state to the requested state after power-on and transition into the Mode 0 power state.

The Mode 0 and Mode 1 power states are the same and fully under software control. Whenever the software decides that the SM107 must go into a different state, the software programs the non-active power state and transitions into that state. This way there are an infinite number of power states supported by software and makes power management very flexible.

The Sleep power state puts the SM107 into a sleep mode. In this mode the SDRAM is put into self-refresh mode, and the crystal and PLL circuits are turned off. The CLKOFF input pin is asserted by the system integrator to turn off the host clock inside the SM107 in order to reduce power consumption even further if the system integrator decides to do so.

Figure 1-15: Power State Diagram

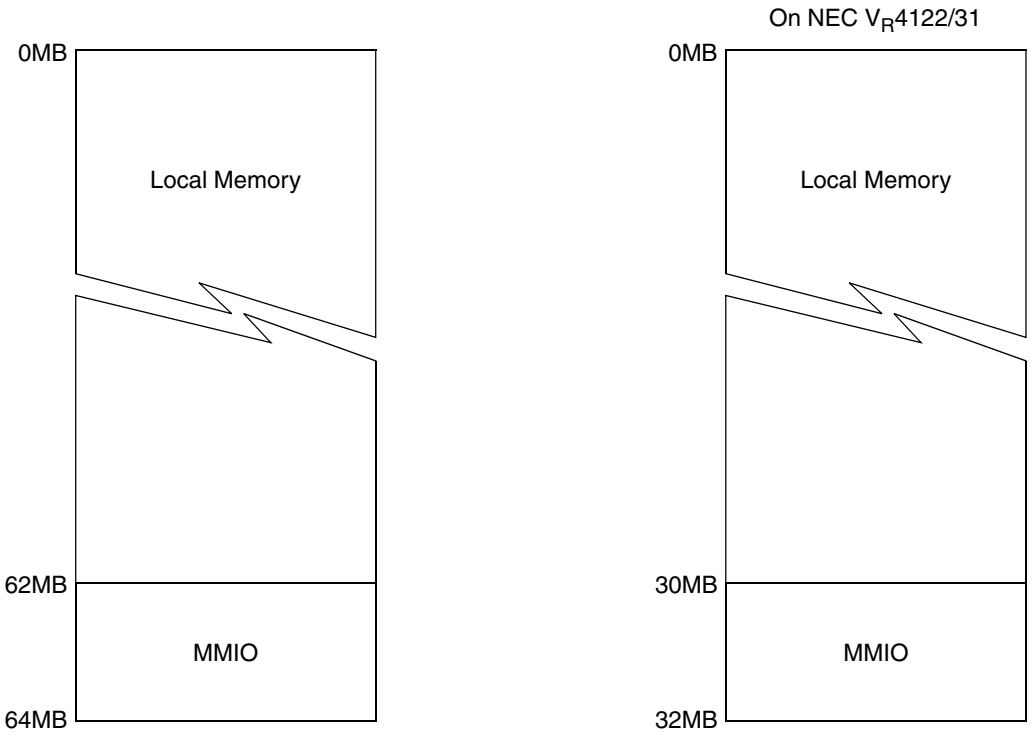


Note: The System Control registers are clocked in the Host clock domain and even shutting off the crystal and PLL circuits does not keep the System Control registers and the host bus from functioning. This way the software is always able to wake up the SM107 from sleep mode. In order to reduce even more power, the CLKOFF input pin should be used for gating the host clock.

Memory Map and Register Space

The memory map is a 64MB chunk divided into two chunks: a local memory space that includes the frame buffer and a memory-mapped I/O space. The size of the local memory depends on the amount of internal memory attached, which is 4MB. The MMIO space contains the SM107 register set. The Local Memory contains the actual frame buffer, 2D command lists, or any other data that can be directly accessed by one of the SM107's functional blocks.

Figure 1-16: Memory Map

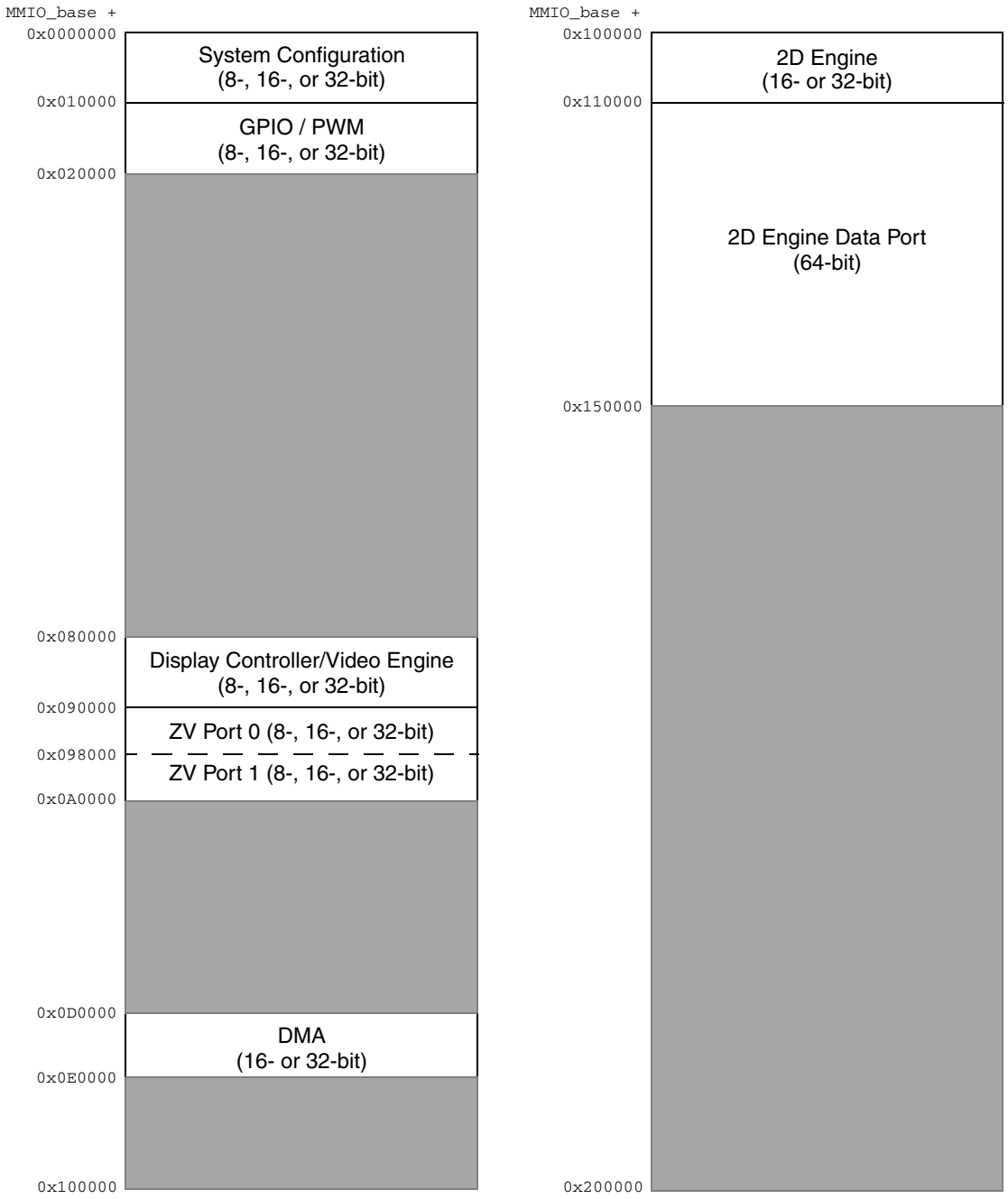


MMIO Space

The MMIO space contains the SM107 register set and is divided into separate 64kB blocks that hold the registers for each individual functional block of the SM107. If a functional block requires a data port to fill its FIFO, a separate 64kB block is specified for the data port.

Figure 1-17 shows the MMIO space. Note that the addresses are offsets from the MMIO base address. The MMIO base address is dependent upon which host processor is being used. Refer to Table 1-5 on page 24 for the different addresses.

Figure 1-17: MMIO Space



MMIO Addressing

For different bus interfaces, the MMIO address is decoded differently. Table 1-5 lists the different MMIO addresses for all possible host interfaces. Note that for the NEC MIPS Host Interface, the MMIO address can be programmed to be moved from 30MB (0x1E00000) to 62MB (0x3E00000) if a newer version of NEC MIPS supports 64MB I/O spaces instead of 32MB.

Table 1-5: MMIO Base Addresses for Host Interface

Host I/F	MMIO Address (MMIO_base address)	
	Power-Up	Programmable
Hitachi SH4	0x3E00000	N/A
Intel XScale	0x3E00000	N/A
NEC MIPS	0x1E00000	0x3E00000
PCI	N/A	PCI_CONFIG_14

2 System Configuration

Functional Overview

The SM107 has only one interrupt to the host bus. All internal interrupts are shared without priority.

Register Descriptions

The SM107 System Configuration Registers are located at base address `MMIO_base+0x0000000`, and contains 28 configuration registers. Every register is 32-bit DWORD aligned with offset addresses from 0x00 to 0x68. Not all of them are 32 bits wide; but if not specified, it should be reserved and read as defaults. Most of them are software programmable, i.e. both write and read, but some of them are set by hardware and should be read only.

Figure 2-1 shows how this 64kB region in the MMIO space is laid out. It contains the System Configuration registers that are clocked from the Host Bus domain, so they are always available as long as there is a host clock, even when all other internal blocks are turned off.

Figure 2-1: System Configuration Register Space

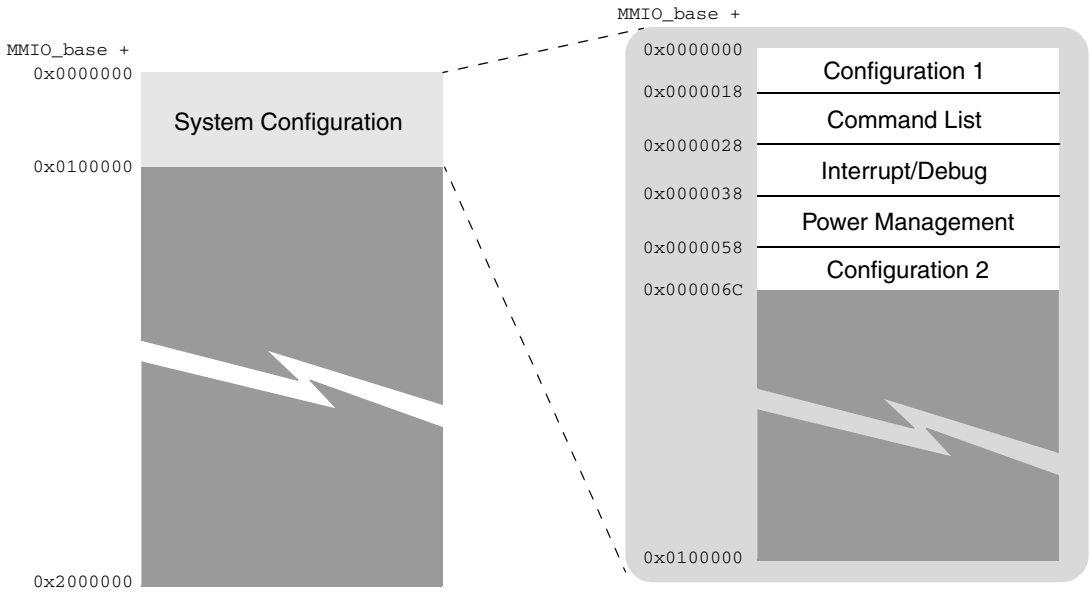


Table 2-1 shows the System Configuration Register offsets and general functions (Base Address: `MMIO_base`).

Table 2-1: SM107 System Configuration Register Summary

Address Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
Configuration 1				
0x000000	R/W	32	0b0000.0000.XX0X.X0XX. 0000.0000.0000.0000	System Control
0x000004	R/W	32	0b0000.0000.0000.00X0. 0001.0000.XXX0.0XXX	Miscellaneous Control
0x000008	R/W	32	0x00000000	$GPIO_{31:0}$ Control
0x00000C	R/W	32	0x00000000	$GPIO_{63:32}$ Control
0x000010	R/W	32	0bX000.0111.1111.0001. XXXX.X111.1100.0000	DRAM Control
0x000014	R/W	32	0x05146732	Arbitration Control
Command List				
0x000024	R	32	0000.0000.000X.XXXX. XXXX.X000.0000.0XXX	Command List Status
Interrupt/Debug				
0x000028	R	32	0x00000000	Raw Interrupt Status
0x000028	W	32	0x00000000	Raw Interrupt Clear
0x00002C	R	32	0x00000000	Interrupt Status
0x000030	R/W	32	0x00000000	Interrupt Mask
0x000034	R/W	32	0x00000000	Debug Control
Power Management				
0x000038	R	32	0x00021807	Current Gate
0x00003C	R	32	0x2A1A0A09	Current Clock
0x000040	R/W	32	0x00021807	Power Mode 0 Gate
0x000044	R/W	32	0x2A1A0A09	Power Mode 0 Clock
0x000048	R/W	32	0x00021807	Power Mode 1 Gate
0x00004C	R/W	32	0x2A1A0A09	Power Mode 1 Clock
0x000050	R/W	32	0x00018000	Sleep Mode Gate

Table 2-1: SM107 System Configuration Register Summary (Continued)

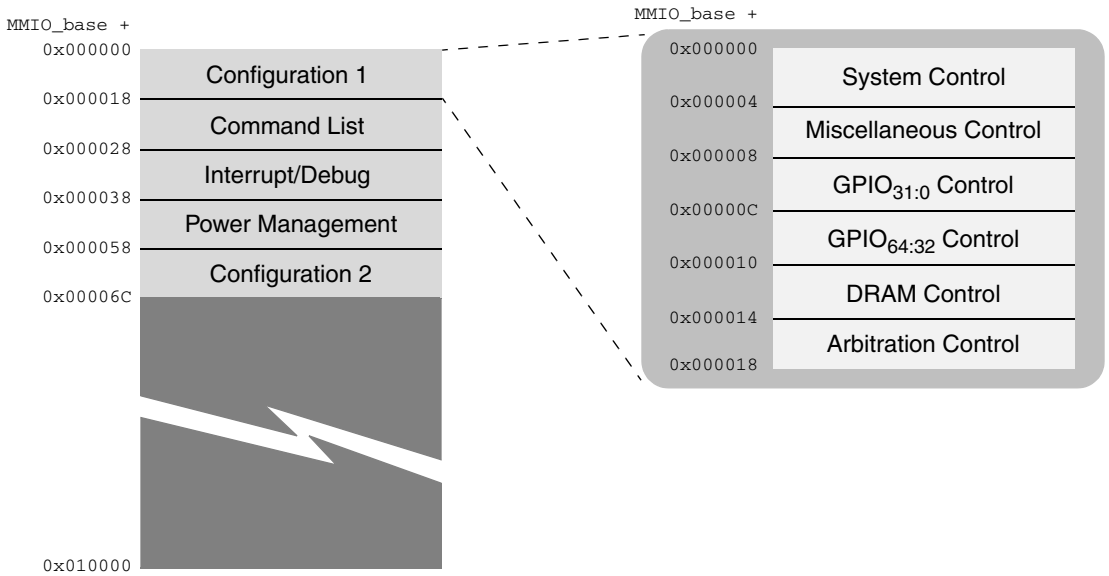
Address Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
0x000054	R/W	32	0x00000000	Power Mode Control
Configuration 2				
0x000058	R/W	32	0x00000000	PCI Master Base Address
0x00005C	R/W	32	0b0000.0000.0000.0000. 0000.0000.0000.0001	Endian Control
0x000060	R	32	0x050100A0	Device Id
0x000064	R	32	0x00000000	PLL Clock Count
0x000068	R/W	32	0x00090900	Miscellaneous Timing
0x00006C	R	32	0x00000009	Current System SDRAM Clock
0x000070	R/W	32	0x0000FFFF	Non-Cache Address
0x000074	R/W	32	0x0000FFFF	PLL Control

1. Refer to Table 1-5 on page 1-24 for MMIO_base values depending on the CPU.
2. In the reset values, “X” indicates don’t care.

Configuration 1 Register Descriptions

The Configuration registers control the way the SM107 chips operates. Figure 2-2 shows the layout of the configuration registers in Configuration Register Space 1.

Figure 2-2: Configuration Register Space 1



System Control

Read/Write MMIO_base + 0x000000

Power-on Default 0b0000.0100.XX0X.X0XX.0000.0000.0000.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPMS R/W		BE R/W	CsB R	SHARDY R/W		BM R/W	Lat R/W	PS R	VS R	Res	2E R	2B R	Res	CS R	ZvS R
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BrE R/W	Res	Abort R/W		Lck R/W	Res			Rty R/W	Clk R/W	BrS R/W		Res	CT R/W	MT R/W	PT R/W

Bit(s)	Name	Description
31:30	DPMS	<table><tr><th>31:30</th><th>Vertical Sync</th><th>Horizontal Sync</th></tr><tr><td>00</td><td>Pulsing</td><td>Pulsing</td></tr><tr><td>01</td><td>Pulsing</td><td>Not pulsing</td></tr><tr><td>10</td><td>Not pulsing</td><td>Pulsing</td></tr><tr><td>11</td><td>Not pulsing</td><td>Not pulsing</td></tr></table>
29	BE	PCI Burst Enable. 0: Disable. 1: Enable.
28	CsB	Color Space Conversion Status. This bit is read-only. 0: Idle. 1: Busy.
27:26	SHARDY	For the SH4 system-extend RDY signal. 00: One clock wide. 01: Two clocks wide. 1X: CS control.
25	BM	PCI Burst Master Control. 0: Stop PCI bus master. 1: Start PCI bus master.
24	Lat	PCI Latency Timer Enable. 0: Enable. 1: Disable.
23	PS	Panel Status. This bit is read-only. 0: Normal. 1: Flip pending.
22	VS	Video Status. This bit is read-only. 0: Normal. 1: Flip pending.
21	Res	This bit is reserved.
20	2E	2D Engine FIFO Status. This bit is read-only. 0: FIFO not empty. 1: FIFO empty.

Bit(s)	Name	Description
19	2B	2D Engine Status. This bit is read-only. 0: Idle. 1: Busy.
18	Res	This bit is reserved.
17	CS	CRT Status. This bit is read-only. 0: Normal. 1: Flip pending.
16	ZvS	ZV-Port Status. This bit is read-only. 0: Normal. 1: Vertical sync detected.
15	BrE	PCI Burst Read Enable. The BE bit must be enabled as well for this bit to take effect. 0: Disable. 1: Enable.
14	Res	This bit is reserved.
13:12	Abort	Drawing Engine Abort. 00: Normal. 11: Abort 2D engine.
11	Lck	Lock PCI Subsystem. 0: Unlocked. 1: Locked.
10:8	Res	These bits are reserved.
7	Rty	PCI Retry Enable. 0: Enable. 1: Disable.
6	Clk	PCI Clock Run Enable. 0: Disable. 1: Enable.
5:4	BrS	PCI Slave Burst Read Size. 00: 1 32-word. 01: 2 32-bit words. 10: 4 32-bit words. 11: 8 32-bit words.
3	Res	This bit is reserved.
2	CT	CRT Interface 3-State. 0: Normal. 1: 3-state.
1	MT	Local Memory Interface 3-State. 0: Normal. 1: 3-state.
0	PT	Panel Interface 3-State. 0: Normal. 1: 3-state.

Miscellaneous Control

Read/Write MMIO_base + 0x000004

Power-on Default 0b0000.0000.0000.00X0.0001.0000.XXX0.0XXX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Pad R/W		Res				FP R/W	Freq R/W	Res	Refresh R/W		Hold R/W			SH R/W	II R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL R/W	Gap R/W		DAC R/W	Res R/W	BL R/W	Res		CDR R G7	Test R T1 T0		VR R/W	Clk R G3	Bus R G2 G1 G0		

Bit(s)	Name	Description
31:30	Pad	PCI Pad Drive Strength. 00: 24 ma. 01: 12 ma. 10: 8 ma.
29:26	Res	These bits are reserved.
25	FP	Flat Panel Data Select (controls function of $GPIO_{63:32}$ Control[31:24]. 0: 8-bit (digital CRT). 1: 24-bit (24-bit panel).
24	Freq	Crystal Frequency Select. 0: 24MHz. 1: 12MHz.
23	Res	This bit is reserved.
22:21	Refresh	Internal Memory Refresh Control. 00: Refresh every 8µs. 01: Refresh every 16µs. 10: Refresh every 32µs. 11: Refresh every 64µs.
20:18	Hold	Bus Hold Time. 000: Hold bus until command FIFO is empty. 001: Hold bus for 8 transactions. 010: Hold bus for 16 transactions. 011: Hold bus for 24 transactions. 100: Hold bus for 32 transactions.
17	SH	Hitachi Ready Polarity. This bit is determined by the GPIO4 pin at reset. 0: (1) For SH series CPU, Active Low (2) For strapped SA1110 mode, the SRAM write shared with the SDRAM write. 1: (1) For SH series CPU, Active high. (2) For strapped SA1110 mode, the SRAM write is separated from the SDRAM write
16	II	Interrupt Inverting. 0: Normal. 1: Inverted.
15	PLL	PLL Clock Count. 0: Disable. 1: Enable.
14:13	Gap	DAC Band Gap Control. 00: Default.

Bit(s)	Name	Description
12	DAC	DAC Power Control. 0: Enable. 1: Disable.
11	Res	This bit is reserved.
10	BL	CPU Master Burst Length Select. 0: Burst of 8. 1: Burst of 1.
9:8	Res	These bits are reserved.
7	CDR	Clock Divider Reset Control. This bit is read-only and is determined by the GPIO7 pin at reset. 0: Do not reset clock divider. 1: Reset clock divider.
6:5	Test	Test Mode Select. These bits are read-only and are determined by the TEST0 and TEST1 pins at reset. 00: Normal mode. 01: Debugging mode. 10: Reserved. 11: Memory test mode.
4	VR	NEC Memory Map Select. 0: MMIO located at 30MB (`0x1E00000`). 1: MMIO located at 62MB (`0x3E00000`).
3	Clk	Clock Select. This bit is read-only and is determined by the GPIO3 pin at reset. 0: PLL. 1: Test clock (14.31818MHz).
2:0	Bus	Host Bus Type. These bits are read-only and are determined by the GPIO2, GPIO1, and GPIO0 pins at reset. 000: Hitachi SH3/SH4. 001: PCI. 010: Intel XScale. 110: NEC VR4122/31.

$GPIO_{31:0}$ Control

Read/Write MMIO_base + 0x000008

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
G_{31} R/W	G_{30} R/W	G_{29} R/W	Reserved					G_{23} R/W	G_{22} R/W	G_{21} R/W	G_{20} R/W	G_{19} R/W	G_{18} R/W	G_{17} R/W	G_{16} R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G_{15} R/W	G_{14} R/W	G_{13} R/W	G_{12} R/W	G_{11} R/W	G_{10} R/W	G_9 R/W	G_8 R/W	G_7 R/W	G_6 R/W	G_5 R/W	G_4 R/W	G_3 R/W	G_2 R/W	G_1 R/W	G_0 R/W

Bit(s)	Name	Description
31	G_{31}	GPIO Pin 31 Control. 0: GPIO. 1: PWM2 or Test Data[10].
30	G_{30}	GPIO Pin 30 Control. 0: GPIO. 1: PWM1 or Test Data[9].
29	G_{29}	GPIO Pin 29 Control. 0: GPIO. 1: PWM0 or Test Data[8].
28:24	Reserved	These bits are reserved.
23	G_{23}	GPIO Pin 23 Control. 0: GPIO. 1: ZV-Port[7] or Test Data[7].
22	G_{22}	GPIO Pin 22 Control. 0: GPIO. 1: ZV-Port[6] or Test Data[6].
21	G_{21}	GPIO Pin 21 Control. 0: GPIO. 1: ZV-Port[5] or Test Data[5].
20	G_{20}	GPIO Pin 20 Control. 0: GPIO. 1: ZV-Port[4] or Test Data[4].
19	G_{19}	GPIO Pin 19 Control. 0: GPIO. 1: ZV-Port[3] or Test Data[3].
18	G_{18}	GPIO Pin 18 Control. 0: GPIO. 1: ZV-Port[2] or Test Data[2].
17	G_{17}	GPIO Pin 17 Control. 0: GPIO. 1: ZV-Port[1] or Test Data[1].
16	G_{16}	GPIO Pin 16 Control. 0: GPIO. 1: ZV-Port[0] or Test Data[0].
15	G_{15}	GPIO Pin 15 Control. 0: GPIO. 1: Reserved.

Bit(s)	Name	Description
14	G_{14}	GPIO Pin 14 Control. 0: GPIO. 1: Reserved.
13	G_{13}	GPIO Pin 13 Control. 0: GPIO. 1: Reserved.
12	G_{12}	GPIO Pin 12 Control. 0: GPIO. 1: Reserved.
11	G_{11}	GPIO Pin 11 Control. 0: GPIO. 1: Reserved.
10	G_{10}	GPIO Pin 10 Control. 0: GPIO. 1: Reserved.
9	G_9	GPIO Pin 9 Control. 0: GPIO. 1: Reserved.
8	G_8	GPIO Pin 8 Control. 0: GPIO. 1: Reserved.
7	G_7	GPIO Pin 7 Control. 0: GPIO. 1: Reserved.
6	G_6	GPIO Pin 6 Control. 0: GPIO. 1: Reserved.
5	G_5	GPIO Pin 5 Control. 0: GPIO. 1: Reserved.
4	G_4	GPIO Pin 4 Control. 0: GPIO. 1: Reserved.
3	G_3	GPIO Pin 3 Control. 0: GPIO. 1: Reserved.
2	G_2	GPIO Pin 2 Control. 0: GPIO. 1: Reserved.
1	G_1	GPIO Pin 1 Control. 0: GPIO. 1: Reserved.
0	G_0	GPIO Pin 0 Control. 0: GPIO. 1: Reserved.

$GPIO_{63:32}$ Control

Read/Write MMIO_base + 0x00000C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
G_{63} R/W	G_{62} R/W	G_{61} R/W	G_{60} R/W	G_{59} R/W	G_{58} R/W	G_{57} R/W	G_{56} R/W	G_{55} R/W	Reserved						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved															

Bit(s)	Name	Description
31	G_{63}	GPIO Pin 63 Control. 0: GPIO & ZV-Port[15]. 1: Digital CRT[7] or Test Data [19].
30	G_{62}	GPIO Pin 62 Control. 0: GPIO & ZV-Port[14]. 1: Digital CRT[6] or Test Data [18].
29	G_{61}	GPIO Pin 61 Control. 0: GPIO & ZV-Port[13]. 1: Digital CRT[5], Flat Panel[17], or Test Data [17].
28	G_{60}	GPIO Pin 60 Control. 0: GPIO & ZV-Port[12]. 1: Digital CRT[4], Flat Panel[16], or Test Data [16].
27	G_{59}	GPIO Pin 59 Control. 0: GPIO & ZV-Port[11]. 1: Digital CRT[3], Flat Panel[9], or Test Data [15].
26	G_{58}	GPIO Pin 58 Control. 0: GPIO & ZV-Port[10]. 1: Digital CRT[2], Flat Panel[8], or Test Data [14].
25	G_{57}	GPIO Pin 57 Control. 0: GPIO & ZV-Port[9]. 1: Digital CRT[1], Flat Panel[1], or Test Data [13].
24	G_{56}	GPIO Pin 56 Control. 0: GPIO & ZV-Port[8]. 1: Digital CRT[0], Flat Panel[0], or Test Data [12].
23	G_{55}	GPIO Pin 55 Control. 0: GPIO. 1: Digital CRT Clock or Test Data [11].
22:0	Reserved	These bits are reserved.

DRAM Control

Read/Write MMIO_base + 0x000010

Power-on Default 0bX000.0111.1111.0001.XXXX.X111.1100.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														BwE R/W	Rfsh R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					BwC R/W	BwP R/W	AP R/W	Rst R/W	RA R/W	Reserved				Bks R/W	WP R/W

Bit(s)	Name	Description
31:18	Reserved	These bits are reserved.
17	BwE	Local Memory Block Write Enable. 0: Disabled. 1: Enabled.
16	Rfsh	Local Memory Refresh to Command Delay. 0: 10 clocks. 1: 12 clocks.
15:11	Reserved	These bits are reserved.
10	BwC	Local Memory Block Write Cycle Time. 0: 1 clock. 1: 2 clocks.
9	BwP	Local Memory Block Write to Pre-charge Delay. 0: 4 clocks. 1: 1 clock.
8	AP	Local Memory Active to Pre-charge Delay. 0: 6 clocks. 1: 7 clocks.
7	Rst	Local Memory Reset. 0: Reset. 1: Normal.
6	RA	Local Memory Remain in Active State. 0: Remain active. 1: Do not remain active.
5:2	Res	These bits are reserved.
1	Bks	Local Memory Number of Banks. 0: 4 banks. 1: 2 banks.
0	WP	Local Memory Write to Pre-charge Delay. 0: 2 clocks. 1: 1 clock.

Arbitration Control

Read/Write MMIO_base + 0x000014

Power-on Default 0x05146732

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Int R/W	Res					Panel R/W			Res	ZVPort R/W		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res	Command R/W			Res	DMA R/W			Res	Video R/W			Res	CRT R/W		

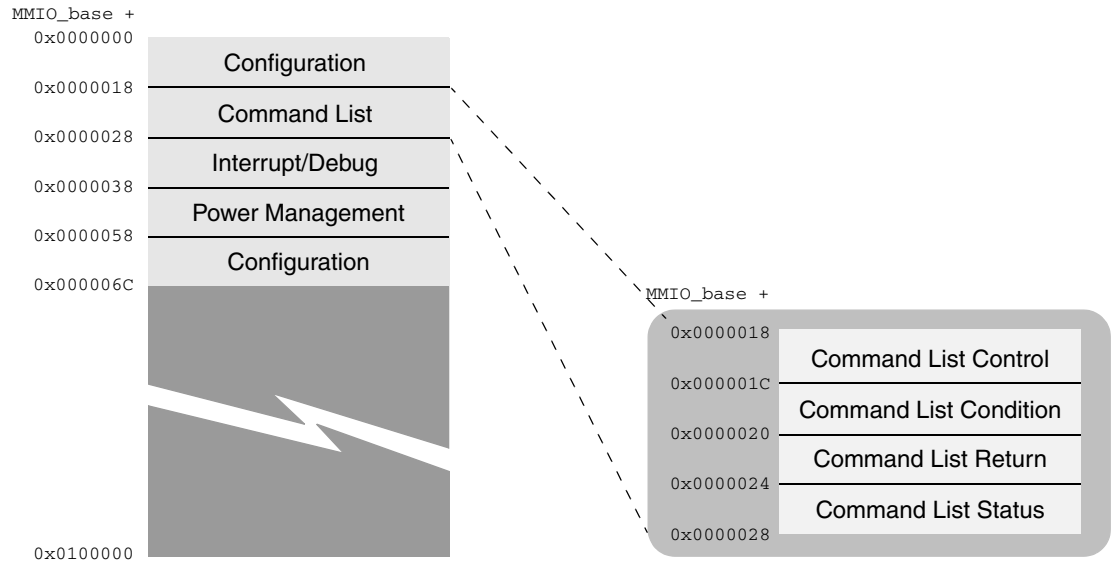
Bit(s)	Name	Description
31:29	Res	These bits are reserved.
28	Int	Internal Memory Priority Scheme. 0: Fixed priority. 1: Revolving priority.
27:23	Res	These bits are reserved.
22:20	Panel	Panel FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
19	Res	This bit is reserved.
18:16	ZVPort	ZV Port FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
15	Res	This bit is reserved.
14:12	Command	Command List Interpreter FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
11	Res	This bit is reserved.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th></tr>
<tr><td>10:8</td><td>DMA</td><td>DMA FIFO Priority.
<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
<tr><td>7</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>6:4</td><td>Video</td><td>Video FIFO Priority.
<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
<tr><td>3</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>2:0</td><td>CRT</td><td>CRT FIFO Priority.
<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
</table>

Command List Register Descriptions

The Command List registers control the Command List Interpreter. Figure 2-3 shows the layout of the registers that control the Command List Interpreter.

Figure 2-3: Command List Register Space



Command List Status

Read MMIO_base + 0x000024

Power-on Default 0b0000.0000.000X.XXXX.XXXX.X000.0000.0XXX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											2_M R	C_F R	2_C R	D_M R	C_S R
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
V_F R	V_S R	P_S R	S_C R	S_P R	Reserved								2_S R	2_F R	2_E R

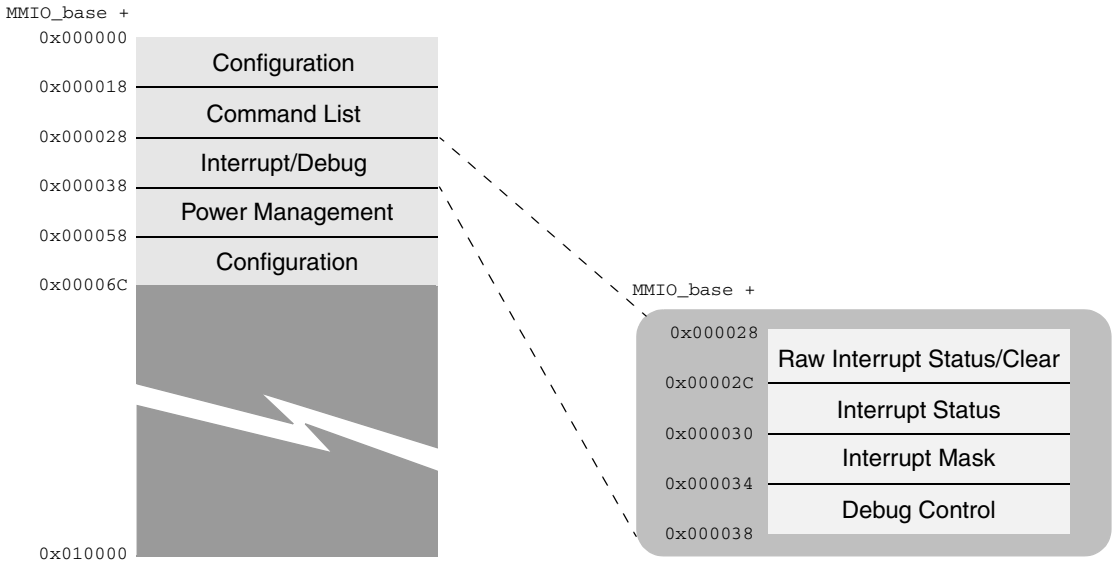
Bit(s)	Name	Description
31:21	Reserved	These bits are reserved.
20	2_M	2D Memory FIFO Status. 0: Not empty. 1: Empty.
19	C_F	Command FIFO on HIF bus. 0: Not empty. 1: Empty.

Bit(s)	Name	Description
18	2_C	2D Color Space Conversion Status. 0: Idle. 1: Busy.
17	D_M	Memory DMA Status. 0: Idle. 1: Busy.
16	C_S	CRT Graphics Layer Status. 0: No flip pending. 1: Flip in progress.
15	V_F	Current Video Field. 0: Odd. 1: Even.
14	V_S	Video Layer Status. 0: No flip pending. 1: Flip in progress.
13	P_S	Panel Graphics Layer Status. 0: No flip pending. 1: Flip in progress.
12	S_C	CRT Vertical Sync Status. 0: Not active. 1: Active.
11	S_P	Panel Vertical Sync Status. 0: Not active. 1: Active.
10:3	Reserved	These bits are reserved.
2	2_S	2D Setup Engine Status. 0: Idle. 1: Busy.
1	2_F	2D Command FIFO Status. 0: Not empty. 1: Empty.
0	2_E	2D Engine Status. 0: Idle. 1: Busy.

Interrupt / Debug Register Descriptions

The Interrupt / Debug registers reflect the status of interrupts, allow for enabling and disabling different interrupts and control which area of the chip is to be debugged in the Debugging Test Mode. Figure 2-4 lists the registers available in the Interrupt and Debug register space.

Figure 2-4: Interrupt / Debug Register Space



Raw Interrupt Status

Read MMIO_base + 0x000028

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved									ZV1 R/W	Res	ZV0 R/W	CV R/W	Res	PV R/W	CI R/W

Note: Write a 1 to clear; writing a 0 has no effect.

Bit(s)	Name	Description
31:7	Reserved	These bits are reserved.
6	ZV1	ZV-Port 1 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
5	Res	This bit is reserved.

Bit(s)	Name	Description
4	ZV0	ZV-Port 0 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
3	CV	CRT Vertical Sync Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
2	Res	This bit is reserved.
1	PV	Panel Vertical Sync Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
0	CI	Command Interpreter Interrupt Status. 0: Interrupt not active. 1: Interrupt active.

Raw Interrupt Clear

Write MMIO_base + 0x000028

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved									ZV0 W	Res	ZV0 W	CV W	Res	PV W	CI W

Note: Write a 1 to clear; writing a 0 has no effect.

Bit(s)	Name	Description
31:7	Reserved	These bits are reserved.
6	ZV1	ZV-Port 1 Interrupt Clear. 0: No action. 1: Clear interrupt.
5	Res	This bit is reserved.
4	ZV0	ZV-Port 0 Interrupt Clear. 0: No action. 1: Clear interrupt.
3	CV	CRT Vertical Sync Interrupt Clear. 0: No action. 1: Clear interrupt.
2	Res	This bit is reserved.
1	PV	Panel Vertical Sync Interrupt Clear. 0: No action. 1: Clear interrupt.
0	CI	Command Interpreter Interrupt Clear. 0: No action. 1: Clear interrupt.

Interrupt Status

Read MMIO_base + 0x00002C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	G_{54} R	Res							PW R	Res	DMA R	PCI R	Res		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res				CV R	Res						ZV1 R	2D R	ZV0 R	PV R	CI R

Bit(s)	Name	Description
31	Res	This bit is reserved.
30	G_{54}	GPIO Pin 54 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
29:23	Res	These bits are reserved.
22	PW	PWM Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
21	Res	This bit is reserved.
20	DMA	DMA Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
19	PCI	PCI Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
18:12	Res	These bits are reserved.
11	CV	CRT Vertical Sync Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
10:5	Res	These bits are reserved.
4	ZV1	ZV Port 1 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
3	2D	2D Engine Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
2	ZV0	ZV Port 0 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
1	PV	Panel Vertical Sync Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
0	CI	Command Interpreter Interrupt Status. 0: Interrupt not active. 1: Interrupt active.

Interrupt Mask

Read/Write MMIO_base + 0x000030

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	G_{54} R/W	Res							PW R/W	Res	DMA R/W	PCI R/W	Res		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res				CV R/W	Res						ZV1 R/W	2D R/W	ZV0 R/W	PV R/W	CI R/W

Bit(s)	Name	Description
31	Res	This bit is reserved.
30	G_{54}	GPIO Pin 54 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
29:23	Res	These bits are reserved.
22	PW	PWM Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
21	Res	This bit is reserved.
20	DMA	DMA Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
19	PCI	PCI Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
18:12	Res	These bits are reserved.
11	CV	CRT Vertical Sync Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
10:5	Res	These bits are reserved.
4	ZV1	ZV Port 1 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
3	2D	2D Engine Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
2	ZV0	ZV Port 0 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
1	PV	Panel Vertical Sync Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
0	CI	Command Interpreter Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.

Debug Control

Read/Write MMIO_base + 0x000034

Power-on Default 0x00000000

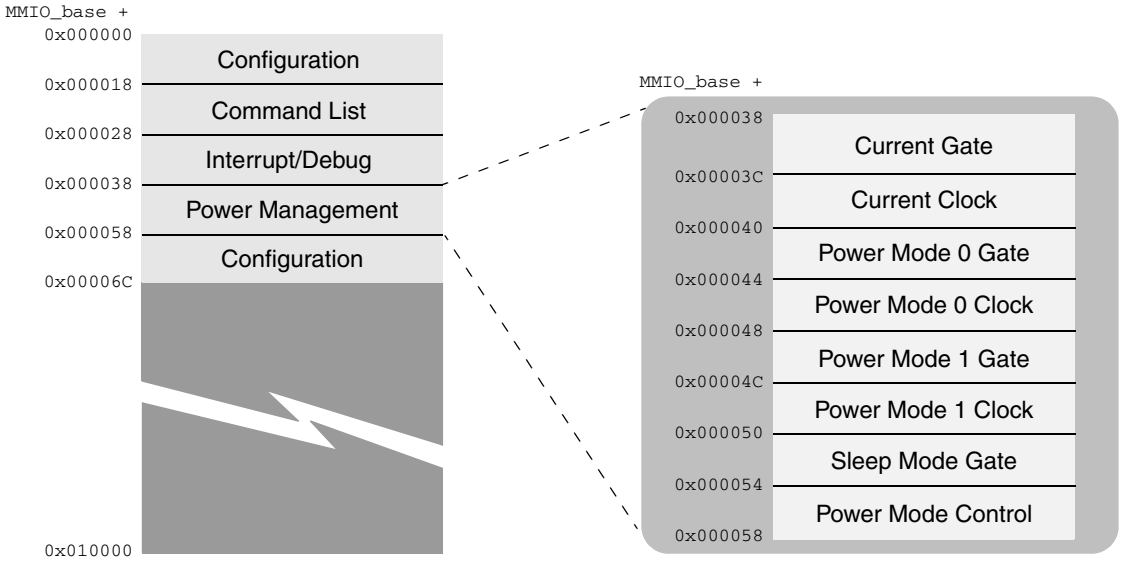
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved								Module R/W			Partition R/W				

Bit(s)	Name	Description
31:8	Reserved	These bits are reserved.
7:5	Module	Module Select for Partition.
4:0	Partition	Partition select for Debugging Test Mode. 00000: HIF controller 00010: PCI controller 00011: Command Interpreter 00100: Display controller 00101: ZV Port 00110: 2D Engine 01000: Local memory interface 11010: Local memory controller 11011: DMA 11100: Simulation test mode

Power Management Register Descriptions

The Power Management registers control which areas of the SM107 are running and at which speed. Figure 2-5 lists the registers available in the Power Management register space.

Figure 2-5: Power Management Register Space



Current Gate

Read MMIO_base + 0x000038

Power-on Default 0x00021807

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															PR
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OR	RR		Reserved						GR	ZVR	CR	2DR	DR	MR	HR

Bit(s)	Name	Description
31:17	Reserved	These bits are reserved.
16	P	PLL Control. 0: Enable. 1: Disable.
15	O	Oscillator Control. 0: Enable. 1: Disable.

Bit(s)	Name	Description
14:13	R	PLL Recovery Time. 00: 1ms. 01: 2ms. 10: 3ms. 11: 4ms.
12:7	Reserved	These bits are reserved.
6	G	GPIO and PWM Clock Control. 0: Disable. 1: Enable.
5	Z	ZV Port Clock Control. 0: Disable. 1: Enable.
4	C	Color Space Conversion Clock Control. 0: Disable. 1: Enable.
3	2D	2D Engine Clock Control. 0: Disable. 1: Enable.
2	D	Display Controller Clock Control. 0: Disable. 1: Enable.
1	M	Memory Controller Clock Control. 0: Disable. 1: Enable.
0	H	Host Interface, Command Interpreter, and DMA Clock Control. 0: Disable. 1: Enable.

Current Clock

Read MMIO_base + 0x00003C

Power-on Default 0x2A1A0A09

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DISP2X R	$P2_S$ R		P2 R					Reserved		DISV2X R	$V2_S$ R	V2 R			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			M_S R	M R				Reserved			$M1_S$ R	M1 R			

Bit(s)	Name	Description
31	DISP2X	Disable 2X P2XCLK. 0: Normal. 1: 1X clock for P2XCLK.
30:29	$P2_S$	P2XCLK Frequency Input Select. 00: 288 MHz. 01: 336 MHz. 1X: Select programmable PLL.
28:24	P2	P2XCLK Frequency Divider.
23:22	Reserved	These bits are reserved.
21	DISV2X	Disable 2X V2XCLK. 0: Normal. 1: No need to feed 2X VCLK.
20	$V2_S$	V2XCLK Frequency Input Select. 0: 288 MHz. 1: 336 MHz.
19:16	V2	V2XCLK Frequency Divider.
15:13	Reserved	These bits are reserved.

00000	÷ 1	01000	÷ 3	10000	÷ 5		
00001	÷ 2	01001	÷ 6	10001	÷ 10		
00010	÷ 4	01010	÷ 12	10010	÷ 20		
00011	÷ 8	01011	÷ 24	10011	÷ 40		
00100	÷ 16	01100	÷ 48	10100	÷ 80		
00101	÷ 32	01101	÷ 96	10101	÷ 160		
00110	÷ 64	01110	÷ 192	10110	÷ 320		
00111	÷ 128	01111	÷ 384	10111	÷ 640		

0000	÷ 1	0100	÷ 16	1000	÷ 3	1100	÷ 48
0001	÷ 2	0101	÷ 32	1001	÷ 6	1101	÷ 96
0010	÷ 4	0110	÷ 64	1010	÷ 12	1110	÷ 192
0011	÷ 8	0111	÷ 128	1011	÷ 24	1111	÷ 384

Bit(s)	Name	Description
12	M_S	MCLK Frequency Input Select. 0: 288 MHz. 1: 336 MHz.
11:8	M	MCLK Frequency Divider. 0000 ÷ 1, 0100 ÷ 16, 1000 ÷ 3, 1100 ÷ 48 0001 ÷ 2, 0101 ÷ 32, 1001 ÷ 6, 1101 ÷ 96 0010 ÷ 4, 0110 ÷ 64, 1010 ÷ 12, 1110 ÷ 192 0011 ÷ 8, 0111 ÷ 128, 1011 ÷ 24, 1111 ÷ 384
7:5	Reserved	These bits are reserved.
4	$M1_S$	M1XCLK Frequency Input Select. 0: 288 MHz. 1: 336 MHz.
3:0	M1	M1XCLK Frequency Divider. 0000 ÷ 1, 0100 ÷ 16, 1000 ÷ 3, 1100 ÷ 48 0001 ÷ 2, 0101 ÷ 32, 1001 ÷ 6, 1101 ÷ 96 0010 ÷ 4, 0110 ÷ 64, 1010 ÷ 12, 1110 ÷ 192 0011 ÷ 8, 0111 ÷ 128, 1011 ÷ 24, 1111 ÷ 384

Power Mode 0 Gate

Read/Write MMIO_base + 0x000040

Power-on Default 0x00021807

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved									G R/W	ZV R/W	C R/W	2D R/W	D R/W	M R/W	H R/W

Bit(s)	Name	Description
31:7	Reserved	These bits are reserved.
6	G	GPIO and PWM Clock Control. 0: Disable. 1: Enable.
5	Z	ZV Port Clock Control. 0: Disable. 1: Enable.

Bit(s)	Name	Description
4	C	Color Space Conversion Clock Control. 0: Disable. 1: Enable.
3	2D	2D Engine Clock Control. 0: Disable. 1: Enable.
2	D	Display Controller Clock Control. 0: Disable. 1: Enable.
1	M	Memory Controller Clock Control. 0: Disable. 1: Enable.
0	H	Host Interface, Command Interpreter, and DMA Clock Control. 0: Disable. 1: Enable.

Power Mode 0 Clock

Read/Write MMIO_base + 0x000044

Power-on Default 0x2A1A0A09

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIS2XP R/W	$P2_S$ R/W		P2 R/W					Reserved		DIS2XV R/W	$V2_S$ R/W	V2 R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			M_S R/W	M R/W				Reserved			$M1_S$ R/W	M1 R/W			

Bit(s)	Name	Description
31	DIS2XP	Disable 2X P2XCLK. 0: Normal. 1: 1X clock for P2XCLK.
30:29	$P2_S$	P2XCLK Frequency Input Select. 00: 288 MHz. 01: 336 MHz. 1X: Select programmable PLL.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th></tr>
<tr><td>28:24</td><td>P2</td><td>P2XCLK Frequency Divider.
<table>
<tr><td>00000</td><td>÷ 1</td><td>01000</td><td>÷ 3</td><td>10000</td><td>÷ 5</td></tr>
<tr><td>00001</td><td>÷ 2</td><td>01001</td><td>÷ 6</td><td>10001</td><td>÷ 10</td></tr>
<tr><td>00010</td><td>÷ 4</td><td>01010</td><td>÷ 12</td><td>10010</td><td>÷ 20</td></tr>
<tr><td>00011</td><td>÷ 8</td><td>01011</td><td>÷ 24</td><td>10011</td><td>÷ 40</td></tr>
<tr><td>00100</td><td>÷ 16</td><td>01100</td><td>÷ 48</td><td>10100</td><td>÷ 80</td></tr>
<tr><td>00101</td><td>÷ 32</td><td>01101</td><td>÷ 96</td><td>10101</td><td>÷ 160</td></tr>
<tr><td>00110</td><td>÷ 64</td><td>01110</td><td>÷ 192</td><td>10110</td><td>÷ 320</td></tr>
<tr><td>00111</td><td>÷ 128</td><td>01111</td><td>÷ 384</td><td>10111</td><td>÷ 640</td></tr>
</table></td></tr>
<tr><td>23:22</td><td>Reserved</td><td>These bits are reserved.</td></tr>
<tr><td>21</td><td>DIS2XV</td><td>Disable 2X V2XCLK.
0: Normal.
1: No need to feed 2X VCLK.</td></tr>
<tr><td>20</td><td>$V2_S$</td><td>V2XCLK Frequency Input Select.
0: 288 MHz.
1: 336 MHz.</td></tr>
<tr><td>19:16</td><td>V2</td><td>V2XCLK Frequency Divider.
<table>
<tr><td>0000</td><td>÷ 1</td><td>0100</td><td>÷ 16</td><td>1000</td><td>÷ 3</td><td>1100</td><td>÷ 48</td></tr>
<tr><td>0001</td><td>÷ 2</td><td>0101</td><td>÷ 32</td><td>1001</td><td>÷ 6</td><td>1101</td><td>÷ 96</td></tr>
<tr><td>0010</td><td>÷ 4</td><td>0110</td><td>÷ 64</td><td>1010</td><td>÷ 12</td><td>1110</td><td>÷ 192</td></tr>
<tr><td>0011</td><td>÷ 8</td><td>0111</td><td>÷ 128</td><td>1011</td><td>÷ 24</td><td>1111</td><td>÷ 384</td></tr>
</table></td></tr>
<tr><td>15:13</td><td>Reserved</td><td>These bits are reserved.</td></tr>
<tr><td>12</td><td>M_S</td><td>MCLK Frequency Input Select.
0: 288 MHz.
1: 336 MHz.</td></tr>
<tr><td>11:8</td><td>M</td><td>MCLK Frequency Divider.
<table>
<tr><td>0000</td><td>÷ 1</td><td>0100</td><td>÷ 16</td><td>1000</td><td>÷ 3</td><td>1100</td><td>÷ 48</td></tr>
<tr><td>0001</td><td>÷ 2</td><td>0101</td><td>÷ 32</td><td>1001</td><td>÷ 6</td><td>1101</td><td>÷ 96</td></tr>
<tr><td>0010</td><td>÷ 4</td><td>0110</td><td>÷ 64</td><td>1010</td><td>÷ 12</td><td>1110</td><td>÷ 192</td></tr>
<tr><td>0011</td><td>÷ 8</td><td>0111</td><td>÷ 128</td><td>1011</td><td>÷ 24</td><td>1111</td><td>÷ 384</td></tr>
</table></td></tr>
<tr><td>7:5</td><td>Reserved</td><td>These bits are reserved.</td></tr>
</table>

Bit(s)	Name	Description
4	$M1_S$	M1XCLK Frequency Input Select. 0: 288 MHz. 1: 336 MHz.
3:0	M21	M1XCLK Frequency Divider. 0000 ÷ 1, 0100 ÷ 16, 1000 ÷ 3, 1100 ÷ 48 0001 ÷ 2, 0101 ÷ 32, 1001 ÷ 6, 1101 ÷ 96 0010 ÷ 4, 0110 ÷ 64, 1010 ÷ 12, 1110 ÷ 192 0011 ÷ 8, 0111 ÷ 128, 1011 ÷ 24, 1111 ÷ 384

Power Mode 1 Gate

Read/Write MMIO_base + 0x000048

Power-on Default 0x00021807

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved									G R/W	ZV R/W	O R/W	2D R/W	D R/W	M R/W	H R/W

Bit(s)	Name	Description
31:7	Reserved	These bits are reserved.
6	G	GPIO and PWM Clock Control. 0: Disable. 1: Enable.
5	Z	ZV Port Clock Control. 0: Disable. 1: Enable.
4	C	Color Space Conversion Clock Control. 0: Disable. 1: Enable.
3	2D	2D Engine Clock Control. 0: Disable. 1: Enable.
2	D	Display Controller Clock Control. 0: Disable. 1: Enable.
1	M	Memory Controller Clock Control. 0: Disable. 1: Enable.
0	H	Host Interface, Command Interpreter, and DMA Clock Control. 0: Disable. 1: Enable.

Power Mode 1 Clock

Read/Write MMIO_base + 0x00004C

Power-on Default 0x2A1A0A09

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIS2XP R/W	$P2_S$ R/W		P2 R/W					Reserved		DIS2XV R/W	$V2_S$ R/W	V2 R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			M_S R/W	M R/W				Reserved			$M1_S$ R/W	M1 R/W			

Bit(s)	Name	Description
31	DIS2XP	Disable 2X P2XCLK. 0: Normal. 1: 1X clock for P2XCLK.
30:29	$P2_S$	P2XCLK Frequency Input Select. 00: 288 MHz. 01: 336 MHz. 1X: Select programmable PLL.
28:24	P2	P2XCLK Frequency Divider. 00000 ÷ 1 | 01000 ÷ 3 | 10000 ÷ 5 00001 ÷ 2 | 01001 ÷ 6 | 10001 ÷ 10 00010 ÷ 4 | 01010 ÷ 12 | 10010 ÷ 20 00011 ÷ 8 | 01011 ÷ 24 | 10011 ÷ 40 00100 ÷ 16 | 01100 ÷ 48 | 10100 ÷ 80 00101 ÷ 32 | 01101 ÷ 96 | 10101 ÷ 160 00110 ÷ 64 | 01110 ÷ 192 | 10110 ÷ 320 00111 ÷ 128 | 01111 ÷ 384 | 10111 ÷ 640
23:22	Reserved	These bits are reserved.
21	DIS2XV	Disable 2X V2XCLK. 0: Normal. 1: No need to feed 2X VCLK.
20	$V2_S$	V2XCLK Frequency Input Select. 0: 288 MHz. 1: 336 MHz.
19:16	V2	V2XCLK Frequency Divider. 0000 ÷ 1 | 0100 ÷ 16 | 1000 ÷ 3 | 1100 ÷ 48 0001 ÷ 2 | 0101 ÷ 32 | 1001 ÷ 6 | 1101 ÷ 96 0010 ÷ 4 | 0110 ÷ 64 | 1010 ÷ 12 | 1110 ÷ 192 0011 ÷ 8 | 0111 ÷ 128 | 1011 ÷ 24 | 1111 ÷ 384
15:13	Reserved	These bits are reserved.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th></tr>
<tr><td>12</td><td>M_S</td><td>MCLK Frequency Input Select.
0: 288 MHz.
1: 336 MHz.</td></tr>
<tr><td>11:8</td><td>M</td><td>MCLK Frequency Divider.
<table>
<tr><td>0000</td><td>÷ 1</td><td>0100</td><td>÷ 16</td><td>1000</td><td>÷ 3</td><td>1100</td><td>÷ 48</td></tr>
<tr><td>0001</td><td>÷ 2</td><td>0101</td><td>÷ 32</td><td>1001</td><td>÷ 6</td><td>1101</td><td>÷ 96</td></tr>
<tr><td>0010</td><td>÷ 4</td><td>0110</td><td>÷ 64</td><td>1010</td><td>÷ 12</td><td>1110</td><td>÷ 192</td></tr>
<tr><td>0011</td><td>÷ 8</td><td>0111</td><td>÷ 128</td><td>1011</td><td>÷ 24</td><td>1111</td><td>÷ 384</td></tr>
</table></td></tr>
<tr><td>7:5</td><td>Reserved</td><td>These bits are reserved.</td></tr>
<tr><td>4</td><td>$M1_S$</td><td>M1XCLK Frequency Input Select.
0: 288 MHz.
1: 336 MHz.</td></tr>
<tr><td>3:0</td><td>M1</td><td>M1XCLK Frequency Divider.
<table>
<tr><td>0000</td><td>÷ 1</td><td>0100</td><td>÷ 16</td><td>1000</td><td>÷ 3</td><td>1100</td><td>÷ 48</td></tr>
<tr><td>0001</td><td>÷ 2</td><td>0101</td><td>÷ 32</td><td>1001</td><td>÷ 6</td><td>1101</td><td>÷ 96</td></tr>
<tr><td>0010</td><td>÷ 4</td><td>0110</td><td>÷ 64</td><td>1010</td><td>÷ 12</td><td>1110</td><td>÷ 192</td></tr>
<tr><td>0011</td><td>÷ 8</td><td>0111</td><td>÷ 128</td><td>1011</td><td>÷ 24</td><td>1111</td><td>÷ 384</td></tr>
</table></td></tr>
</table>

Sleep Mode Gate

Read/Write MMIO_base + 0x000050

Power-on Default 0x00018000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									D R/W				Reserved		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res	R R/W		Reserved												

Bit(s)	Name	Description
31:23	Reserved	These bits are reserved.
22:19	D	PLL Recovery Clock Divider. 0000 ÷ 4096 | 0100 ÷ 256 | 1000 ÷ 16 0001 ÷ 2048 | 0101 ÷ 128 | 1001 ÷ 8 0010 ÷ 1024 | 0110 ÷ 64 | 1010 ÷ 4 0011 ÷ 512 | 0111 ÷ 32 | 1011 ÷ 2 Internally, the PLL recovery time counters are based on a 32µs clock. So you have to program the *D* field to make the host clock come as close to 32µs as possible.
18:15	Reserved	These bits are reserved.
14:13	R	PLL Recovery. 00: 1ms (32 counts). 01: 2ms (64 counts). 10: 3ms (96 counts). 11: 4ms (128 counts).
12:0	Reserved	These bits are reserved.

Power Mode Control

Read/Write MMIO_base + 0x000054

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved													S R/W	Mode R/W	

Bit(s)	Name	Description
31:3	Reserved	These bits are reserved.
2	S	Current Sleep Status. 0: Not in sleep mode. 1: In sleep mode. When the SM107 is transitioning back from sleep mode to a normal power mode (Modes 0 or 1), the software needs to poll this bit until it becomes “0” before writing any other commands to the chip.
1:0	Mode	Power Mode Select. 00: Power Mode 0. 01: Power Mode 1. 10: Sleep Mode.

Clock Multiply PLLs

An external crystal combined with the on-chip oscillator provides the SM107 clock source. The external crystal frequency should be fixed at 24 MHz ±5%.

The SM107 contains three clock multiply PLLs:

- PLL0

  Input frequency = 24 MHz oscillator
  Output frequency = Input frequency x 4 = 96 MHz fixed

- PLL1

  Input frequency = Output of PLL0 / 2 = 48 MHz
  Output frequency = Input frequency x 6 = 288 MHz fixed

- PLL2

  Input frequency = Output of PLL0 / 2 = 48 MHz
  The output of PLL2 = 48 MHz x 7 = 336 MHz

Power Mode 0, Power Mode 1, and Sleep Mode

There are two operational power modes (Power Mode 0 and Power Mode 1) and Sleep Mode. Each operational power mode has its own Power Mode Gate register to control the clock gating for each functional block. Each operational power mode also has its own Power Mode Clock register that selects the different clock frequencies for each clock branch. In Sleep Mode, all clocks are shut down.

The power mode switch should be controlled by power management software; for example, Power Mode 0 can be programmed to a high clock rate for maximum performance. Power Mode 1 can be programmed to a lower clock rate for sustaining operation.

The Power Mode Control Register at MMIO_base + `0x000054` determines the power mode selection as follows:

- Bits [1:0] = 00, select Power Mode 0 (power on default).
- Bits [1:0] = 01, select Power Mode 1.
- Bits [1:0] = 10, Sleep Mode. The PLLs and the oscillator are shut down in this mode.
- Bits [1:0] = 11, Reserved.

In Power Mode 0, the Power Mode 0 Clock Register at MMIO_base + `0x000044` controls the clock settings. The default of the Power Mode 0 Clock Register is `0x2A1A0A09`. The Power Mode 0 Gate Register at MMIO_base + `0x000040` controls clock gating. The default of the Power Mode 0 Gate Register is `0x00021807`.

In Power Mode 1, Power Mode 1 Clock Register at MMIO_base + `0x00004C` controls the clock settings. The default of the Power Mode 1 Clock Register is `0x2A1A0A09`. The Power Mode 1 Gate Register at MMIO_base + `0x000048` controls clock gating. The default of the Power Mode 1 Gate Register is `0x00021807`.

Adjusting the Clock Frequency

There are five clock branches that can be programmed through the Power Mode 0 Clock, Power Mode 1 Clock, and Miscellaneous Timing registers:

Table 2-2: Programmable Clock Branches

Clock	Description
P2XCLK	2X clock source for the Panel interface timing. The actual rate at which the pixels are shifted out is P2XCLK divided by two.
V2XCLK	2X clock source for the CRT interface timing. The actual rate at which the pixels are shifted out is V2XCLK divided by two.
M1XCLK	Clock source for the local SDRAM controller.
MCLK	Main clock source for all functional blocks, such as the 2D engine, GPIO, Video Engine, DMA Engine.
SYSCLK	Clock source for the system memory (CPU memory) controller. This clock also can be selected as the XScale CPU interface logic clock.

In the Miscellaneous Timing Register (MMIO_base + 0x000068):

- Bits [20:16]: SYSCLK control if Power Mode 1 is selected. The power-on default for these bits is 0x09.
- Bits [12:8]: SYSCLK control if Power Mode 0 is selected. The power-on default for these bits is 0x09.

Current Gate and Current Clock Registers

The Current Gate (MMIO_base + 0x000038) and Current Clock (MMIO_base + 0x00003C) registers are read-only registers that reflect the current clock control selection. When Power Mode 0 is selected, the value read from this register should be the same as the value in the Power Mode 0 Clock register.

Rules to Program the Power Mode Clock Registers for Clock Selection

1. There should be only one clock source changed at a time. To change clock source for P2XCLK, V2XCLK, MCLK, M1XCLK simultaneously may cause the internal logic normal operation to be disrupted. There should be a minimum of **16ms wait** from change one clock source to another.

2. When adjusting the clock rate, the PLL selection bit should be programmed first before changing the divider value for each clock source. For example, to change the P2XCLK clock rate:
   - bit 29 should be set first
   - wait for a minimum of 16ms (about one Vsync time)
   - adjust bits [28:24].

   The minimum 16 ms wait is necessary for logic to settle down before the clock rate is changed.
3. There should be a minimum 16 ms wait after a clock source is changed before any operation that could result in a bus transaction.

Power Down (Sleep Mode)

There are three ways to power down the SM107 chip (sleep mode):

1. For CPU local bus interface only:
   MMIO_base + 0x000068, bit 6 = 0; disable PCI ACPI mode

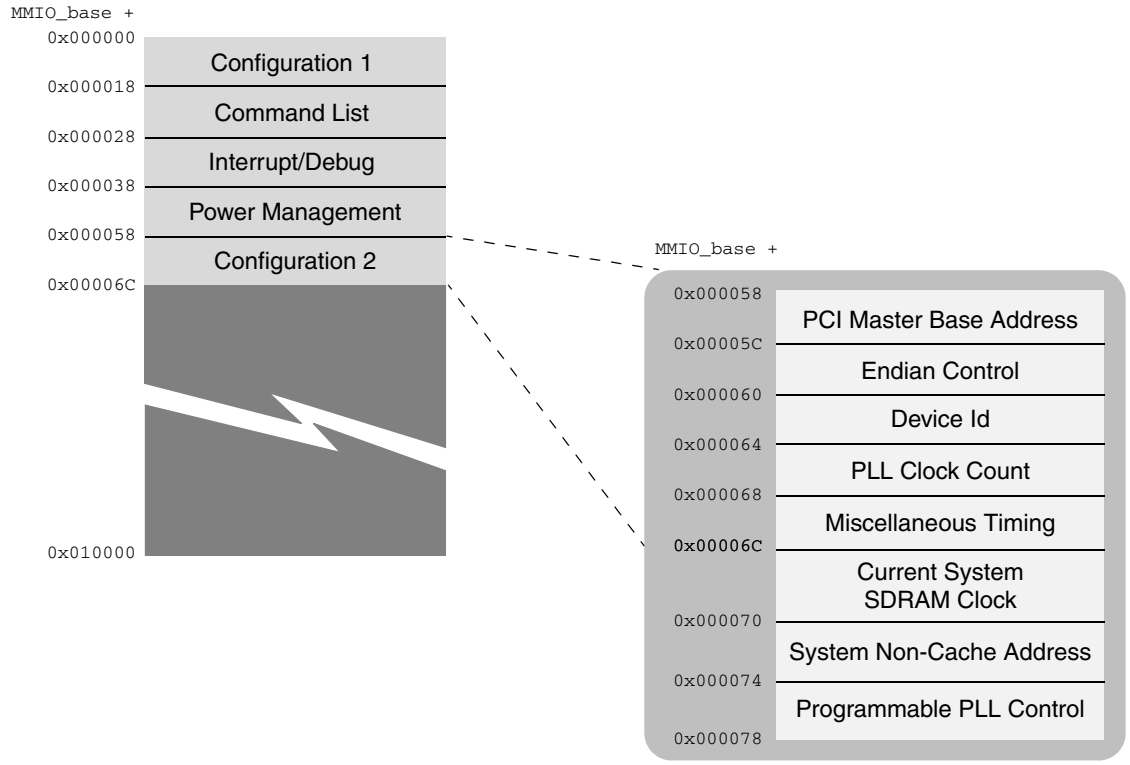
MMIO_base + 0x000054, bits [1:0] = 10
PCI Config register 44, bits [1:0] = xx (don't care)

2. For PCI bus interface only, without support PCI ACPI protocol:
   MMIO_base + 0x000068, bit 6 = 0; disable PCI ACPI mode
   MMIO_base + 0x000054 bits [1:0] = 10
   PCI Config register 44, bits [1:0] = xx (don't care)
3. For PCI bus interface only, with support of PCI ACPI protocol:
   MMIO_base + 0x000068, bit 6 = 0; enable PCI ACPI mode
   MMIO_base + 0x000054, bits [1:0] = xx (don't care)
   PCI Config register 44, bits [1:0] = 1x (ACPI power down mode)

Configuration 2 Register Descriptions

The Configuration registers control the way the SM107 chips operates. Figure 2-2 shows the layout of the configuration registers in Configuration Register Space 2.

Figure 2-6: Configuration Register Space 2



PCI Master Base Address

Read/Write MMIO_base + 0x000058

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Base_{31:20}$ R/W												Reserved			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved															

Bit(s)	Name	Description
31:20	$Base_{31:20}$	PCI Master Base Address Bits [31:20].
19:0	Reserved	These bits are reserved.

Endian Control

Read/Write MMIO_base + 0x00005C

Power-on Default 0b0000.0000.0000.0000.0000.0000.0000.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved															E G4

Bit(s)	Name	Description
31:1	Reserved	These bits are reserved.
0	E	Endian Select. To program the correct endianess for the CPU, the CPU should either write 0x00000000 (for little endian) or 0xFFFFFFFF (for big endian) into this register before touching any other register on the SM107. 0: Little endian. 1: Big endian.

Device Id

Read MMIO_base + 0x000060

Power-on Default 0x050100A0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DeviceId R															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved								RevisionId R							

Bit(s)	Name	Description
31:16	DeviceId	Device Identification: 0x0501.
15:8	Reserved	These bits are reserved.
7:0	RevisionId	Revision Identification: 0xC0.

PLL Clock Count

Read MMIO_base + 0x000064

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ClockCount R															

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:0	ClockCount	Number of clocks since enabling. These clock counts verify if there is a PLL function.

Miscellaneous Timing

Read/Write MMIO_base + 0x000068

Power-on Default 0b0000.00xx.0000.1001.0000.1001.0000.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Ex				Res		Xc R/W		Res			S_{SM1} R/W	S_{M1} R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res			S_{SM0} R/W	S_{M0} R/W				Res	A R/W	Res			Delay R/W		

Bit(s)	Name	Description
31:28	Ex	Extend the bus holding when the SM107 is a host bus master to access system SDRAM. The extension period starts to count down when the SM107 gets an asserted bus acknowledge signal from the CPU.

0000	No Extension	1000	Extend 128 Host Clock
0001	Extend 16 Host Clock	1001	Extend 144 Host Clock
0010	Extend 32 Host Clock	1010	Extend 160 Host Clock
0011	Extend 48 Host Clock	1011	Extend 176 Host Clock
0100	Extend 64 Host Clock	1100	Extend 192 Host Clock
0101	Extend 80 Host Clock	1101	Extend 208 Host Clock
0110	Extend 96 Host Clock	1110	Extend 224 Host Clock
0111	Extend 112 Host Clock	1111	Extend 240 Host Clock

27:26	Res	These bits are reserved.
25:24	Xc	XScale Clock Input Source. 00: From clock generated by internal PLL. 01: From HCLK pin. 1x: From GPIO30 pin. **Note:** Bit 25 is strapped by GPIO31, and bit 24 is strapped by GPIO29.
23:21	Res	These bits are reserved.
20	S_{SM1}	System SDRAM/Host Clock Select for PW Mode 1. 0: 288 MHz. 1: 336 MHz.
19:16	S_{M1}	System SDRAM Clock Frequency Divider for PW Mode 1.

0000	÷ 1	0100	÷ 16	1000	÷ 3	1100	÷ 48
0001	÷ 2	0101	÷ 32	1001	÷ 6	1101	÷ 96
0010	÷ 4	0110	÷ 64	1010	÷ 12	1110	÷ 192
0011	÷ 8	0111	÷ 128	1011	÷ 24	1111	÷ 384

15:13	Res	These bits are reserved.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th></tr>
<tr><td>12</td><td>S_{SM0}</td><td>System SDRAM/Host Clock Select for PW Mode 0.
0: 288 MHz.
1: 336 MHz.</td></tr>
<tr><td>11:8</td><td>S_{M0}</td><td>System SDRAM Clock Frequency Divider for PW Mode 0.
<table>
<tr><td>0000</td><td>÷ 1</td><td>0100</td><td>÷ 16</td><td>1000</td><td>÷ 3</td><td>1100</td><td>÷ 48</td></tr>
<tr><td>0001</td><td>÷ 2</td><td>0101</td><td>÷ 32</td><td>1001</td><td>÷ 6</td><td>1101</td><td>÷ 96</td></tr>
<tr><td>0010</td><td>÷ 4</td><td>0110</td><td>÷ 64</td><td>1010</td><td>÷ 12</td><td>1110</td><td>÷ 192</td></tr>
<tr><td>0011</td><td>÷ 8</td><td>0111</td><td>÷ 128</td><td>1011</td><td>÷ 24</td><td>1111</td><td>÷ 384</td></tr>
</table></td></tr>
<tr><td>7</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>6</td><td>A</td><td>ACPI Control.
0: No ACPI control.
1: ACPI control.</td></tr>
<tr><td>5:3</td><td>Res</td><td>These bits are reserved.</td></tr>
<tr><td>2:0</td><td>Delay</td><td>Delay time to latch read data for external SDRAM controller.
000: No delay.
001: Delay ½ns.
010: Delay 1ns.
011: Delay 1½ns.
100: Delay 2ns.
101: Delay 2½ns.</td></tr>
</table>

Current System SDRAM Clock

Read MMIO_base + 0x00006C

Power-on Default 0x00000009

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved											S_S R	S R			

Bit(s)	Name	Description
31:5	Reserved	These bits are reserved.
4	Ss	System SDRAM/Host Clock Select. 0: 288 MHz. 1: 336 MHz.
3:0	S	System SDRAM/Host Clock Frequency Divider.

0000	÷ 1	0100	÷ 16	1000	÷ 3	1100	÷ 48
0001	÷ 2	0101	÷ 32	1001	÷ 6	1101	÷ 96
0010	÷ 4	0110	÷ 64	1010	÷ 12	1110	÷ 192
0011	÷ 8	0111	÷ 128	1011	÷ 24	1111	÷ 384

System Non-Cache Address

Read/Write MMIO_base + 0x000070

Power-on Default 0x000000FF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		Non$ R/W													

Bit(s)	Name	Description
31:14	Reserved	These bits are reserved.
13:0	Non$	Non-Cache Address. Reading this address [Non$, xxxx] does not get data from the previous read. It fetches data directly from memory.

Programmable PLL Control

Read/Write MMIO_base + 0x000074

Power-on Default 0x000000FF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											TSTOE R/W	TST R/W		PON R/W	SEL R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
K R/W	PLL_N R/W							PLL_M R/W							

Bit(s)	Name	Description
31:21	Reserved	These bits are reserved.
20	TSTOE	Test Clock Output Enable. The PLL clock will output to GPIO_[54]. 0: Disable. 1: Enable.
19:18	TST	PLL Test Mode.
17	PON	PLL Power On. 0: Power down. 1: Power on.
16	SEL	PLL Clock Select. 0: Crystal input. 1: Test clock input.

Bit(s)	Name	Description
15	K	PLL Output Divided by 2. 0: Disable. 1: Enable.
14:8	PLL_N	PLL N Value. Valid values for this field range from 2 to 24.
7:0	PLL_M	PLL M Value.

3 PCI Configuration Space

Register Descriptions

The PCI specification defines the configuration space for auto-configuration (plug-and-play), and device and memory relocation.

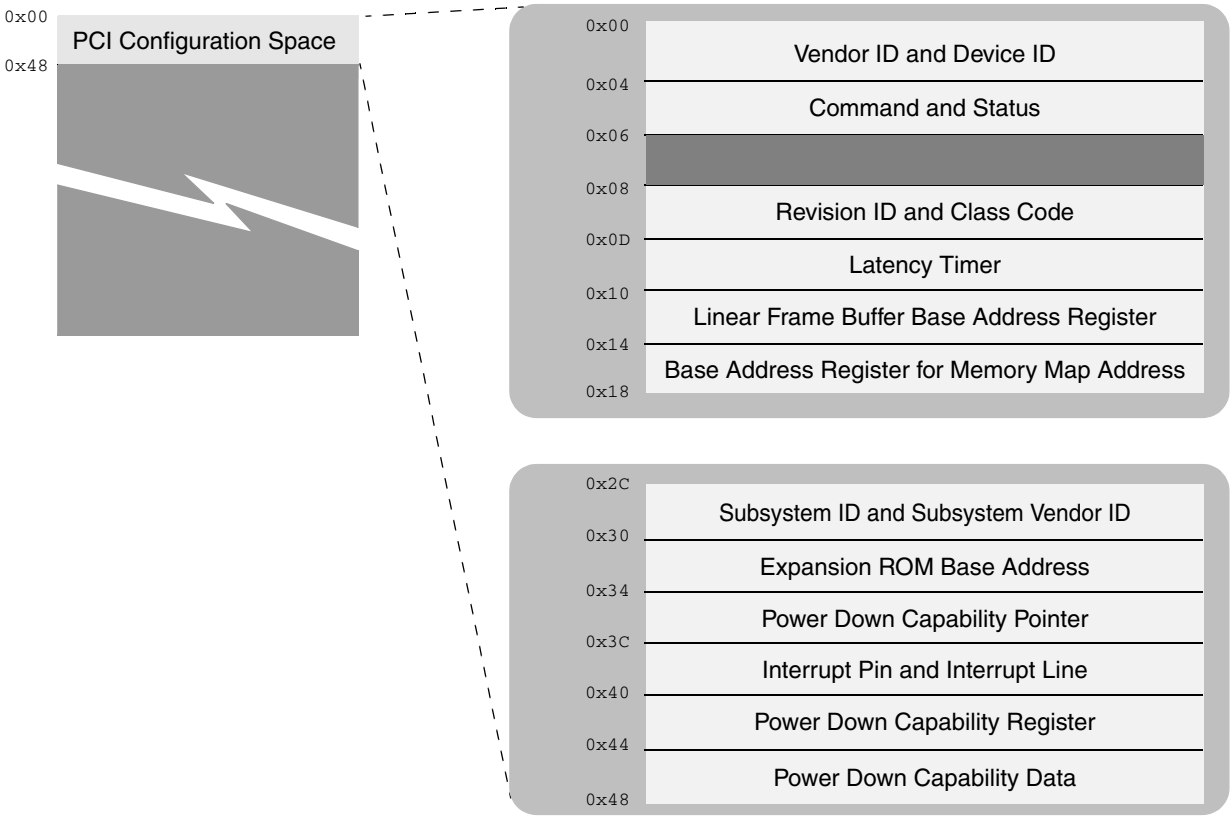
Table 3-1 summarizes the PCI Configuration Space Registers.

Table 3-1: PCI Configuration Space Register Summary

Address	Type	Width	Reset Value	Register Name
0x00	R	32	0x0501126F	CSR00: Vendor ID and Device ID
0x04	R/W	32	0x02300000	CSR04: Command and Status
0x08	R	32	0x380000C0	CSR08: Revision ID and Class Code
0x0D	R	8	0x00	CSR0C: Latency Timer
0x10	R/W	32	0x00000000	CSR10: Linear Frame Buffer Base Address Register
0x14	R/W	32	0x00000000	CSR14: Base Address Register for Memory Map Address
0x2C	R	32	0x00000000	CSR2C: Subsystem ID and Subsystem Vendor ID
0x30	R/W	32	0x00000000	CSR30: Expansion ROM Base Address
0x34	R	32	0x00000040	CSR34: Power Down Capability Pointer
0x3C	R/W	32	0x00000000	CSR3C: Interrupt Pin and Interrupt Line
0x40	R	32	0x06010001	CSR40: Power Down Capability Register
0x44	R/W	32	0x00000000	CSR44: Power Down Capability Data

Figure 3-1 lists the registers available in the PCI Configuration register space.

Figure 3-1: PCI Configuration Register Space



CSR00: Vendor ID and Device ID

Read Address `0x00`

Power-on Default `0x0501126F`

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device ID R															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Vendor ID R															

This register specifies the device and vendor IDs.

Bit(s)	Name	Description
31:16	Device ID	These bits are hardwired to `0x0501` to identify the SM107 device.
15:0	Vendor ID	These bits are hardwired to `0x126F` to identify the vendor as Silicon Motion®, Inc.

CSR04: Command and Status

Read/Write Address 0x04
Power-on Default 0x02300000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPE R	Res		DTA R	Res	DEVSEL R		Res			66C R	NCD R	Res			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res										PSE R/W	MWR R/W	Res	PBM R/W	MS R/W	IO R

This register controls which types of PCI command cycles are supported by the SM107.

Note: Reserved bits are read only.

Bit(s)	Name	Description
31	DPE	Data Parity Error Detected. 0: Correct. 1: Error detected.
30:29	Res	These bits are reserved.
28	DTA	Received Target Abort. 0: Correct. 1: Abort detected.
27	Res	This bit is reserved.
26:25	DEVSEL	Timing Select Medium.
24:22	Res	These bits are reserved.
21	66C	66 MHz Capable.
20	NCD	New Capability Definition.
19:6	Res	These bits are reserved.
5	PSE	Palette Snooping Enable. 0: Disable. 1: Enable.
4	MWR	Memory Write and Invalidate Enable. 0: Disable. 1: Enable.
3	Res	This bit is reserved.
2	PBM	PCI Bus Master Enable.
1	MS	Memory Space Access Enable. 0: Disable. 1: Enable.
0	IO	I/O Space Access Enable. 0: Disable.

CSR08: Revision ID and Class Code

Read Address 0x08

Power-on Default 0x038000C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Base Class Code R								Subclass Code R							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Register Level Programming Interface R								Revision ID R							

This register specifies the silicon revision ID and the Class Code that the silicon supports.

Bit(s)	Name	Description
31:24	Base Class Code	0x03 = For Video Controller
23:16	Subclass Code	0x80 = Other Display Controller
15:8	Register Level Programming Interface	0x00 = Hardwired setting
7:0	Revision ID	0xC0 = SM107

CSR0C: Latency Timer

Read Address 0x0D

Power-on Default 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LT R								Reserved							

This register specifies the latency timer that the SM107 supports for burst master mode.

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:8	LT	Latency Timer. The default for this field is 0x00.
7:0	Reserved	These bits are reserved.

CSR10: Linear Frame Buffer Base Address Register

Read/Write Address 0x10
Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Linear Addressing Memory Base R/W/R											Linear Frame Buffer Base Address R				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Linear Frame Buffer Base Address R															MB R

This register specifies the PCI configuration space for address relocation

Note: Reserved bits are read only.

Bit(s)	Name	Description
31:21	Linear Address Memory Base Address	Memory segment allocated within 64 MB boundary. • If 2 MB: **Bits 26:21** = FBA (Read/Write) • If 4 MB: **Bits 26:22** = FBA (Read/Write) **Bit 21** = 0b • If 8 MB: **Bits 26:23** = FBA (Read/Write) **Bits 22:21** = 00b (Read Only) • If 16 MB: **Bits 26:24** = FBA (Read/Write) **Bits 23:21** = 000b (Read Only) • If 32 MB: **Bit 26** = FBA (Read/Write) **Bits 24:21** = 0000b (Read Only) • If 64 MB: **Bit 26** = FBA (Read/Write) **Bits 25:21** = 00000b (Read Only)
20:1	Linear Frame Buffer Base Address	The default for this read-only field is 0x000000.
0	MB	Memory Base Read. The default for this bit is 0.

CSR14: Base Address Register for Memory Map Address

Read/Write Address 0x14
Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Memory Map Address Base Address R/W/R											Memory Map Address Base Address R				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Memory Map Address Base Address R															MB R

This register specifies the PCI configuration space for address relocation.

Note: Reserved bits are read only.

Bit(s)	Name	Description
31:21	FBA	Memory Map Address Base Address. • If One Endian: **Bits [31:21]** = FBA (Read/Write) • If Big and Small Endian: **Bit [31:22]** = FBA (Read/Write) **Bit [21]** = 0b (Read Only)
20:1	ABA	Memory Map Address Base Address. The default for this read-only field is 0x000000.
0	MB	Memory Base. The default for this read-only bit is 0.

CSR2C: Subsystem ID and Subsystem Vendor ID

Read Address 0x2C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Subsystem ID R															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Subsystem Vendor ID R															

This register specifies both the Subsystem device ID and the Subsystem Vendor ID.

Bit(s)	Name	Description
31:16	Subsystem ID	This System ID is written by the system BIOS during POST.
15:0	Subsystem Vendor ID	This field contains the Subsystem Vendor ID.

CSR30: Expansion ROM Base Address

Read/Write Address 0x30

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROM Base Address R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved															BIOS R/W

This register specifies the expansion ROM base address.

Note: Reserved bits are read only.

Bit(s)	Name	Description
31:16	ROM Base Address	Memory segment allocated for BIOS ROM in 64KB boundary [15:0].
15:1	Reserved	These bits are reserved.
0	BIOS Address Decode Enable	This bit is valid only if memory space access is enabled (CSR04 bit 1 = 1). 0: Disable. 1: Enable.

CSR34: Power Down Capability Pointer

Read Address `0x34`

Power-on Default `0x00000040`

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Power Down Capability Pointer															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Power Down Capability Pointer															

This register contains the address where PCI power down management registers are located.

Bit(s)	Name	Description
31:0	Power Down Capability Pointer	The Capability pointer contains the address where the PCI Power Down Management Register is located.

CSR3C: Interrupt Pin and Interrupt Line

Read/Write Address `0x3C`

Power-on Default `0x00000000`

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Interrupt Pin R								Interrupt Line R/W							

This register specifies the PCI interrupt pin and interrupt line.

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:8	Interrupt Pin	
7:0	Interrupt Line	

CSR40: Power Down Capability Register

Read Address 0x40

Power-on Default 0x06010001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI Power Down Management Capability (0x0601) R															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Next Capability Pointer Link List R								PCI Power Down Mgmt Capability (0x01) R							

This register contains the address for PCI power-down management capabilities.

Bit(s)	Name	Description
31:16	PCI Power Down Management Capability	Offset 2. This field is hardwired to 0x0601.
15:8	No More Extra Capability Pointer	This field is hardwired to 0x00.
7:0	PCI Power Down Management Capability ID	Offset 0. This field is hardwired to 0x01.

CSR44: Power Down Capability Data

Read/Write Address 0x44

Power-on Default 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data R								Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCI Power Down Mgmt Control/Status R/W														PDS R/W	

This register contains the address for PCI power-down management Control, Status and Data.

Bit(s)	Name	Description
31:24	Data	Offset 7. This data field is read-only.
23:16	Reserved	Offset 6.
15:2	PCI Power Down Management Control/Status	Offset 4.
1:0	PDS	Power Down Management Control and Status. 00: Power Down Management State D0. 01: Power Down Management State D1. 10: Power Down Management State D2. 11: Power Down Management State D3.

4 Drawing Engine

Functional Overview

The SM107's Drawing Engine is designed to accelerate Microsoft's DirectDraw and Direct3D applications. The engine contains a 3-operand ALU with 256 raster operations, source and destination FIFOs, as well as a host data FIFO. The drawing engine pipeline allows single cycle operations and runs at the memory clock speed.

The Drawing Engine includes several key functions to achieve the high GUI performance. The device supports color expansion with packed mono font, color pattern fill, host BLT, stretch BLT, short stroke, line draw, and others. Dedicated pathways are designed to transfer data between the host interface (HIF) bus and the Drawing Engine, and memory interface (MIF) bus and the Drawing Engine. In addition, the Drawing Engine supports rotation BIBLT for any block size, and automatic self activate rotation BLIT. This feature allows conversion between landscape and portrait display without the need for special software drivers.

Programmer's Model

The Drawing Engine supports various drawing functions, including Bresenham line draw, short stroke line draw, BITBLT, rectangle fill, HOSTBLT, Rotation Blit, and others. Hardware clipping is supported by 4 registers, DPR2C-DPR32, which define a rectangular clipping area.

The drawing engine supports two types of addressing formats for its source and destination locations. In XY addressing mode, the location is specified in X-Y coordinates, where the upper left corner of the screen is defined to be (0,0). In linear addressing mode, the location is specified based on its position in the display memory sequentially from the first pixel of the visible data. The addressing mode is set by the Addressing field of the 2D Stretch & Format register. The Command field of the 2D Control register selects other drawing functions, for example, Bresenham line draw, host write and short stroke.

Register Descriptions

All Drawing Engine control registers can be accessed via memory mapping. The address is at DP_Base + XXXh, where DP_Base is at PCI graphics base address + 4MB + 32K. Figure 4-1 shows how this 64kB region in the MMIO space is laid out. It controls the Drawing Engine registers.

Figure 4-1: Drawing Engine Register Space

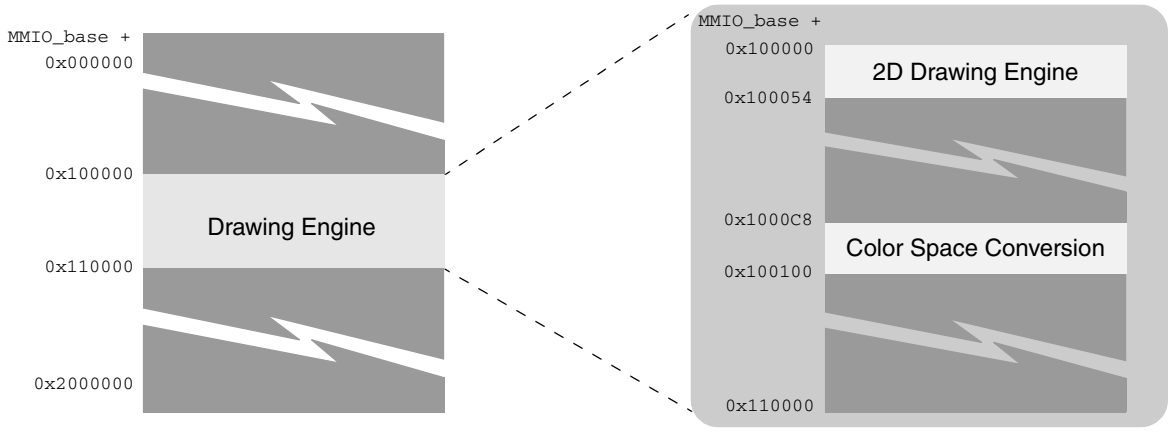


Table 4-1 summarizes the Drawing Engine registers.

Table 4-1: Drawing Engine Register Summary

Offset from MMIO_base[1]	Type	Width	Reset Value	Register Name
0x100000	R/W	32	0x00000000	2D Source
0x100004	R/W	32	0x00000000	2D Destination
0x100008	R/W	32	0x00000000	2D Dimension
0x10000C	R/W	32	0x00000000	2D Control
0x100010	R/W	32	0x00000000	2D Pitch
0x100014	R/W	32	0x00000000	2D Foreground
0x100018	R/W	32	0x00000000	2D Background
0x10001C	R/W	32	0x00000000	2D Stretch & Format
0x100020	R/W	32	0x00000000	2D Color Compare
0x100024	R/W	32	0x00000000	2D Color Compare Mask
0x100028	R/W	32	0x00000000	2D Mask
0x10002C	R/W	32	0x00000000	2D Clip TL
0x100030	R/W	32	0x00000000	2D Clip BR
0x100034	R/W	32	0x00000000	2D Mono Pattern Low
0x100038	R/W	32	0x00000000	2D Mono Pattern High
0x10003C	R/W	32	0x00000000	2D Window Width
0x100040	R/W	32	0x00000000	2D Source Base
0x100044	R/W	32	0x00000000	2D Destination Base
0x100048	R/W	32	0x00000000	2D Alpha
0x10004C	R/W	32	0x00000000	2D Wrap
0x100050	R/W	32	0x00000000	2D Status
0x1000C8	R/W	32	0x00000000	CSC Y Source Base
0x1000CC	R/W	32	0x00000000	CSC Constants
0x1000D0	R/W	32	0x00000000	CSC Y Source X

Table 4-1: Drawing Engine Register Summary (Continued)

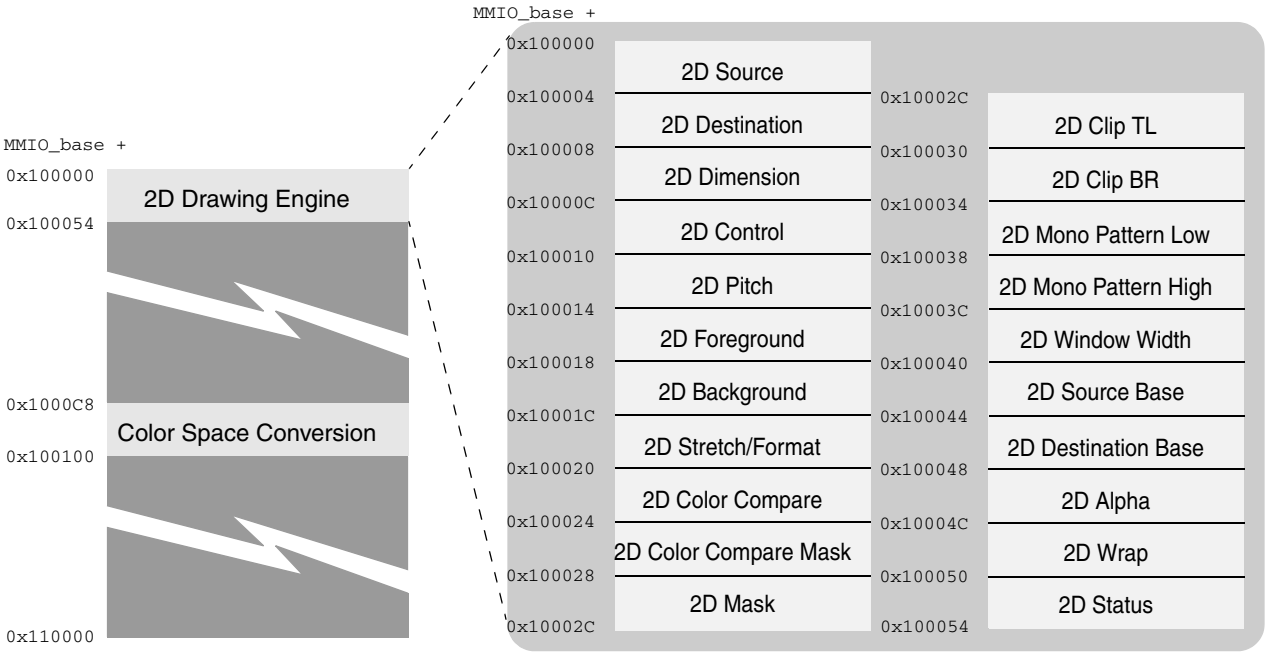
Offset from MMIO_base[1]	Type	Width	Reset Value	Register Name
0x1000D4	R/W	32	0x00000000	CSC Y Source Y
0x1000D8	R/W	32	0x00000000	CSC U Source Base
0x1000DC	R/W	32	0x00000000	CSC V Source Base
0x1000E0	R/W	32	0x00000000	CSC Source Dimension
0x1000E4	R/W	32	0x00000000	CSC Source Pitch
0x1000E8	R/W	32	0x00000000	CSC Destination
0x1000EC	R/W	32	0x00000000	CSC Destination Dimension
0x1000F0	R/W	32	0x00000000	CSC Destination Pitch
0x1000F4	R/W	32	0x00000000	CSC Scale Factor
0x1000F8	R/W	32	0x00000000	CSC Destination Base
0x1000FC	R/W	32	0x00000000	CSC Control

1. Refer to Table 1-5 on page 24 for MMIO_base values depending on the CPU.

2D Drawing Engine Registers

The 2D Drawing Engine register space is shown in Figure 4-2.

Figure 4-2: 2D Drawing Register Space



2D Source

Read/Write MMIO_base + 0x100000

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res / Res	Res	X_K1 R/W													
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y_K2 R/W															

Bit(s)	Name	Description
31	Res	This bit is reserved.
30	Res	This bit is reserved.

Bit(s)	Name	Description
29:16	X_K1	In XY addressing mode, the 12-bit X-coordinate of source (bits 27:16). In linear addressing mode, the lower 12-bits of the source address (bits 27:16). In host write mode, the 5-bit mono source for alignment (bits 20:16) In Bresenham line drawing mode, the 14-bit K1 constant for line drawing (bits 29:16): K1 = 2 * min(|dx|, |dy|).
15:0	Y_K2	In XY addressing mode, the 12-bit Y-coordinate of source (bits 11:0). In linear addressing mode, the higher 12-bits of the source address (bits 11:0). In host write mode, this field is not used. In Bresenham line drawing mode, the 14-bit K2 constant for line drawing (bits 13:0): K2 = 2 * (min(|dx|, |dy|) – max(|dx|, |dy|).

2D Destination

Read/Write MMIO_base + 0x100004

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res / Res	Reserved		X R/W												
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y R/W															

Bit(s)	Name	Description
31	Reserved	This bit is reserved.
30:29	Reserved	These bits are reserved.
28:16	X	In XY addressing mode, the 12-bit X-coordinate of source (bits 27:16). In linear addressing mode, the lower 12-bits of the source address (bits 27:16). In Bresenham mode, the vector X start address (bits 27:16)
15:0	Y	In XY addressing mode, the 12-bit Y-coordinate of source (bits 11:0). In linear addressing mode, the higher 12-bits of the source address (bits 11:0). In Bresenham mode, the vector Y start address (bits 11:0)

2D Dimension

Read/Write MMIO_base + 0x100008

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			X_VL R/W												
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y_ET R/W															

Bit(s)	Name	Description
31:29	Reserved	These bits are reserved.
28:16	X_VL	In XY addressing mode, the X dimension in pixels. In Bresenham mode, the vector length. In short stroke mode, horizontal length
15:0	Y_ET	In XY addressing mode, the Y dimension in pixels. In Bresenham mode, the vector error term given by: ET = 2 * min(|dx|, |dy|) – max(|dx|, |dy|) if start X > end X, or ET = 2 * min(|dx|, |dy|) – max(|dx|, |dy|) – 1 if start X <= end X. In short stroke mode, the non-horizontal length.

2D Control

Read/Write MMIO_base + 0x10000C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	P R/W	U R/W	Q R/W	D R/W	M R/W	X R/W	Y R/W	St R/W	H R/W	LP R/W	Command R/W				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R R/W	R2 R/W	Mono R/W		RR R/W	TM R/W	TS R/W	T R/W	ROP R/W							

Bit(s)	Name	Description
31	S	Drawing Engine Status. 0: Stop. 1: Start.
30	P	Pattern Select. 0: Monochrome. 1: Color.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th></tr>
<tr><td>29</td><td>U</td><td>Update Destination X after Operation Control.
0: Disable.
1: Enable.</td></tr>
<tr><td>28</td><td>Q</td><td>Quick Start Control. Quick start will start the drawing engine after the X field in the 2D Dimension register has been written to.
0: Disable.
1: Enable.</td></tr>
<tr><td>27</td><td>D</td><td>Direction Control for Operation.
0: Left to right.
1: Right to left.</td></tr>
<tr><td>26</td><td>M</td><td>Major Axis for Line Drawing.
0: X axis.
1: Y axis.</td></tr>
<tr><td>25</td><td>X</td><td>X Step Control for Line Drawing.
0: Positive.
1: Negative.</td></tr>
<tr><td>24</td><td>Y</td><td>Y Step Control for Line Drawing.
0: Positive.
1: Negative.</td></tr>
<tr><td>23</td><td>St</td><td>Stretch in Y Direction Control.
0: Disable.
1: Enable.</td></tr>
<tr><td>22</td><td>H</td><td>Host BitBlt Select.
0: Color.
1: Monochrome.</td></tr>
<tr><td>21</td><td>LP</td><td>Draw Last Pixel Control for Line Drawing.
0: Don’t draw last pixel.
1: Draw last pixel.</td></tr>
<tr><td>20:16</td><td>Command</td><td>Command Code.
<table>
<tr><td>00000</td><td>BitBlt</td><td>00111</td><td>Line Draw</td></tr>
<tr><td>00001</td><td>Rectangle Fill</td><td>01000</td><td>Host Write</td></tr>
<tr><td>00010</td><td>De-Tile</td><td>01001</td><td>Host Read</td></tr>
<tr><td>00011</td><td>Trapezoid Fill</td><td>01010</td><td>Host Write bottom-to-top</td></tr>
<tr><td>00100</td><td>Alpha Blend</td><td>01011</td><td>Rotate</td></tr>
<tr><td>00101</td><td>RLE Strip</td><td>01100</td><td>Font</td></tr>
<tr><td>00110</td><td>Short Stroke</td><td>01111</td><td>Texture Load</td></tr>
</table></td></tr>
<tr><td>15</td><td>R</td><td>ROP Control.
0: ROP3.
1: ROP2.</td></tr>
<tr><td>14</td><td>R2</td><td>ROP2 Control.
0: ROP2 source is bitmap.
1: ROP2 source is pattern.</td></tr>
<tr><td>13:12</td><td>Mono</td><td>Monochrome Data Pack Control.
00: Not packed.
01: Packed at 8-bit.
10: Packed at 16-bit.
11: Packed at 32-bit.</td></tr>
</table>

Bit(s)	Name	Description
11	RR	Repeat Rotation Control. Only valid when *Command* is 01011 (Rotate). When enabled, the drawing engine is started again at every vertical sync. 0: Disable. 1: Enable.
10	TM	Transparency Match Select. 0: Matching pixel is opaque. 1: Matching pixel is transparent.
9	TS	Transparency Select. 0: Transparency is controlled by source. 1: Transparency is controlled by destination.
8	T	Transparency Control. 0: Disabled. 1: Enabled.
7:0	ROP	ROP2 or ROP3 code (see tables below).

Binary Raster Operations (ROP2)

Each raster-operation code represents a Boolean operation in which the values of the pixels in the selected pen and the destination bitmap are combined. The operands used in these operations are:

- P = selected pen
- D = destination bitmap

		Bit[2:0]							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Bit 3	0	0	~(D+S)	D*~S	~S	~D*S	~D	D^S	(~D*S)
	1	D*S	(~D^S)	D	D+~S	S	~D+S	D+S	1

Ternary Raster Operations (ROP3)

Each raster-operation code represents a Boolean operation in which the values of the pixels in the source, the selected brush, and the destination are combined. The operands and operands are:

- D = destination bitmap
- P = selected brush (pattern)
- S = source bitmap
- a = bitwise AND
- n = bitwise NOT (inverse)
- o = bitwise OR
- x = bitwise XOR (exclusive OR)

All Boolean operations are presented in reverse Polish notation. For example, the following operation replaces the pixel values in the destination bitmap with a combination of the pixel values of the source and brush:

PSo = (P+S)

The following operation combines the values of the pixels in the source and brush with the pixel values of the destination bitmap (there are alternative spellings of the same function, so although a particular spelling may not be in the list, an equivalent form would be):

DPSoo = (P+S) + D

The SM107 supports all the 256 operations. However, the pattern must be monochrome.

Table 4-2 lists all the possible ROP3 operations.

Table 4-2: ROP3 Operations

		Bits [7:4]							
		0	1	2	3	4	5	6	7
bit [3:0]	0	0	PDSona	DPSnaa	PSna	PSDnaa	PDna	PDSxa	PDSana
	1	DPSoon	DSon	SDPxon	SDPnaon	DPSxon	DSPnaon	DSPDSaoxxn	SSDxPDxaxn
	2	DPSona	SDPxnon	DSna	SDPSoox	SDxPDxa	DPSDaox	DSPDoax	SDPSxox
	3	PSon	SDPaon	SPDnaon	Sn	SPDSanaxn	SPDSxaxn	SDPnox	SDPnoan
	4	SDPona	DPSxnon	SPxDSxa	SPDSaox	SDna	DPSonon	SDPSoax	DSPDxox
	5	DPon	DPSaon	PDSPanaxn	SPDSxnox	DPSnaon	Dn	DSPnox	DSPnoan
	6	PDSxnon	PSDPSanaxx	SDPSaox	SDPox	DSPDaox	DPSox	DSx	SDPSnaox
	7	PDSaon	SSPxDSxaxn	SDPSxnox	SDPoan	PSDPxaxn	DPSoan	SDPSonox	DSan
	8	SDPnaa	SPxPDxa	DPSxa	PSDPoax	SDPxa	PDSPoax	DSPDSonoxxn	PDSax
	9	PDSxon	SDPSanaxn	PSDPSaoxxn	SPDnox	PDSPDaoxxn	DPSnox	PDSxxn	DSPDSoaxxn
	A	DPna	PDSPaox	DPSana	SPDSxox	DPSDoax	DPx	DPSax	DPSDnoax
	B	PSDnaon	SDPSxaxn	SSPxPDxaxn	SPDnoan	PDSnox	DPSDonox	PSDPSoaxxn	SDPxnan
	C	SPna	PSDPaox	SPDSoax	PSx	SDPana	DPSDxox	SDPax	SPDSnoax
	D	PDSnaon	DSPDxaxn	PSDnox	SPDSonox	SSPxDSxoxn	DPSnoan	PDSPDoaxxn	DPSxnan
	E	PDSonon	PDSox	PSDPxox	SPDSnaox	PDSPxox	DPSDnaox	SDPSnoax	SPxDSxo
	F	Pn	PDSoan	PSDnoan	PSan	PDSnoan	DPan	PDSxnan	DPSaan

		Bits [7:4]							
		8	9	A	B	C	D	E	F
bit [3:0]	0	DPSaa	PDSxna	DPa	PDSnoa	PSa	PSDnoa	PDSoa	P
	1	SPxDSxon	SDPSnoaxn	PDSPnaoxn	PDSPxoxn	SPDSnaoxn	PSDPxoxn	PDSoxn	PDSono
	2	DPSxna	DPSDPoaxx	DPSnoa	SSPxDSxox	SPDSonoxn	PDSnax	DSPDxax	PDSnao
	3	SPDSnoaxn	SPDaxn	DPSDxoxn	SDPanan	PSxn	SPDSoaxn	PSDPaoxn	PSno
	4	SDPxna	PSDPSoaxx	PDSPonoxn	PSDnax	SPDnoa	SSPxPDxax	SDPSxax	PSDnao
	5	PDSPnoaxn	DPSaxn	PDxn	DPSDoaxn	SPDSxoxn	DPSanan	PDSPaoxn	PDno
	6	DSPDSoaxx	DPSxx	DSPnax	DPSDPaoxx	SDPnax	PSDPSaoxx	SDPSanax	PDSxo
	7	PDSaxn	PSDPSonoxx	PDSPoaxn	SDPxan	PSDPoaxn	DPSxan	SPxPDxan	PDSano
	8	DSa	SDPSonoxn	DPSoa	PSDPxax	SDPoa	PDSPxax	SSPxDSxax	PDSao
	9	SDPSnaoxn	DSxn	DPSoxn	DSPDaoxn	SPDoxn	SDPSaoxn	DSPDSanaxxn	PDSxno
	A	DSPnoa	DPSnax	D	DPSnao	DPSDxax	DPSDanax	DPSao	DPo
	B	DSPDxoxn	SDPSoaxn	DPSono	DSno	SPDSaoxn	SPxDSxan	DPSxno	DPSnoo
	C	SDPnoa	SPDnax	SPDSxax	SPDSanax	S	SPDnao	SDPao	PSo
	D	SDPSxoxn	DSPDoaxn	DPSDaoxn	SDxPDxan	SDPono	SDno	SDPxno	PSDnoo
	E	SSDxPDxax	DSPDSaoxx	DSPnao	DPSxo	SDPnao	SDPxo	DSo	DPSoo
	F	PDSanan	PDSxan	DPno	DPSano	SPno	SDPano	SDPnoo	1

Rotate Command

For the Rotate command, the *X* and *Y* bits determine the rotation angle. For the Short Stroke command, the D, M, X, and Y bits determine the direction of the vector.

X	Y	Rotation Direction
0	0	0 degrees
0	1	270 degrees
1	0	90 degrees
1	1	180 degrees

D	M	X	Y	Vector Direction
0	0	0	0	225 degrees
0	0	0	1	135 degrees
0	0	1	0	315 degrees
0	0	1	1	45 degrees
0	1	0	0	270 degrees
0	1	0	1	90 degrees
1	0	0	0	180 degrees
1	0	1	0	0 degrees

2D Pitch

Read/Write MMIO_base + 0x100010

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			Destination R/W												
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			Source R/W												

Bit(s)	Name	Destination
31:29	Reserved	These bits are reserved.
28:16	Destination	Pitch of destination specified in pixels.
15:13	Reserved	These bits are reserved.
12:0	Source	Pitch of source specified in pixels.

2D Foreground

Read/Write MMIO_base + 0x100014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Foreground R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Foreground R/W															

Bit(s)	Name	Description
31:0	Foreground	

Bits Per Pixel	Foreground Color
8	Index color.
16	RGB565 color.
32	RGBx888 color.

2D Background

Read/Write MMIO_base + 0x100018

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Background R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Background R/W															

Bit(s)	Name	Description
31:0	Background	

Bits Per Pixel	Background Color
8	Index color.
16	RGB565 color.
32	RGBx888 color.

In monochrome transparency, the *Background* must be programmed with the invert of the *Foreground* pixels in the *2D Foreground* register.

2D Stretch & Format

Read/Write MMIO_base + 0x10001C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	XY R/W	Y R/W			Res	X R/W			Res	Format R/W		Addressing R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res				Height R/W											

Bit(s)	Name	Description
31	Res	This bit is reserved.
30	XY	Pattern XY Select. 0: Only use *X* and *Y* fields in linear mode. 1: Use *X* and *Y* fields in XY mode.
29:27	Y	Pattern Y Origin. This field is only valid in linear mode (*Addressing* = 1111) or when *XY* is enabled.
26	Res	This bit is reserved.
25:23	X	Pattern X Origin. This field is only valid in linear mode (*Addressing* = 1111) or when *XY* is enabled.
22	Res	This bit is reserved.
21:20	Format	Pixel Format. 00: 8-bits per pixel. 01: 16-bits per pixel. 10: 32-bits per pixel.
19:16	Addressing	Addressing Mode. 0000: XY mode. 1111: Linear mode.
15:12	Res	These bits are reserved.
11:0	Height.	Source height when stretch is enabled.

2D Color Compare

Read/Write MMIO_base + 0x100020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								Color R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Color R/W															

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:0	Color	**Bits Per Pixel** / **Color Compare** 8 / Index color. 16 / RGB565 color. 32 / RGB888 color.

In monochrome transparency, the *Color* must be programmed with the same value as the *Foreground* pixels in the *2D Foreground* register.

2D Color Compare Mask

Read/Write MMIO_base + 0x100024

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								Mask R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mask R/W															

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:0	Mask	Mask Bits for Color Compare. 0: Color compare always matches. 1: Color compare only matches when bits are equal.

2D Mask

Read/Write MMIO_base + 0x100028

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit R/W															

Bit(s)	Name	Description
31:16	Byte	Byte mask for each of the 16 bytes on the 128-bit memory bus. 0: Disable write. 1: Enable write.
15:0	Bit	Bit mask for 8- and 16-bits per pixel modes. 0: Disable write. 1: Enable write.

2D Clip TL

Read/Write MMIO_base + 0x10002C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Top R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		E R/W	S R/W	Left R/W											

Bit(s)	Name	Description
31:16	Top	Top Coordinate of Clipping Rectangle.
15:14	Reserved	These bits are reserved.
13	E	Clipping Control. 0: Disable. 1: Enable.
12	S	Clipping Select Control. 0: Write outside clipping rectangle disabled. 1: Write inside clipping rectangle disabled.
11:0	Left	Left Coordinate of Clipping Rectangle.

2D Clip BR

Read/Write MMIO_base + 0x100030

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bottom R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			Right R/W												

Bit(s)	Name	Description
31:16	Bottom	Bottom Coordinate of Clipping Rectangle.
15:13	Reserved	These bits are reserved.
12:0	Right	Right Coordinate of Clipping Rectangle.

2D Mono Pattern Low

Read/Write MMIO_base + 0x100034

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Pattern R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pattern R/W															

Bit(s)	Name	Description
31:0	Pattern	Bits [31:0] of monochrome pattern.

2D Mono Pattern High

Read/Write MMIO_base + 0x100038

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Pattern R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pattern R/W															

Bit(s)	Name	Description
31:0	Pattern	Bits [63:32] of monochrome pattern.

2D Window Width

Read/Write MMIO_base + 0x10003C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			Destination R/W												
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			Source R/W												

Bit(s)	Name	Description
31:29	Reserved	These bits are reserved.
28:16	Destination	Width of destination window specified in pixels.
15:13	Reserved	These bits are reserved.
12:0	Source	Width of source window specified in pixels.

2D Source Base

Read/Write MMIO_base + 0x100040

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Destination
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of source window with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

2D Destination Base

Read/Write MMIO_base + 0x100044

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.

Bit(s)	Name	Description
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of destination window with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

2D Alpha

Read/Write MMIO_base + 0x100048

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Alpha R/W							

Bit(s)	Name	Description
31:8	Reserved	These bits are reserved.
7:0	Alpha	Alpha Value for Alpha Blend.

2D Wrap - Width and Height

Read/Write MMIO_base + 0x10004C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Width R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Height R/W															

Bit(s)	Name	Description
31:16	Width	Horizontal pitch (H_Pitch) in pixels.
15:0	Height	Vertical pitch (V_Pitch) in lines.

2D Status

Read/Write MMIO_base + 0x100050

Power-on Default 0x00000000

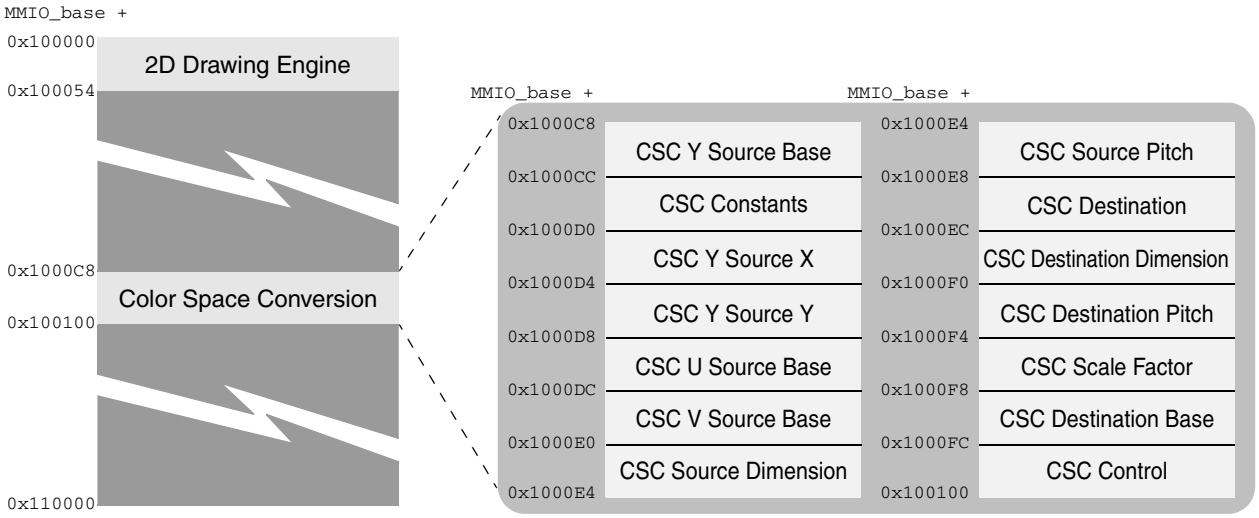
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved														CSC R/W	2D R/W

Bit(s)	Name	Description
31:2	Reserved	These bits are reserved.
1	CSC	Color Space Conversion Interrupt Status. Write a 0 into this field to clear the interrupt status. 0: CSC not active or job not done. 1: CSC interrupt.
0	2D	2D Engine Interrupt Status. Write a 0 into this field to clear the interrupt status. 0: 2D not active or job not done. 1: 2D interrupt.

Color Space Conversion Registers

The Color Space Conversion register space is shown in Figure 4-3.

Figure 4-3: Color Space Conversion Register Space



CSC Y Source Base (UV Source Base in 420i)

Read/Write MMIO_base + 0x1000C8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of Source Y-plane with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC Constants

Read/Write MMIO_base + 0x1000CC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Conversion Constant (luminosity).
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	Blue Conversion Constant.

CSC Y Source X

Read/Write MMIO_base + 0x1000D0

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				X_I R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X_F R/W													Reserved		

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	X_I	Integer Part of Starting X-coordinate into Y-plane.
15:3	X_F	Fractional Part of Starting X-coordinate into Y-plane.
2:0	Reserved	These bits are reserved.

CSC Y Source Y

Read/Write MMIO_base + 0x1000D4

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Y_I R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y_F R/W													Reserved		

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	Y_I	Integer Part of Starting Y-coordinate into Y-plane.
15:3	Y_F	Fractional Part of Starting Y-coordinate into Y-plane.
2:0	Reserved	These bits are reserved.

CSC U Source Base

Read/Write MMIO_base + 0x1000D8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of source Y-plane with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC V Source Base

Read/Write MMIO_base + 0x1000DC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of source Y-plane with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC Source Dimension

Read/Write MMIO_base + 0x1000E0

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Width R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Height R/W															

Bit(s)	Name	Description
31:16	Width	Width of Source in Pixels.
15:0	Height	Height of Source in Lines.

CSC Source Pitch

Read/Write MMIO_base + 0x1000E4

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UV R/W															

Bit(s)	Name	Destination
31:16	Y	Pitch of Y-plane specified in bytes ÷ 16.
15:0	UV	Pitch of UV-planes specified in bytes ÷ 16.

CSC Destination

Read/Write MMIO_base + 0x1000E8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res / Res	Reserved			X R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				Y R/W											

Bit(s)	Name	Description
31	Reserved	This bit is reserved.
30:28	Reserved	These bits are reserved.
27:16	X	X-coordinate of Destination.
15:12	Reserved	These bits are reserved.
11:0	Y	Y-coordinate of Destination.

CSC Destination Dimension

Read/Write MMIO_base + 0x1000EC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Width R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Height R/W															

Bit(s)	Name	Description
31:16	Width	Width of Destination.
15:0	Height	Height of Destination.

CSC Destination Pitch

Read/Write MMIO_base + 0x1000F0

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
X R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y R/W															

Bit(s)	Name	Description
31:16	X	Horizontal Pitch of Destination specified in bytes ÷ 16.
15:0	Y	Vertical Pitch of Destination specified in pixels.

CSC Scale Factor

Read/Write MMIO_base + 0x1000F4

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
X R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Y R/W															

Bit(s)	Name	Description
31:16	X	Horizontal scale factor specified in 3.13 format. Scale factor = 2^{13} * ($Width_S$ – 1) / ($Width_D$ – 1).
15:0	Y	Vertical scale factor specified in 3.13 format. Scale factor = 2^{13} * ($Height_S$ – 1) / ($Height_D$ – 1).

CSC Destination Base

Read/Write MMIO_base + 0x1000F8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of Destination Window with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC Control

Read/Write MMIO_base + 0x1000FC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	$Format_S$ R/W			$Format_D$ R/W		H R/W	V R/W	B R/W	Reserved						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved															

Bit(s)	Name	Description
31	S	Color Space Conversion Control. 0: Stop. 1: Start.
30:28	$Format_S$	Source Pixel Format.
27:26	$Format_D$	Destination Pixel Format. 00: RGB565. 01: RGBx888.
25	H	Horizontal Linear Filter Control. 0: Disable. 1: Enable.
24	V	Vertical Linear Filter Control. 0: Disable. 1: Enable.
23	B	Byte Order for YUV422 and YUV420I.
22:0	Reserved	These bits are reserved.

000	YUV422	100	Reserved
001	YUV420I	101	Reserved
010	YUV420	110	RGB565
011	Reserved	111	RGBx888

	YUV422	**YUV420I**
0	YUYV	UVUV
1	UYVY	VUVU

5 Display Controller

Programmer's Model

The SM107 integrates a concurrent video processor to control LCD display. Some of the features are:

- Background graphic supports from 4-bit index color, 8-bit index color, 15-bit direct color, and 16-bit direct color. Background graphic can be programmed to pan to the left/right and to up/down automatically according to number of VSYNC.
- Support 1 independent video surface using hardware scaling for any size of video windows at any location of the screen display and using hardware YUV to RGB color space conversion.
- Support 1 Alpha blend surface at any location of the screen display. It can use as hardware cursor or popup icon or sub picture for the video. Data format is 4-bit alpha and 4-bit color.
- The LCD module manages data flow and generate timing to select LCD display. It provides support for 18-bit and 24-bit TFT and 8-bit and 12-bit DSTN panels up to SXGA.

The Video Processor Control Registers specify the control registers for Video Processor. The Video Processor Control Registers can only be accessed through memory-mapping.

Register Descriptions

Table 5-1 summarizes the Display Controller registers.

Table 5-1: Display Controller Register Summary

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
Panel Graphics Control				
0x080000	R/W	32	0x00010000	Panel Display Control
0x080004	R/W	32	Undefined	Panel Panning Control
0x080008	R/W	32	Undefined	Panel Color Key
0x08000C	R/W	32	Undefined	Panel FB Address
0x080010	R/W	32	Undefined	Panel FB Offset/Window Width
0x080014	R/W	32	Undefined	Panel FB Width
0x080018	R/W	32	Undefined	Panel FB Height
0x08001C	R/W	32	Undefined	Panel Plane TL Location
0x080020	R/W	32	Undefined	Panel Plane BR Location
0x080024	R/W	32	Undefined	Panel Horizontal Total
0x080028	R/W	32	Undefined	Panel Horizontal Sync
0x08002C	R/W	32	Undefined	Panel Vertical Total
0x080030	R/W	32	Undefined	Panel Vertical Sync
0x080034	R	32	0b0000.0000.0000.0000. 0000.0XXX.XXXX.XXXX	Panel Current Line
Video Control				
0x080040	R/W	32	0b0000.0000.0000.0001. X000.0000.0000.0000	Video Display Control
0x080044	R/W	32	Undefined	Video FB 0 Address
0x080048	R/W	32	Undefined	Video FB Width
0x08004C	R/W	32	Undefined	Video FB 0 Last Address
0x080050	R/W	32	Undefined	Video Plane TL Location
0x080054	R/W	32	Undefined	Video Plane BR Location

Table 5-1: Display Controller Register Summary (Continued)

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
0x080058	R/W	32	0x00000000	Video Scale
0x08005C	R/W	32	0x00000000	Video Initial Scale
0x080060	R/W	32	0x00EDEDED	Video YUV Constants
0x080064	R/W	32	Undefined	Video FB 1 Address
0x080068	R/W	32	Undefined	Video FB 1 Last Address
Video Alpha Control				
0x080080	R/W	32	0x00000000	Video Alpha Display Control
0x080084	R/W	32	Undefined	Video Alpha FB Address
0x080088	R/W	32	Undefined	Video Alpha FB Offset/Window Width
0x08008C	R/W	32	Undefined	Video Alpha FB Last Address
0x080090	R/W	32	Undefined	Video Alpha Plane TL Location
0x080094	R/W	32	Undefined	Video Alpha Plane BR Location
0x080098	R/W	32	0x00000000	Video Alpha Scale
0x08009C	R/W	32	0x00000000	Video Alpha Initial Scale
0x0800A0	R/W	32	Undefined	Video Alpha Chroma Key
0x0800A4 - 0x0800C0	R/W	32	Undefined	Video Alpha Color Lookup
Panel Cursor Control				
0x0800F0	R/W	32	Undefined	Panel HWC Address
0x0800F4	R/W	32	Undefined	Panel HWC Location
0x0800F8	R/W	32	Undefined	Panel HWC Color 1 & 2
0x0800FC	R/W	32	Undefined	Panel HWC Color 3
Alpha Control				
0x080100	R/W	32	0x00010000	Alpha Display Control
0x080104	R/W	32	Undefined	Alpha FB Address
0x080108	R/W	32	Undefined	Alpha FB Offset/Window Width

Table 5-1: Display Controller Register Summary (Continued)

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
0x08010C	R/W	32	Undefined	Alpha Plane TL Location
0x080110	R/W	32	Undefined	Alpha Plane BR Location
0x080114	R/W	32	Undefined	Alpha Chroma Key
0x080118 - 0x080134	R/W	32	Undefined	Alpha Color Lookup
CRT Graphics Control				
0x080200	R/W	32	0x00010000	CRT Display Control
0x080204	R/W	32	Undefined	CRT FB Address
0x080208	R/W	32	Undefined	CRT FB Offset/Window Width
0x08020C	R/W	32	Undefined	CRT Horizontal Total
0x080210	R/W	32	Undefined	CRT Horizontal Sync
0x080214	R/W	32	Undefined	CRT Vertical Total
0x080218	R/W	32	Undefined	CRT Vertical Sync
0x08021C	R/W	32	Undefined	CRT Signature Analyzer
0x080220	R	32	0b0000.0000.0000.0000. 0000.0XXX.XXXX.XXXX	CRT Current Line
0x080224	R/W	32	0b0000.0000.XXXX.XXXX. XXXX.XXXX.XXXX.XXXX	CRT Monitor Detect
CRT Cursor Control				
0x080230	R/W	32	Undefined	CRT HWC Address
0x080234	R/W	32	Undefined	CRT HWC Location
0x080238	R/W	32	Undefined	CRT HWC Color 1 & 2
0x08023C	R/W	32	Undefined	CRT HWC Color 3
Palette RAM				
0x080400 - 0x0807FC	R/W	32	Undefined	Panel Palette RAM
0x080800 - 0x080BFC	R/W	32	Undefined	Video Palette RAM

Table 5-1: Display Controller Register Summary (Continued)

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
0x080C00 - 0x080FFC	R/W	32	Undefined	CRT Palette RAM

1. Refer to Table 1-5 on page 24 for MMIO_base values depending on the CPU.
2. In the reset values, “X” indicates don’t care.

Figure 5-1 shows how this 64kB region in the MMIO space is laid out. It controls the backend of the display controller as shown in Figure 5-2.

Figure 5-1: Display Controller Register Space

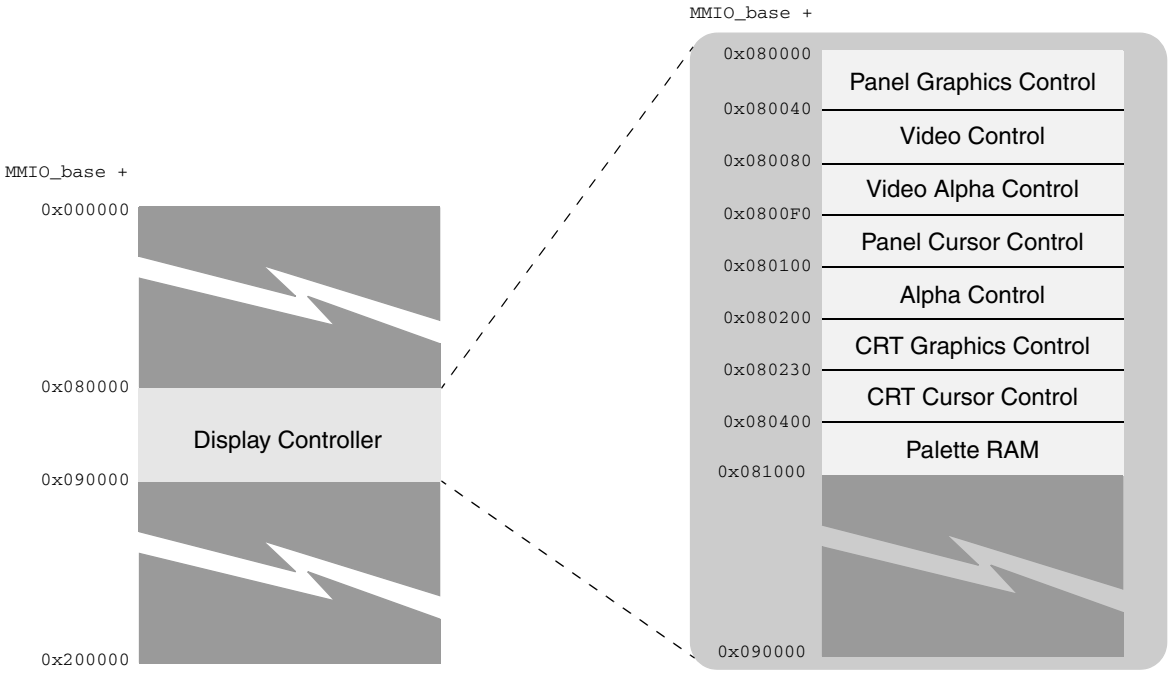
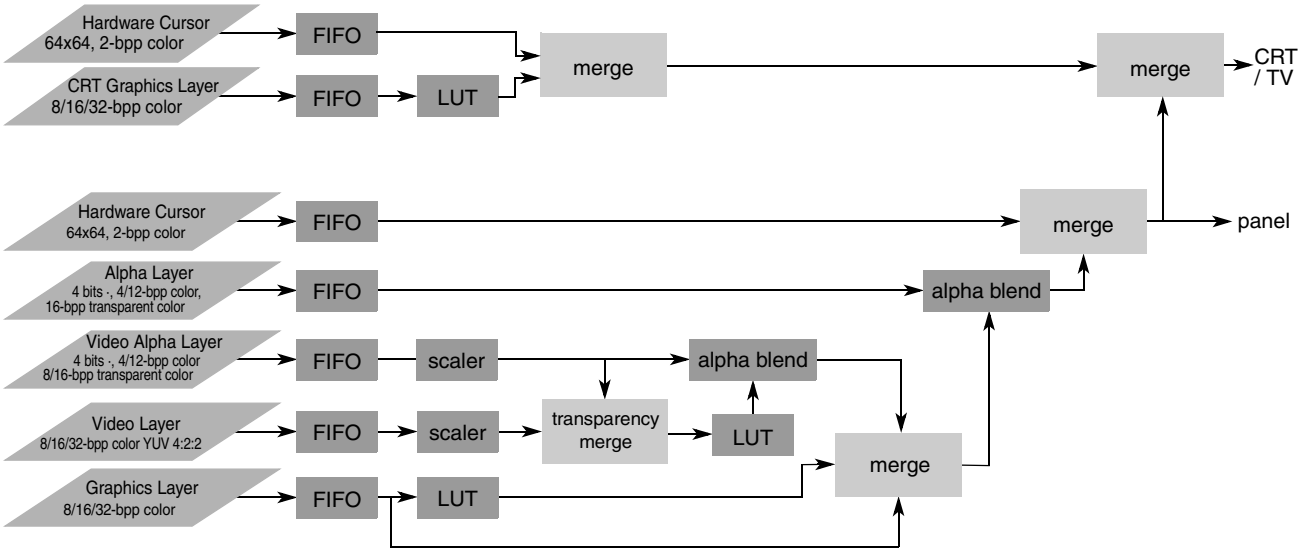


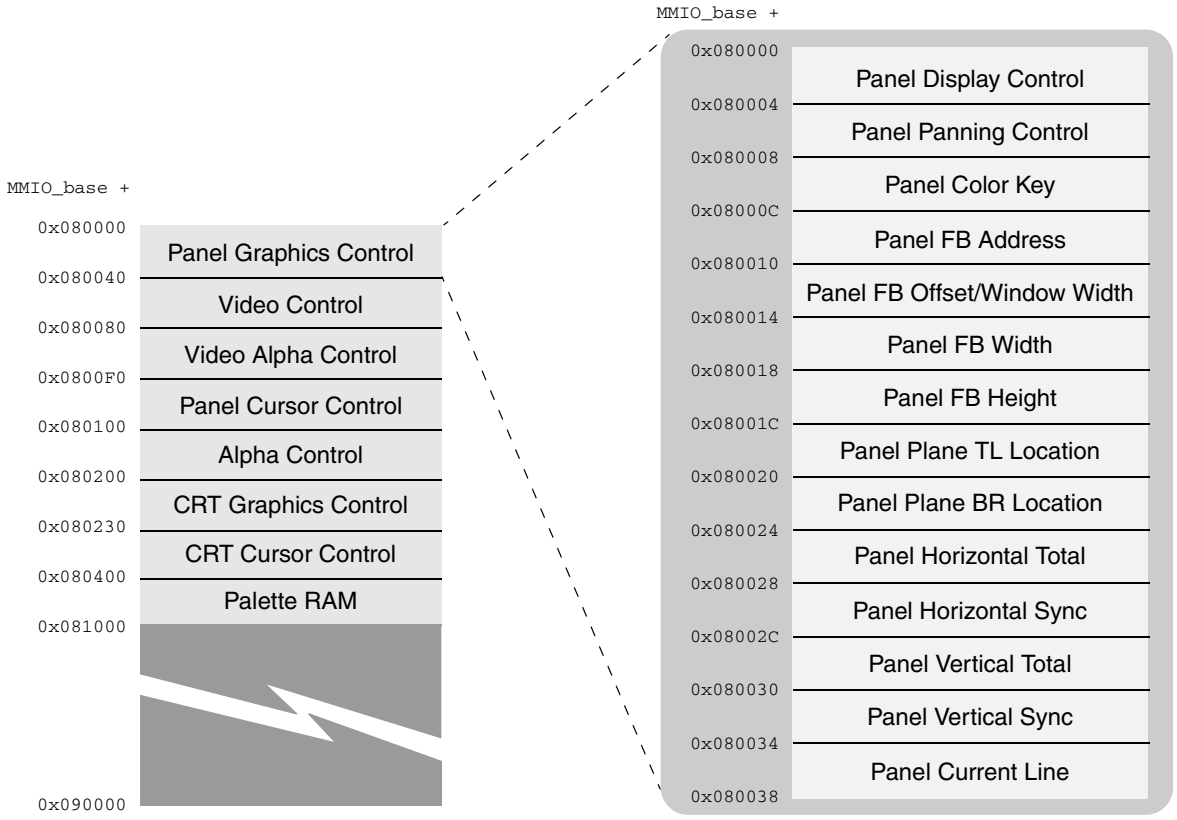
Figure 5-2: Video Layers



Panel Graphics Control Registers

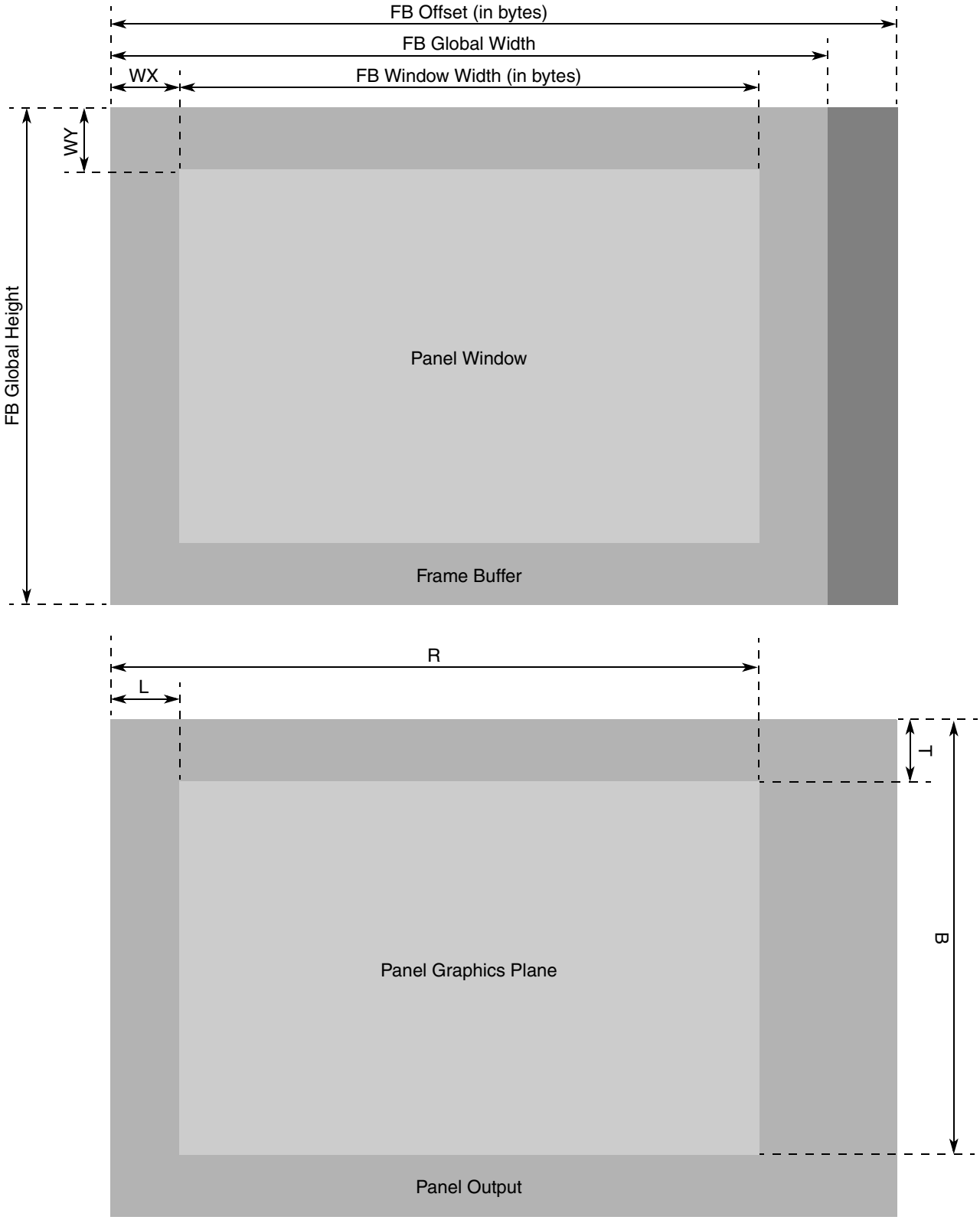
Figure 5-3 shows the layout of the Panel Graphics Control registers.

Figure 5-3: Panel Graphics Control Register Space



To understand video windowing, please refer to Figure 5-4. Here a window is created inside a much large frame buffer. That window is then being displayed on the panel as the Panel Graphics Plane.

Figure 5-4: Video Windowing



Panel Display Control

Read/Write MMIO_base + 0x080000

Power-on Default 0x00010000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				En R/W	Bias R/W	Data R/W	VDD R/W	DP R/W	TFT R/W		DE R/W	LCD R/W		FIFO R/W	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
8-BIT R/W	CP R/W	VSP R/W	HSP R/W	Res	CAPT R/W	CK R/W	TE R/W	VPD R/W	VP R/W	HPD R/W	HP R/W	γ R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	En	Control FPEN Output Pin. 0: Driven low. 1: Driven high.
26	Bias	Control VBIASEN Output Pin. 0: Driven low. 1: Driven high.
25	Data	Panel Control Signals and Data Lines Enable. 0: Disable panel control signals and data lines. 1: Enable panel control signals and data lines.
24	VDD	Control FPVDDEN Output Pin. 0: Driven low. 1: Driven high.
23	DP	Select TFT Dithering Pattern. 0: 4-gray level dithering pattern. 1: 8-gray level dithering pattern.
22:21	TFT	Select TFT Panel Interface. 00: 24-bit RGB 8:8:8. 01: 9-bit RGB 3:3:3. 10: 12-bit RGB 4:4:4.
20	DE	Enable TFT Dithering. 0: Disable. 1: Enable.
19:18	LCD	Select LCD Type. 00: TFT panel. 01: 8-bit STN panel. 11: 12-bit STN panel.
17:16	FIFO	Panel Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15	8-BIT	Enable 8-Bit TV Output. 0: Disable. 1: Enable.

Bit(s)	Name	Description
14	CP	Clock Phase Select. 0: Clock active high. 1: Clock active low.
13	VSP	Vertical Sync Pulse Phase Select. 0: Vertical sync pulse active high. 1: Vertical sync pulse active low.
12	HSP	Horizontal Sync Pulse Phase Select. 0: Horizontal sync pulse active high. 1: Horizontal sync pulse active low.
11	Res	This bit is reserved.
10	CAPT	Enable Capture Timing (Frame Lock). 0: Disable capture timing. 1: Lock panel timing to ZV Port 0 timing.
9	CK	Enable Color Key. 0: Disable color key. 1: Enable color key.
8	TE	Enable Panel Timing. 0: Disable panel timing. 1: Enable panel timing.
7	VPD	Vertical Panning Direction. 0: Panning down. 1: Panning up.
6	VP	Enable Automatic Vertical Panning. 0: Disable. 1: Enable.
5	HPD	Horizontal Panning Direction. 0: Pan to the right. 1: Pan to the left.
4	HP	Enable Automatic Horizontal Panning. 0: Disable. 1: Enable.
3	γ	Enable Gamma Control. Gamma control can only be enabled in RGB 5:6:5 and RGB 8:8:8 modes. 0: Disable. 1: Enable.
2	E	Panel Graphics Plane Enable. 0: Disable panel graphics plane. 1: Enable panel graphics plane.
1:0	Format	Panel Graphics Plane Format. 00: 8-bit indexed mode. 01: 16-bit RGB 5:6:5 mode. 10: 32-bit RGB 8:8:8 mode.

Panel Panning Control

Read/Write MMIO_base + 0x080004

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VPan R/W								Reserved		VWait R/W					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HPan R/W								Reserved		HWait R/W					

Bit(s)	Name	Description
31:24	VPan	Number of lines to pan vertically.
23:22	Reserved	These bits are reserved.
21:16	VWait	Number of vertical sync pulses for each vertical pan.
15:8	HPan	Number of pixels to pan horizontally.
7:6	Reserved	These bits are reserved.
5:0	HWait	Number of horizontal sync pulses for each horizontal pan.

Panel Color Key

Read/Write MMIO_base + 0x080008

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mask R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value R/W															

Bit(s)	Name	Description
31:16	Mask	Color key mask for video window plane.
15:0	Value	Color key value for video window plane.

Panel FB Address

Read/Write MMIO_base + 0x08000C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of frame buffer for the panel graphics plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Panel FB Offset/Window Width

Read/Write MMIO_base + 0x080010

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		FB Window Width R/W										0 0 0 0			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		FB Offset R/W										0 0 0 0			

Bit(s)	Name	Description
31:30	Reserved	These bits are reserved.
29:20	FB Window Width	Number of bytes per line of the frame buffer window specified in 128-bit aligned bytes.

Bit(s)	Name	Description
19:16	0000	These bits are hardwired to zeros.
15:14	Reserved	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the FB graphics plane (see Figure 5-4).
3:0	0000	These bits are hardwired to zeros.

Panel FB Width

Read/Write MMIO_base + 0x080014

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				FB Global Width R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				WX R/W											

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	FB Global Width	Width of FB graphics window specified in pixels (see Figure 5-4).
15:12	Reserved	These bits are reserved.
11:0	WX	Starting x-coordinate of panel graphics window specified in pixels (see Figure 5-4).

Panel FB Height

Read/Write MMIO_base + 0x080018
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				FB Global Height R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				WY R/W											

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	FB GLobal Height	Height of FB graphics window specified in lines (see Figure 5-4).
15:12	Reserved	These bits are reserved.
11:0	WY	Starting y-coordinate of panel graphics window specified in lines (see Figure 5-4).

Panel Plane TL Location

Read/Write MMIO_base + 0x08001C
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					T R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					L R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	T	Top location of the panel graphics plane specified in lines (see Figure 5-4).
15:11	Reserved	These bits are reserved.
10:0	L	Left location of the panel graphics plane specified in pixels (see Figure 5-4).

Panel Plane BR Location

Read/Write MMIO_base + 0x080020
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					B R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					R R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	B	Bottom location of the panel graphics plane specified in lines (see Figure 5-4).
15:11	Reserved	These bits are reserved.
10:0	R	Right location of the panel graphics plane specified in pixels (see Figure 5-4).

Panel Horizontal Total

Read/Write MMIO_base + 0x080024
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				HT R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				HDE R/W											

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	HT	Panel horizontal total specified as number of pixels - 1.
15:12	Reserved	These bits are reserved.
11:0	HDE	Panel horizontal display end specified as number of pixels - 1.

Panel Horizontal Sync

Read/Write MMIO_base + 0x080028

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								HSW R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				HS R/W											

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:16	HSW	Panel horizontal sync width specified in pixels.
15:12	Reserved	These bits are reserved.
11:0	HS	Panel horizontal sync start specified as pixel number - 1.

Panel Vertical Total

Read/Write MMIO_base + 0x08002C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					VT R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					VDE R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	VT	Panel vertical total specified as number of lines - 1.
15:11	Reserved	These bits are reserved.
10:0	VDE	Panel vertical display end specified as number of lines - 1.

Panel Vertical Sync

Read/Write MMIO_base + 0x080030
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										VSH R/W					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					VS R/W										

Bit(s)	Name	Description
31:22	Reserved	These bits are reserved.
21:16	VSH	Panel vertical sync height specified in lines.
15:11	Reserved	These bits are reserved.
10:0	VS	Panel vertical sync start specified as line number - 1.

Panel Current Line

Read MMIO_base + 0x080034
Power-on Default 0b0000.0000.0000.0000.0000.0XXX.XXXX.XXXX

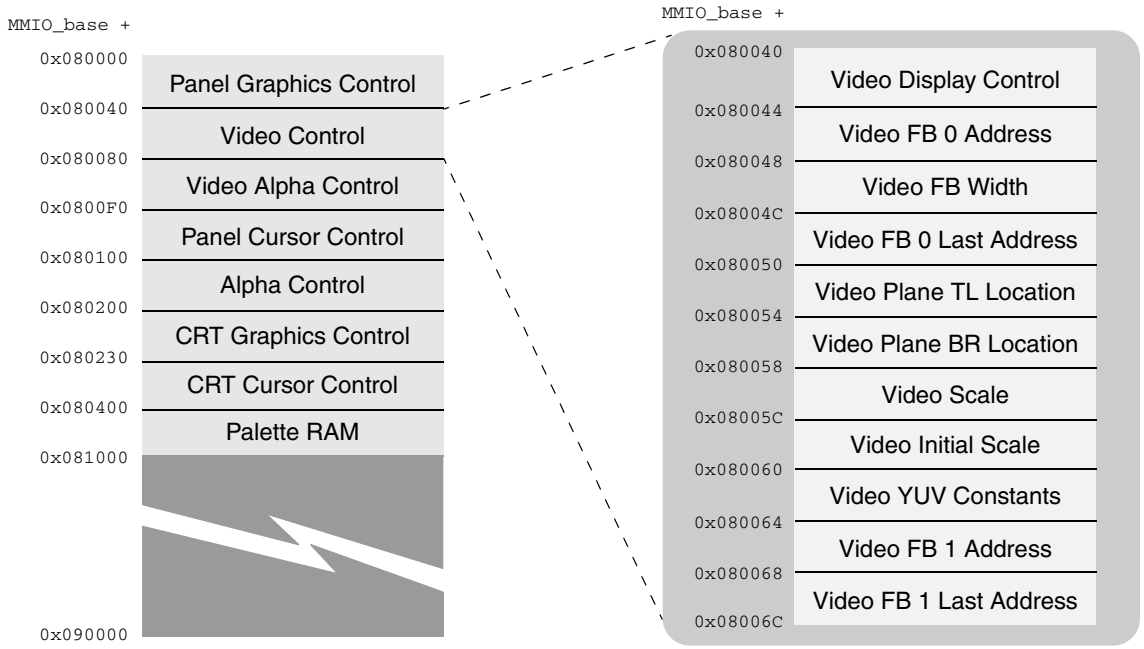
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					Line R										

Bit(s)	Name	Description
31:11	Reserved	These bits are reserved.
10:0	Line	Panel current line being fetched.

Video Control Registers

Figure 5-5 shows the layout of the Video Control registers.

Figure 5-5: Video Control Register Space



Video Display Control

Read/Write MMIO_base + 0x080040

Power-on Default 0b0000.0000.0000.0001.X000.0000.0000.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														FIFO R/W	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Buf R	CB R/W	DB R/W	BS R/W	VS R/W	HS R/W	VI R/W	HI R/W	Pixel R/W				γ R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:18	Reserved	These bits are reserved.
17:16	FIFO	Video Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.

Bit(s)	Name	Description
15	Buf	Current Video Frame Buffer Used. This bit is read-only. 0: Buffer 0. 1: Buffer 1.
14	CB	Use Capture Frame Buffer as Video Frame Buffer. 0: Disable. 1: Enable.
13	DB	Enable Double Buffering. 0: Disable. 1: Enable.
12	BS	Enable Byte Swapping for YUV Data. 0: Disable (YUYV). 1: Enable (UYVY).
11	VS	Force Vertical Scale Factor to ½. 0: Disable. 1: Enable.
10	HS	Force Horizontal Scale Factor to ½. 0: Disable. 1: Enable.
9	VI	Enable Vertical Interpolation. 0: Disable. 1: Enable.
8	HI	Enable Horizontal Interpolation. 0: Disable. 1: Enable.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	γ	Enable Gamma Control. Gamma control can be enabled only in RGB 5:6:5 and RGB 8:8:8 modes.[1] 0: Disable. 1: Enable.
2	E	Video Plane Enable. 0: Disable video plane. 1: Enable video plane.
1:0	Format	Video Plane Format. 00: 8-bit indexed mode. 01: 16-bit RGB 5:6:5 mode. 10: 32-bit RGB 8:8:8 mode. 11: 16-bit YUYV mode.

1. All display devices have an inherent non-linearity so that the intensity of the output is not linearly proportional to the input signal over the full range of input values. The gamma control helps to correct this nonlinearity.

Video FB 0 Address

Read/Write MMIO_base + 0x080044

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of frame buffer 0 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video FB Width

Read/Write MMIO_base + 0x080048

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		Width R/W										0 0 0 0			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		Offset R/W										0 0 0 0			

Bit(s)	Name	Description
31:30	Reserved	These bits are reserved.
29:20	Width	Number of bytes per line of the video plane specified in 128-bit aligned bytes.

Bit(s)	Name	Description
19:16	0000	These bits are hardwired to zeros.
15:14	Reserved	These bits are reserved.
13:4	Offset	Number of 128-bit aligned bytes per line of the video plane.
3:0	0000	These bits are hardwired to zeros.

Video FB 0 Last Address

Read/Write MMIO_base + 0x08004C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of last byte of frame buffer 0 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video Plane TL Location

Read/Write MMIO_base + 0x080050
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					T R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					L R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	T	Top location of the video plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	L	Left location of the video plane specified in pixels.

Video Plane BR Location

Read/Write MMIO_base + 0x080054
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					B R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					R R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	B	Bottom location of the video plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	R	Right location of the video plane specified in pixels.

Video Scale

Read/Write MMIO_base + 0x080058

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VS R/W	Reserved			VScale R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HS R/W	Reserved			HScale R/W											

Bit(s)	Name	Description
31	VS	Select Vertical Video Scaling. 0: Video expands vertically. 1: Video shrinks vertically.
30:28	Reserved	These bits are reserved.
27:16	VScale	Vertical Video Scale Factor. For expansion: VScale = ($height_{src}$ / $height_{dest}$) * 2^{12}. For shrinking: VScale = ($height_{dest}$ / $height_{src}$) * 2^{12}.
15	HS	Select Horizontal Video Scaling. 0: Video expands horizontally. 1: Video shrinks horizontally.
14:12	Reserved	These bits are reserved.
11:0	HScale	Horizontal Video Scale Factor. For expansion: HScale = ($width_{src}$ / $width_{dest}$) * 2^{12} For shrinking: HScale = ($width_{dest}$ / $width_{src}$) *2^{12}

Scaling example: To expand (magnify) the horizontal scale by a factor of 3:

1. Set HS = 0.
2. Calculate the scaling factor:

   ($width_{src}$ / $width_{dest}$) * 2^{12} = (1/3) * 2^{12}
3. Set HScale. In this example, HScale = 0101 0101 0101 binary or 555 hex.

To shrink the horizontal scale by a factor of 3:

1. Set HS = 1.
2. Calculate the scaling factor:

   ($width_{dest}$ / $width_{src}$) * 2^{12} = ((1/3)/1) * 2^{12} = 1/3 * 2^{12}
3. Set HScale. Note that the HScale setting is the same for shrinking by 1/3 as it is for magnifying by a factor of 3, only the setting of HS differs

Video Initial Scale

Read/Write MMIO_base + 0x08005C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				$VScale_1$ R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				$VScale_0$ R/W											

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	$VScale_1$	Initial vertical scale factor for video buffer 1.
15:12	Reserved	These bits are reserved.
11:0	$VScale_0$	Initial vertical scale factor for video buffer 0.

Video YUV Constants

Read/Write MMIO_base + 0x080060

Power-on Default 0x00EDEDED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Adjustment.
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	Blue Conversion Constant.

Video FB 1 Address

Read/Write MMIO_base + 0x080064

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W R/W	Address									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of frame buffer 1 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video FB 1 Last Address

Read/Write MMIO_base + 0x080068

Power-on Default Undefined

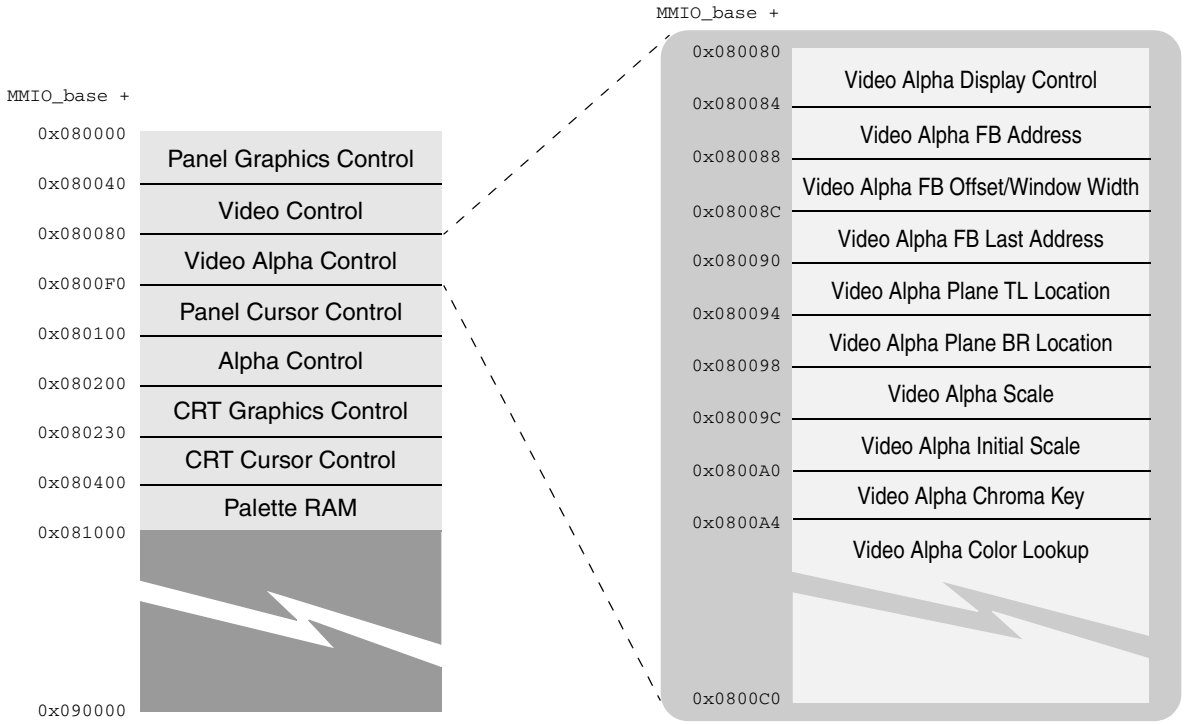
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of last byte of frame buffer 1 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video Alpha Control Registers

Figure 5-6 shows the layout of the Video Alpha Control registers.

Figure 5-6: Video Alpha Control Register Space



Video Alpha Display Control

Read/Write MMIO_base + 0x080080

Power-on Default 0x00010000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			Sel R/W	Alpha R/W				Reserved						FIFO R/W	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				VS R/W	HS R/W	VI R/W	HI R/W	Pixel R/W				CK R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:29	Reserved	These bits are reserved.
28	Sel	Alpha Select. 0: Use per-pixel alpha values. 1: Use alpha value specified in *Alpha*.

Bit(s)	Name	Description
27:24	Alpha	Video Alpha Plane Alpha Value. This field is only valid when the *Sel* bit is 1.
23:18	Reserved	These bits are reserved.
17:16	FIFO	Video Alpha Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15:12	Reserved	These bits are reserved.
11	VS	Force Vertical Scale Factor to ½. 0: Disable. 1: Enable.
10	HS	Force Horizontal Scale Factor to ½. 0: Disable. 1: Enable.
9	VI	Enable Vertical Interpolation. 0: Disable. 1: Enable.
8	HI	Enable Horizontal Interpolation. 0: Disable. 1: Enable.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	CK	Enable Chroma Key. 0: Disable. 1: Enable.
2	E	Video Alpha Plane Enable. 0: Disable video plane. 1: Enable video plane.
1:0	Format	Video Alpha Plane Format. 00: 8-bit indexed mode. 01: 16-bit RGB 5:6:5 mode. 10: 8-bit indexed αI 4:4 mode. 11: 16-bit αRGB 4:4:4:4 mode.

Video Alpha FB Address

Read/Write MMIO_base + 0x080084

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of frame buffer for the video alpha plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video Alpha FB Offset/Window Width

Read/Write MMIO_base + 0x080088

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		Window Width R/W										0 0 0 0			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		FB Offset R/W										0 0 0 0			

Bit(s)	Name	Description
31:30	Reserved	These bits are reserved.
29:20	Window Width	Number of bytes per line of the video alpha window specified in 128-bit aligned bytes.

Bit(s)	Name	Description
19:16	0000	These bits are hardwired to zeros.
15:14	Reserved	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the video alpha FB.
3:0	0000	These bits are hardwired to zeros.

Video Alpha FB Last Address

Read/Write MMIO_base + 0x08008C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of last byte of frame buffer for the video alpha plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video Alpha Plane TL Location

Read/Write MMIO_base + 0x080090
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Top R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					Left R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Top	Top location of the video alpha plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	Left	Left location of the video alpha plane specified in pixels.

Video Alpha Plane BR Location

Read/Write MMIO_base + 0x080094
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Bottom R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					Right R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Bottom	Bottom location of the video alpha plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	Right	Right location of the video alpha plane specified in pixels.

Video Alpha Scale

Read/Write MMIO_base + 0x080098

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VS R/W	Reserved			VScale R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HS R/W	Reserved			HScale R/W											

Bit(s)	Name	Description
31	VS	Select Vertical Video Scaling. 0: Video expands vertically. 1: Video shrinks vertically.
30:28	Reserved	These bits are reserved.
27:16	VScale	Vertical Video Scale Factor. For expansion: VScale = $height_{src}$ / $height_{dest}$ * 2^{12}. For shrinking: VScale = $height_{dest}$ / $height_{src}$ * 2^{12}.
15	HS	Select Horizontal Video Scaling. 0: Video expands horizontally. 1: Video shrinks horizontally.
14:12	Reserved	These bits are reserved.
11:0	HScale	Horizontal Video Scale Factor. For expansion: HScale = $width_{src}$ / $width_{dest}$ * 2^{12}. For shrinking: HScale = $width_{dest}$ / $width_{src}$ * 2^{12}.

Video Alpha Initial Scale

Read/Write MMIO_base + 0x08009C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				VScale R/W											

Bit(s)	Name	Description
31:12	Reserved	These bits are reserved.
11:0	VScale	Initial Vertical Scale Factor.

Video Alpha Chroma Key

Read/Write MMIO_base + 0x0800A0

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mask R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value R/W															

Bit(s)	Name	Description
31:16	Mask	Chroma Key Mask for Video Alpha Plane. 0: Compare respective bit. 1: Do not compare respective bit.
15:0	Value	Chroma Key Value for Video Alpha Plane.

Video Alpha Color Lookup

Read/Write MMIO_base + 0x0800A4 - 0x0800C0

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Lookup_1$ R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$Lookup_0$ R/W															

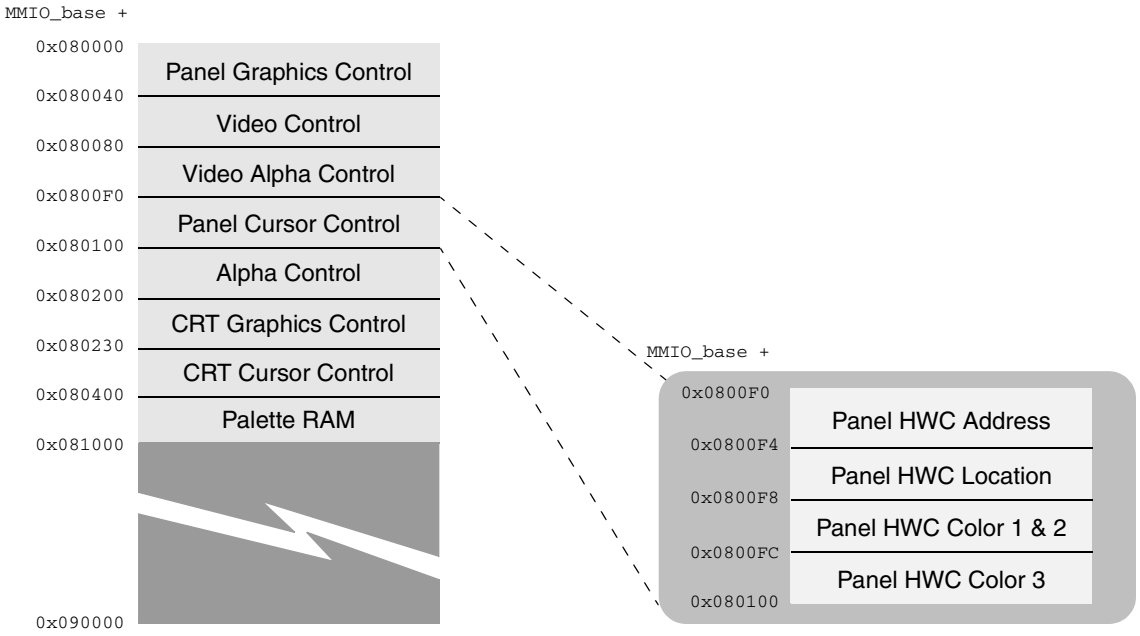
Bit(s)	Name	Description
31:16	$Lookup_1$	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 1.
15:0	$Lookup_0$	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 0.

There are 8 Video Alpha Color Lookup registers, each containing two RGB 5:6:5 color lookup values for each of the 16 4-bit indexed colors.

Panel Cursor Control Registers

Figure 5-7 shows the layout of the Panel Cursor Control registers.

Figure 5-7: Panel Cursor Control Register Space



Panel HWC Address

Read/Write MMIO_base + 0x0800F0
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	E	Enable Panel Hardware Cursor. 0: Disable. 1: Enable.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.

Bit(s)	Name	Description
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of panel hardware cursor with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Panel HWC Location

Read/Write MMIO_base + 0x0800F4

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				T R/W	Y R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				L R/W	X R/W										

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	T	Top Boundary Select. 0: Panel hardware cursor is within screen top boundary. 1: Panel hardware cursor is partially outside screen top boundary.
26:16	Y	Panel Hardware Cursor Y Position.
15:12	Reserved	These bits are reserved.
11	L	Left Boundary Select. 0: Panel hardware cursor is within screen left boundary. 1: Panel hardware cursor is partially outside screen left boundary.
10:0	X	Panel Hardware Cursor X Position.

Panel HWC Color 1 & 2

Read/Write MMIO_base + 0x0800F8

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Color_2$ R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$Color_1$ R/W															

Bit(s)	Name	Description
31:16	$Color_2$	Panel hardware cursor color 2 in RGB 5:6:5.
15:0	$Color_1$	Panel hardware cursor color 1 in RGB 5:6:5.

Panel HWC Color 3

Read/Write MMIO_base + 0x0800FC

Power-on Default Undefined

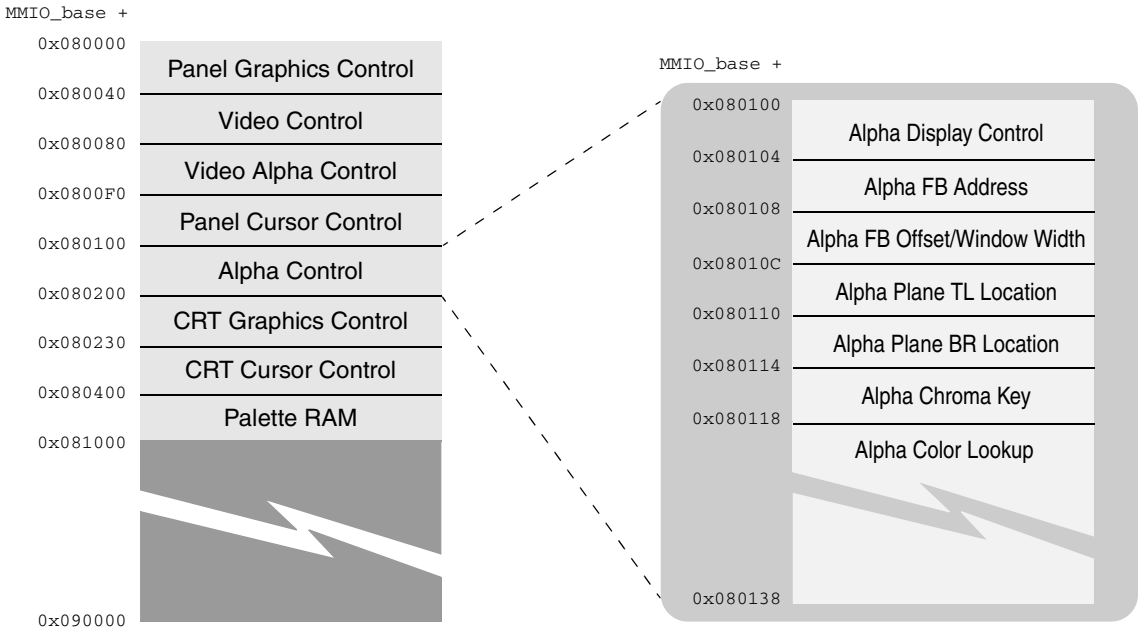
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$Color_3$ R/W															

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:0	$Color_3$	Panel hardware cursor color 3 in RGB 5:6:5.

Alpha Control Registers

Figure 5-8 shows the layout of the Alpha Control registers.

Figure 5-8: Alpha Control Register Space



Alpha Display Control

Read/Write MMIO_base + 0x080100

Power-on Default 0x00010000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			Sel R/W	Alpha R/W				Reserved						FIFO R/W	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved								Pixel R/W				CK R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:29	Reserved	These bits are reserved.
28	Sel	Alpha Select. 0: Use per-pixel alpha values. 1: Use alpha value specified in *Alpha*.
27:24	Alpha	Alpha Plane Alpha Value. This field is only valid when the *Sel* bit is 1.
23:18	Reserved	These bits are reserved.

Bit(s)	Name	Description
17:16	FIFO	Video Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15:8	Reserved	These bits are reserved.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	CK	Enable Chroma Key. 0: Disable chroma key. 1: Enable chroma key.
2	E	Alpha Plane Enable. 0: Disable alpha plane. 1: Enable alpha plane.
1:0	Format	Alpha Plane Format. 01: 16-bit RGB 5:6:5 mode. 10: 8-bit indexed αl 4:4 mode. 11: 16-bit αRGB 4:4:4:4 mode.

Alpha FB Address

Read/Write MMIO_base + 0x080104

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of frame buffer for the alpha plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Alpha FB Offset/Window Width

Read/Write MMIO_base + 0x080108

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		Window Width R/W										0 0 0 0			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		FB Offset R/W										0 0 0 0			

Bit(s)	Name	Description
31:30	Reserved	These bits are reserved.
29:20	Window Width	Number of bytes per line of the alpha window specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Reserved	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the alpha FB.
3:0	0000	These bits are hardwired to zeros.

Alpha Plane TL Location

Read/Write MMIO_base + 0x08010C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Top R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					Left R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Top	Top location of the alpha plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	Left	Left location of the alpha plane specified in pixels.

Alpha Plane BR Location

Read/Write MMIO_base + 0x080110

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Bottom R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					Right R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Bottom	Bottom location of the alpha plane specified in lines.
15:11	Reserved	These bits are reserved.
10:0	Right	Right location of the alpha plane specified in pixels.

Alpha Chroma Key

Read/Write MMIO_base + 0x080114

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mask R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value R/W															

Bit(s)	Name	Description
31:16	Mask	Chroma Key Mask for Alpha Plane. 0: Compare respective bit. 1: Do not compare respective bit.
15:0	Value	Chroma Key Value for Alpha Plane.

Alpha Color Lookup

Read/Write MMIO_base + 0x080118 - 0x080134

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Lookup_1$ R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$Lookup_0$ R/W															

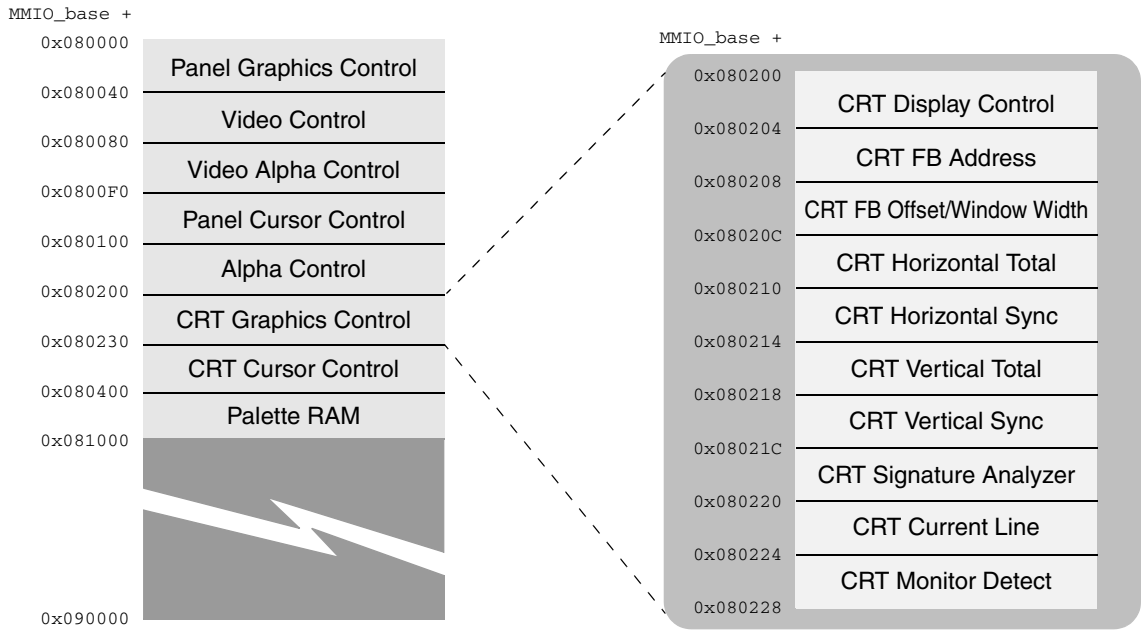
Bit(s)	Name	Description
31:16	$Lookup_1$	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 1.
15:0	$Lookup_0$	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 0.

There are 8 Alpha Color Lookup registers, each containing two RGB 5:6:5 color lookup values for each of the 16 4-bit indexed colors.

CRT Graphics Control Registers

Figure 5-9 shows the layout of the CRT Graphics Control registers.

Figure 5-9: CRT Graphics Control Register Space



CRT Display Control

Read/Write MMIO_base + 0x080200

Power-on Default 0x00010000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														FIFO R/W	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TVP R/W	CP R/W	VSP R/W	HSP R/W	VS R	B R/W	Sel R/W	TE R/W	Pixel R/W				γ R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:18	Reserved	These bits are reserved.
17:16	FIFO	CRT Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.

Bit(s)	Name	Description
15	TVP	TV Clock Phase Select. 0: TV clock active high. 1: TV clock active low.
14	CP	CRT Clock Phase Select. 0: CRT clock active high. 1: CRT clock active low.
13	VSP	Vertical Sync Pulse Phase Select. 0: Vertical sync pulse active high. 1: Vertical sync pulse active low.
12	HSP	Horizontal Sync Pulse Phase Select. 0: Horizontal sync pulse active high. 1: Horizontal sync pulse active low.
11	VS	Vertical Sync. This bit is read only.
10	B	CRT Data Blanking. 0: CRT will show pixels. 1: CRT will be blank.
9	Sel	CRT Data Select. 0: CRT will display panel data. 1: CRT will display CRT data.
8	TE	Enable CRT Timing. 0: Disable CRT timing. 1: Enable CRT timing.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	γ	Enable Gamma Control. Gamma control can be enabled only in RGB 5:6:5 and RGB 8:8:8 modes. 0: Disable gamma control. 1: Enable gamma control.
2	E	CRT Graphics Plane Enable. 0: Disable CRT Graphics plane. 1: Enable CRT Graphics plane.
1:0	Format	CRT Graphics Plane Format. 00: 8-bit indexed mode. 01: 16-bit RGB 5:6:5 mode. 10: 32-bit RGB 8:8:8 mode.

CRT FB Address

Read/Write MMIO_base + 0x080204

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of the frame buffer for the CRT graphics plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

CRT FB Offset/Window Width

Read/Write MMIO_base + 0x080208

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		Window Width R/W										0 0 0 0			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		FB Offset R/W										0 0 0 0			

Bit(s)	Name	Description
31:30	Reserved	These bits are reserved.
29:20	Window Width	Number of bytes per line of the CRT graphics window specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Reserved	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the CRT graphics FB.
3:0	0000	These bits are hardwired to zeros.

CRT Horizontal Total

Read/Write MMIO_base + 0x08020C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				HT R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				HDE R/W											

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27:16	HT	CRT horizontal total specified as number of pixels - 1.
15:12	Reserved	These bits are reserved.
11:0	HDE	CRT horizontal display end specified as number of pixels - 1.

CRT Horizontal Sync

Read/Write MMIO_base + 0x080210
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								HSW R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				HS R/W											

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:16	HSW	CRT horizontal sync width specified in pixels.
15:12	Reserved	These bits are reserved.
11:0	HS	CRT horizontal sync start specified as pixel number - 1.

CRT Vertical Total

Read/Write MMIO_base + 0x080214
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					VT R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					VDE R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	VT	CRT vertical total specified as number of lines - 1.
15:11	Reserved	These bits are reserved.
10:0	VDE	CRT vertical display end specified as number of lines - 1.

CRT Vertical Sync

Read/Write MMIO_base + 0x080218

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										VSH R/W					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					VS R/W										

Bit(s)	Name	Description
31:22	Reserved	These bits are reserved.
21:16	VSH	CRT vertical sync height specified in lines.
15:11	Reserved	These bits are reserved.
10:0	VS	CRT vertical sync start specified as line number - 1.

CRT Signature Analyzer

Read/Write MMIO_base + 0x08021C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Status R															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved												E R/W	R R/W	Sel R/W	

Bit(s)	Name	Description
31:16	Status	Analyzer Signature. This field is read-only.
15:4	Reserved	These bits are reserved.
3	E	Enable Signature Analyzer. 0: Disable. 1: Enable.

Bit(s)	Name	Description
2	R	Reset Signature Analyzer. 0: Normal. 1: Reset.
1:0	Sel	Source Select for Signature Analyzer. 00: Red color. 01: Green color. 10: Blue color.

CRT Current Line

Read MMIO_base + 0x080220

Power-on Default 0b0000.0000.0000.0000.0000.0XXX.XXXX.XXXX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					Line R										

Bit(s)	Name	Description
31:11	Reserved	These bits are reserved.
10:0	Line	CRT Current Line Being Fetched.

CRT Monitor Detect

Read/Write MMIO_base + 0x080224

Power-on Default 0b0000.0000.XXXX.XXXX.XXXX.XXXX.XXXX.XXXX

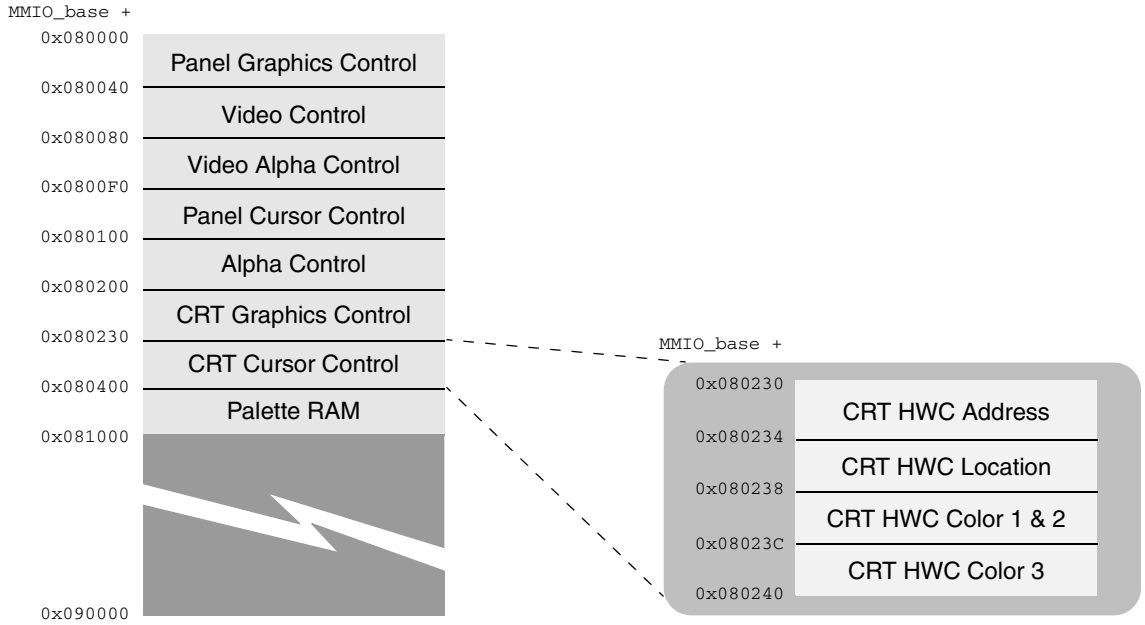
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						MDET R	E R/W	Data R							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data R															

Bit(s)	Name	Description
31:26	Reserved	These bits are reserved.
25	MDET	Monitor Detect Read Back. 1: All R, G, and B voltages are greater than 0.325 V. 0: All R, G, and B voltages are less than or equal to 0.325 V.
24	E	Monitor Detect Enable. 0: Disable. 1: Enable.
23:0	Data	Monitor Detect Data in RGB 8:8:8. This field is read-only.

CRT Cursor Control Registers

Figure 5-10 shows the layout of the CRT Cursor Control registers.

Figure 5-10:CRT Cursor Control Register Space



CRT HWC Address

Read/Write MMIO_base + 0x080230

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E R/W	Reserved			Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	E	Enable CRT Hardware Cursor. 0: Disable. 1: Enable.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.

Bit(s)	Name	Description
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of CRT hardware cursor with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

CRT HWC Location

Read/Write MMIO_base + 0x080234

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				T R/W	Y R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				L R/W	X R/W										

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	T	Top Boundary Select. 0: CRT hardware cursor is within screen top boundary. 1: CRT hardware cursor is partially outside screen top boundary.
26:16	Y	CRT Hardware Cursor Y Position.
15:12	Reserved	These bits are reserved.
11	L	Left Boundary Select. 0: CRT hardware cursor is within screen left boundary. 1: CRT hardware cursor is partially outside screen left boundary.
10:0	X	CRT Hardware Cursor X Position.

CRT HWC Color 1 & 2

Read/Write MMIO_base + 0x080238

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Color_2$ R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$Color_1$ R/W															

Bit(s)	Name	Description
31:16	$Color_2$	CRT Hardware Cursor Color 2 in RGB 5:6:5.
15:0	$Color_1$	CRT Hardware Cursor Color 1 in RGB 5:6:5.

CRT HWC Color 3

Read/Write MMIO_base + 0x08023C

Power-on Default Undefined

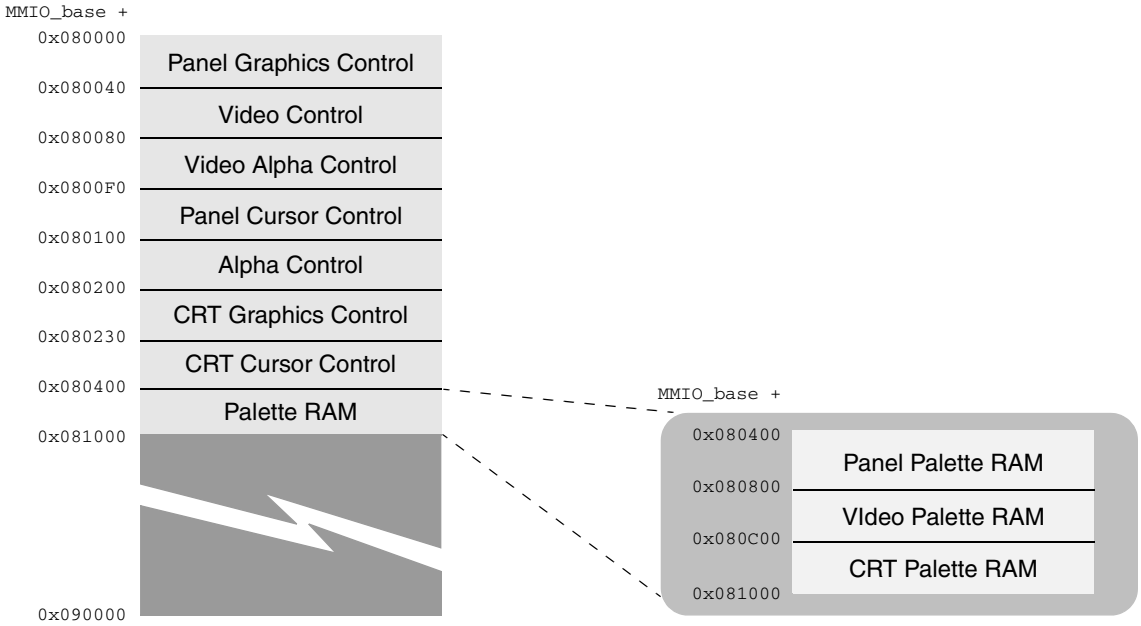
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$Color_3$ R/W															

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:0	$Color_3$	CRT Hardware Cursor Color 3 in RGB 5:6:5.

Palette RAM Registers

Figure 5-11 shows the layout of the Palette RAM registers.

Figure 5-11:Palette RAM Register Space



Panel Palette RAM

Read/Write MMIO_base + 0x080400 - 0x0807FC

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								Red R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Green R/W								Blue R/W							

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:16	Red	For indexed color modes: 8-bit red color value. For 16- and 32-bit color modes: 8-bit red alpha value.
15:8	Green	For indexed color modes: 8-bit green color value. For 16- and 32-bit color modes: 8-bit green alpha value.
7:0	Blue	For indexed color modes: 8-bit blue color value. For 16- and 32-bit color modes: 8-bit blue alpha value.

There are 256 Panel Palette RAM registers, each containing a 24-bit RGB 8:8:8 color value.

Video Palette RAM

Read/Write MMIO_base + 0x080800 - 0x080BFC

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								Red R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Green R/W								Blue R/W							

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:16	Red	For indexed color modes: 8-bit red color value. For 16- and 32-bit color modes: 8-bit red alpha value.
15:8	Green	For indexed color modes: 8-bit green color value. For 16- and 32-bit color modes: 8-bit green alpha value.
7:0	Blue	For indexed color modes: 8-bit blue color value. For 16- and 32-bit color modes: 8-bit blue alpha value.

There are 256 Video Palette RAM registers, each containing a 24-bit RGB 8:8:8 color value.

CRT Palette RAM

Read/Write MMIO_base + 0x080C00 - 0x080FFC

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								Red R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Green R/W								Blue R/W							

Bit(s)	Name	Description
31:24	Reserved	These bits are reserved.
23:16	Red	For indexed color modes: 8-bit red color value. For 16- and 32-bit color modes: 8-bit red alpha value.

Bit(s)	Name	Description
15:8	Green	For indexed color modes: 8-bit green color value. For 16- and 32-bit color modes: 8-bit green alpha value.
7:0	Blue	For indexed color modes: 8-bit blue color value. For 16- and 32-bit color modes: 8-bit blue alpha value.

There are 256 Video Palette RAM registers, each containing a 24-bit RGB 8:8:8 color value.

6 Command List Interpreter

Functional Overview

The Command List allows a number of tasks to be executed by a state machine to offload the CPU. Most of the commands are to write to registers and local memory in the SM107 memory map. There are also some flow commands that allow jumping to different locations in the Command List or calling common subroutines stored in the main memory.

The basic layout of an entry in the Command List looks like this:

Command **OPCODE**

63															**32**
Data															
31		**28**	**27**												**0**
				Address											

The command is a 4-bit field that is split into two regions. When bit 31 (bit 3 of the command) is 0, the command is to be executed. If bit 31 is 1, the specified command is a flow command and as a result the Command List FIFO will be flushed.

The Address field is specified in the SM107 Address Space. For internal memory, only bits 0 through 25 are used to address the 64MB address range. In this case, bits 26 and 27 are “0”. When bit 27 is set to “1”, the address space does not specify an internal memory address, but rather a memory address that lives on the host bus. Bits 0 through 26 specify a 128MB address range.

Programming

To execute the Command List, the CPU is first building a valid Command List structure and then programs the start address of the Command List in the Command List Start Address register. The Command List should be terminated by the FINISH command.

Flow Commands

Several commands can be used to change the flow of the Command List. There are GOTO and GOSUB commands, as well as a conditional JUMP command.

All destination addresses can be either relative or absolute. This makes it easy to jump over certain commands in the Command List or jump to common subroutines stored in main memory.

The conditional JUMP command can be used to test for any of the 32 software-programmable conditional states. If any of the requested conditional states is set, the jump is taken.

Appending to the Command List

The procedure for chaining command lists is:

1. Fill the command list buffer after the last FINISH command. The software should always keep track of the address of the last FINISH command.
2. Terminate the command list with a FINISH and remember the address of this FINISH.
3. Stop the command list by programming “0” in bit 31 of the Command List Address register.
4. Read and remember the current program counter.
5. Replace the previous FINISH command with a NOP command (00000000C0000000).
6. Restart the command list by programming the saved program counter and “1” in bit 31 of the Command List Address register.

Register Descriptions

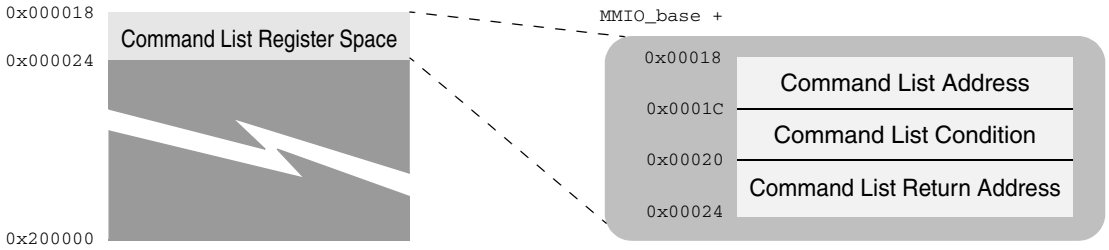
Table 6-1 summarizes the Command List registers.

Table 6-1: Command List Register Summary

Address	Type	Width	Reset Value	Register Name
0x000018	R/W	32	N/A	Command List Address
0x00001C	R/W	32	N/A	Command List Condition
0x000020	R	32	N/A	Command List Return Address

Figure 6-1 defines the register layout for the Command List registers.

Figure 6-1: Command List Register Space



Command List Address

Read/Write Address 0x000018

Power-on Default N/A

31	30	29	28	27								3	2		0
S R/W	Res	Res		Command List Address R/W									000		

Bit(s)	Name	Description
S	Start	When this bit is programmed to “1”, the Command List will fetch the first instruction from the Command List specified by the Command List Address field. It will remain “1” as long as the Command List is executing code in the Command List. As soon as you program this bit to “0”, the Command List will stop executing. Programming it back to “1” will continue the Command List at the address it has left off.
30	Idle	Idle status. 0: busy. 1: idle (default).
29:28	Res	These bits are reserved.
27:0	Command List Address	The current address of the Command List. The Command List updates this address continuously. Bits [2:0] are hardwired to “0” since every command must be aligned on a 64-bit boundary. It always points to the instruction being executed.

When the *Start* bit is programmed to “0”, the command interpreter will stop after the current command has been executed. This means the *Command List Address* (program counter) will contain the address of the next instruction that is going to be executed when the Start bit is programmed to “1” again.

When programming the *Start* bit to “0” when conditional jumps are being executed, the *Command List Address* contains the next logical address of the instruction to fetch, depending if the jump is taken or not.

Note: Note that a read of this register returns the Program Counter from the command list. This value is different than the value programmed into the *Command List Address* field. So if you want to restart the command list after a STOP (clearing the *S* bit), you need to program the correct Program Counter value into the *Command List Address* field. This normally is not a program since you need to do a read/modify/write instruction anyway to clear the *S* bit.

Command List Condition

Read/Write Address 0x00001C

Power-on Default N/A

31															0
Conditions R/W															

Bit(s)	Name	Description
31:0	Conditions	Every bit in the Conditions field holds one condition. The conditions are totally controlled by software. The Conditional Jump command will mask the requested condition with this Condition field. If any bit is set after this mask, the condition returns TRUE and the jump is taken.

Command List Return Address

Read Address 0x000020

Power-on Default N/A

31			28	27								3	2		0
Res				Return Address R									000		

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:0	Return Address	The GOSUB command will store the address of the next command in the Command List in this register. The RETURN command will jump to the address specified in this register. Bits [2:0] are hardwired to “0” since every command must be aligned on a 64-bit boundary.

Commands

Table 6-2 lists the 16 commands recognized by the Command List Interpreter.

Table 6-2: SM107 Commands

0000	Load Memory	1000	Finish
0001	Load Register	1001	Goto
0010	Load Memory Immediate	1010	Gosub
0011	Load Register Immediate	1011	Return
0100	Load Memory Indirect	1100	Conditional Jump
0101	Load Register Indirect	1101	Reserved
0110	Status Test	1110	Reserved
0111	Reserved	1111	Reserved

Load Memory

Load Memory **0000b**

63	**62**	**61**													**32**
B2	B1	Data													
31		**28**	**27**											**1**	**0**
0000			Memory Address												W

Data — The data to be loaded in the memory address specified by Memory Address. The data format is either 32-bit DWords or 16-bit Words.

Memory Address — The Memory Address to write data to. Bits [3:0] are hardwired to “0” since all Memory Addresses should be 128-bit aligned.

W — When this bit is programmed to “0”, the 32-bit DWord data (bits [63:32]) is written to the Memory Address. When this bit is programmed to “1”, the 16-bit Word data (bits [47:32]) is written to the Memory Address.

B2, B1 — Bits [63:62] are the byte-enable signals for the Word data. They are active high.

Load Register

Load Register **0001b**

63															32
Data															
31		**28**	**27**										**2**	**1**	**0**
0001			Register Address											00	

Data The data to be loaded in the register specified by Register Address.

Register Address The register address (in the space `0x00000000` – `0x001FFFFF`) to write data to. Bits [0:1] are hardwired to “0” since all register addresses should be 32-bit aligned.

Load Memory Immediate

Load Memory Immediate **0010b**

63															32
DWORD Count															
31		**28**	**27**										**2**	**1**	**0**
0010			Memory Address											00	

DWORD Count The number of DWORDs to load into the memory.

Memory Address The starting memory address to write data to. Bits [1:0] are hardwired to “0”.

The data that must be loaded into the memory directly follows this command. Make sure the correct number of DWORDs (*DWORD Count*) is provided, otherwise unpredicted results will happen. Also, if an odd number of DWORDs is specified, the last DWORD should be padded with a dummy DWORD to align the next command to 64-bit again.

Load Register Immediate

Load Register Immediate **0011b**

63															32
DWORD Count															
31		**28**	**27**										**2**	**1**	**0**
0011			Register Address											00	

DWORD Count The number of DWORDs to load into the registers.

Register Address The starting register address (in the space `0x00000000` – `0x001FFFFF`) to write data to. Bits [0:1] are hardwired to “0” since all register addresses should be 32-bit aligned.

The data that must be loaded into the registers directly follows this command. Make sure the correct number of DWORDs (*DWORD Count*) is provided, otherwise unpredicted results will happen. Also, if an odd number of DWORDs is specified, the last DWORD should be padded with a dummy DWORD to align the next command to 64-bit again.

Load Memory Indirect

Load Memory Indirect **0100b**

127															96
95		92	91										66	65	64
			Source Memory Address											00	
63															32
DWORD Count															
31		28	27										2	1	0
0100			Memory Address											00	

Source Memory Address The starting memory address to read data from. Bits [65:64] are hardwired to “0”.

DWORD Count The number of DWORDs to copy into the memory.

Memory Address The starting memory address to write data to. Bits [1:0] are hardwired to “0”.

This command copies data from the memory location specified by *Source Memory Address* into the memory location specified by *Memory Address*. The *DWORD Count* specifies the number of DWORDs to copy. This command is most useful to copy texture, bitmap, or vertex data to off-screen memory for caching purposes.

Load Register Indirect

Load Register Indirect **0101b**

127															96
95		92	91										66	65	64
			Source Memory Address											00	
63															32
DWORD Count															
31		28	27										2	1	0
0101			Register Address											00	

Source Memory Address The starting memory address to read data from. Bits [65:64] are hardwired to “0”.

DWORD Count The number of DWORDs to copy into the registers.

Register Address The starting register address (in the space `0x00000000` – `0x001FFFFF`) to write data to. Bits [1:0] are hardwired to “0” since all register addresses should be 32-bit aligned.

This command copies data from the memory location specified by *Source Memory Address* into the register bank location specified by *Register Address*. The *DWORD Count* specifies the number of DWORDs to copy. This command is most useful to copy texture, bitmap, or vertex data to the engine FIFOs for processing.

Status Test

Status Test **0110b**

63						53	52																	32
							Bit Values																	
31		28	27			21	20	19	18	17	16	15	14	13	12	11	10					3	2	1	0
0110							2_M	C_F	2_C	D_M	C_S	V_F	V_S	P_S	S_C	S_P							2_S	2_F	2_E

2D Memory FIFO (2_M)	2D and Color Space Conversion memory FIFO (0 = not empty, 1 = empty).
Command FIFO (C_F)	Command FIFO on HIF bus (0 = not empty, 1 = empty).
Color Space Conversion (2_C)	Color Space Conversion busy bit.
Memory DMA Busy (D_M)	Memory DMA busy bit.
CRT Status Bit (C_S)	CRT Graphics Layer status bit.
Current Field (V_F)	Current Video Layer field for BOB (0 = odd, 1 = even).
Video Status Bit (V_S)	Video Layer status bit.
Panel Status Bit (P_S)	Panel Graphics Layer status bit.
CRT Sync (S_C)	Vertical Sync for CRT pipe (0 = not active, 1 = active).
Panel Sync (S_P)	Vertical Sync for Panel pipe (0 = not active, 1 = active).
2D Setup (2_S)	2D Setup Engine (0 = idle, 1 = busy).
2D FIFO (2_F)	2D and Color Space Conversion command FIFO (0 = not empty, 1 = empty).
2D Engine (2_E)	2D Drawing Engine (0 = idle, 1 = busy).

The Status Test command will wait until the requested status is met. The value of the Status Test register is masked with the internal hardware state and compared to the state in the *Bit Values*. If the result does not equal the *Bit Values*, the command list interpreter will wait until the hardware status changes. The pseudo code looks like this:

WHILE (Hardware State *& Mask* [20:0] != *Bit Values* [52:32] & Mask [20:0]) NOP;

Finish

Finish **1000b**

63															32
31		**28**	**27**											**1**	**0**
1000															I

Interrupt (I) — If the *Interrupt* bit is set, the FINISH command will generate an interrupt that can still be masked by the *Command List* mask bit in the Interrupt Mask register. When an interrupt is generated, the *Command List* bit in Interrupt Status register will be set to "1".

The FINISH command stops executing commands in the Command List and clears the *Start* bit ([31]) of the Command List Address register.

Goto

Goto **1001b**

63														**33**	**32**
															R
31		**28**	**27**									**3**	**2**		**0**
1001			Address											000	

Relative (R) — If the *Relative* bit is set, the specified *Address* is relative to the address of the current command (signed addition).

Address — The address of the new code to execute. Bits [2:0] are hardwired to "0" since all addresses need to be 64-bit aligned.

The GOTO command will jump to the Command List code located at the specified *Address*.

Gosub

Gosub **1010b**

63														**33**	**32**
															R
31		**28**	**27**									**3**	**2**		**0**
1010			Address											000	

Relative (R) — If the *Relative* bit is set, the specified *Address* is relative to the address of the current command (signed addition).

Address — The address of the new code to execute. Bits [2:0] are hardwired to "0" since all addresses need to be 64-bit aligned.

The GOSUB command will store the address of the next instruction it would execute in the Command List Return Address register and starts executing the Command List code located at the specified *Address*.

Return

Return **1011b**

63															32
31		28	27												0
1011															

The RETURN command will jump to the address specified in the Command List Return Address register. The RETURN command should terminate a subroutine that is being called by GOSUB.

Conditional Jump

Conditional Jump **1100b**

63															32
Condition															
31		28	27									3	2		0
1100			Address										000		

Condition — The Condition field consists of a 32-bit mask that will be applied to the Command List Condition Register. If the result of this mask is TRUE (any bit set), the condition shall return TRUE and the jump is taken by adding the signed value of Address to the address of the next command in the Command List.
The formula of the condition is:
RESULT = Condition • Command List Condition register

Address — A signed relative value that will be added to the address of the next command in the Command List if the result of the condition is TRUE. Bits [2:0] are hardwired to “0” since all addresses need to be 64-bit aligned.

7 GPIO

Functional Overview

GPIO Interface

The GPIO peripheral includes the following registers:

- Data register
- Data Direction register
- Interrupt Setup register
- Interrupt Status register
- Interrupt Reset register

Programmer's Model

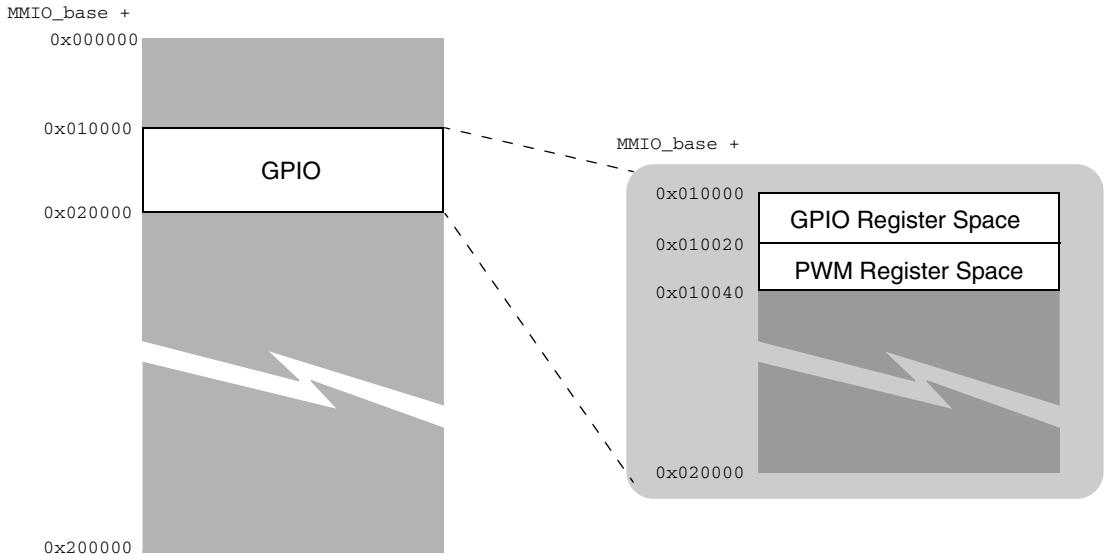
The base address of the GPIO is not fixed, and can be different for any particular system implementation. However, the offset of any particular register from the base address is fixed.

The following locations are reserved and must not be used during normal operation:

- Locations at offsets `0x424` to `0xFCC` are reserved for possible future extensions and test purposes
- Locations at offsets `+0xFDO` to `+0xFDC` are reserved for future ID expansion.

Figure 7-1 shows how this 64kB region in the MMIO space is laid out. It controls the GPIO registers.

Figure 7-1: GPIO Register Space



The following sections define each region in more detail.

Register Descriptions

The GPIO registers are shown in Table 7-1.

Table 7-1: GPIO Register Summary

Offset from MMIO_base[1]	Type	Width	Reset Value	Register Name
0x010000	R/W	32	0x00000000	GPIO Data Low
0x010004	R/W	32	0x00000000	GPIO Data High
0x010008	R/W	32	0x00000000	GPIO Data Direction Low
0x01000C	R/W	32	0x00000000	GPIO Data Direction High
0x010010	R/W	32	0x00000000	GPIO Interrupt Setup
0x010014	R	32	0x00000000	GPIO Interrupt Status
0x010014	W	32	0x00000000	GPIO Interrupt Reset

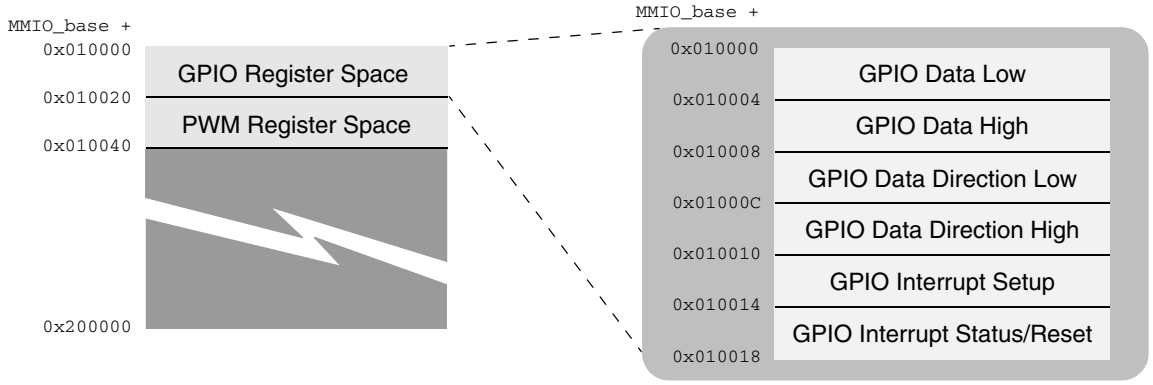
1. Refer to Table 1-5 on page 24 for MMIO_base values depending on the CPU.

GPIO Register Descriptions

The GPIO registers are described in this section.

The GPIO registers control the GPIO pins. There are seven GPIO registers, two of which share the same address for interrupt status/reset. Figure 7-2 defines the register layout for the GPIO registers.

Figure 7-2: GPIO Register Space



GPIO Data Low

Read/Write Address 0x010000

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Data_{31:16}$ R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$Data_{15:0}$ R/W															

Bit(s)	Name	Description
31:0	$Data_{31:0}$	The values in the $Data_{31:0}$ bits reflect the value on the $GPIO_{31:0}$ pins.

This register reflects the value on a GPIO pin. If it is programmed as an input, the value of the GPIO pin is transferred to the corresponding bit in this register. If it is programmed as an output, the value of the bit is transferred to the corresponding GPIO pin.

GPIO Data High

Read/Write Address 0x010004

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Data_{63:48}$ R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$Data_{47:32}$ R/W															

Bit(s)	Name	Description
31:0	$Data_{63:32}$	The values in the $Data_{63:32}$ bits reflect the value on the $GPIO_{63:32}$ pins.

This register reflects the value on a GPIO pin. If it is programmed as an input, the value of the GPIO pin is transferred to the corresponding bit in this register. If it is programmed as an output, the value of the bit is transferred to the corresponding GPIO pin.

GPIO Data Direction Low

Read/Write Address 0x010008

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Direction_{31:16}$ R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$Direction_{15:0}$ R/W															

Bit(s)	Name	Description
31:0	$Direction_{31:0}$	This register defines whether a GPIO pin is programmed as in input or as an output. 0: Input. 1: Output.

GPIO Data Direction High

Read/Write Address 0x01000C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Direction_{63:48}$ R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$Direction_{47:32}$ R/W															

Bit(s)	Name	Description
31:0	$Direction_{63:32}$	This register defines whether a GPIO pin is programmed as in input or as an output. 0: Input. 1: Output.

GPIO Interrupt Setup

Read/Write Address 0x010010

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									$Trigger_{54:48}$ R/W						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res	$Active_{54:48}$ R/W							Res	$Enable_{54:48}$ R/W						

Bit(s)	Name	Description
31:23	Reserved	These bits are reserved.
22:16	$Trigger_{54:48}$	Triggering Type. 0: Edge triggered. 1: Level triggered.
15	Res	This bit is reserved.
14:8	$Active_{54:48}$	Active State. 0: Active low or falling edge. 1: Active high or rising edge.
7	Res	This bit is reserved.
6:0	$Enable_{54:48}$	This register defines whether GPIO54:48 pins are programmed as regular input/output pins or as interrupt input pins. It also defines the interrupt type. 0: Regular GPIO Input/Output. 1: GPIO Interrupt.

GPIO Interrupt Status

Read Address 0x010014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									$Status_{54:48}$ R/W						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved															

Bit(s)	Name	Description
31:23	Reserved	These bits are reserved.
22:16	$Status_{54:48}$	This read/only register reflects the status of the interrupt pins. When an external interrupt happens on a GPIO interrupt pin, the status bit will be set to “1” until the software resets the interrupt by writing to the GPIO Interrupt Status. 0: Interrupt inactive. 1: Interrupt active.
15:0	Reserved	These bits are reserved.

GPIO Interrupt Reset

Write Address 0x010014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									$Reset_{54:48}$ W						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved															

Bit(s)	Name	Description
31:23	Reserved	These bits are reserved.
22:16	$Reset_{54:48}$	This field resets the GPIO interrupt. 0: No action. 1: Reset interrupt.
15:0	Reserved	These bits are reserved.

8 ZV Port

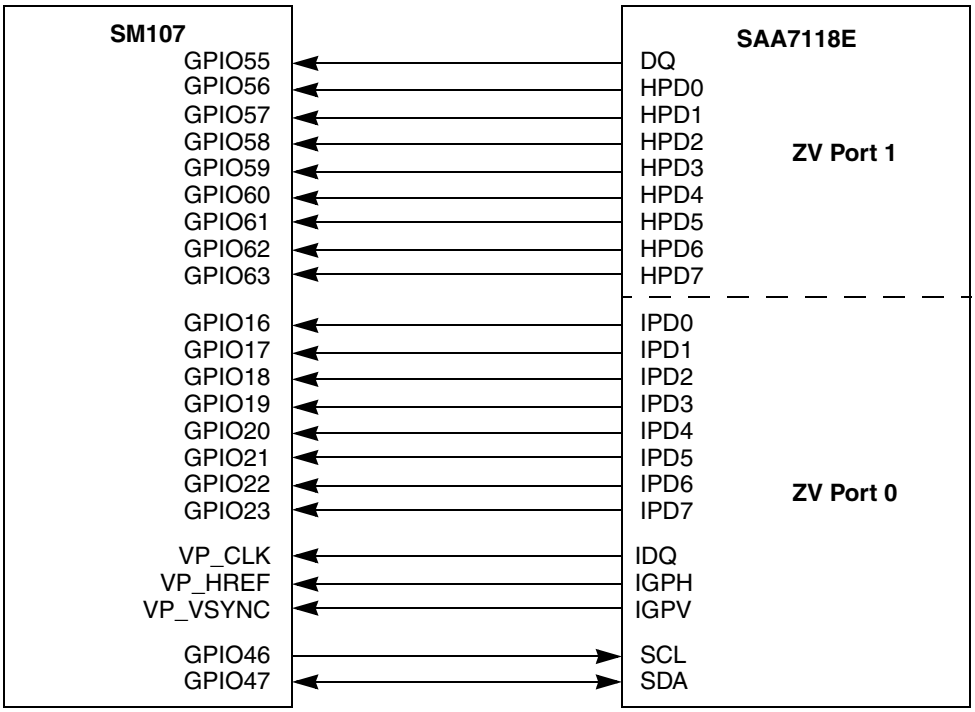
Functional Overview

This section covers the ZV Port and the Video Capture Unit.

ZV Port Overview

The SM107 Zoom Video Port (ZV Port) can interface with video decoders, such as NTSC/PAL decoders, MPEG-2 decoders, and JPEG codecs. The ZV Port also can interface directly to an NTSC/PAL decoder, such as the Philips SA7111 or BT819. Figure 8-1 illustrates an example of the interface between the Philips SA7118 TV decoder and the ZV Port.

Figure 8-1: TV Decoder Interface through the ZV Port



Incoming video data from the ZV Port can be interlaced or non-interlaced and YUV or RGB format. By disabling the video capture function, the ZV Port can be configured in output mode. In output mode, the ZV Port can send video data and 18-bit graphics in RGB format.

Video Capture Unit Overview

The Video Capture Unit captures incoming video data from the ZV Port and then stores the data into the frame buffer. The Video Capture Unit maintains display quality and balances the capture rate. Its key features are:

- 2-to-1 reduction for horizontal and vertical frame size
- YUV 4:2:2, YUV 4:2:2 with byte swapping, and RGB 5:6:5

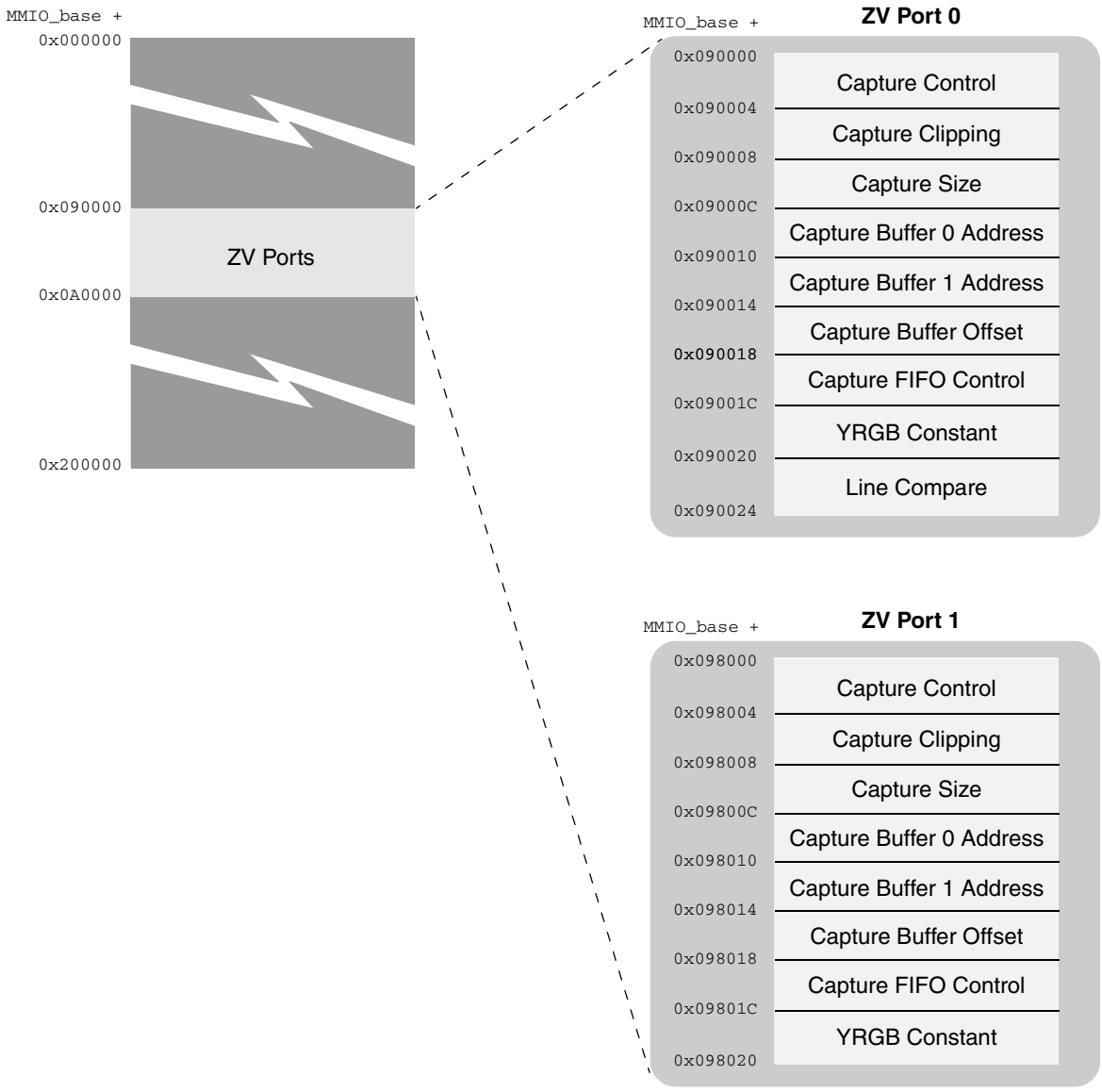
- Interlaced data and non-interlaced data capture
- Single buffer and double buffer capture
- Cropping

The SM107 uses the Video Processor block to display captured data on the display (LCD, TV, or CRT). The Video Window displays the captured data. The Video Processor does the stretching, color interpolation, YUV-to-RGB conversion, and color key functions.

Programmer's Model

Figure 8-2 shows how this 64kB region in the MMIO space is laid out. It controls the ZV Port capture registers.

Figure 8-2: ZV Port Register Space



Register Descriptions

ZV Port 0 Registers

The ZV Port 0 registers are shown in Table 8-1.

Table 8-1: ZV Port 0 Register Summary

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
0x090000	R/W	32	0b0000.XXXX.0000.0000. 0000.0000.0000.0000	Capture Control
0x090004	R/W	32	Undefined	Capture Clipping
0x090008	R/W	32	Undefined	Capture Size
0x09000C	R/W	32	Undefined	Capture Buffer 0 Address
0x090010	R/W	32	Undefined	Capture Buffer 1 Address
0x090014	R/W	32	Undefined	Capture Buffer Offset
0x090018	R/W	32	0x00000004	Capture FIFO Control
0x09001C	R/W	32	0x00EDEDED	YRGB Constant
0x090020	R/W	32	0x00000000	Line Compare

1. Refer to Table 1-5 on page 24 for MMIO_base values depending on the CPU.
2. In the reset values, “X” indicates don’t care.

Capture Control

Read/Write MMIO_base + 0x090000

Power-on Default 0b0000.XXXX.0000.0000.0000.0000.0000.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				F R	I R	CB R	VSS R	Reserved				ADJ R/W	HA R/W	VS R/W	HS R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FD R/W	VP R/W	HP R/W	CP R/W	UVS R/W	BS R/W	CS R/W	CF R/W	FS R/W	W R/W	B R/W	DB R/W	CC R/W	RGB R/W	656 R/W	E R/W

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	F	Field Input Status. This bit is read-only. o: Even field. 1: Odd field.
26	I	Interlace Status. This bit is read-only. 0: Non-interlaced. 1: Interlaced.
25	CB	Current Buffer Status. This bit is read-only. 0: Capturing data into buffer 0. 1: Capturing data into buffer 1.
24	VSS	Vertical Sync Status. This bit is read-only. 0: VSync pulse is inactive. 1: VSync pulse is active.
23:20	Reserved	These bits are reserved.
19	ADJ	Delay HREF. 0: Do not delay HREF. 1: Delay HREF by one clock.
18	HA	Enable Horizontal Averaging. 0: Disable. 1: Enable.
17	VS	Enable 2÷1 Vertical Shrink. 0: Disable. 1: Enable.
16	HS	Enable 2÷1 Horizontal Shrink. 0: Disable. 1: Enable.
15	FD	Field Detect Method. 0: Rising edge of VSync. 1: Falling edge of VSync.
14	VP	Select VSync Phase. 0: Active high. 1: Active low.
13	HP	Select HRef Phase. 0: Active high. 1: Active low.

Bit(s)	Name	Description
12	CP	Select Input Clock Polarity. 0: Active high. 1: Active low.
11	UVS	Enable UV Swap. 0: Disable. 1: Enable.
10	BS	Enable Byte Swap. 0: Disable. 1: Enable.
9	CS	Capture Size. 0: 16-bit. 1: 8-bit.
8	CF	Capture Format. 0: YUV. 1: RGB.
7	FS	Enable Field Swap. 0: Disable. 1: Enable.
6	W	Enable Interlaced Data Capturing in Weave. 0: Disable. 1: Enable.
5	B	Enable Interlaced Data Capturing in Bob. 0: Disable. 1: Enable.
4	DB	Enable Double Buffering. 0: Disable. 1: Enable.
3	CC	Select Capture Control. 0: Continuous capture. 1: Conditional capture by using the S bit.
2	RGB	Enable YUV to RGB Color Conversion. 0: Disable. 1:Enable.
1	656	Enable 8-bit ITU-656 Input. 0: Disable. 1: Enable.
0	E	Enable Capture. 0: Disable. 1: Enable.

Capture Clipping

Read/Write MMIO_base + 0x090004
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						YClip R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved						XClip R/W									

Bit(s)	Name	Description
31:26	Reserved	These bits are reserved.
25:16	YClip	Number of lines to skip after VSync.
15:10	Reserved	These bits are reserved.
9:0	XClip.	Number of pixels to skip after HRef.

Capture Size

Read/Write MMIO_base + 0x090008
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Height R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					Width R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Height	Number of lines to capture.
15:11	Reserved	These bits are reserved.
10:0	Width	Number of pixels to capture.

Capture Buffer 0 Address

Read/Write MMIO_base + 0x09000C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Memory Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Memory Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory.
25:4	Memory Address	Memory address of capture buffer 0 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer 1 Address

Read/Write MMIO_base + 0x090010

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Memory Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Memory Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory.
25:4	Memory Address	Memory address of capture buffer 1 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer Offset

Read/Write MMIO_base + 0x090014
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset R/W												0000			

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:4	Offset	Number of 128-bit aligned bytes per line of the capture buffer.
3:0	0000	These bits are hardwired to zeros.

Capture FIFO Control

Read/Write MMIO_base + 0x090018
Power-on Default 0x00000004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													FIFO R/W		

Bit(s)	Name	Description
31:3	Reserved	These bits are reserved.
2:0	FIFO	FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 000: 2 or more empty. 001: 3 or more empty. 010: 4 or more empty. 011: 5 or more empty. 100: 6 or more empty. 101: 8 or more empty. 110: 10 or more empty. 111: 12 or more empty.

YRGB Constant

Read/Write MMIO_base + 0x09001C

Power-on Default 0x00EDEDED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Adjustment.
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	Blue Conversion Constant.

Line Compare

Read/Write MMIO_base + 0x090020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					L-COMP R/W										

Bit(s)	Name	Description
31:11	Reserved	These bits are reserved.
10:0	L-COMP	Line Compare. The current line number is used to trigger the panel display.

ZV Port 1 Registers

The ZV Port 1 registers are shown in Table 8-2.

Table 8-2: ZV Port 1 Register Summary

Offset from MMIO_base[1]	Type	Width	Reset Value[2]	Register Name
0x098000	R/W	32	0b0000.XXXX.0000.0000. 0000.0000.0000.0000	Capture Control
0x098004	R/W	32	Undefined	Capture Clipping
0x098008	R/W	32	Undefined	Capture Size
0x09800C	R/W	32	Undefined	Capture Buffer 0 Address
0x098010	R/W	32	Undefined	Capture Buffer 1 Address
0x098014	R/W	32	Undefined	Capture Buffer Offset
0x098018	R/W	32	0x00000004	Capture FIFO Control
0x09801C	R/W	32	0x00EDEDED	YRGB Constant

1. Refer to Table 1-5 on page 24 for MMIO_base values depending on the CPU.
2. In the reset values, “X” indicates don’t care.

Capture Control

Read/Write MMIO_base + 0x098000

Power-on Default 0b0000.XXXX.0000.0000.0000.0000.0000.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				F R	I R	CB R	VSS R	Reserved			Panel R/W	ADJ R/W	HA R/W	VS R/W	HS R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FD R/W	VP R/W	HP R/W	CP R/W	UVS R/W	BS R/W	CS R/W	CF R/W	FS R/W	W R/W	B R/W	DB R/W	CC R/W	RGB R/W	656 R/W	E R/W

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	F	Field Input Status. This bit is read-only. o: Even field. 1: Odd field.

Bit(s)	Name	Description
26	I	Interlace Status. This bit is read-only. 0: Non-interlaced. 1: Interlaced.
25	CB	Current Buffer Status. This bit is read-only. 0: Capturing data into buffer 0. 1: Capturing data into buffer 1.
24	VSS	Vertical Sync Status. This bit is read-only. 0: VSync pulse is inactive. 1: VSync pulse is active.
23:21	Reserved	These bits are reserved.
20	Panel	Enable Capture Panel Output. 0: Disable. 1: Enable.
19	ADJ	Delay HREF. 0: Do not delay HREF. 1: Delay HREF by one clock.
18	HA	Enable Horizontal Averaging. 0: Disable. 1: Enable.
17	VS	Enable 2÷1 Vertical Shrink. 0: Disable. 1: Enable.
16	HS	Enable 2÷1 Horizontal Shrink. 0: Disable. 1: Enable.
15	FD	Field Detect Method. 0: Rising edge of VSync. 1: Falling edge of VSync.
14	VP	Select VSync Phase. 0: Active high. 1: Active low.
13	HP	Select HRef Phase. 0: Active high. 1: Active low.
12	CP	Select Input Clock Polarity. 0: Active high. 1: Active low.
11	UVS	Enable UV Swap. 0: Disable. 1: Enable.
10	BS	Enable Byte Swap. 0: Disable. 1: Enable.
9	CS	Capture Size. 0: 16-bit. 1: 8-bit.
8	CF	Capture Format. 0: YUV. 1: RGB.
7	FS	Enable Field Swap. 0: Disable. 1: Enable.

Bit(s)	Name	Description
6	W	Enable Interlaced Data Capturing in Weave. 0: Disable. 1: Enable.
5	B	Enable Interlaced Data Capturing in Bob. 0: Disable. 1: Enable.
4	DB	Enable Double Buffering. 0: Disable. 1: Enable.
3	CC	Select Capture Control. 0: Continuous capture. 1: Conditional capture by using the S bit.
2	RGB	Enable YUV to RGB Color Conversion. 0: Disable. 1:Enable.
1	656	Enable 8-bit ITU-656 Input. 0: Disable. 1: Enable.
0	E	Enable Capture. 0: Disable. 1: Enable.

Capture Clipping

Read/Write MMIO_base + 0x098004

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						YClip R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved						XClip R/W									

Bit(s)	Name	Description
31:26	Reserved	These bits are reserved.
25:16	YClip	Number of lines to skip after VSync.
15:10	Reserved	These bits are reserved.
9:0	XClip.	Number of pixels to skip after HRef.

Capture Size

Read/Write MMIO_base + 0x098008
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					Height R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					Width R/W										

Bit(s)	Name	Description
31:27	Reserved	These bits are reserved.
26:16	Height	Number of lines to capture.
15:11	Reserved	These bits are reserved.
10:0	Width	Number of pixels to capture.

Capture Buffer 0 Address

Read/Write MMIO_base + 0x09800C
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Memory Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Memory Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory.

Bit(s)	Name	Description
25:4	Memory Address	Memory address of capture buffer 0 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer 1 Address

Read/Write MMIO_base + 0x098010

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Reserved			Ext R/W	CS R/W	Memory Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Memory Address R/W												0 0 0 0			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory.
25:4	Memory Address	Memory address of capture buffer 1 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer Offset

Read/Write MMIO_base + 0x098014
Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Offset R/W												0000			

Bit(s)	Name	Description
31:16	Reserved	These bits are reserved.
15:4	Offset	Number of 128-bit aligned bytes per line of the capture buffer.
3:0	0000	These bits are hardwired to zeros.

Capture FIFO Control

Read/Write MMIO_base + 0x098018
Power-on Default 0x00000004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved													FIFO R/W		

Bit(s)	Name	Description
31:3	Reserved	These bits are reserved.
2:0	FIFO	FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 000: 2 or more empty. 001: 3 or more empty. 010: 4 or more empty. 011: 5 or more empty. 100: 6 or more empty. 101: 8 or more empty. 110: 10 or more empty. 111: 12 or more empty.

YRGB Constant

Read/Write MMIO_base + 0x09801C

Power-on Default 0x00EDEDED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G R/W								B R/W							

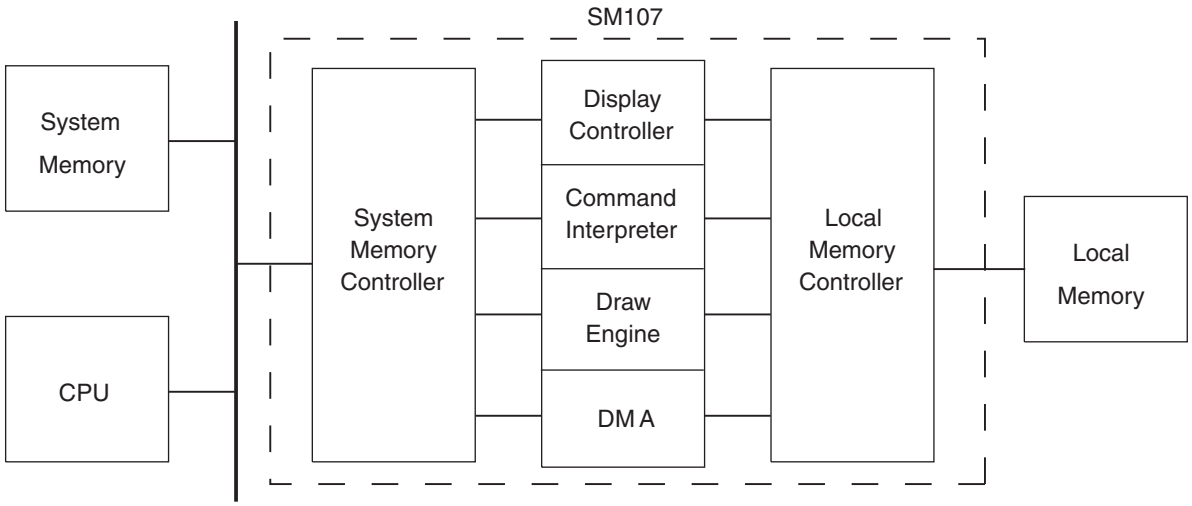
Bit(s)	Name	Description
31:24	Y	Y Adjustment.
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	Blue Conversion Constant.

9 DMA Controller (DMAC)

Functional Overview

In the SM107, the Display Controller, Command Interpreter, Draw Engine, and DMA can access system memory through the on-chip system memory controller (see Figure 9-1).

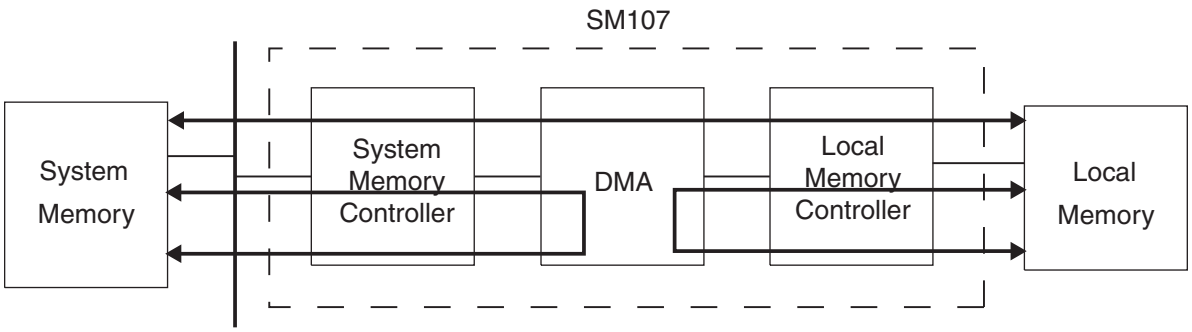
Figure 9-1: SM107 Functional Block Connections to Memory Controllers



The DMA channel within the SM107 handles memory data transfers, thus offloading the CPU. The DMA channel moves data between internal and system memory.

- DMA1—Moves data between system memory and local memory (see Figure 9-2)
  There are four ways to transfer data in DMA1:
  - System memory to system memory
  - System memory to local memory
  - Local memory to system memory
  - Local memory to local memory

Figure 9-2: DMA Channel 1



Register Descriptions

Figure 9-3 shows how this 64kB region in the MMIO space is laid out. It controls the DMA registers.

Figure 9-3: DMA Register Space

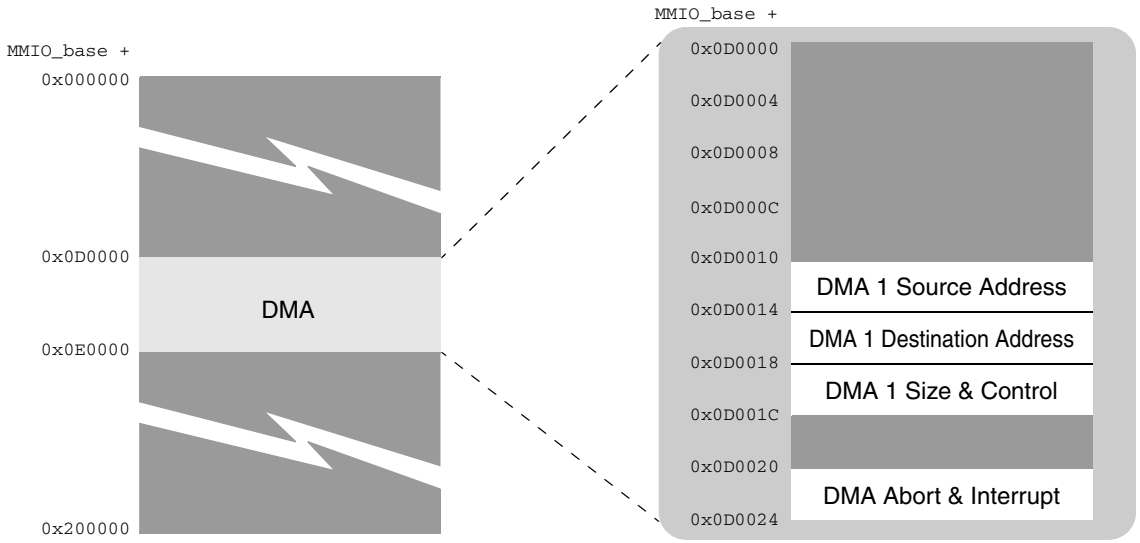


Table 9-1 shows the DMA Controller registers.

Table 9-1: DMA Controller Register Summary

Offset from MMIO_base[1]	Type	Width	Reset Value	Register Name
0x0D0010	R/W	32	0x00000000	DMA 1 Source Address
0x0D0014	R/W	32	0x00000000	DMA 1 Destination Address
0x0D0018	R/W	32	0x00000000	DMA 1 Size & Control
0x0D0020	R/W	32	0x00000000	DMA Abort & Interrupt

1. Refer to Table 1-5 on page 24 for MMIO_base values depending on the CPU.

DMA 1 Source Address

Read/Write MMIO_base + 0x0D0010

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Memory Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Memory Address R/W														0	0

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:2	Memory Address	Memory address with 32-bit alignment.
1:0	00	These bits are hardwired to zeros.

DMA 1 Destination Address

Read/Write MMIO_base + 0x0D0014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				Ext R/W	CS R/W	Memory Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Memory Address R/W														0	0

Bit(s)	Name	Description
31:28	Reserved	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.

Bit(s)	Name	Description
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:2	Memory Address	Memory address with 32-bit alignment.
1:0	00	These bits are hardwired to zeros.

DMA 1 Size & Control

Read/Write MMIO_base + 0x0D0018

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Act R/W	Reserved							Size R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Size R/W														0	0

Bit(s)	Name	Description
31	Act	DMA Channel 1 Activation. The *Act* bit will be cleared to “0” by the hardware when the DMA is finished. 0: Idle. 1: Activate DMA channel 1.
30:24	Reserved	These bits are reserved.
23:2	Size	Number of 32-bit aligned bytes to transfer (up to 16MB).
1:0	00	These bits are hardwired to zeros.

DMA Abort & Interrupt

Read/Write MMIO_base + 0x0D0020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved										$Abort_{1:0}$ R/W		Reserved		$Int_{1:0}$ R/W	

Bit(s)	Name	Description
31:6	Reserved	These bits are reserved.
5:4	$Abort_{1:0}$	Enable or Abort DMA Channel. Aborting will reset the corresponding DMA controller. For normal operation, the *Abort* bits should be set to “0”. 0: Enable corresponding DMA channel. 1: Abort corresponding DMA channel.
3:2	Reserved	These bits are reserved.
1:0	$Int_{1:0}$	Interrupt Status Bit. The *Int* bit should be cleared to “0” by software when the interrupt has been serviced. Writing a “1” has no effect. 0: DMA is not active or still busy – no interrupt. 1: DMA is finished – interrupt.

10 PWM Specification

Functional Overview

The Pulse Width Modulation (PWM) module is a simple counter that can pulse with programmable pulse widths. The pulse optionally can be tied to the PWM interrupt signal to generate a periodic interrupt for timing or watchdog support. The input clock is the peripheral clock at 96 MHz. The output pulse starts high.

The following subsections provide some different samples of PWM usage.

Delay Counter with Interrupt

Any of the three available PWM circuits can be programmed to perform a single shot delay. Once the delay is finished, an interrupt is triggered. The required delay is assumed to be 20 ms.

The values for the PWM *n* register are calculated as follows:

- Delay * clock = 20 ms * 96 MHz = 1,920,000
- A 50% duty cycle means 960,000 clocks are LOW and 960,000 clocks are HIGH
- The shift to a 12-bit value is done by dividing by 2^8: (3,750 – 1) clocks LOW and (3,750 – 1) clocks HIGH
- The value for the PWM *n* register is: `0xEA5EA585`

Internal Timer with Interrupt

Any of the three available PWM circuits can be programmed to act as a periodic timer to support a clock. The periodic timer generates an interrupt after each cycle. The required periodic interval is assumed to be 1 s. For this example, there is a 30/70% duty cycle.

The values for the PWM *n* register are calculated as follows:

- Delay * clock = 1 s * 96 MHz = 96,000,000
- A 30% duty cycle means 28,800,000 clocks are LOW and 67,200,000 clocks are HIGH
- The shift to a 12-bit value is done by dividing by 2^{15}: (879 – 1) clocks LOW and (2,051 – 1) clocks HIGH
- The value for the PWM *n* register is: `0x80236EF5`

External Pulse

In this example, the PWM is programmed for an external pulse with a frequency of 44.1 kHz and a duty cycle of 15%.

The values for the PWM *n* register are calculated as follows:

- Delay * clock = (1 / 44.1 kHz) * 96 MHz = 2,177
- A 15% duty cycle means (327 – 1) clocks are LOW and (1,850 – 1) clocks are HIGH
- The value for the PWM *n* register is: `0x73914601`

Register Descriptions

The PWM registers are shown in Table 10-1.

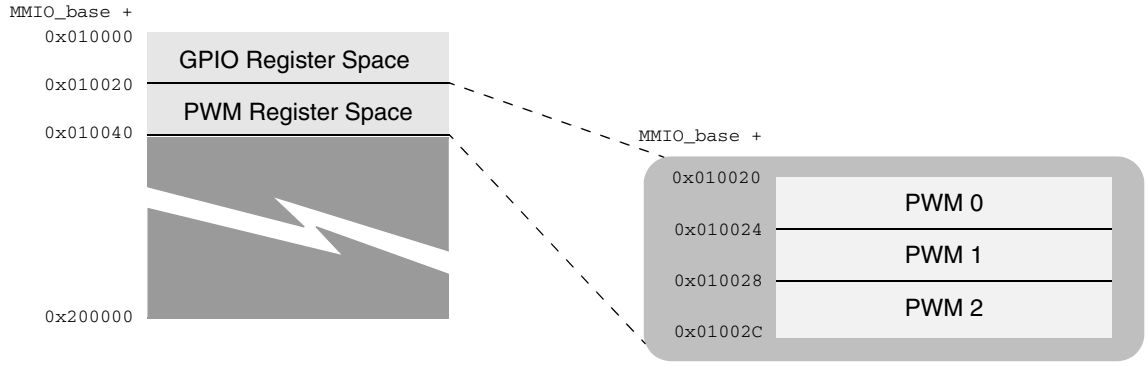
Table 10-1: PWM Register Summary

Offset from MMIO_base[1]	Type	Width	Reset Value	Register Name
0x010020	R/W	32	0x00000000	PWM 0
0x010024	R/W	32	0x00000000	PWM 1
0x010028	R/W	32	0x00000000	PWM 2

1. Refer to Table 1-5 on page 24 for MMIO_base values depending on the CPU.

The PWM registers control the three PWM pins. It contains three registers, one for each PWM pin. Figure 10-1 defines the register layout for the PWM registers.

Figure 10-1: PWM Register Space



PWM 0

Read/Write Address 0x010020
Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
High Counter R/W												Low Counter R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Low Counter R/W								Clock Divide R/W				IP R/W	I R/W	Res	E R/W

Bit(s)	Name	Description
31:20	High Counter	Number of clocks - 1 the PWM should remain high before switching to low.
19:8	Low Counter	Number of clocks - 1 the PWM should remain low before switching to high.
7:4	Clock Divide	Select divisor for 96MHz input clock.
3	IP	PWM Interrupt Pending. In order to clear a pending interrupt, write a “1” in the IP bit. 0: No interrupt pending. 1: Interrupt pending.
2	I	Enable or Disable PWM Interrupt. 0: Disable PWM interrupt. 1: Enable PWM interrupt whenever a single cycle is completed.
1	Res	This bit is reserved.
0	E	Enable or Disable the PWM. 0: Disabled. 1: Enabled.

0000	÷ 1	96MHz	1000	÷ 256	375kHz
0001	÷ 2	48MHz	1001	÷ 512	187.5kHz
0010	÷ 4	24MHz	1010	÷ 1,024	93.75kHz
0011	÷ 8	12MHz	1011	÷ 2,048	46.875kHz
0100	÷ 16	6MHz	1100	÷ 4,096	23.438kHz
0101	÷ 32	3MHz	1101	÷ 8,192	11.719kHz
0110	÷ 64	1.5MHz	1110	÷ 16,384	5.859kHz
0111	÷ 128	750kHz	1111	÷ 32,768	2.93kHz

PWM 1

Read/Write Address 0x010024

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
High Counter R/W												Low Counter R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Low Counter R/W								Clock Divide R/W				IP	I	Res	E

Bit(s)	Name	Description
31:20	High Counter	Number of clocks - 1 the PWM should remain high before switching to low.
19:8	Low Counter	Number of clocks - 1 the PWM should remain low before switching to high.
7:4	Clock Divide	Select divisor for 96MHz input clock.
3	IP	PWM Interrupt Pending. In order to clear a pending interrupt, write a “1” in the IP bit. 0: No interrupt pending. 1: Interrupt pending.
2	I	Enable or Disable PWM Interrupt. 0: Disable PWM interrupt. 1: Enable PWM interrupt whenever a single cycle is completed.
1	Res	This bit is reserved.
0	E	Enable or Disable the PWM. 0: Disabled. 1: Enabled.

0000	÷ 1	96MHz	1000	÷ 256	375kHz
0001	÷ 2	48MHz	1001	÷ 512	187.5kHz
0010	÷ 4	24MHz	1010	÷ 1,024	93.75kHz
0011	÷ 8	12MHz	1011	÷ 2,048	46.875kHz
0100	÷ 16	6MHz	1100	÷ 4,096	23.438kHz
0101	÷ 32	3MHz	1101	÷ 8,192	11.719kHz
0110	÷ 64	1.5MHz	1110	÷ 16,384	5.859kHz
0111	÷ 128	750kHz	1111	÷ 32,768	2.93kHz

PWM 2

Read/Write Address 0x010028
Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
High Counter R/W												Low Counter R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Low Counter R/W								Clock Divide R/W				IP R/W	I R/W	Res	E R/W

Bit(s)	Name	Description
31:20	High Counter	Number of clocks - 1 the PWM should remain high before switching to low.
19:8	Low Counter	Number of clocks - 1 the PWM should remain low before switching to high.
7:4	Clock Divide	Select divisor for 96MHz input clock.
3	IP	PWM Interrupt Pending. In order to clear a pending interrupt, write a “1” in the IP bit. 0: No interrupt pending. 1: Interrupt pending.
2	I	Enable or Disable PWM Interrupt. 0: Disable PWM interrupt. 1: Enable PWM interrupt whenever a single cycle is completed.
1	Res	This bit is reserved.
0	E	Enable or Disable the PWM. 0: Disabled. 1: Enabled.

0000	÷ 1	96MHz	1000	÷ 256	375kHz
0001	÷ 2	48MHz	1001	÷ 512	187.5kHz
0010	÷ 4	24MHz	1010	÷ 1,024	93.75kHz
0011	÷ 8	12MHz	1011	÷ 2,048	46.875kHz
0100	÷ 16	6MHz	1100	÷ 4,096	23.438kHz
0101	÷ 32	3MHz	1101	÷ 8,192	11.719kHz
0110	÷ 64	1.5MHz	1110	÷ 16,384	5.859kHz
0111	÷ 128	750kHz	1111	÷ 32,768	2.93kHz

11 Pin & Packaging Information

Signal List

Table 11-1 summarizes the pins for the SM107 chip.

Table 11-1: Signal Summary for the SM107

Signal Category	Number of Pins	Signal Name
GPIO Related Signals (39)		
GPIO	19	GPIO / Interrupt
Zoom Video	8	ZV[7:0]
PWM	3	PWM[0:2]
Digital CRT / Zoom Video / FP	9	Digital CRT[7:0], CLK / ZV[15:8] / FP[17:16, 9:8, 1:0]
Panel (25)		
	18	FP[23:18], FP[15:10], FP[7:2]
	7	FP_HSYNC, FP_VSYNC, M/DE, FPCLK, FPEN, VDEN, BIAS, FP_DISP
CPU Interface (75)		
Address	24	CA[25:2]
Data	32	CD[31:0]
Control	19	RST#, INTR, HCS#, BS#, HRDY#, HCLK, HCKE, BREQ#, ACK#, MCS#[1:0], HWE#, HRAS#, HCAS#, BE[3:0], CPURD#
CRT Interface (6)		
CRT Output	6	R, G, B, CRT_HSYNC, CRT_VSYNC, IREF
ZV Port Interface (3)		
Zoom Video	3	VP_VSYNC, VP_HREF, VP_CLK
Clock and Test Signals (8)		
Clocks + Signals	6	XTALIN, XTALOUT, Power, GND, CLKOFF, TESTCLK
Test	2	TEST[1:0]

Table 11-1: Signal Summary for the SM107

Signal Category	Number of Pins	Signal Name
Miscellaneous (1)		
No Connection	1	MVREF
Subtotal (157)		
Power & Ground (51)		
Power & GND	51	
Grand Total (208)		

Pinout

Figure 11-1 shows the pinout for the SM107 chip.

Figure 11-1:SM107 Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	CD5	CD8	CD10	CD12	CD14	CA21 (DEVSEL#)	CA24 (IRDY#)	CA19 (BE2#)	CD19	CD21	CD23	CD25	CD27	CD29	CD31	BREQ #	HCLK
B	CD3	CD7	CD9	CD13	CD15	CA18 (BE1#)	CA23 (TRDY#)	CA25 (FRAME#)	CD17	CD20	CD22	CA20 (BE3#)	CD26	CD30	ACK#	RST#	BE3
C	CD1	CD6	CA17 (BE0#)	CD11	GND	CA16 (PAR)	CA22 (STOP#)	GND	CD16	CD18	CA15 (IDSEL)	GND	CD24	CD28	INTR	BE2	HCKE
D	CD2	CD4	CA10	MVDD2	MVDD	HVDD	GND	VDD	HVDD	GND	VDD	HVDD	VDD	HVDD	BE0	BE1	CPURD #
E	CA5	CD0	CA14 (CLKRUN#)	GND										GND	MCS0 #	MCS1 #	BS#
F	CA4	CA9	CA13	MVDD										XTAL PWR	HCS#	HRDY #	HCAS #
G	CA3	CA8	GND	MVDD2										GVDD	GND	HRAS #	HWE #
H	CA2	CA7	CA12	MVDD					208					VDD	CLK OFF	TEST CLK	XTAL IN
J	FP2	CA6	CA11	GND					Pins					GND	GPIO 0	PLL GND	XTAL OUT
K	FP5	FP4	FP3	MVDD2										GVDD	GPIO 1	GPIO 2	PLL PWR
L	FP7	FP6	GND	MVDD										VDD	GND	GPIO 3	GPIO 4
M	FP12	FP11	FP10	MVDD2										GVDD	GPIO 5	GPIO 6	GPIO 7
N	FP15	FP14	FP13	GND										GND	GPIO 8	GPIO 9	GPIO 10
P	FP19	FP18	GND	MVDD	PVDD	VDD	GND	PVDD	VDD	PVDD	GND	AVDD	AVSS	VDD	GPIO 11	GPIO 12	GPIO 13
R	FP21	FP20	FPEN	VDEN	BIAS	GND	TEST0	GPIO 62	GND	GPIO 59	GPIO 56	GPIO 54	GPIO 30	GND	GPIO 14	GPIO 15	GPIO 16
T	FP22	FP_ HSYNC	FP_ VSYNC	FP_ DISP	CRT_ HSYNC	CRT_ VSYNC	TEST1	GPIO 63	GPIO 61	GPIO 60	GPIO 57	GPIO 55	GPIO 31	GPIO 23	GPIO 20	GPIO 17	GPIO 18
U	FP23	FPCLK	IREF	B	G	R	NC	VP_ VSYNC	VP_ HREF	VP_ CLK	GPIO 58	GPIO 47	GPIO 46	GPIO 29	GPIO 22	GPIO 21	GPIO 19

Pin Descriptions

Each BGA ball of the MMCC is one of the following types:

- I: Input signal
- O: Output signal
- I/O: Input or Output signal

All outputs and I/O signals are 3-stated. Internal pull-ups for I/O pads are all 100KΩ resistors. Internal pull-downs for I/O pads are all 100KΩ resistors.

Table 11-2: Pin Descriptions

Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
Host/PCI Interface (75)					
ACK#	B15	I	CMOS 3.3V		CPU Bus Acknowledge / PCI Bus Grant.
BE[3:0]	B17, C16, D16, D15	I/O	CMOS 3.3V	8	CPU Byte Enable / SDRAM Data Mask.
BREQ#	A16	O	CMOS 3.3V	8, 12, 24	CPU Bus Request / PCI Bus Request.
BS#	E17	I	CMOS 3.3V		SH4 Cycle Start / XScale or NEC CPU Write Enable.
CA[11:2]	J3, D3, F2, G2, H2, J2, E1, F1, G1, H1	I/O	CMOS 3.3V	8	CPU Address [11:2] / SDRAM MA.
CA[13:12]	F3, H3	I/O	CMOS 3.3V	8	CPU Address [13:12] / SDRAM BA / SDRAM MA.
CA[20:17]	B12, A8, B6, C3	I/O	CMOS 3.3V	8, 12, 24	CPU Address [20:17] / PCI C/BE#[3:0] / SDRAM MA.
CA14	E3	I/O	CMOS 3.3V	8	CPU Address 14 / PCI CLKRUN# / SDRAM BA / SDRAM MA.
CA15	C11	I/O	CMOS 3.3V	8, 12, 24	CPU Address 15 / PCI IDSEL / SDRAM BA / SDRAM MA.
CA16	C6	I/O	CMOS 3.3V	8, 12, 24	CPU Address 16 / PCI PAR / SDRAM BA / SDRAM MA.
CA21	A6	I/O	CMOS 3.3V	8, 12, 24	CPU Address 21 / PCI DEVSEL# / SDRAM MA.
CA22	C7	I/O	CMOS 3.3V	8, 12, 24	CPU Address 22 / PCI STOP# / SDRAM BA / SDRAM MA.
CA23	B7	I/O	CMOS 3.3V	8, 12, 24	CPU Address 23 / PCI TRDY# / SDRAM BA / SDRAM MA.
CA24	A7	I/O	CMOS 3.3V	8, 12, 24	CPU Address 24 / PCI IRDY# / SDRAM BA.

Table 11-2: Pin Descriptions (Continued)

Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
CA25	B8	I/O	CMOS 3.3V	8, 12, 24	CPU Address 25 / PCI FRAME#.
CD[31:0]	A1, A2, A3, A4, A5, A9, A10, A11, A12, A13, A14, A15, B1, B2, B3, B4, B5, B9, B10, B11, B13, B14, C1, C2, C4, C9, C10, C13, C14, D1, D2, E2	I/O	CMOS 3.3V	8, 12, 24	CPU Data Bus / PCI AD Bus / SDRAM Data Bus.
CPURD#	D17	I/O	CMOS 3.3V		XScale or NEC Read Enable.
HCAS#	F17	O	CMOS 3.3V	8	SDRAM Column Address select.
HCKE	C17	I/O	CMOS 3.3V	8	SDRAM Clock Enable.
HCLK	A17	I/O	CMOS 3.3V	8, 12, 24	CPU clock / PCI clock.
HCS#	F15	I	CMOS 3.3V		SM107 chip select. This signal has a weak internal pull-up.
HRAS#	G16	O	CMOS 3.3V	8	SDRAM Row Address select.
HRDY#	F16	O	CMOS 3.3V	8	CPU Ready. This signal must be externally pulled-up for SH4. For all other CPUs, this signal must be pulled up.
HWE#	G17	I/O	CMOS 3.3V	8	SH4 Write Enable / SDRAM Write Enable.
INTR	C15	O	CMOS 3.3V	8, 12, 24	CPU Interrupt / PCI Interrupt.
MCS#[1:0]	E16, E15	O	CMOS 3.3V	8	SDRAM Chip Select.
RST#	B16	I	CMOS 3.3V		SM107 reset.
Power Down Interface (1)					
CLKOFF	H15	I	CMOS 3.3V		Used to shut off host interface clock. This signal has a weak internal pull-down.
Clock Interface (5)					
PLLGND	J16	I			PLL ground.
PLLPWR	K17	I	1.8 V		PLL power.

Table 11-2: Pin Descriptions (Continued)

Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
TESTCLK	H16	I	CMOS 3.3V		For testing purposes.
XTALIN	H17	I	CMOS 3.3V		12/24MHz crystal input connection.
XTALOUT	J17	O	CMOS 3.3V		12/24MHz crystal output connection.
Test Interface (2)					
TEST[1:0]	T7, R7	I	CMOS 3.3V		Test mode selection. Both signals have a weak internal pull-down.
Flat Panel Interface (25)					
BIAS	R5	O	CMOS 3.3V	4	Flat panel voltage bias enable.
FP[23:18], FP[15:10], FP[7:2]	J1, K1, K2, K3, L1, L2, M1, M2, M3, N1, N2, N3, P1, P2, R1, R2, T1, U1	O	CMOS 3.3V	4	Flat panel data bus {23:18,15:10,7:2}.
FP_DISP	T4	O	CMOS 3.3V	4	Flat panel display enable.
FP_HSYNC	T2	O	CMOS 3.3V	4	Flat panel TFT horizontal sync / STN line pulse.
FP_VSYNC	T3	O	CMOS 3.3V	4	Flat panel TFT vertical sync / STN frame pulse.
FPCLK	U2	O	CMOS 3.3V	4	Flat panel pixel clock.
FPEN	R3	O	CMOS 3.3V	4	Flat panel enable.
VDEN	R4	O	CMOS 3.3V	4	Flat panel VDD enable.
CRT Interface (6)					
B	U4	O	Analog		CRT blue output.
CRT_HSYNC	T5	O	CMOS 3.3V	4	CRT vertical sync.
CRT_VSYNC	T6	O	CMOS 3.3V	4	CRT horizontal sync.
G	U5	O	Analog		CRT green output.
IREF	U3	I	Analog		CRT IREF input.
R	U6	O	Analog		CRT red output.

Table 11-2: Pin Descriptions (Continued)

Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
Video Port Interface (3)					
VP_CLK	U10	I	CMOS 3.3V		Video port clock.
VP_HREF	U9	I	CMOS 3.3V		Video port horizontal reference.
VP_VSYNC	U8	I	CMOS 3.3V		Video port vertical sync.
GPIO Interface (39) — All 39 GPIO pins have weak, internal pull-down resistors					
GPIO[7:0]	J15, K15, K16, L16, L17, M15, M16, M17	I/O	CMOS 3.3V	4	GPIO[7:0]. Note that these signals also function as strap pins. Refer to Table 1-4 on page 1-19 for more information.
GPIO8	N15	I/O	CMOS 3.3V	4	GPIO8.
GPIO9	N16	I/O	CMOS 3.3V	4	GPIO9.
GPIO10	N17	I/O	CMOS 3.3V	4	GPIO10.
GPIO11	P15	I/O	CMOS 3.3V	4	GPIO11.
GPIO[15:12]	P16, P17, R15, R16	I/O	CMOS 3.3V	4	GPIO[15:12]. Note that these signals also function as strap pins. Refer to Table 1-4 on page 1-19 for more information.
GPIO[23:16]	R17, T16, T17, U17, T15, U16, U15, T14	I/O	CMOS 3.3V	4	GPIO[23:16] / Video Port D[7:0] / Test Bus [7:0].
GPIO29	U14	I/O	CMOS 3.3V	4	GPIO29 / PWM 0 output / Test Bus [8]. This signal also functions as a strap pin (refer to Table 1-4 on page 1-19).
GPIO30	R13	I/O	CMOS 3.3V	4	Output: GPIO30 / PWM 1 output / Test Bus [9]. Input: GPIO30 / XScale input clock.
GPIO31	T13	I/O	CMOS 3.3V	4	GPIO31 / PWM 2 output / Test Bus [10]. This signal also functions as a strap pin (refer to Table 1-4 on page 1-19).
GPIO46	U13	I/O	CMOS 3.3V	4	GPIO46
GPIO47	U12	I/O	CMOS 3.3V	4	GPIO47
GPIO[63:54]	R8, R10, R11, R12, T8, T9, T10, T11, T12, U11	I/O	CMOS 3.3V	4	GPIO[63:54] / Digital CRT Data [7:0] / Test Bus [19:12] / Video Port Data [15:8] / FPDATA [17:16,9:8,1:0] in lower 6 bits / Embedded Memory Test [7:0].

Table 11-2: Pin Descriptions (Continued)

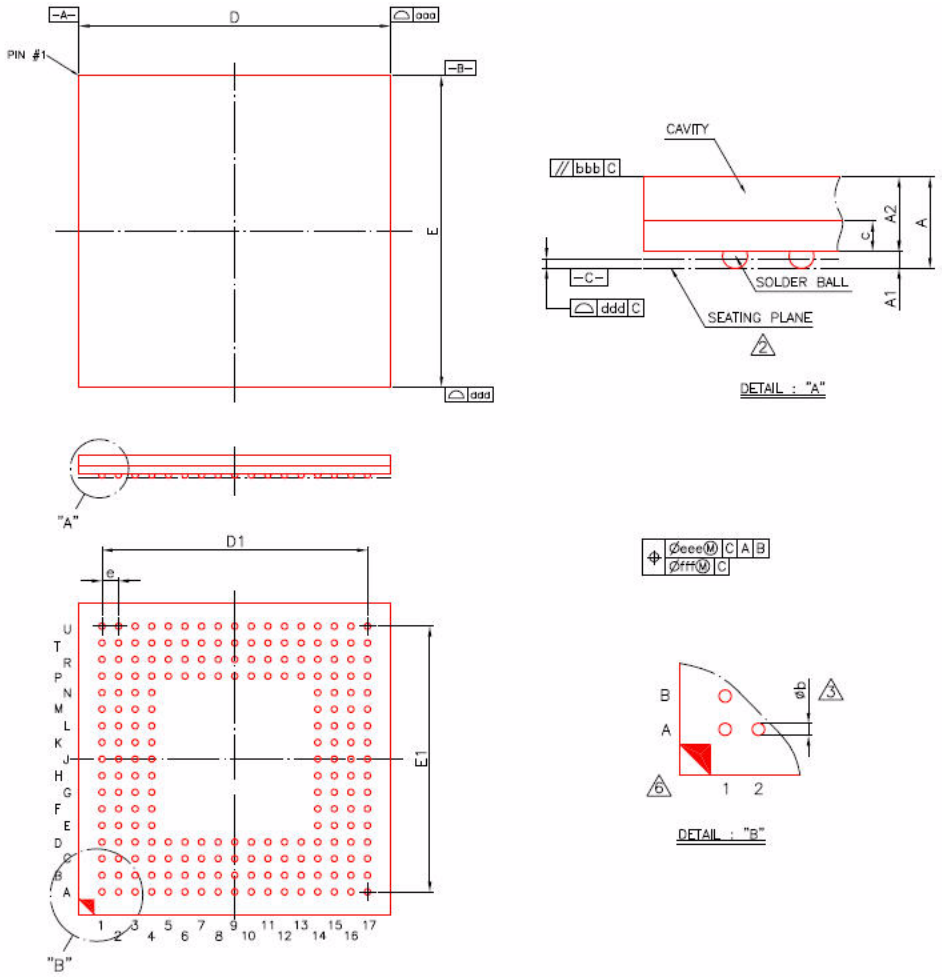
Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
Power and Ground (51)					
AVDD	P12	I	3.3V		DAC
AVSS	P13	I	0 V		DAC Ground
GND	C5, C8, C12, D7, D10, E4, E14, G3, G15, J4, J14, L13, L15, N4, N14, P3, P7, P11, R6, R9, R14	I	0 V		Core Ground
GVDD	G14, K14, M14	I	3.3V		GPIO
HVDD	D6, D9, D12, D14	I	3.3V		Host/PCI I/O
MVDD	D5, F4, L4, P4, H4	I	2.5V/3.3V		SDRAM Core
MVDD2	D4, G4, M4, K4	I	CMOS 3.3V or 2.5V		SDRAM or DDR
PVDD	P5, P8, P10	I	3.3V		LCD Panel I/O
VDD	D8, D11, D13, H14, L14, P14, P9, P5	I	1.8 V		Core
XTALPWR	F14	I	3.3 V		Crystal

Note: All output pins can be 3-stated.

Packaging

The SM107 is available in a 208-pin BGA package (see Figure 11-2). The total package size is 15mm x 15mm.

Figure 11-2:SM107 Package Outline



Symbol	Dimensions in mm			Dimensions in inches		
	Min	Nom	Max	Min	Nom	Max
A	–	–	1.20	–	–	0.047
A1	0.16	0.24	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	–	12.80	–	–	0.504	–
E1	–	12.80	–	–	0.504	–
e	–	0.80	–	–	0.031	–
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.12			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	17/17			17/17		

Note:

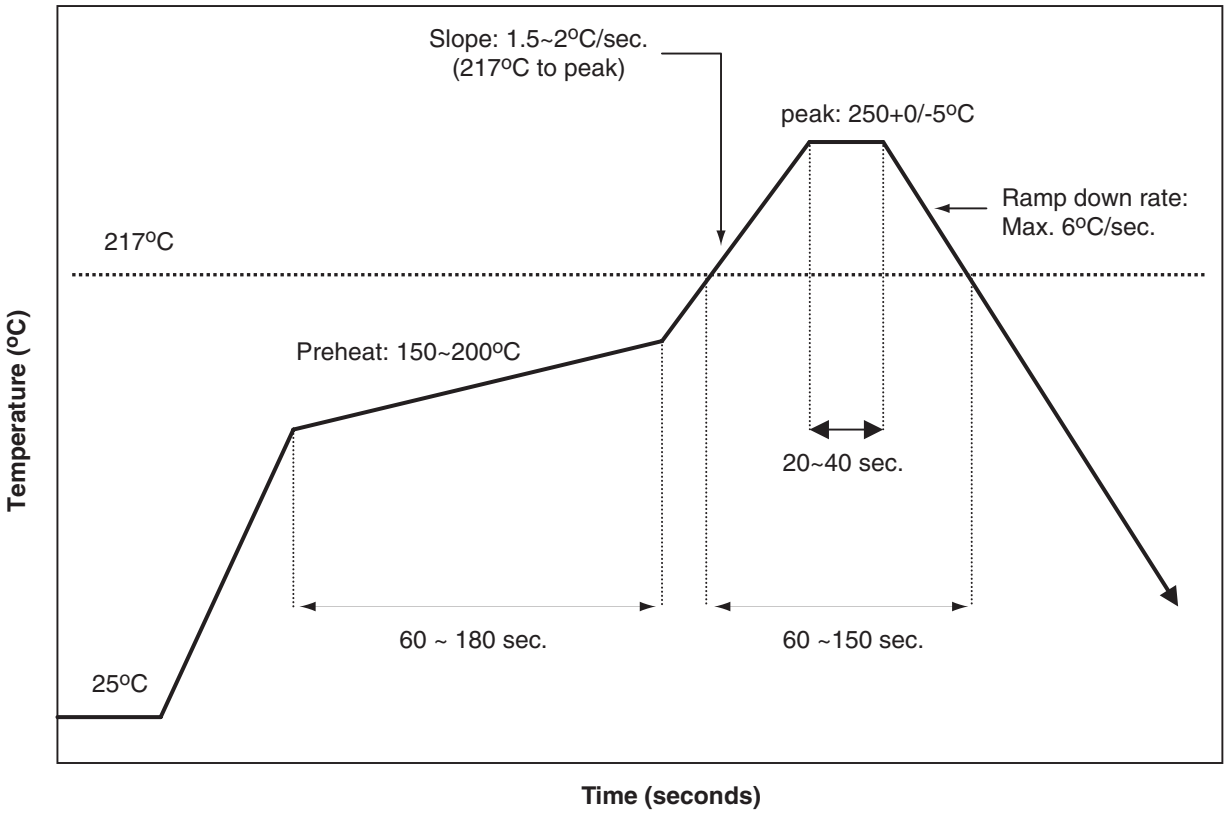
1. Controlling dimension: millimeter.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. There shall be a minimum clearance of 0.25mm between the edge of the solder ball and the body edge.
5. Reference document: JEDEC MO-205.
6. The pattern of pin 1 Fiducial is for reference only.

12 Specifications

Soldering Profile

Figure 12-1 shows the soldering profile for the SM107 device. This profile is designed for use with Sn63 or Sn62 (tin measurements in the PCB) and can serve as a general guideline in establishing a reflow profile.

Figure 12-1: Temperature Profile



The reflow profile is defined as follows:

- Average ramp-up rate (217°C to peak): 1.5~2°C/second
- Preheat (150~200°C): 60~180 seconds
- Temperature maintained above 217°C: 60~150 seconds
- Time within 5°C of actual peak temperature: 20 ~ 40 seconds
- Peak temperature: 250+0/-5°C
- Ramp-down rate: 6°C/second max.
- Time 25°C to peak temperature: 8 minutes max.
- Cycle interval: 5 minutes

DC Characteristics

Table 12-1: Absolute Maximum Ratings

Parameter	Maximum Rating	Units
Ambient Temperature	0 to 75	degrees C
Storage Temperature	-40 to 125	degrees C
VDD I/O[1] with respect to VSS	3.3 +/- 5%	V
VDD core with respect to VSS	1.8 +/- 5%	V
ESD Rating (human body), all signal pins	>2000	V
ESD Rating (human body), all VDD pins (AVDD, PVDD, VDD)	>1500	V
Voltage on I/O pins with respect to VSS	-0.5V to VDD + 5%	V

1. VDD I/O refers to AVDD, GVDD, HVDD, MVDD, MVDD2, PVDD, XTALPWR.

Table 12-2: DC Characteristics

Symbol	Parameter	Min	Max	Units
V_{IL}	Input Low Voltage	-0.3	0.8	V
V_{IH}	Input High Voltage	2.4	5.5	V
V_{OL}	Output Low Voltage	-	0.4	V
V_{OH}	Output High Voltage	2.8	VDD + 0.5	V
I_{OZL}	Output 3-State Current	-	10	µA
I_{OZH}	Output 3-State Current	-	10	µA
I_{OZL} (pull up pins)	Output 3-State Current	-130	-10	µA
I_{OZH} (pull up pins)	Output 3-State Current	-	10	µA
I_{OZL} (pull down pins)	Output 3-State Current	-	10	µA
I_{OZH} (pull down pins)	Output 3-State Current	10	130	µA
C_{IN}	Input Capacitance	-	7	pF
C_{OUT}	Output Capacitance	-	7	pF

AC Timing

This section provides the AC timing waveforms and parameters:

PCI Interface Timing

Figure 12-2 shows the PCI clock and its timing parameters. Table 12-3 provides the values for the PCI clock timing parameters shown in Figure 12-2.

Figure 12-2: PCI Clock Timing

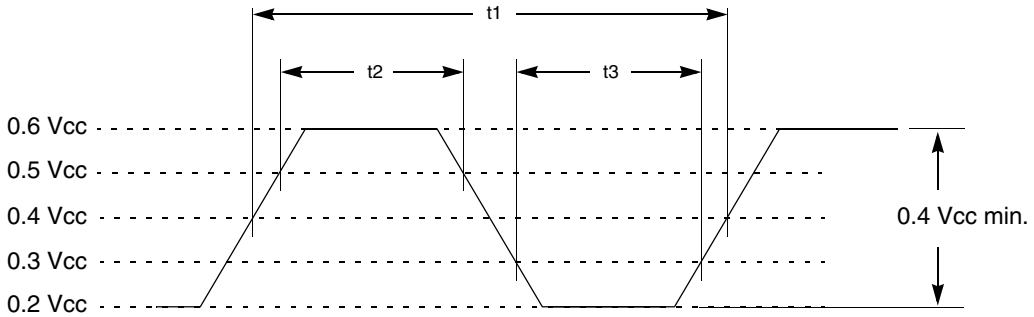


Table 12-3: PCI Clock Timing Parameters

Sym	Parameter	66 MHz		33 MHz		Unit
		Min	Max	Min	Max	
t1	CLK cycle time	15	30	30		ns
t2	CLK high time	6		11		ns
t3	CLK low time	6		11		ns
–	CLK skew rate	1.5	4	1	4	V/ns

Figure 12-3 and Figure 12-4 show the PCI outputs and inputs, respectively, and their relationship to the PCI clock. Table 12-4 provides the values for the timing parameters shown in the two figures.

Figure 12-3: PCI Clock to Output Timing

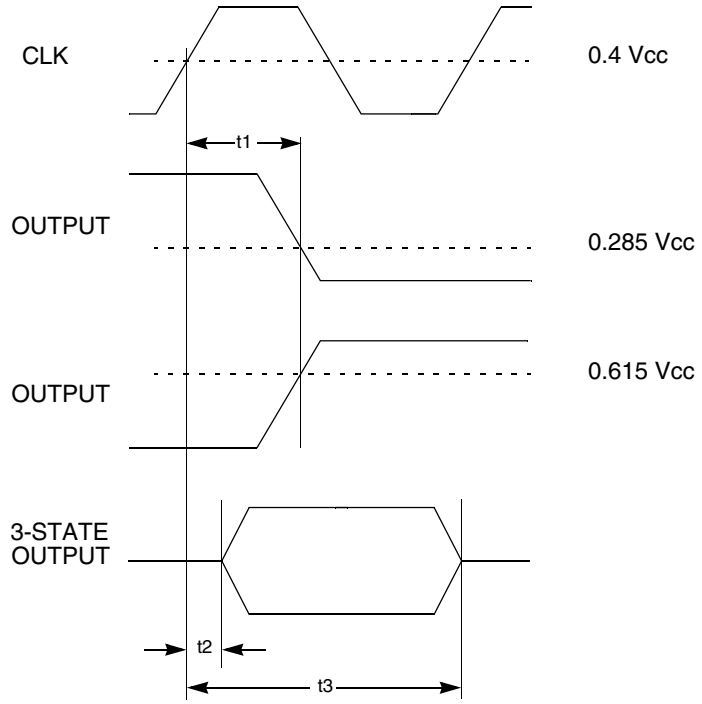


Figure 12-4: PCI Clock to Input Timing

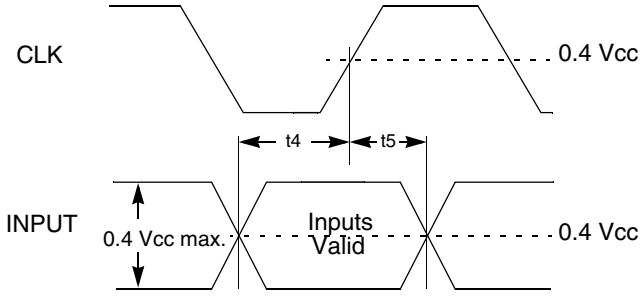


Table 12-4: PCI I/O Timing Parameters

Sym	Parameter	66 MHz		33 MHz		Unit
		Min	Max	Min	Max	
t1	CLK to signal valid delay	2	6	2	11(12)[1]	ns
t2	Float to active delay	2		2		ns
t3	Active to float delay		14		28	ns
t4	Input setup time to CLK	3(5)		7(10.12)		ns
t5	Input hold time from CLK	0		0		ns

1. Values shown in parentheses are for point-to-point signals.

Figure 12-5 shows the remaining timing PCI bus waveforms. Table 12-5 provides the values for the timing parameters shown in Figure 12-5.

Figure 12-5: PCI Bus Timing Diagram

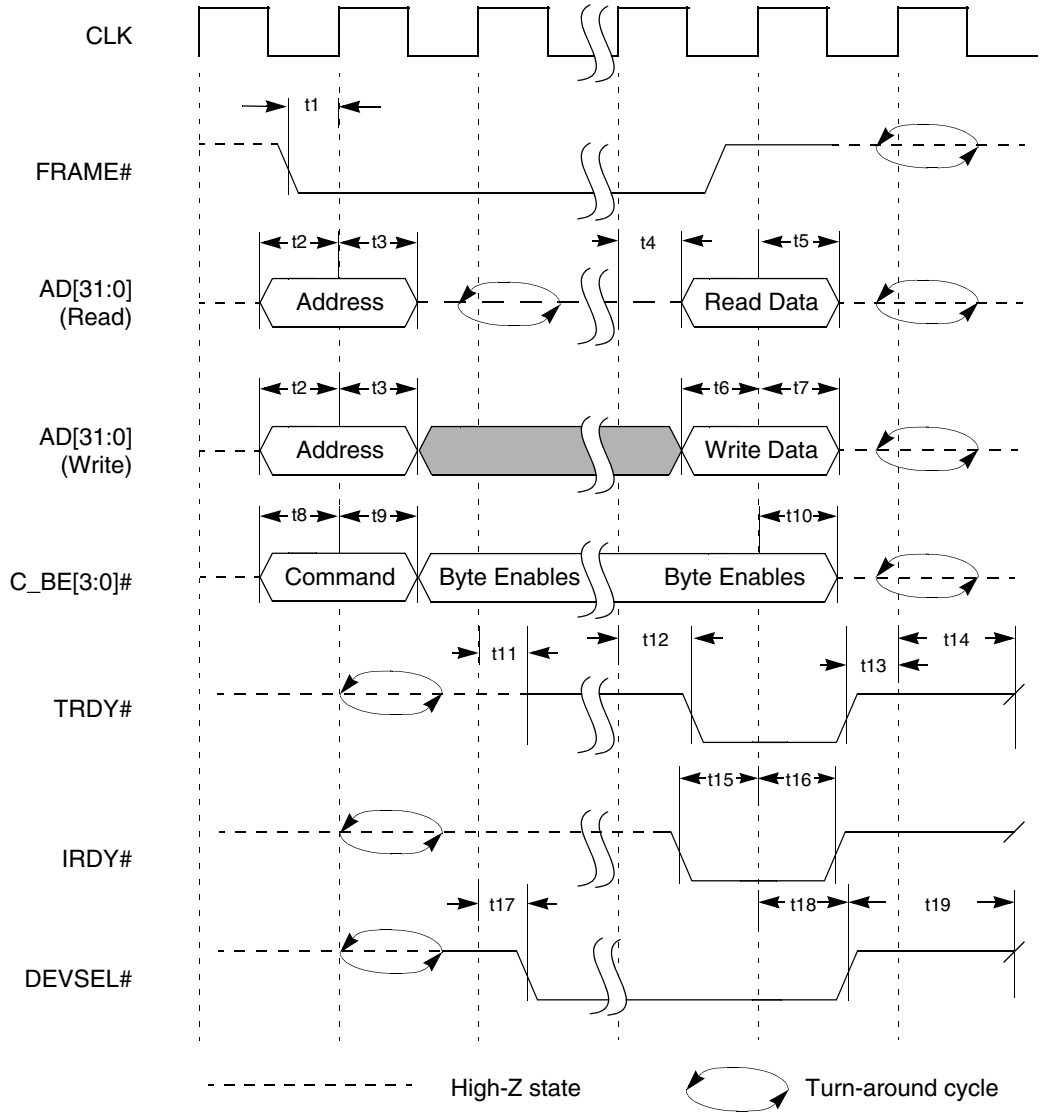


Table 12-5: PCI Bus Timing Parameters (33 MHz)

Symbol	Parameter	Min	Max	Unit
t1	FRAME# setup to CLK	7	-	ns
t2	AD[31:0] (address) setup to CLK	7	-	ns
t3	AD[31:0] (address) hold from CLK	0	-	ns
t4	AD[31:0] (Read Data) valid from CLK	2	11	ns
t5	AD[31:0] (Read Data) hold from CLK	0	-	ns
t6	AD[31:0] (Write Data) setup to CLK	7	-	ns
t7	AD[31:0] (Write Data) hold from CLK	0	-	ns
t8	C/BE[3:0]# (Command) setup to CLK	7	-	ns
t9	C/BE[3:0]# (Command) hold from CLK	0	-	ns
t10	C/BE[3:0]# (Byte Enable) hold from CLK	0	-	ns
t11	TRDY High-Z to High from CLK	2	-	ns
t12	TRDY# active from CLK	2	11	ns
t13	TRDY# inactive from CLK	2	11	ns
t14	TRDY# High before High-Z	1T	-	CLK
t15	IRDY# setup to CLK	7	-	ns
t16	IRDY# hold from CLK	0	-	ns
t17	DEVSEL# active from CLK	2	11	ns
t18	DEVSEL# inactive from CLK	2	11	ns
t19	DEVSEL# High before High-Z	1T	-	CLK

Host Interface Timing

Intel XScale Host

Figure 12-6 shows the timing waveforms for XScale System DRAM operations. Figure 12-7 shows the timing waveforms for XScale read operations. Figure 12-8 shows the timing waveforms for XScale write operations. Table 12-6 through Table 12-8 list the AC timing values for the parameters shown in the three XScale figures.

Figure 12-6: XScale System DRAM (Master) Timing

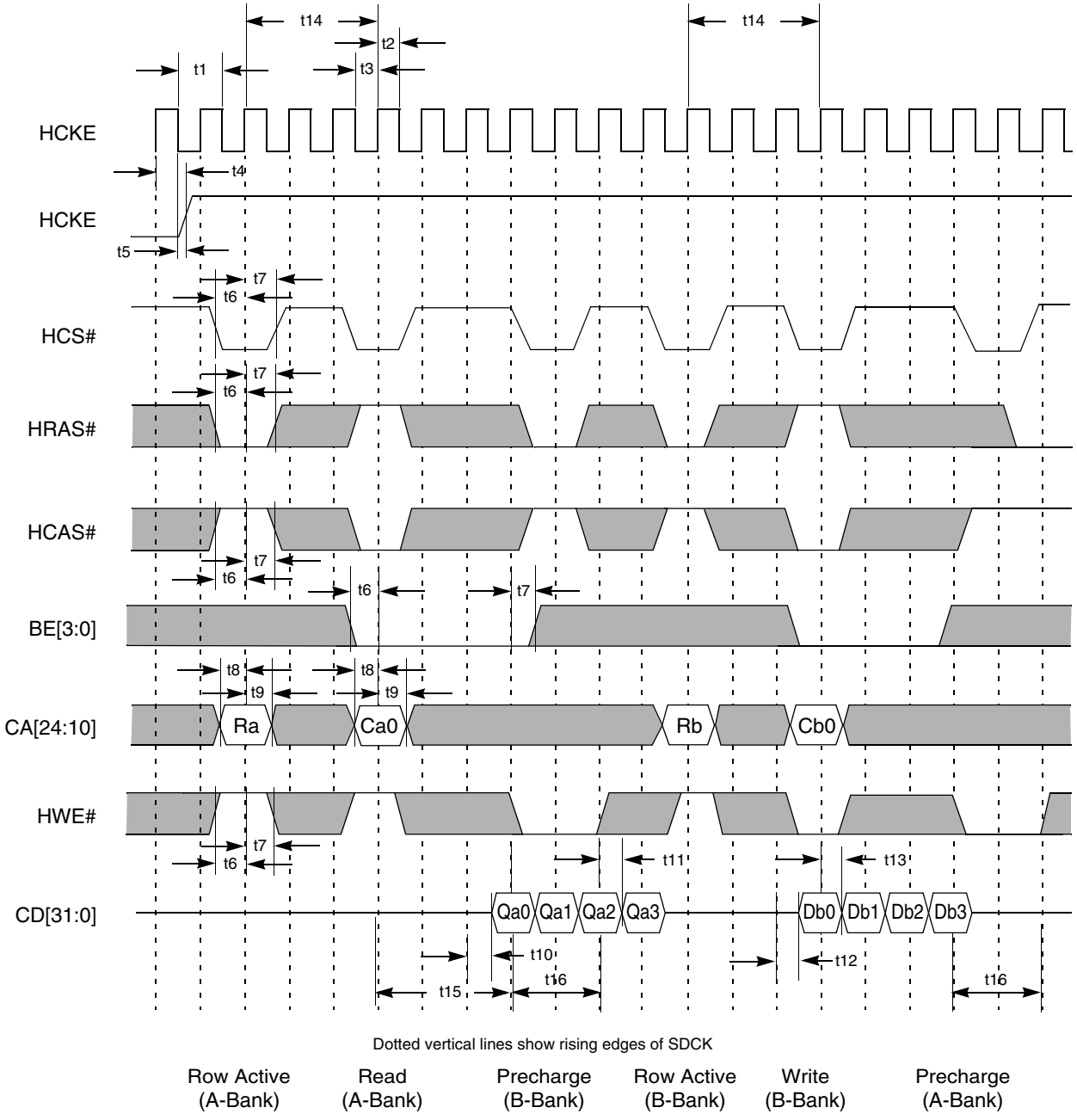


Figure 12-7: XScale Read Timing

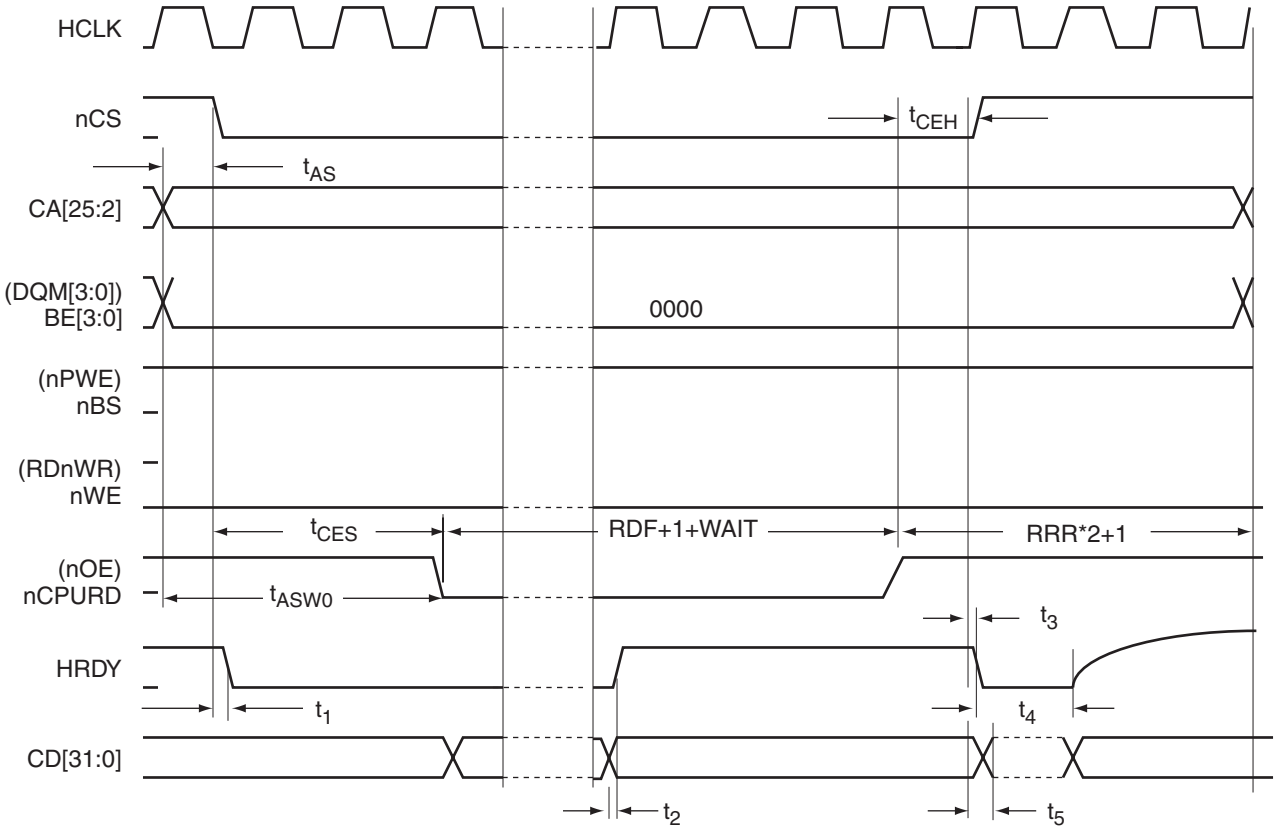


Figure 12-8: XScale Write Timing

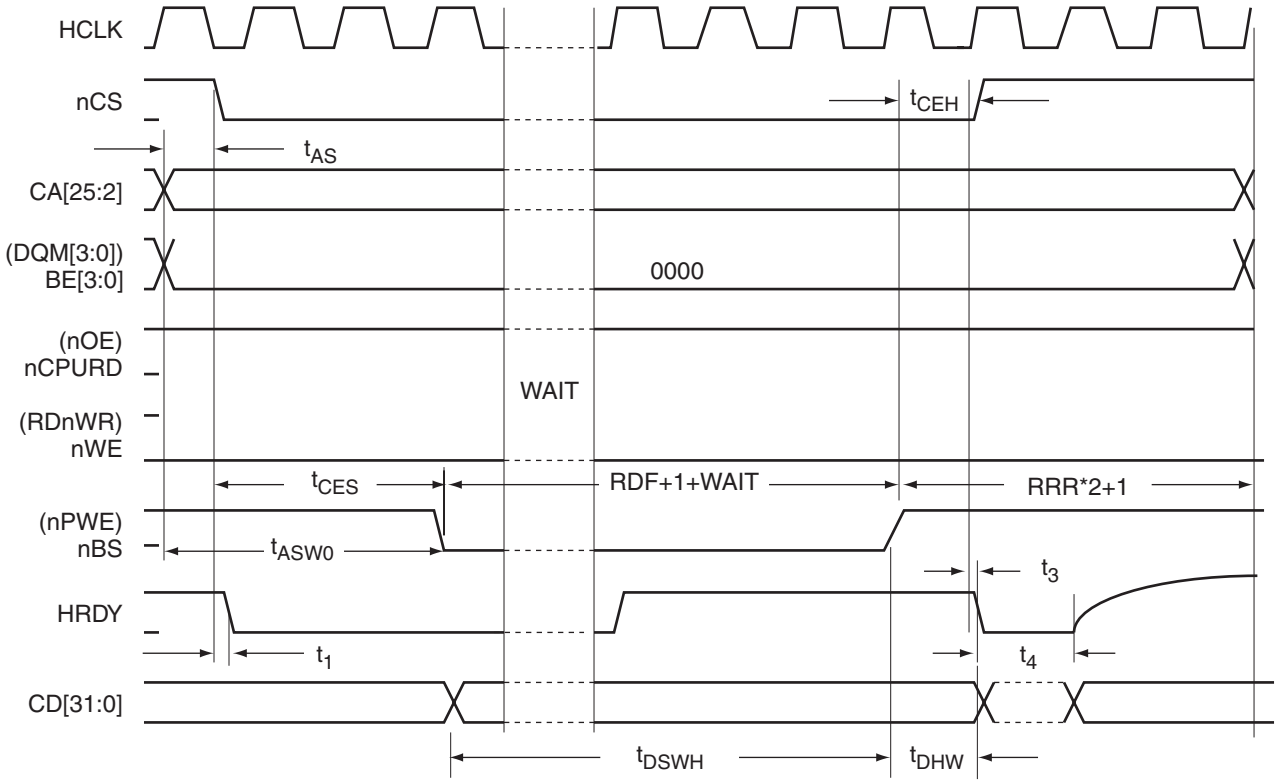


Table 12-6: XScale Timing Parameters

Symbol	Parameter	Min	Max	Units
XScale SDRAM Timing				
t1	HCLK cycle time	12		ns
t2	HCLK high time	4		ns
t3	HCLK low time	4		ns
t4	HCKE hold time	3.5		ns
t5	HCKE setup time	3.5		ns
t6	Command setup time	3.5		ns
t7	Command hold time	3.5		ns
t8	Address setup time	3.5		ns
t9	Address hold time	2.5		ns
t10	Access time from HCLK		t1 - 2	ns
t11	CD Out hold time from HCLK	4		ns
t12	CD In setup time from HCLK	3.5		ns
t13	CD In hold time from HCLK	3.5		ns
t14	Active to READ, WRITE delay (Row Active)	3* t1		ns
t15	READ Latency	3* t1 or 2* t1[1]		ns
t16	Write recovery time (Precharge)	2* t1		ns

1. Programmable value in DRAM Control register, bit 27 (see “DRAM Control” on page 2-11).

Table 12-7: XScale Read Timing Specification (Bus Slave)

Parameter	Timing Descriptions	Control Side	Specified[1]
tAS	Address Setup to nCS	CPU	1 MCLK
tCES	nCS Setup to nOE or nPWE asserted (Low)	CPU	2 MCLKs
tASRW0	Address Setup to nOE or nPWE asserted (Low)	CPU	3 MCLKs
tCEH	nCS Held Asserted After nOE or nPWE Deasserted	CPU	1 MCLK
tAH	Address Hold After nOE or nPWE Deasserted	CPU	RDF+2 MCLKs min.
t1	From nCS Asserted to HRDY Driven	SM107	4 ns max.
t2	Data Setup to HRDY Rise	SM107	1 ns min.
t3	HRDY Deasserted Delay	SM107	4 ns max.
t4	HRDY Driven Low After nCS Deasserted	SM107	1 HCLK
t5	Data Hold After HRDY Deasserted	SM107	1 ns min.

1. HCLK is the bus clock input used by the SM107, and MCLK is the system clock run on the XScale CPU side. When using the first clock option, MCLK and HCLK have the same frequency.

Table 12-8: XScale Write Timing Specification

Parameter	Timing Descriptions	Control Side	Specified[1]
tAS	Address Setup to nCS	CPU	1 MCLK
tCES	nCS Setup to nOE or nPWE Asserted (Low)	CPU	2 MCLKs
tASRW0	Address Setup to nOE or nPWE Asserted (Low)	CPU	3 MCLKs
tDSWH	Write Data Setup to nPWE Deasserted (High)	CPU	RDF+2 MCLKs min.
tDHW	Data Hold After nPWE Deasserted (High)	CPU	1 MCLK
tCEH	nCS Held Asserted After nOE or nPWE Deasserted	CPU	1 MCLK
tAH	Address Hold After nOE or nPWE Deasserted	CPU	RDN+1 MCLK
t1	From nCS Asserted to HRDY Driven	SM107	4 ns max.
t3	HRDY Deasserted Delay	SM107	4 ns max.
t4	HRDY Driven Low After nCS Deasserted	SM107	1 HCLK

1. HCLK is the bus clock input used by the SM107, and MCLK is the system clock run on the XScale CPU side. When using the first clock option, MCLK and HCLK have the same frequency.

Hitachi SH4 Host

Figure 12-9 shows the timing waveforms for SH4 System DRAM operations. Figure 12-10 shows the timing waveforms for SH4 read and write operations. Table 12-9 and Table 12-10 lists the AC timing values for the parameters shown in the three SH4 figures.

Figure 12-9: SH4 System DRAM (Master) Timing

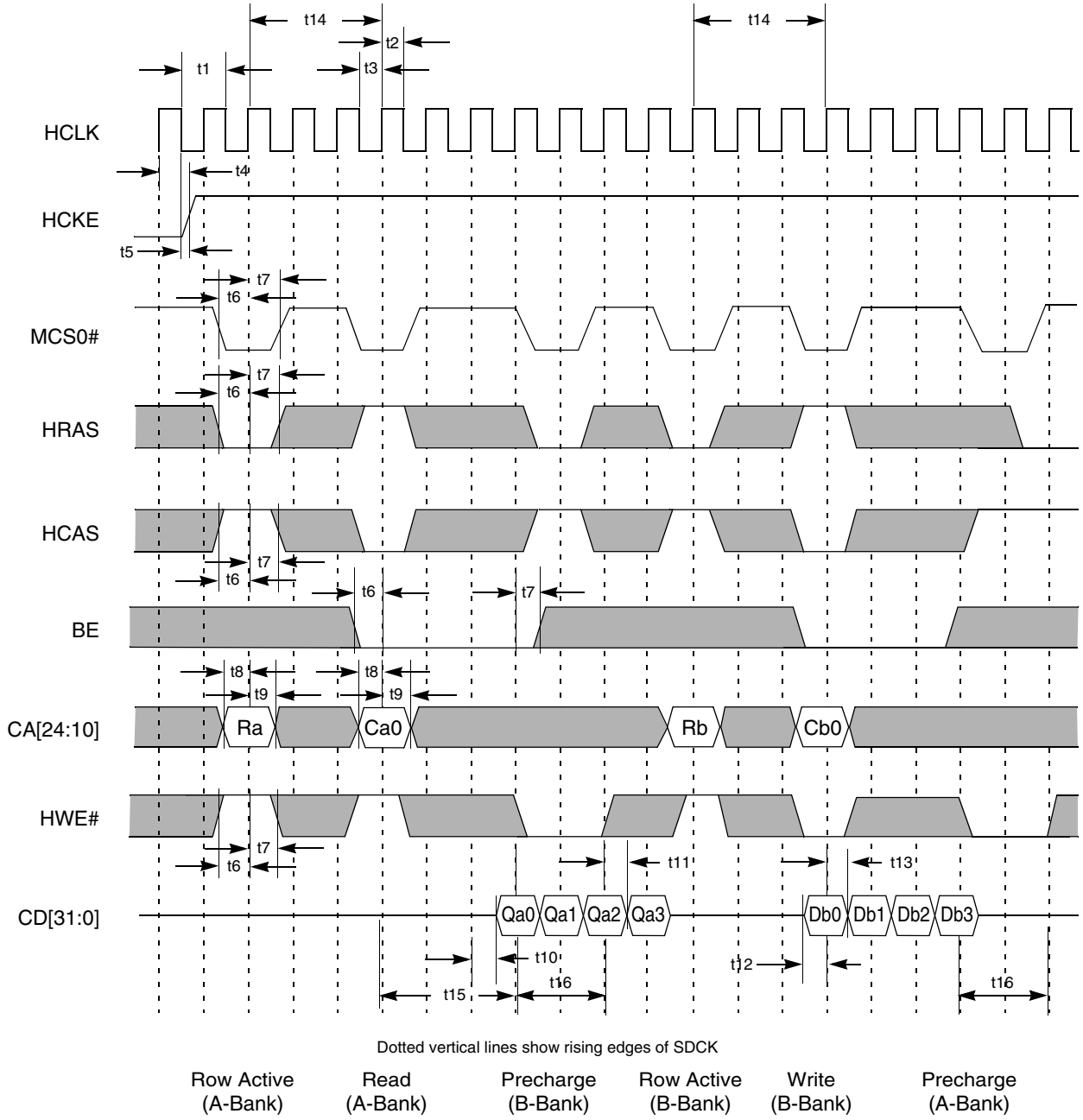


Figure 12-10: SH4 Read and Write Timing

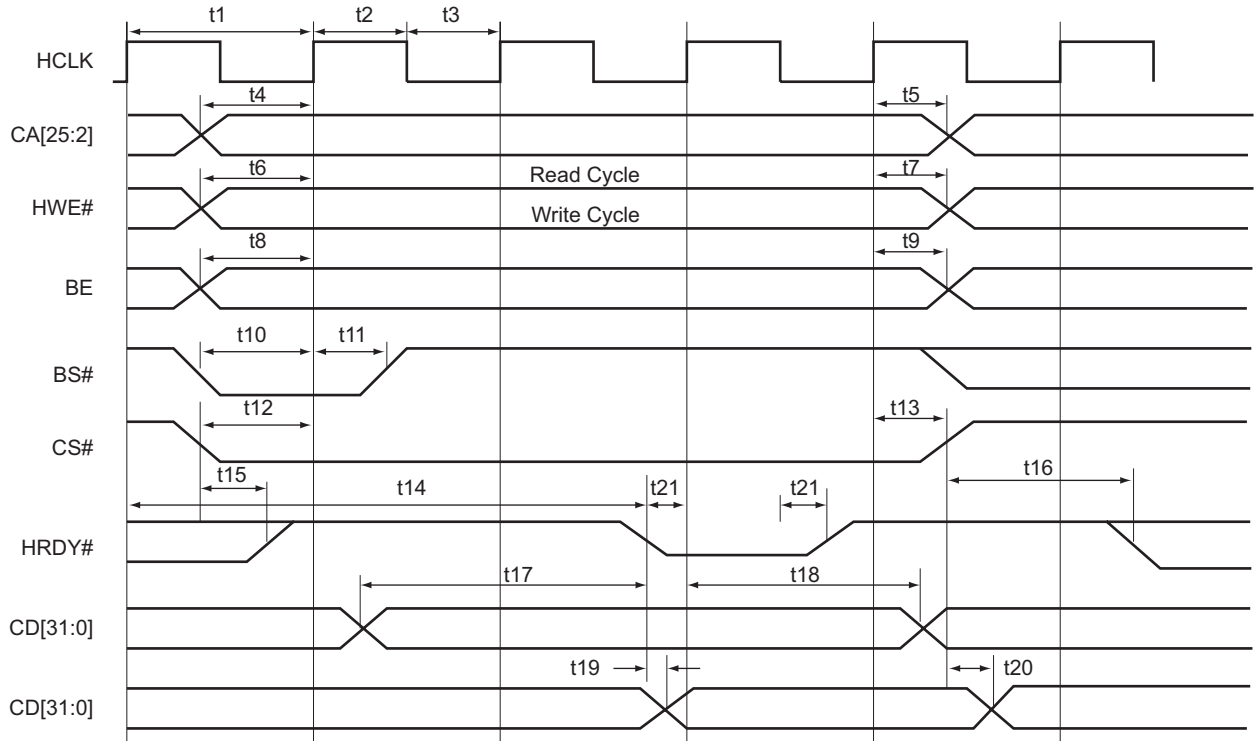


Table 12-9: SH4 Timing Parameters

Symbol	Parameter	Min	Max	Units
SH4 SDRAM Timing				
t1	HCLK cycle time	12		ns
t2	HCLK high time	4		ns
t3	HCLK low time	4		ns
t4	HCKE hold time	3.5		ns
t5	HCKE setup time	3.5		ns
t6	Command setup time		6	ns
t7	Command hold time		2	ns
t8	Address/BA setup time	3.5		ns
t9	Address/BA hold time	2.5		ns
t10	Access time from SDCK		t1 - 2	ns
t11	Data Out hold time from HCLK	4		ns
t12	Data In setup time from HCLK	3.5		ns
t13	Data In hold time from HCLK	3.5		ns
t14	Active to READ, WRITE delay (Row Active)	3* t1		ns
t15	READ latency	3* t1 or 2* t1[1]		ns
t16	Write recovery time (Precharge)	2* t1		ns

1. Programmable value in DRAM Control register, bit 27 (see “DRAM Control” on page 2-11).

Table 12-10: SH4 Read/Write Timing Parameters

Symbol	Parameter	Min	Max	Units
SH4 SDRAM Timing				
t1	HCLK cycle time	12		ns
t2	HCLK high time	4[1]		ns
t3	HCLK low time	4[1]		ns
t4, t6, t8, t12	Command setup time	4		ns
t5, t7, t9, t13	Command hold time	0		ns
t10	BS# setup time	4		ns
t11	BS# hold time	3		ns
t14	Earliest Ready	24[2,3]		ns
t15	Falling edge of CS# to Ready driven	2	12[3]	ns
t16	Rising edge of CS# to Ready 3-stated		12[3]	ns
t17	Data setup time (write cycle)	4		ns
t18	Data hold time (write cycle)	4		ns
t19	Data delay time from falling edge of Ready (read cycle)	0[4]	4[4]	ns
t20	Data hold time from rising edge of CS# or a new BS# (read cycle)	0	4	ns
t21	Falling edge of HCLK to Ready delay	1	4	ns

1. This timing is based on a 12 ns HCLK cycle time.
2. Extension of the Ready signal is recommended. Refer to the SM501 SH4 nRDY Consideration application note for more information.
3. This timing is based on a 12 ns HCLK cycle time. If HCLK is faster than 12 ns t14 should be 2 HCLKs, and t15 and t16 should be 1 HCLK.
4. Data is driven at the same time as Ready with a maximum delay of 4 ns. For SH4 with higher HCLK frequencies, extension of the Ready signal is recommended. Refer to the SM501 SH4 nRDY Consideration application note for more information.

NEC MIPS VR4122/4131 Host

Figure 12-11: NEC System DRAM (Master) Timing

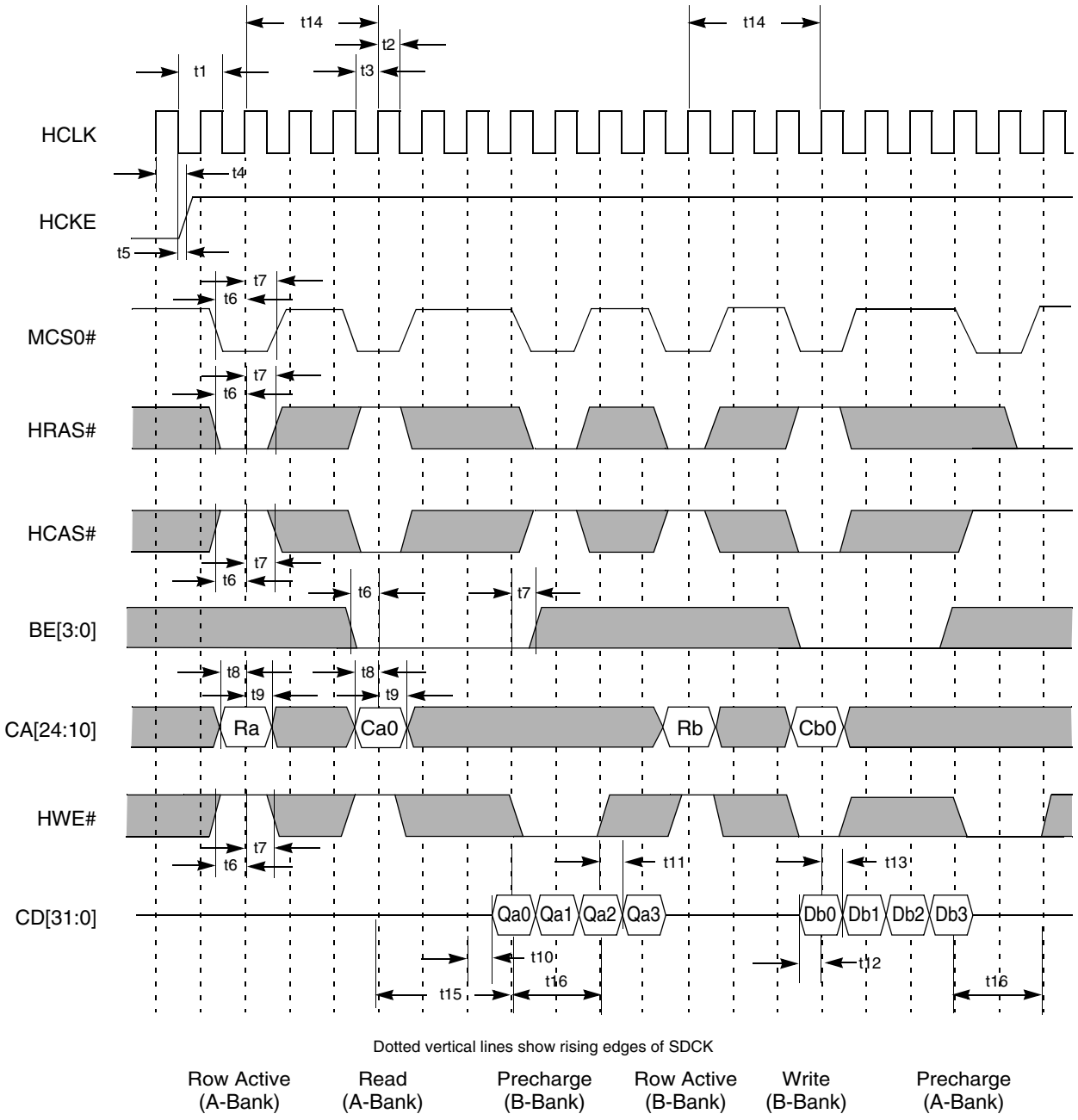


Figure 12-12: NEC DRAM (Slave) Timing

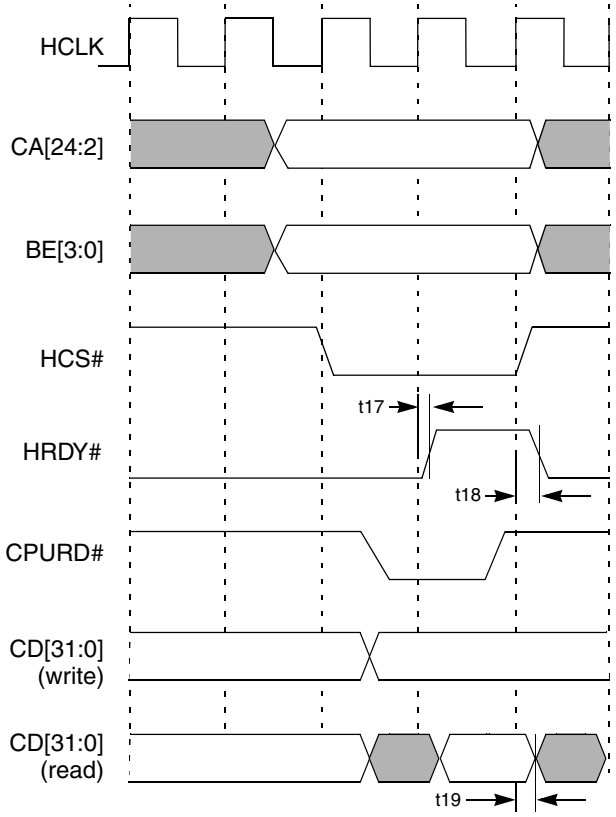


Table 12-11: NEC MIPS Timing Parameters

Symbol	Parameter	Min	Max	Units
NEC SDRAM Master Timing				
t1	HCLK Cycle Time	12		ns
t2	HCLK High Time	4		ns
t3	HCLK Low Time	4		ns
t4	HCKE hold time	3.5		ns
t5	HCKE setup time	3.5		ns
t6	Command setup time		6	ns
t7	Command hold time		2	ns
t8	Address/BA setup time	3.5		ns
t9	Address/BA hold time	2.5		ns
t10	Access time from HCLK		t1 - 2	ns
t11	Data Out hold time from HCLK	4		ns
t12	Data In setup time from HCLK	3.5		ns
t13	Data In hold time from HCLK	3.5		ns
t14	Active to READ, WRITE delay (Row Active)	3* t1		ns

Table 12-11: NEC MIPS Timing Parameters (Continued)

Symbol	Parameter	Min	Max	Units
t15	READ Latency	3* t1 or 2* t1[1]		ns
t16	Write recovery time (Precharge)	2* t1		ns
NEC DRAM Slave Timing				
t17	Ready latency		4	ns
t18	Ready hold time		2	ns
t19	Data hold time		2	ns

1. Programmable value in DRAM Control register, bit 27 (see "DRAM Control" on page 2-11).

Display Controller Timing

Color TFT Interface

Figure 12-13 shows the timing waveforms for the FP and FP_DISP signals. Figure 12-14 shows the timing waveforms for the FP_HSYNC and FP_VSYNC signals. Table 12-12 lists the AC timing values for the parameters shown in the two figures.

Figure 12-13: FP and FP_DISP Timing

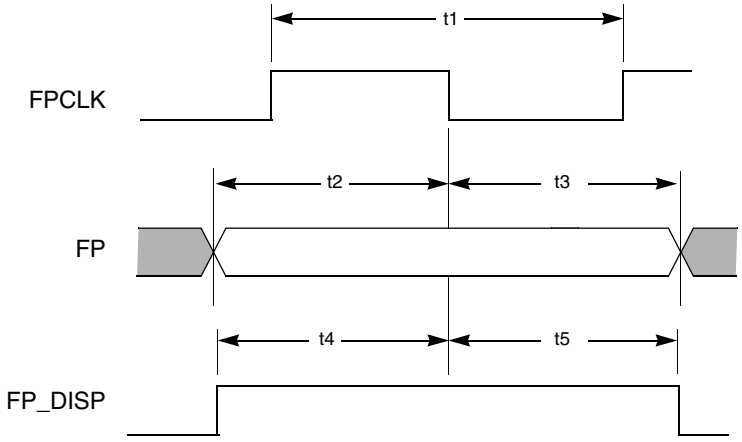
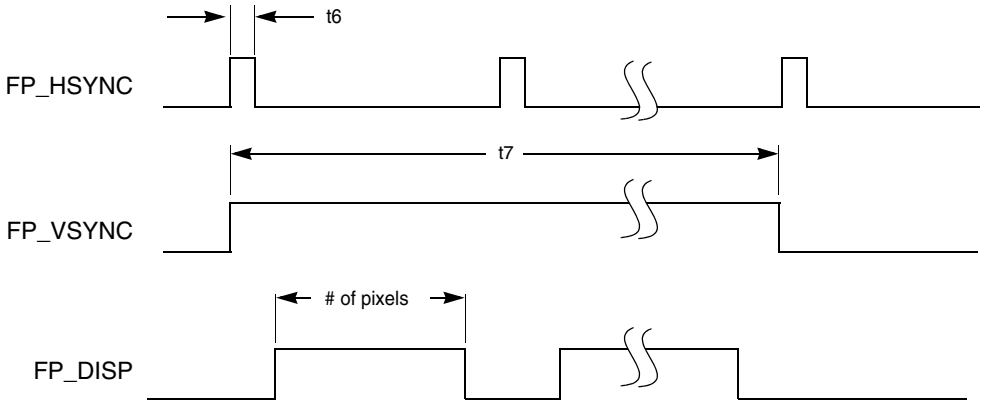


Figure 12-14: FHSYNC and FVSYNC Timing



Note: Number of pixels is programmed in the Panel Horizontal Total register, bits [11:0] (see "Panel Horizontal Total" on page 5-15).

Table 12-12: Color TFT Interface Timing Parameters

Symbol	Parameter	Min	Max	Units
t1	TFT FPCLK cycle time	12		ns
t2	FP setup to FPCLK falling edge	0.5*T[1] - 2		ns
t3	FP hold from FPCLK falling edge	0.5*T - 2		ns
t4	FP_DISP setup to FPCLK falling edge	0.5*T - 2		ns
t5	FP_DISP hold from FPCLK falling edge	0.5*T - 2		ns
t6	FP_HSYNC pulse width	8	16	T
t7	FP_VSYNC pulse width	1		FP_HSYNC

1. T is pixel clock rate on LCD.

ZV Port Timing

Figure 12-15 depicts the relationship amongst the ZV Port signals. Table 12-13 shows the AC parameters associated with the ZV Port signals when the ZV Port custom interface is in use at 50 MHz.

Figure 12-15: ZV Port Timing

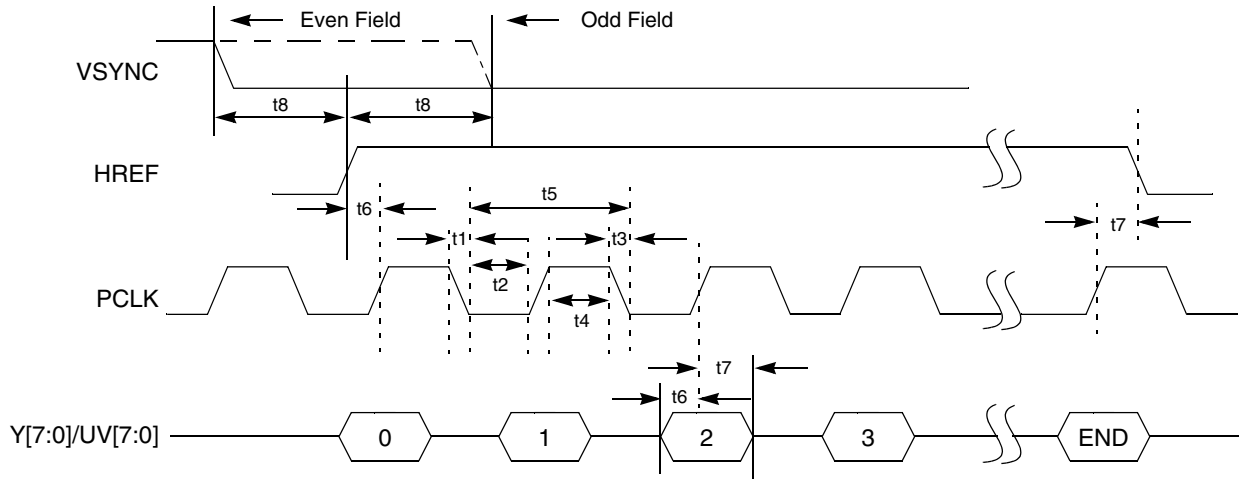


Table 12-13: ZV Port Timing Parameters

Symbol	Parameter	Min	Max	Units
t1	PCLK fall time	2		ns
t2	PCLK low time	7		ns
t3	PCLK rise time	2		ns
t4	PCLK high time	7		ns
t5	PCLK cycle time	20		ns
t6	Y[7:0] / UV[7:0] / HREF setup time	10		ns
t7	Y[7:0] / UV[7:0] / HREF hold time	3		ns
t8	VSYNC setup / hold time to HREF	30		ns

Note: All video signals have minimum rise and fall times of 4 ns and maximum rise and fall times of 8 ns. Non-interlaced data asserts VSYNC at the Odd Field timing.

Local SDRAM Timing

Figure 12-16 shows the timing waveforms for the Local SDRAM. Table 12-14 lists the AC timing values for the parameters shown in Figure 12-16.

Figure 12-16: Local SDRAM Timing

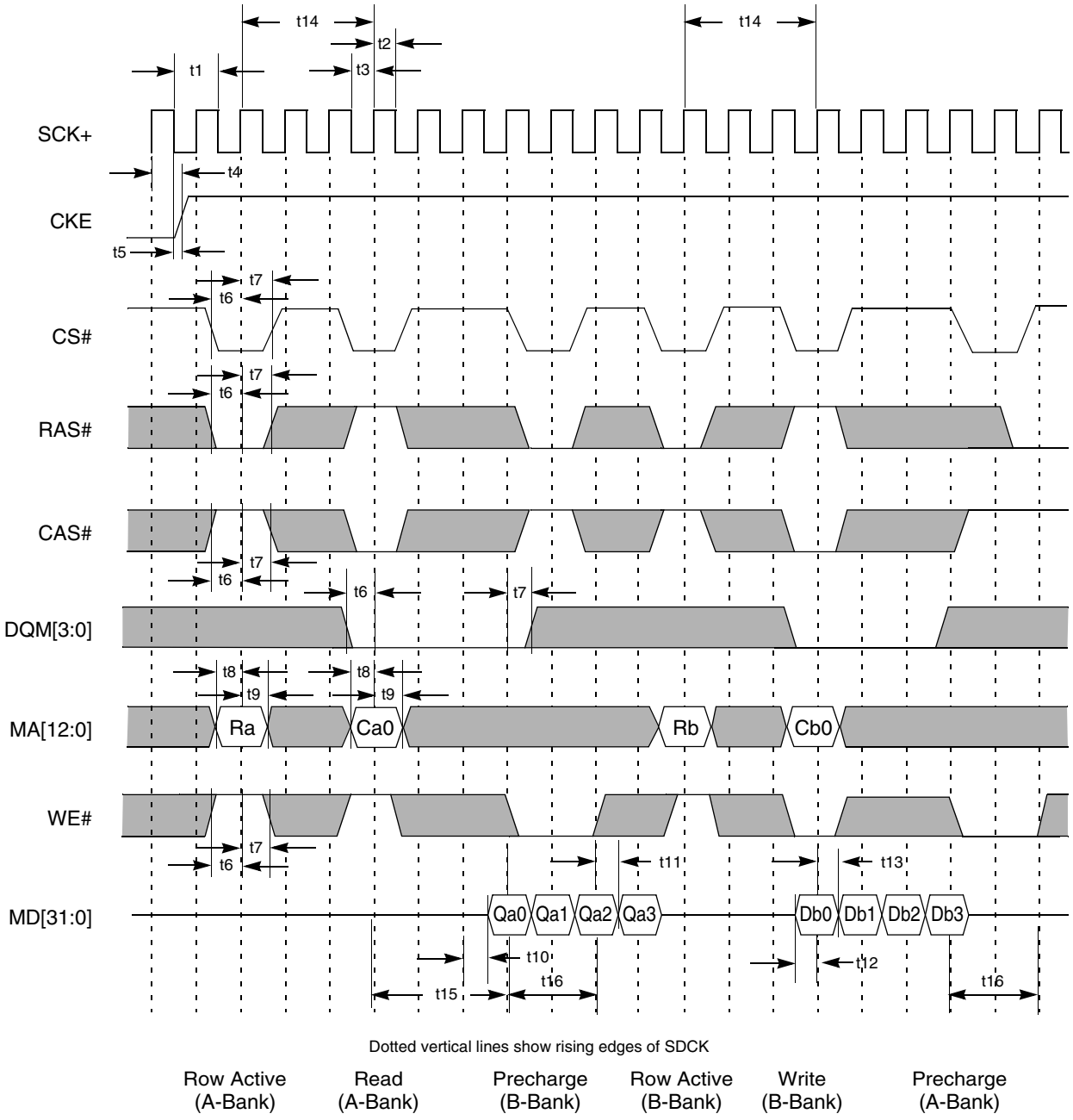


Table 12-14: Local SDRAM Timing Parameters

Symbol	Parameter	Min	Max	Units
t1	SCK+ Cycle Time	6		ns
t2	SCK+ High Time	2.5		ns
t3	SCK+ Low Time	2.5		ns
t4	CKE hold time	0.8		ns
t5	CKE setup time	1.5		ns
t6	Command setup time	1.5		ns
t7	Command hold time	0.8		ns
t8	Address/BA setup time	1.5		ns
t9	Address/BA hold time	0.8		ns
t10	Access time from SCK+		t1 - 2	ns
t11	Data Out hold time from SCK+	1.8		ns
t12	Data In setup time from SCK+	1.5		ns
t13	Data In hold time from SCK+	0.8		ns
t14	Active to READ, WRITE delay (Row Active)	3* t1		ns
t15	READ Latency	3* t1		ns
t16	Write recovery time (Precharge)	2* t1		ns