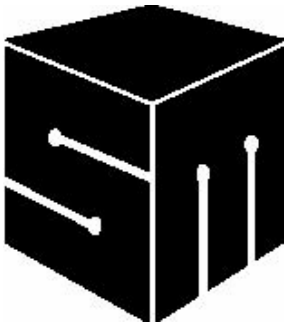

Silicon Motion, Inc.

Mobile Computer Display Controller

Preliminary

Version 1.5

Last Updated 2/6/03

SM731 Databook

Silicon Motion®, Inc.

SM731 DataBook

Notice

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Version Number	Date	Note
0.1	10/10/00	All registers are the same as the Lynx3DM except the 3D registers. All registers other than the 3D registers have been included in a single chapter. Document includes the new 385-ball BGA schematics and ball-diagram. Several sections have been temporarily removed until the final details are completed. Updated headers and footers. Added a numerical ball list.
0.2	11/1/00	Added panel registers FPR 100h to FPR 119h.
0.3	1/16/01	Completed ball diagram and signal definitions. Added LVDS registers.
0.4	2/23/01	Changed Video Registers
0.5	3/29/01	Updated or Changed Clock control, VGA, Power down control, and Memory control registers.
0.6	5/1/01	Updated 3D section, added 2D3D DMA registers, and made changes per engineering specifications.
0.7	8/15/01	Updated Flat Panel Registers
0.8	9/25/01	Updated 2D Drawing Engine Registers Chapter and 2D3D DMA Registers Chapter
1.0	11/20/01	Updated databook per engineering specifications
1.1	1/16/02	Updated databook per engineering specifications
1.2	2/25/02	Updated databook per engineering specifications
1.3	4/1/02	Added definitions for MA[6:0] Power-on Configuration Table

Version Number	Date	Note
1.4	7/11/02	• Changed SM730 to SM731 • Updated power configuation table • Changed Pin B7 from ~PME to VPVDD • Updated NAND Tree Scan Test Order • Deleted RAMDAC Block Diagram • Added description for Activity Output Pin (P22) • Changed the following registers: CCR65_[4], CRT9E_[6], SVR4A_[6], SVR4C_[7:0], FPR100_[25:24], FPR100_[17:15], FPR100_[10:9], FPR120_[15:0] • Added LVDS Transmitter Device Transition Times Diagram and LVDS Specification Table
1.5	2/6/03	• Remove external memory support, 0/32 MB support, and DDR support. • Changed register CPR00, bit 25 to reserved

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Chapter 1: Overview

The SM731 is a power managed, low-power display controller for portable devices including notebooks and Tablet PCs. This device delivers full featured 3D, an unique memory architecture designed to enhance 3D/2D performance, enhanced multi-display capabilities, and Motion Compensation for DVD.

ReduceON™ is a technology that enables systems to lower power consumptions, and provides a mechanism to intelligently manage the chip's internal clock core voltage and each major functional block of the graphics chip. By turning off the clock to the block that is not used, the power consumption is significantly reduced during normal operation. Thus ReduceON provides a method in further reducing the overall system power resulting in longer battery life.

The SM731 incorporates an IEEE Floating Point Setup engine as well as a full featured 3D rendering engine. The 3D engine pipeline was designed to operate in a balanced manner, allowing setup of 6 million triangles per second (125MHz core frequency) and rasterization of 125 million pixels per second. The dual pipe Texture engine can output 250 million Texels per second. Among other features, SM731 natively supports Mip mapping, Alpha blend, Specular highlights and Fog, Stencil planes, W buffer and fog, Bump Mapping, and Z engine.

The SM731 integrates 16 Mbytes of on-board SGRAM (SDR) over a 64-bit memory bus operating at up to 150 MHz. The total maximum peak bandwidth available (1.2 Gbytes/sec) allows concurrent support of large displays and other processing functions at optimum performance.

SM731 continues to support all the Dual Application/Dual View capabilities of its predecessors. In addition, SM731 can drive two independent digital displays (dual-digital), as well as simultaneously drive LCD, CRT and TV displays (DualMon). SM731 also incorporates two 112 MHz Max pix clock LVDS channels that can drive two separate panels or a single high resolution panel (up to UXGA). The above capabilities are available under Windows 98/ME, Windows 2000, Windows XP, and future Microsoft operating systems.

A robust 128-bit Drawing Engine provides no compromise 2D performance. The Drawing Engine supports 3 ROPs, BitBLT, transparent BLT, pattern BLT, color expansion, line draw and Alpha blending. The Host interface Unit allows support for PCI and AGP up to 4X with SB signals and over a 1.5V or 3.3V interface. Support for all ACPI power states is provided. A high quality TV encoder, VGA Core, LCD Backend Controller and 235 MHz RAMDAC are incorporated as well.

The SM731's Motion Compensation block, Video Processor block, and Video Capture Unit provide superior video quality for real-time video playback and capture. When combined with performance CPUs, the Motion Compensation block allows full frame playback of DVD video content without the need for additional hardware. The Video Processor supports multiple independent full screen, full motion video windows with overlay. Each motion video window uses hardware YUV-to-RGB conversion, scaling, and color interpolation. When combined with multi-view capabilities of the chip, these independent video streams can be output to each of two display devices and bilinear scaled to support applications such as full screen display of local and remote images for video conferencing.

SM731 is designed with 0.25m, 5LM, 2.5V CMOS process technology. A hierarchical layout approach provides enhanced internal timing control. In addition to built-in test modes and a signature analyzer, the SM731 incorporates a 20 bit test bus which can be used to simultaneously monitor internal signals through the Zoom Video (ZV) Port Interface. The capability

can be used to increase fault coverage, and to reduce silicon validation and debugging time. The SM731 is available in a 385-pin BGA packages.

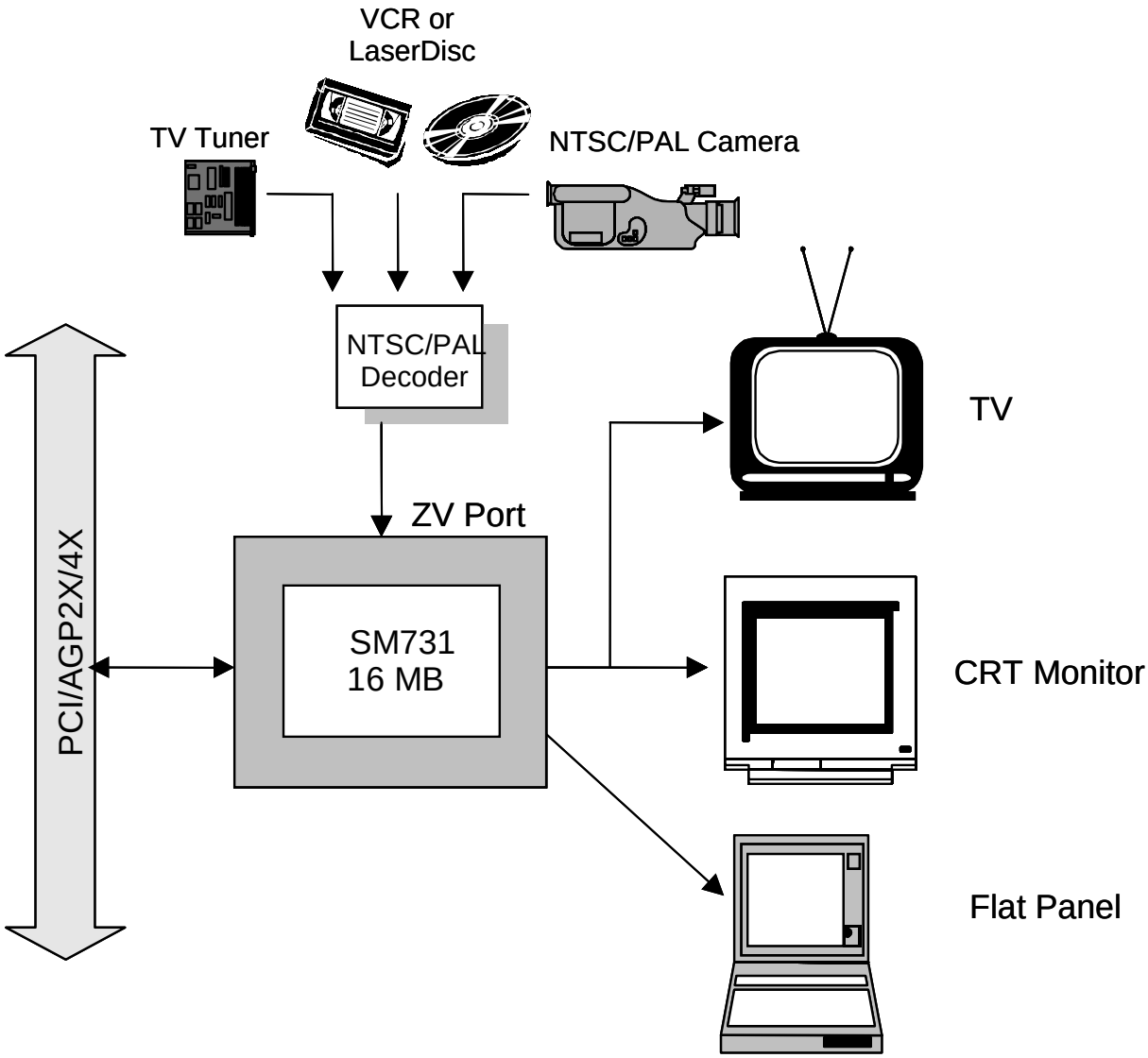


Figure 1: System Block Diagram for SM731

Features	Benefits
High performance, power managed 3D	Desktop level 3D performance within the power budget of a notebook system
Motion Compensation	Allows full frame playback of DVD content in software
DualMon support	• Applications available at the same time across multiple display devices • Single chip implementation ideal for mobile systems
Dual View support	Any rectangular portion of primary display can be zoomed up for display on multiple secondary displays
Dual-Digital support	Independent display support for external digital LCD monitor or LCD projector
Hardware support for LCD landscape/portrait rotation	Portrait view for desktop publishing, and word processing applications for Tablet PCs.
Tabview support	LCD and CRT with different orientations which is key for Tablet PCs. (LCD in portrait and CRT in landscape)
Adaptive Power Management • Dynamic functional block shut-down, clock control	• Reduce average power consumption when in operation mode
Multiple independent hardware video windows	• Independent full screen, motion video for separate displays. • Complete dual view support for video
128-bit, single clock cycle Drawing Engine	No compromise 2D graphics performance for mobile systems
High performance memory interface	Delivers over 1.2GB/s bandwidth to support 3D graphics, DVD
AGP 2X/4X sideband and PCI 2.1 support	Provides interface capability for today's most popular PC graphics busses
TFT panel support up to 1600x1200 with two independent built-in LVDS transceiver channels	Supports all panel requirements for mobile systems
Integrated TV Encoder with Macrovision	Graphics/video display on TV with no external support logic
235MHz 24-bit RAMDAC	Supports resolutions up to 1600x1200
Zoom Video Port	Provides support for camera, TV tuner input, or output to VCR
PC99, PC2001 Compliant, ACPI Compliant	Meets WHQL certification requirements
SW support for Microsoft Windows 98, Windows 2000, Windows XP, and Linux (xfree86.org)	Complete OS software support

Chapter 2: Initialization

SM731 generates an internal power-on reset during system power-on. After receiving the system ~RESET signal, SM731 will release its internal power-on reset circuit and enter the RESET period until the host de-asserts the ~RESET signal. During the RESET period, SM731 resets its internal state machines and registers to the power-on default states. During power-on, SM731 is configured based on configuration lines MD [37:0].

Table 1 provides a detailed description of each configuration line. All MD (memory data) lines have internal pull-up resistors on I/O pads which are latched into the corresponding register as logic "1" on the rising edge (trailing edge) of the ~RESET. To set a specific bit as logic "0" during power-on reset, an external pull-down resistor must be added on the corresponding MD line.

In addition to power-on configuration, SM731 performs an initialization sequence for the integrated memory.

After memory initialization has been completed, SM731's video BIOS is ready to service system BIOS requests. System BIOS passes a pointer to the SM731 video BIOS to start the video BIOS initialization sequence.

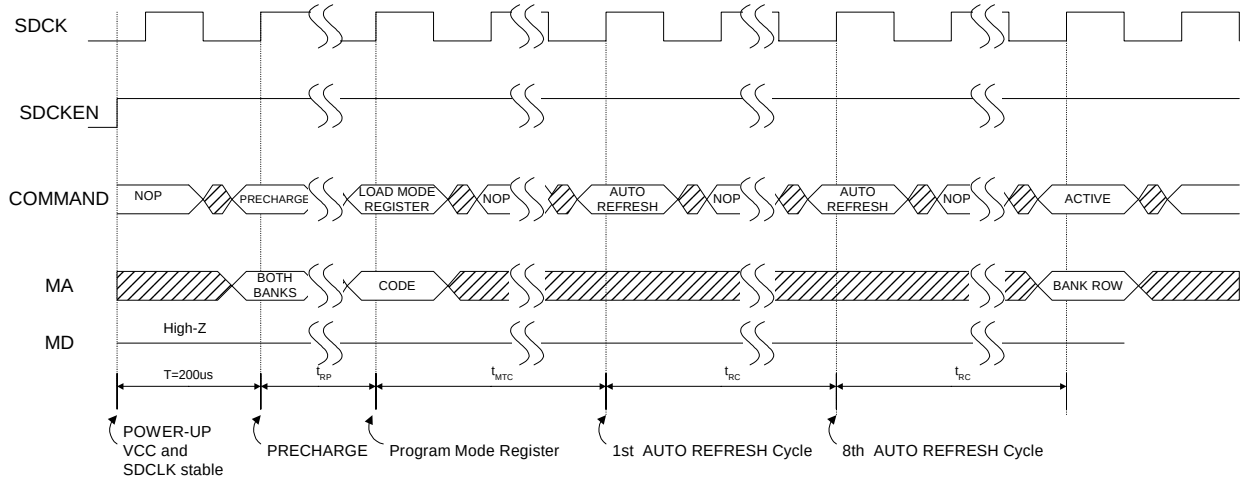


Figure 2: SGRAM Power-Up and Initialization Sequence

Figure 3 illustrates the SM731 Video BIOS initialization flow. The initialization sequence consists of the following stages:

- Load configuration table
- Get panel 2D
- Initialize INT10 function
- Initialize hardware
- Query system BIOS via Int 15 calls
- Set initial mode
- Enable the display

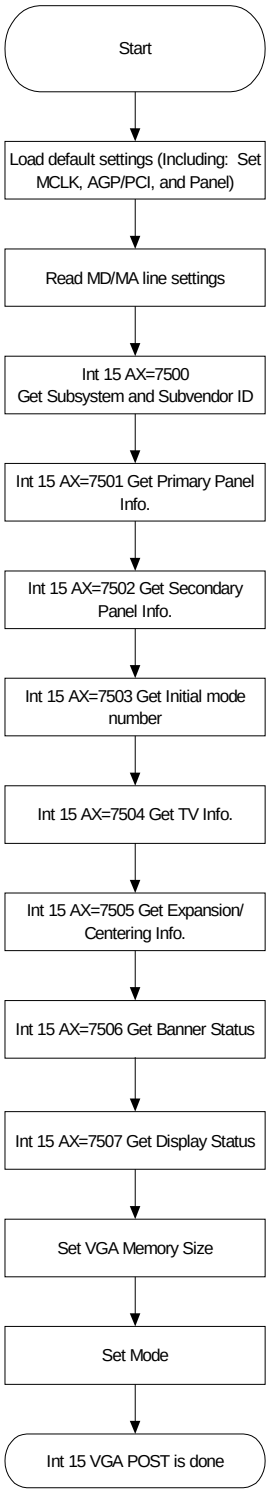


Figure 3: SM731 Video BIOS Initialization Flow

SM731 Power-On Configurations

- Bit MD[63:0], MA[11:0], and MBA[1:0] have internal pull-up resistors on the I/O pads
- 0 = external pull-down resistor
- 1 = no external pull-down resistor

Table 1: Power On Configuration

Signal Name	Read/Write	Register Address	IO Address	Description
MD[37]	Config Only			PLL selection. This is a hardware test feature which is used for debug purpose only) Definition: pllvck = new,high performance pll pllvrck = existing pll from SM731 pllmck = existing pll from SM731 pllmck2 = new,high performance pll If MD[37] config = 1 (default) Vclk(video clock) = pllvck VrClk(LCD Panel clock) = pllvrck Mclk(Engine clock) = pllmck Mclk2(memory controller clock) = pllmck2 else Vclk(video clock) = pllvrck VrClk(LCD Panel clock) = pllvrck Mclk(Engine clock) = pllmck / 2 Mclk2(memory controller clock) = pllmck * See also definition of CCR67[3:2]
MD[36:35]	Config Only			Size of Base Memory selection 00=4MB 01=8MB 10=16MB 11=32MB
MD[34]	Config Only			Being used when only one Endian selected 0=Small Endian 1=Big Endian
MD[33]	Config Only			0=Only one Endian 1=Both Endian
MD[32]				Reserved
MD[31]	R/W	MCR76[7]	3c5.76	0=Reserved 1=Normal (default)
MD[30:25]				Reserved
MD[24]	R/W	MCR76[0]	3c5.76	0=SDRAM interface 1=Reserved
MD[23]				0=AND with RESETN to reset the free running clock divider for simulation and testing 1=Normal (default)
MD[22}				Reserved
MBA[1]	Config Only			0=Enable C0000 EPROM access 1=Disable C0000 EPROM access
MBA[0]	Config Only			0=>PCI Config Reg54[2]=1=>AGP4X capable 1=>PCI Config Reg54[2]=0=>Not AGP4X capable

Signal Name	Read/Write	Register Address	IO Address	Description
MA[11:8]	R/W	GPR70[3:0]	3c5.70	Panel ID 0000 = 640x480 TFT 0001 = 800x600 TFT 0010 = 1024x768 TFT 0011 = 1280x1024 TFT 0100 = 1600x1200 TFT
MA[7]	R/W			AGP pad configuration 0=For 1.5V AGP bus 1=For 3.3V AGP bus
MA[6]	R/W			LVDS interface 0 = 18 bit TFT 1 = 24 bit TFT
MA[5]	R/W			LVDS Panel 0 = MSB of R,G,B at TX3-+. For 24 bits LVDS 1 = LSB of R,G,B at Tx3-+. For 24 bits LVSDS (Hitachi type)
MA[4]	R/W			Panel Sequence 0 = Software panel on/off sequence 1 = Hardware panel on/off sequence
MA[3]	R/W			LVDS Configuration 0 = Use double LVDS configuration (two LVDS chips on panel side) 1 = Use single LVDS configuration (only single LVDS receiver on panel)
MA[2:1]	R/W			00=Reserved 01=Select non-LVDS panel as primary panel display 10=Select LVDS1 as primary panel display 11=Both LVDS1 and non-LVDS panel as primary panel display
MA[0]	R/W			Reserved for software purposes
MD[21:0]				Reserved

Note: For Windows XP, Windows NT, Windows 9X, and Windows Me, the setting for MD [36:35, 33] should be set at [111]. However, for Windows CE, the setting for MD [36:35, 33] should be set at [1,0,0].

Chapter 3: PCI/AGP Bus Interface

SM731 provides a glue-less interface to the PCI and AGP system bus. The device is fully compliant with PCI Version 2.2. SM731's PCI Host Interface Unit supports both slave and master mode. To maximize performance, the Host Interface Unit also supports burst write, and burst read with Read Look Ahead. When connected to the AGP interface, SM731 supports AGP 2X/4X with sideband.

The PCI/AGP Host Interface Unit manages data transfer between the external PCI/AGP bus and internal Host Interface (HIF) bus. All functional blocks, with the exception of the Drawing Engine, are tied to the HIF bus through a proprietary protocol. Separate decode logic and a dedicated FIFO are used for the Drawing Engine.

In addition to PCI Configuration Space Registers, the PCI/AGP Host Interface Unit contains Power Down Control Registers (PDR20-PDR23) and System Control Registers (SCR10-SCR1A). These Registers may accessed by the CPU even while internal PLLs are turned off.

PCI Configuration Registers

The PCI configuration registers are designated CSR00 - CSR3D. A brief description of key elements of the register set follows:

- Vendor ID register (CSR00) - hardwired to 126Fh to identify Silicon Motion, Inc. as the chip vendor.
- Device ID register (CSR02) - hardwired to 0730h to identify the SM731 device.
- Status register (CSR06) - hardwired to 01b, which indicates medium speed for ~DEVSEL.
- Class Code register (CSR08) - hardwired to 030000h to specify SM731 as a VGA compatible device. Bit [7:0] used to identify the revision of the SM731.
- Memory Base Address register (CSR10) - specifies the PCI configuration space for address relocation. After power-on, the register defaults to 00h, which indicates the base register can be located anywhere in a 32-bit address space and that the base register is located in memory space.
- Subsystem Vendor ID and Subsystem ID (addressable at CSR2C and CSR2E respectively) - 32-bit read only registers. These registers are used to differentiate between multiple graphics adapters within the same system.

Chapter 4: Signal Descriptions

The SM731 is packaged in a 385 BGA package. Table 2 lists each ball and its associated signal. Figure 4 illustrates the pinout diagram for the SM731 package. Figure 35 illustrates the mechanical dimensions of the BGA package.

SM731 Ball Descriptions

The following table, Table 2, provides a listing in numerical order of each ball and its associated signal. Table 3, offers a brief description of each signal used by SM731 sorted by functional block. Signal names with ~ preceding are active "LOW" signals, whereas signal names without ~ preceding are active "HIGH" signals. Also, the following abbreviations are used for Pin Type.

I - INPUT SIGNAL
O - Output Signal
I/O - Input or Output Signal
‘Note: All Outputs and I/O signals are tri-stated. Internal pull-up for I/O pad are all 100KΩ resistor. Internal pull-down for I/O pad are all 100KΩ resistor.

Table 2: Ball Functions

Ball	Function
A1	VSS
A2	VDD2
A3	MD1
A4	MD0
A5	MD31
A6	MD30
A7	~SIP_AGP
A8	ST2
A9	AD2
A10	AD0
A11	VDD3
A12	VDD2
A13	AD12
A14	AD14
A15	~BE0
A16	PAR
A17	~FRAME
A18	~BE2
A19	AD16
A20	AD18
A21	AD21
A22	VDD2

Ball	Function
A23	VSS
B1	VDD2
B2	VDD3
B3	MD2
B4	MD3
B5	MD28
B6	MD29
B7	VPVDD
B8	~AGP_BUSY
B9	ST1
B10	AD1
B11	AD5
B12	AD4
B13	AD9
B14	AD10
B15	AD13
B16	~BE1
B17	~TRDY
B18	~STOP
B19	AD17
B20	AD20
B21	AD23

Ball	Function
B22	RS2
B23	VDD2
C1	MD4
C2	MD5
C3	MD6
C4	MD25
C5	MD26
C6	MD27
C7	~RBF
C8	~PIPE
C9	ST0
C10	AD3
C11	AD6
C12	AD7
C13	AD8
C14	AD11
C15	AD15
C16	~DEVSEL
C17	~IRDY
C18	AD19
C19	AD22
C20	~BE3

Ball	Function
C21	IDSEL
C22	AD24
C23	AD25
D1	MD16
D2	MD7
D3	MD12
D4	MD13
D5	MD14
D6	DQS0
D7	MD15
D8	MD24
D9	SBA7
D10	SBA6
D11	SBA5
D12	SBA4
D13	SBA3
D14	SBA2
D15	SBA1
D16	SBA0
D17	HVREF
D18	~SB_STB
D19	SB_STB

Ball	Function
D20	~AD_STB1
D21	AD26
D22	AD27
D23	AD28
E1	MD18
E2	MD17
E3	MD10
E4	MD11
E5	VSS
E6	VDD2
E7	VSS
E8	VDD3
E9	VSS
E10	VDD2
E11	VSS
E12	HVDD
E13	VSS
E14	HVDD
E15	VSS
E16	VDD1
E17	HVDD
E18	VDD2
E19	VSS
E20	AD_STB1
E21	AD29
E22	AD30
E23	AD31
F1	MD19
F2	MD20
F3	MD8
F4	MD9
F5	VDD3
F19	HVDD
F20	AD_STB0
F21	~REQ
F22	~GNT
F23	P0
G1	MD22
G2	MD21
G3	~DQM3
G4	MVREF
G5	VSS
G19	VSS
G20	~AD_STB0
G21	~RST
G22	~INTA
G23	P1
H1	~DQM0
H2	MD23
H3	SDCKE
H4	~DQM1
H5	VDD2

Ball	Function
H19	VDD2
H20	CLK
H21	P2
H22	P3
H23	P4
J1	~DQM2
J2	~WE
J3	MA8
J4	DSF
J5	VSS
J19	VSS
J20	P7
J21	P6
J22	P5
J23	PCLK
K1	~CAS
K2	~RAS
K3	~CS
K4	MA11
K5	VDD3
K10	VDD3
K11	VDD3
K12	VSS
K13	VSS
K14	VDD1
K19	HVDD
K20	P9
K21	P11
K22	P8
K23	P12
L1	MA0
L2	BA0
L3	BA1
L4	MA1
L5	VSS
L10	VDD3
L11	VDD3
L12	VSS
L13	VSS
L14	VDD1
L19	VSS
L20	P13
L21	P15
L22	HREF
L23	P14
M1	VDD2
M2	MA6
M3	MA3
M4	MA2
M5	VDD2
M10	VDD3
M11	VDD2

Ball	Function
M12	VSS
M13	VSS
M14	VDD1
M19	VPVDD
M20	BLANK
M21	PALCLK
M22	P10
M23	RS5
N1	VDD3
N2	MA7
N3	MA5
N4	RS1
N5	VSS
N10	VDD2
N11	VDD2
N12	VSS
N13	VSS
N14	VDD1
N19	VSS
N20	EXCKEN
N21	~PDOWN
N22	MCKIN
N23	VREF
P1	SDCK
P2	~SDCK
P3	MA9
P4	MA4
P5	VDD3
P10	VDD2
P11	VDD2
P12	VSS
P13	VSS
P14	VDD1
P19	VDD2
P20	CRTHSYNC
P21	CRTVSYNC
P22	~CLKRUN
P23	ACON
R1	~DQM7
R2	~DQM5
R3	~DQM4
R4	MA10
R5	VSS
R19	VSS
R20	USR3
R21	USR2
R22	USR1
R23	USR0
T1	MD41
T2	MD40
T3	MD55
T4	~DQM6

Ball	Function
T5	VDD2
T19	VDD1
T20	RS6
T21	TEST0
T22	TEST1
T23	CKIN
U1	MD43
U2	MD42
U3	MD54
U4	MD53
U5	VSS
U19	VSS
U20	TVSS1
U21	CVDD
U22	CVSS
U23	IREF2
V1	MD45
V2	MD44
V3	MD52
V4	MD51
V5	VDD3
V19	VDD1
V20	TVDD
V21	Y
V22	C
V23	CVBS
W1	MD47
W2	MD46
W3	MD50
W4	MD49
W5	VSS
W6	VDD2
W7	RS4
W8	FPVDD
W9	VSS
W10	FPVDD
W11	VSS
W12	FPVDD
W13	LVDD2
W14	LVSS2
W15	PLLVDD
W16	PLLVSS
W17	LVSS1
W18	LVDD1
W19	VSS
W20	TVSS2
W21	AVDD
W22	AVSS2
W23	RED
Y1	MD56
Y2	MD57
Y3	MD38

Ball	Function
Y4	MD39
Y5	VDD3
Y6	MD48
Y7	~ROM
Y8	FPDE
Y9	FPSCLK
Y10	FPVSYNC
Y11	FD11
Y12	FD14
Y13	FD15
Y14	FD19
Y15	TX7-
Y16	TXCLK2+
Y17	TX6-
Y18	TX5-
Y19	TX1-
Y20	TX2-
Y21	RS0
Y22	IREF
Y23	GREEN
AA1	MD58
AA2	MD59
AA3	MD60
AA4	MD35
AA5	MD36
AA6	MD37
AA7	FD2
AA8	FD7
AA9	FPHSYNC
AA10	FPVDDEN1
AA11	FD8
AA12	FD12
AA13	FD16
AA14	FD18
AA15	TX7+
AA16	TXCLK2-
AA17	TX6+
AA18	TX5+
AA19	TX1+
AA20	TX2+
AA21	AVSS
AA22	AVSS1
AA23	BLUE
AB1	VDD2
AB2	VDD3
AB3	MD61
AB4	MD32
AB5	MD33
AB6	MD34
AB7	FD1
AB8	FD4
AB9	FD6

Ball	Function
AB10	FPVBIASEN1
AB11	FD9
AB12	FD13
AB13	FD17
AB14	FD22
AB15	FPVDDEN2
AB16	FPEN2
AB17	TX4-
AB18	TX0-
AB19	TXCLK1+
AB20	TX3-
AB21	SPNLCKI
AB22	VDD1
AB23	RS3
AC1	VSS
AC2	VDD2
AC3	MD62
AC4	MD63
AC5	DSQ1
AC6	FPEN1
AC7	FD0
AC8	FD3
AC9	FD5
AC10	FD10
AC11	VDD2
AC12	VDD1
AC13	FD20
AC14	FD21
AC15	FPVBIASEN2
AC16	FD23
AC17	TX4+
AC18	TX0+
AC19	TXCLK1-
AC20	TX3+
AC21	SPNLCKO
AC22	VDD1
AC23	VSS

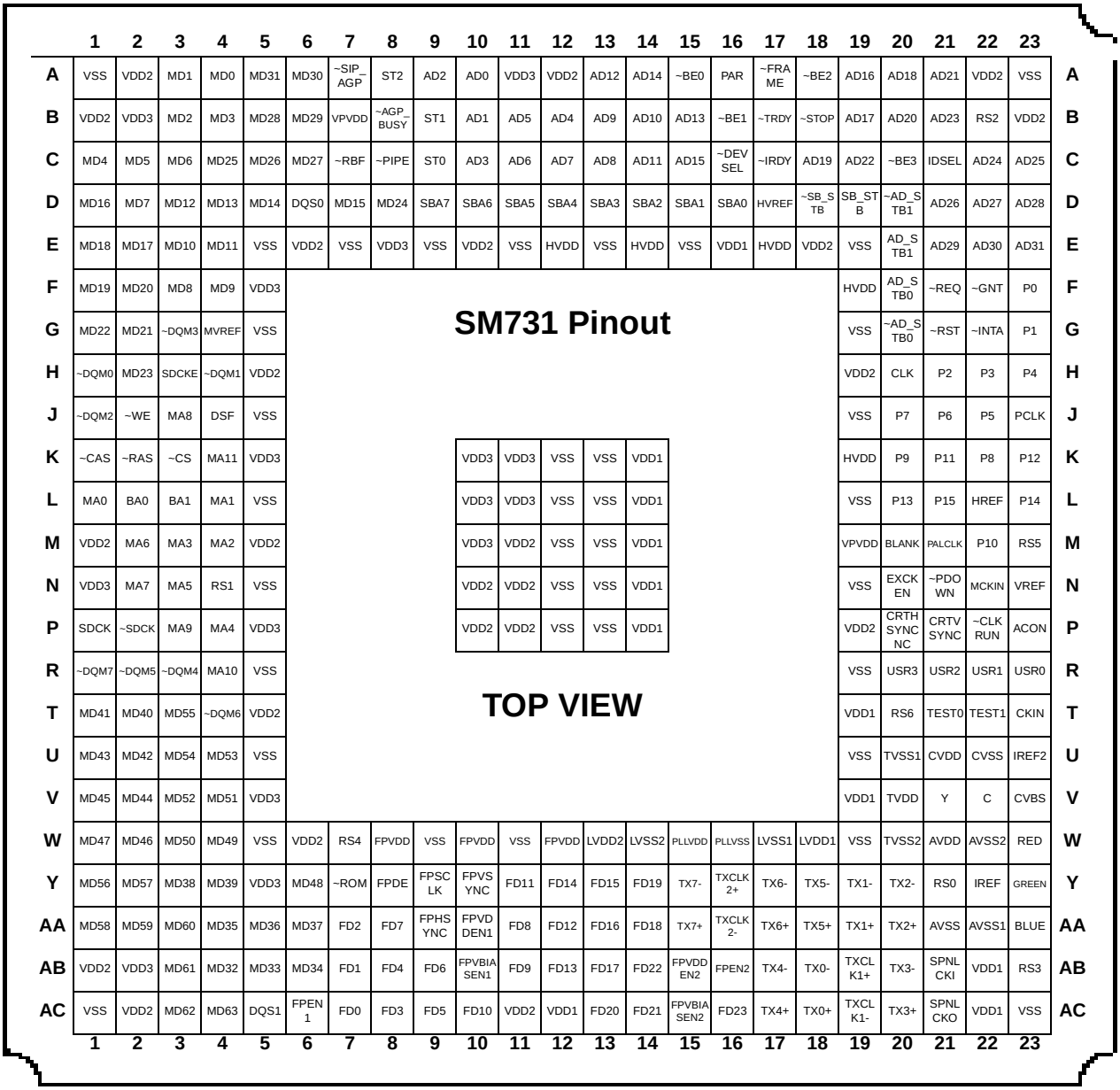
Table 3: Signal Descriptions

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
Host Interface (PCI or AGP)					
AD [31:0]	I/O		TBD	120	Multiplexed Address and Data Bus. A bus transaction consists of an address cycle followed by one or more data cycles.
~BE [3:0]	I/O		TBD	120	Bus Command and Byte Enables. These signals carry the bus command during the address cycle and byte enable during data cycles.
PAR	I/O		TBD	120	Parity. SM731 asserts this signal to verify even parity across AD [31:0] and C/~BE [3:0].
~FRAME	I/O		TBD	120	Cycle Frame. SM731 asserts this signal to indicate the beginning and duration of a bus transaction. It is de-asserted during the final data cycle of a bus transaction.
~TRDY	I/O		TBD	120	Target Ready. A bus data cycle is completed when both ~IRDY and ~TRDY are asserted on the same cycle.
~IRDY	I/O		TBD	120	Initiator Ready. A bus data cycle is completed when both ~IRDY and ~TRDY are asserted on the same cycle.
~STOP	I/O		TBD	120	Stop. SM731 asserts this signal to indicate that the current target is requesting the master to stop current transaction.
~DEVSEL	I/O		TBD	120	Device Select. SM731 asserts this signal when it decodes its addresses as the target of the current transaction.
IDSEL	I				ID Select. This input is used during PCI configuration read/write cycles.
CLK	I				System Clock, 33MHz. for PCI and 66MHz for AGP
~RST	I				System Reset. SM731 asserts this signal to force registers and state machines to initial default values
~REQ	O		TBD	120	Bus Request (bus master mode)
~GNT	I				Bus Grant (bus master mode)
~INTA	O		TBD	120	Interrupt
~PIPE	O		TBD	120	Pipe signal. Initiates pipelined AGP request. Signal indicates beginning and duration of pipelined AGP access.
~RBF	O		TBD	120	Read Buffer Full. Indicates if graphics device can accept previously low priority read data
AD_STB[1:0]	I/O		TBD	120	Address Strobes for AGP 2X, 4X transfer support
~AD_STB[1:0]	I/O		TBD	120	Inverted Address Strobes 1, 0
ST[2:0]	I				Status bus for AGP support
SBA[7:0]	O		TBD	120	Sideband address bits 7-0
SB_STB	O		TBD	120	Sideband strobe
~SB_STB	O		TBD	120	inverted sideband strobe
~AGP_BUSY	O		TBD	120	Power management signal for AGP bus.
~STP_AGP	I				Power management signal for AGP bus.
HVREF	I				Host Bus Voltage reference (AGP Bus Voltage)

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
Power Down Interface					
~PDOWN	I	pull-up			Deep power down mode enable. When PDOWN = 0 • All PLLs are shut down • All AGP/PCI pads except CLK and RST pads are power down When in deep power down mode SM731 will not respond to any host bus cycle • PDOWN = 1 (default) is the normal setting
~CLKRUN/ ACTIVITY	O	pull-up	TBD	60	~CLKRUN or SM731 Memory and I/O activity detection depending on SCR18 [7] 0 = select ~CLKRUN 1 = select ACTIVITY
ACON	I	pull-up			1 = AC power supply is connected
Clock Interface					
PALCLK	I	pull-up			27MHz clock source for PAL TV
CKIN	I	pull-up			14.318MHz clock (~EXCKEN = 1) or Video Clock (~EXCKEN = 0)
MCKIN/ TMDSCLK	I/O	pull-up	TBD	60	Memory Clock In (~EXCKEN = 0) or TMDSCLK Out (~EXCKEN = 1). TMDSCLK is a free running clock which can be used to drive a TMDS transmitter for DVI interface implementation. Note: this pin is used as a secondary clock source for dual panel configuration. For this case configure as TMDSCLK.
~EXCKEN	I	pull-up		60	External Clock Enable. Select external VCLK from CKIN and MCLK from MCKIN.
SPNLCLKO	O		TBD	20	Vrclk PLL clock out used as input to optional, external Spread Spectrum inducer IC.
SPNLCLKI	I	pull-down			Vrclk clock tree input, connected to optional, external Spread Spectrum inducer IC.
Flat Panel Interface					
FDATA [23:0]	O	pull-down	TBD	50	Flat Panel Data Bits 23 to 0 for direct connection to 18 or 24 bbp panel or to external TMDS transceiver. These lines can be programmed to convey information from the Panel Controller (primary display source) or the CRT controller (secondary display source). Single Pixel per clock mode support only. FDATA[23:22], FDATA[14:15] and FDATA[6:7] are driven low if panel type is set to 18 bpp.
FPHSYNC	O	pull-down	TBD	50	Horizontal Sync signal from Panel Controller (primary display source) or CRT Controller (secondary source).
FPVSYNC	O	pull-down	TBD	50	Vertical Sync signal from Panel Controller (primary display source) or CRT Controller (secondary source).
FPDE	O	pull-down	TBD	50	Display Enable signal from Panel Controller (primary display source) or CRT Controller (secondary source). This signal is used to indicate the active horizontal display time.
FPSCLK	O	pull-down	TBD	50	Flat Panel Shift Clock. This is the pixel clock for Flat Panel Data.

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
FPEN2	O	pull-down	TBD	20	Flat Panel Enable. This signal needs to become active after all panel voltages, clocks, and data are stable. This signal also needs to become inactive before any panel voltages or control signals are removed. FPEN is part of the VESA FPDI-1B specification. Panel Controller or CRT Controller can be timing source.
FPVDDEN2	O	pull-down	TBD	20	Flat Panel VDD Enable. This signal is used to control LCD Panel power. Panel Controller or CRT Controller can be timing source.
FPVBIASEN2	O	pull-down	TBD	20	Flat Panel Voltage Bias Enable. This signal is used to control LCD Bias power. Panel Controller or CRT Controller can be timing source.
LVDS1 Interface					
TX[3:0]+, TX[3:0]-	O				LVDS1 transmitter encoded data differential pairs. Data source is always from Panel Controller (primary display).
TXCLK1+, TXCLK1-	O				LVDS1 transmitter encoded clock differential pair. Source is always Virtual_Clock, from Panel Controller (primary display).
FPEN1	O				Flat Panel Enable. This signal needs to become active after all panel voltages, clocks, and data are stable. This signal also needs to become inactive before any panel voltages or control signals are removed. Timing source is always from Panel Controller
FPVDDEN1	O				Flat Panel VDD Enable. This signal is used to control LCD Panel power. Timing source is always from Panel Controller.
FPVBIASEN1	O				Flat Panel Voltage Bias Enable. This signal is used to control LCD Bias power. Timing source is always from Panel Controller.
LVDS2 Interface					
TX[7:4]+, TX[7:4]-	O				LVDS2 transmitter encoded data differential pairs. Data source Panel Controller (primary display) or CRT Controller (secondary display).
TXCLK2+, TXCLK2-	O				LVDS2 transmitter encoded clock differential pair. Source is Virtual_Clock, from Panel Controller (primary display) or Video Clock, from CRT Controller (secondary display).
CRT Interface					
RED	O				Analog Red Current Output
GREEN	O				Analog Green Current Output
BLUE	O				Analog Blue Current Output
IREF	I				Current Reference Input
CRTVSYNC	O	pull-down	TBD	50	CRT Vertical Sync
CRTHSYNC	O	pull-down	TBD	50	CRT Horizontal Sync
TV Interface					
Y	O				Luminance Output
C	O				Chrominance Output
CVBS	O				Composite Video Output

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
IREF2	I				Current Reference Input
Video Port Interface					
P [15:0]	I/O	pull-down	TBD	20	RGB or YUV input/ RGB digital output
PCLK	I/O	pull-up	TBD	20	Pixel Clock
VREF	I/O	pull-up	TBD	20	VSYNC input from PC Card or video decoder
HREF	I/O	pull-up	TBD	20	HSYNC input from PC Card or video decoder
BLANK	O	pull-up	TBD	20	Blank output 0 = BLANK output
General Purpose Registers / I²C					
USR3	I/O	pull-up	TBD	20	General Purpose I/O
USR2	I/O	pull-up	TBD	20	General Purpose I/O
USR1 / SDA	I/O	pull-up	TBD	20	General Purpose I/O. USR1/ DDC2/ I²C Data for CRT. Can be used to select different test modes.
USR0 / SCL	I/O	pull-up	TBD	20	General Purpose I/O. USR0/ DDC2/ I²C Clock for CRT. Can be used to select different test modes.
Test Mode Pins					
TEST [1:0]	I	pull-down			Test mode selects
Reserved					
RS[6:0]					Reserved - Do not connect



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	VSS	VDD2	MD1	MD0	MD31	MD30	~SIP_AGP	ST2	AD2	AD0	VDD3	VDD2	AD12	AD14	~BE0	PAR	~FRAME	~BE2	AD16	AD18	AD21	VDD2	VSS	A
B	VDD2	VDD3	MD2	MD3	MD28	MD29	VPVDD	~AGP_BUSY	ST1	AD1	AD5	AD4	AD9	AD10	AD13	~BE1	~TRDY	~STOP	AD17	AD20	AD23	RS2	VDD2	B
C	MD4	MD5	MD6	MD25	MD26	MD27	~RBF	~PIPE	ST0	AD3	AD6	AD7	AD8	AD11	AD15	~DEVSEL	~IRDY	AD19	AD22	~BE3	IDSEL	AD24	AD25	C
D	MD16	MD7	MD12	MD13	MD14	DQS0	MD15	MD24	SBA7	SBA6	SBA5	SBA4	SBA3	SBA2	SBA1	SBA0	HVREF	~SB_STB	SB_STB	~AD_STB1	AD26	AD27	AD28	D
E	MD18	MD17	MD10	MD11	VSS	VDD2	VSS	VDD3	VSS	VDD2	VSS	HVDD	VSS	HVDD	VSS	VDD1	HVDD	VDD2	VSS	AD_STB1	AD29	AD30	AD31	E
F	MD19	MD20	MD8	MD9	VDD3														HVDD	AD_STB0	~REQ	~GNT	P0	F
G	MD22	MD21	~DQM3	MVREF	VSS														VSS	~AD_STB0	~RST	~INTA	P1	G
H	~DQM0	MD23	SDCKE	~DQM1	VDD2														VDD2	CLK	P2	P3	P4	H
J	~DQM2	~WE	MA8	DSF	VSS														VSS	P7	P6	P5	PCLK	J
K	~CAS	~RAS	~CS	MA11	VDD3					VDD3	VDD3	VSS	VSS	VDD1					HVDD	P9	P11	P8	P12	K
L	MA0	BA0	BA1	MA1	VSS					VDD3	VDD3	VSS	VSS	VDD1					VSS	P13	P15	HREF	P14	L
M	VDD2	MA6	MA3	MA2	VDD2					VDD3	VDD2	VSS	VSS	VDD1					VPVDD	BLANK	PALCLK	P10	RS5	M
N	VDD3	MA7	MA5	RS1	VSS					VDD2	VDD2	VSS	VSS	VDD1					VSS	EXCKEN	~PDOWN	MCKIN	VREF	N
P	SDCK	~SDCK	MA9	MA4	VDD3					VDD2	VDD2	VSS	VSS	VDD1					VDD2	CRTHSYNCNC	CRTVSYNC	~CLKRUN	ACON	P
R	~DQM7	~DQM5	~DQM4	MA10	VSS														VSS	USR3	USR2	USR1	USR0	R
T	MD41	MD40	MD55	~DQM6	VDD2														VDD1	RS6	TEST0	TEST1	CKIN	T
U	MD43	MD42	MD54	MD53	VSS														VSS	TVSS1	CVDD	CVSS	IREF2	U
V	MD45	MD44	MD52	MD51	VDD3														VDD1	TVDD	Y	C	CVBS	V
W	MD47	MD46	MD50	MD49	VSS	VDD2	RS4	FPVDD	VSS	FPVDD	VSS	FPVDD	LVDD2	LVSS2	PLLVDD	PLLVSS	LVSS1	LVDD1	VSS	TVSS2	AVDD	AVSS2	RED	W
Y	MD56	MD57	MD38	MD39	VDD3	MD48	~ROM	FPDE	FPSCLK	FPVSYNC	FD11	FD14	FD15	FD19	TX7-	TXCLK2+	TX6-	TX5-	TX1-	TX2-	RS0	IREF	GREEN	Y
AA	MD58	MD59	MD60	MD35	MD36	MD37	FD2	FD7	FPHSYNC	FPVDDEN1	FD8	FD12	FD16	FD18	TX7+	TXCLK2-	TX6+	TX5+	TX1+	TX2+	AVSS	AVSS1	BLUE	AA
AB	VDD2	VDD3	MD61	MD32	MD33	MD34	FD1	FD4	FD6	FPVBIASEN1	FD9	FD13	FD17	FD22	FPVDDEN2	FPEN2	TX4-	TX0-	TXCLK1+	TX3-	SPNLCKI	VDD1	RS3	AB
AC	VSS	VDD2	MD62	MD63	DQS1	FPEN1	FD0	FD3	FD5	FD10	VDD2	VDD1	FD20	FD21	FPVBIASEN2	FD23	TX4+	TX0+	TXCLK1-	TX3+	SPNLCKO	VDD1	VSS	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Figure 4: SM731 Pin Diagram for 385 BGA Package

Table 4: SM731 VCC and GROUND Connections

VCC Pin	Location	Supply Voltage	Description
AVDD	W21	3.3V	CRT DAC analog power
CVDD	U21	2.5V	Clock PLL analog power
FPVDD	W8, W10, W12	3.3V	Flat panel interface VDD
HVDD	E12,E14,E17,F19,K19	3.3V/1.5V for AGP4x	Host interface VDD
LVDD1	W18	2.5V	LVDS core VDD
LVDD2	W13	2.5V	LVDS core VDD
PLLVDD	W15	2.5V	LVDS PLL analog power
TVDD	V20	3.3V	TV DAC power
VPVDD	M19, B7	3.3V	ZV port interface VDD and 3.3 AGP Pad VDD
VDD1	E16, K14, L14, M14, N14, P14, T19, V19, AB22, AC12, AC22	2.5V	Core VDD
VDD2	A2, A12, A22, B1, B23, E6, E10, E18, H5, H19, M1, M5, M11, N10, N11, P10, P11, P19, T5, W6, AB1, AC2, AC11	2.5V/3.3V*	Memory I/O power
VDD3	A11, B2, E8, F5, K5, K10, K11, L10, L11, M10, N1, P5, V5, Y5, AB2	2.5V/3.3V*	Memory core power
GND Pin	**Location**	**Supply Voltage**	**Description**
GROUND			
AVSS	AA21		DAC analog ground
AVSS1	AA22		DAC analog ground
AVSS2	W22		DAC analog ground
CVSS	U22		Clock PLL analog ground
LVSS1	W17		LVDS core ground
LVSS2	W14		LVDS core ground
PLLVSS	W16		LVDS PLL analog ground
TVSS1	U20		TV DAC Ground
TVSS2	W20		TV DAC Ground
VSS	A1, A23, E5, E7, E9, E11, E13, E15, E19, G5, G19, J5, J19, K12, K13, L5, L12, L13, L19, M12, M13, N5, N12, N13, N19, P12, P13, R5, R19, U5, U19, W5, W9, W11, W19, AC1, AC23		Digital Ground

SM731 NAND Tree Scan Testing

The SM731 NAND Tree scan test circuit is designed for verifying the device being properly soldered to the board (NAND support for SM721 only). It detects opened/shorted traces of a signal pin with a simple test pattern which, for this particular case, only ~243 vectors in length. Since the NAND Tree scan test circuit uses Combination logic; therefore, no clock pulses are required during the testing.

General Information

The SM731 NAND Tree scan test circuit is a long chain of 2-input NAND gates. The first pin of the NAND chain is an input (signal pin "~ROMEN"), the last pin of the chain is an output (signal pin "BLANK"). In order to setup SM731 for NAND Tree testing, USR[3:0] pins are programmed to 0010h and Test[1:0] pins to 10h. ALL VDD's, VSS's, and Analog pins RED, GREEN, BLUE, IREF, C, Y, CVBS, IREF2 are not included in the scan chain.

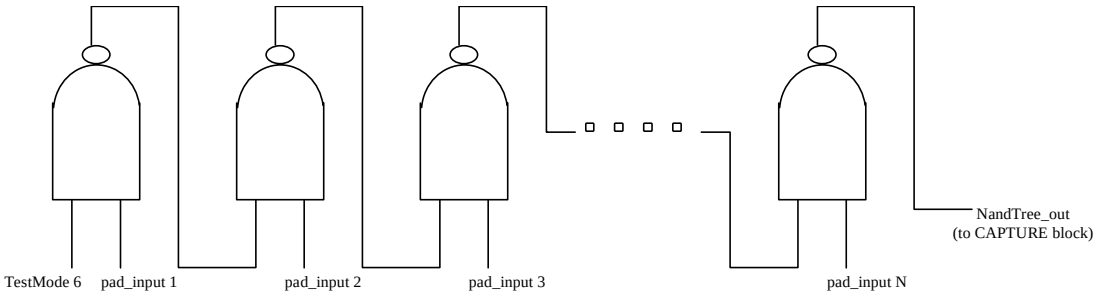


Figure 5: NAND Tree Connection

NAND Tree Simulation

In order to setup SM731 to NAND Tree scan test mode, USR[3:0] and Test[1:0] pins are programmed to 0010h and 10h respectively. In NAND Tree mode, internal signal TestMode6 is a "1" (active "High" signal). In the beginning of the simulation, all inputs are forced to "1". Then, follow the NAND Tree PAD sequence and change each input to "0" every 400ns, starting with input_0 (signal "~ROMEN"). The Output pin (signal "BLANK") should be a clock waveform that toggles every 400ns (a 2.5MHz square waveform) (See Figure 6). Any mismatch in the waveform would mean the device was not properly soldered to the board.

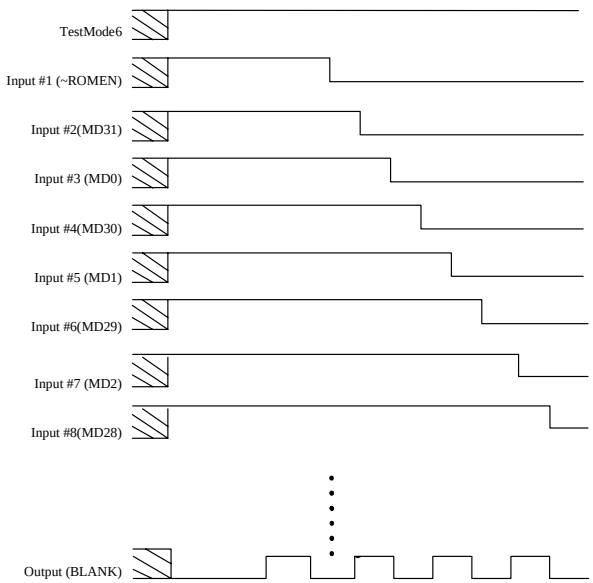


Figure 6: NAND Tree Simulation Timing Diagram

Table 5: NAND Tree Scan Test Order

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
1	STOPAGP	In
2	RBFN	In
3	AGPBUSYN	In
4	PIPEN	In
5	ST0	In
6	ST1	In
7	ST2	In
8	SBA_[7]	In
9	SBA_[6]	In
10	SBA_[5]	In
11	SBA_[4]	In
12	SBA_[3]	In
13	SBA_[2]	In
14	SBA_[1]	In
15	SBA_[0]	In
16	PCIAD_[0]	In
17	PCIAD_[1]	In
18	PCIAD_[2]	In
19	PCIAD_[3]	In
20	PCIAD_[4]	In
21	PCIAD_[5]	In
22	PCIAD_[6]	In
23	PCIAD_[7]	In
24	PCIAD_[8]	In
25	PCIAD_[9]	In
26	PCIAD_[10]	In
27	PCIAD_[11]	In
28	PCIAD_[12]	In
29	PCIAD_[13]	In
30	PCIAD_[14]	In
31	PCIAD_[15]	In
32	CBE_[3]	In
33	CBE_[2]	In
34	CBE_[1]	In
35	CBE_[0]	In
36	DEVSEL	In
37	IRDYN	In
38	TRDYN	In
39	PCIPAR	In
40	STOPN	In
41	FRAMEN	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
42	PCICLK	In
43	ADSTBN_1	In
44	ADSTB_1	In
45	ADSTBN_0	In
46	ADSTB_1	In
47	SBSTBN	In
48	SBSTB	In
49	IDSEL	In
50	PCIAD_16	In
51	PCIAD_17	In
52	PCIAD_18	In
53	PCIAD_19	In
54	PCIAD_20	In
55	PCIAD_21	In
56	PCIAD_22	In
57	PCIAD_23	In
58	PCIAD_24	In
59	PCIAD_25	In
60	PCIAD_26	In
61	PCIAD_27	In
62	PCIAD_28	In
63	PCIAD_29	In
64	PCIAD_30	In
65	PCIAD_31	In
66	PCIREQN	In
67	PCIGNTN	In
68	PCIRSTN	In
69	INTAN	In
70	ACTIVITY	In
71	VPDATA_0	In
72	VPDATA_1	In
73	VPDATA_2	In
74	VPDATA_3	In
75	VPDATA_4	In
76	VPDATA_5	In
77	VPDATA_6	In
78	VPDATA_7	In
79	VPDATA_8	In
80	VPDATA_9	In
81	VPDATA_10	In
82	VPDATA_11	In
83	VPDATA_12	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
84	VPDATA_13	In
85	VPDATA_14	In
86	VPDATA_15	In
87	VPHSYNC	In
88	VPVSYNC	In
89	VPCLK	In
90	PALCLK	In
91	XMCK	In
92	ACON	In
93	ENXCLK	In
94	CRTHSYNC	In
95	CRTVSYNC	In
96	SPNLCKI	In
97	SPNLCK0	In
98	XVCK	In
99	VBIASEN2	In
100	FPVDDEN2	In
101	FPEN2	In
102	FPDATA_23	In
103	FPDATA_22	In
104	FPDATA_21	In
105	FPDATA_20	In
106	FPDATA_19	In
107	FPDATA_18	In
108	FPDATA_17	In
109	FPDATA_16	In
110	FPDATA_15	In
111	FPDATA_14	In
112	FPDATA_13	In
113	FPDATA_12	In
114	VBIASEN	In
115	FPVDDEN	In
116	FPEN	In
117	FPDE	In
118	FPSCLK	In
119	FPVSYNC	In
120	FPHSYNC	In
121	FPDATA_11	In
122	FPDATA_10	In
123	FPDATA_9	In
124	FPDATA_8	In
125	FPDATA_7	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
126	FPDATA_6	In
127	FPDATA_5	In
128	FPDATA_4	In
129	FPDATA_3	In
130	FPDATA_2	In
131	FPDATA_1	In
132	FPDATA_0	In
133	MEMROM	In
134	EXTMEMDATA_63	In
135	EXTMEMDATA_62	In
136	EXTMEMDATA_61	In
137	EXTMEMDATA_60	In
138	EXTMEMDATA_59	In
139	EXTMEMDATA_58	In
140	EXTMEMDATA_57	In
141	EXTMEMDATA_56	In
142	EXTMEMDATA_55	In
143	EXTMEMDATA_54	In
144	EXTMEMDATA_53	In
145	EXTMEMDATA_52	In
146	EXTMEMDATA_51	In
147	EXTMEMDATA_50	In
148	EXTMEMDATA_49	In
149	EXTMEMDATA_48	In
150	EXTMEMDQS1	In
151	EXTMEMDATA_47	In
152	EXTMEMDATA_46	In
153	EXTMEMDATA_45	In
154	EXTMEMDATA_44	In
155	EXTMEMDATA_43	In
156	EXTMEMDATA_42	In
157	EXTMEMDATA_41	In
158	EXTMEMDATA_40	In
159	EXTMEMDATA_39	In
160	EXTMEMDATA_38	In
161	EXTMEMDATA_37	In
162	EXTMEMDATA_36	In
163	EXTMEMDATA_35	In
164	EXTMEMDATA_34	In
165	EXTMEMDATA_33	In
166	EXTMEMDATA_32	In
167	EXTMEMDQM_7	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
168	EXTMEMDQM_6	In
169	EXTMEMDQM_5	In
170	EXTMEMDQM_4	In
171	EXTMEMDSF	In
172	EXTMEMWEN	In
173	EXTMEMCASN	In
174	EXTMEMRASN	In
175	EXTMEMCSN	In
176	EXTMEMCKE	In
177	EXTMEMBA_1	In
178	EXTMEMBA_0	In
179	EXTMEMSCLKN	In
180	EXTMEMSCKP	In
181	EXTMEMMA_11	In
182	EXTMEMMA_10	In
183	EXTMEMMA_9	In
184	EXTMEMMA_8	In
185	EXTMEMMA_7	In
186	EXTMEMMA_6	In
187	EXTMEMMA_5	In
188	EXTMEMMA_4	In
189	EXTMEMMA_3	In
190	EXTMEMMA_2	In
191	EXTMEMMA_1	In
192	EXTMEMMA_0	In
193	EXTMEMDQM_3	In
194	EXTMEMDQM_2	In
195	EXTMEMDQM_1	In
196	EXTMEMDQM_0	In
197	EXTMEMDATA_31	In
198	EXTMEMDATA_30	In
199	EXTMEMDATA_29	In
200	EXTMEMDATA_28	In
201	EXTMEMDATA_27	In
202	EXTMEMDATA_26	In
203	EXTMEMDATA_25	In
204	EXTMEMDATA_24	In
205	EXTMEMDATA_23	In
206	EXTMEMDATA_22	In
207	EXTMEMDATA_21	In
208	EXTMEMDATA_20	In
209	EXTMEMDATA_19	In

NAND TREE SCAN PIN ORDER#	Pin Name	In/Out
210	EXTMEMDATA_18	In
211	EXTMEMDATA_17	In
212	EXTMEMDATA_16	In
213	EXTMEMDQS_0	In
214	EXTMEMDATA_15	In
215	EXTMEMDATA_14	In
216	EXTMEMDATA_13	In
217	EXTMEMDATA_12	In
218	EXTMEMDATA_11	In
219	EXTMEMDATA_10	In
220	EXTMEMDATA_9	In
221	EXTMEMDATA_8	In
222	EXTMEMDATA_7	In
223	EXTMEMDATA_6	In
224	EXTMEMDATA_5	In
225	EXTMEMDATA_4	In
226	EXTMEMDATA_3	In
227	EXTMEMDATA_2	In
228	EXTMEMDATA_1	In
229	EXTMEMDATA_0	In

Chapter 5: Display Memory Interface

Memory Configuration

The SM731 memory interface is 64-bits wide and is clocked at 150 MHz, for a total bandwidth of 1.2GB/s peak. The SM731 supports both single and double data rate SGRAM.

Page Break Look Ahead

For standard architectures, the memory controller will break cycle when bus agent changes. SM731 can allow a "No Wait Cycle" during agent changes if the preceding and current agents are in the same page.

Memory Timing Control

Memory timing control is configured via MD [7:0] and MD [31:24] during power-on reset. They should always be set the same. See Reference Table 20 in the Initialization section for a complete description of these memory configuration bits.

Note: MD[32-0] has pull-up resistors on I/O pads. The default configuration is therefore a logical "1" during power-on reset. To set an MD line to 0, an external pull-down resistor needs to be added. After power-on initialization, software can be used to overwrite the initial setting by writing to MCR62 - bits [7:0] correspond to MD [7:0], and MCR76 - bits [7:0] correspond to MD [31:24].

Chapter 6: 2D Drawing Engine

SM731's 128-bit Drawing Engine is designed to accelerate Microsoft's DirectDraw and Direct3D applications. The engine contains a 3-operand ALU with 256 raster operations, source and destination FIFOs, as well as a host data FIFO. The drawing engine pipeline allows single cycle operations and runs at the memory clock speed.

SM731's Drawing Engine includes several key functions to achieve the high GUI performance. The device supports color expansion with packed mono font, color pattern fill, host BLT, stretch BLT, short stroke, line draw, and others. Dedicated pathways are designed to transfer data between host interface (HIF) bus and Drawing Engine, and memory interface (MIF) bus and Drawing Engine. In addition, the drawing engine supports rotation BIBLT for any block size. This feature allows conversion between landscape and portrait display without the need for special software drivers.

The Drawing Engine offers several 3D assist features. The Drawing Engine supports low-resolution modes and hardware arithmetic stretching to allow 3D to be rendered to a smaller back buffer and scaled up to the front buffer. SM731 also supports fast DMA BLT, source clear during BLT, transparent BLT, programmable blter stride, page flip, and alpha blending bitblt.

Chapter 7: Display Processors

SM731 has two fully independent Display Processors, which mix graphics data with up to two overlaid video windows. Each processor can output the combined image to a separate display device (LCDOUT, CRT or TV). By implementing two processors (or controllers), SM731 allows for Dual View/ DualMon implementations, where two independent display devices are used simultaneously, each one with its own timing, resolution and content.

The primary display processor, also referred to as the Panel Controller, is more complex than the secondary processor (referred to "Video processor" or CRT controller) because its back-end is specifically designed to drive LCD panels. It has built in controls and registers that are specific for those display devices. Section "Flat Panel Registers" details the registers for the primary display processor while section "CRT Controller registers" details the registers for the secondary display processor.

In order to accommodate a wider range of applications, some SM731 display interfaces can display data from either processor, according to the diagram below. The interface data path is controlled by register FPR100.

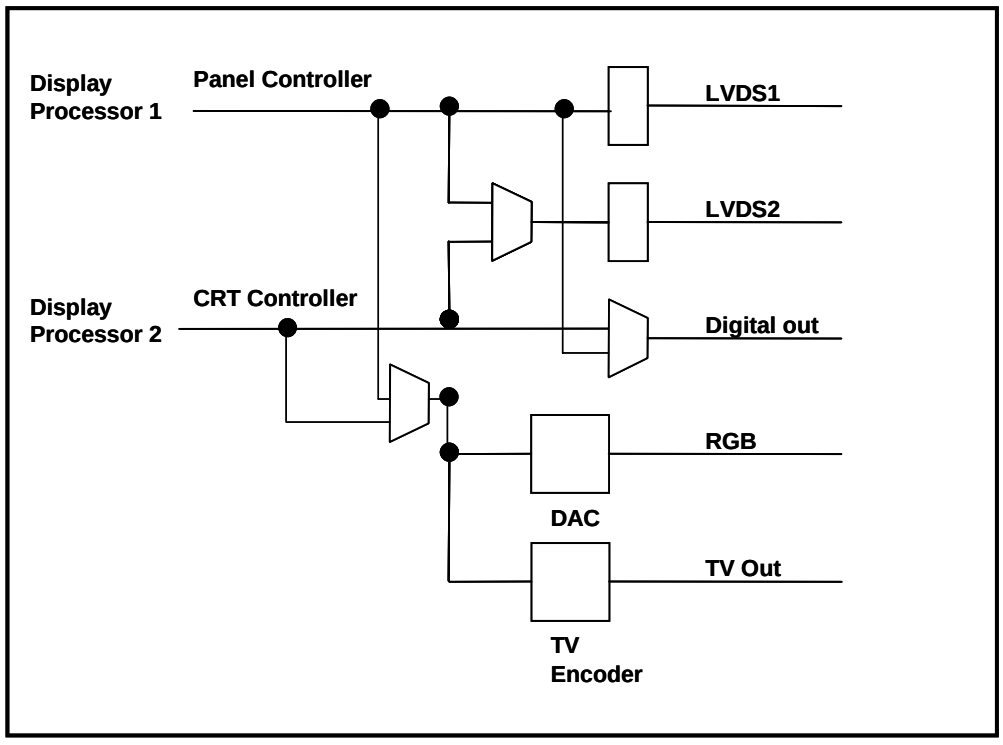


Figure 7: Display Data Source

Each display processor has it’s own LUT to support index mode as well as gamma correction. The size of the RAM list is 256x24. Each display processor also has it’s own hardware cursor (32x32) and pop icon generator.

Chapter 8: Zoom Video Port and Video Capture Unit

Zoom Video Port

SM731's Zoom Video Port (ZV Port) is designed to interface with video solutions implemented as PCMCIA (or PC CardBus) cards: examples are NTSC/PAL decoders, MPEG-2 decoders, and JPEG Codecs. The ZV Port can also directly interface with an NTSC/PAL decoder, such as Phillips 7111 or BT819. Figure 8 illustrates an example of the Phillips video encoder interface via the ZV Port.

Incoming video data from the ZV Port interface can be YUV or RGB format. The data can be interlaced or non-interlaced. The ZV Port can be configured for output if the video capture function is disabled. 18-bit graphics and video data in RGB format can be sent out when the ZV Port is configured for output mode.

The ZV Port may also be configured as a test port. Up to 20 signals from each of the logic blocks within SM731 can be brought out to an internal test bus (TD Bus) connected to the ZV Port. System designers or silicon validation engineers can access these signals by setting the TEST0, TEST1, USR0, USR1, and USR2 pins. This approach can bring out a total of 180 internal signals to the primary I/O pins. The test port capability can be used to enhance fault coverage, as well as reduce silicon validation or debugging time.

Table 6 lists signal definitions for the following ZV Port interface configurations: YUV input mode, RGB input mode, and graphics/video (output mode).

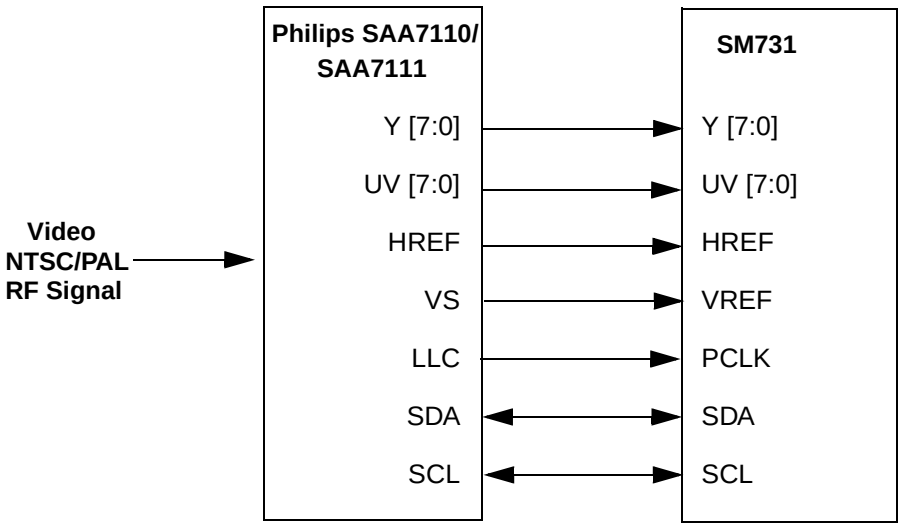


Figure 8: Video Encoder Interface via Video Port

Table 6: SM731 Video Port Interface I/O Compliance

Video Port Interface	ZV Port (Input mode)	I/O	NTSC/PAL Decoder (Input mode)	I/O	Graphics/Video (Output mode)	I/O
VREF	VS	I	VS	I	R7	O
HREF	HREF	I	HREF	I	R6	O
BLANK	(note1)		(note1)		BLANK	O
PCLK	PCLK	I	PCLK	I	PCLK	O
P15	UV7	I	R7	I	R5	O
P14	UV6	I	R6	I	R4	O
P13	UV5	I	R5	I	R3	O
P12	UV4	I	R4	I	R2	O
P11	UV3	I	R3	I	G7	O
P10	UV2	I	G7	I	G6	O
P9	UV1	I	G6	I	G5	O
P8	UV0	I	G5	I	G4	O
P7	Y7	I	G4	I	G3/Vindex_[7]	O
P6	Y6	I	G3	I	G2/Vindex_[6]	O
P5	Y5	I	G2	I	G7/Vindex_[5]	O
P4	Y4	I	B7	I	G6/Vindex_[4]	O
P3	Y3	I	B6	I	G5/Vindex_[3]	O
P2	Y2	I	B5	I	G4/Vindex_[2]	O
P1	Y1	I	B4	I	G3/Vindex_[1]	O
P0	Y0	I	B3	I	G2/Vindex_[0]	O

Note 1: BLANK pin can used as TVCLK output, which is independent of ZV port.
Note 2: Vindex [7:0] is indexed video out
Note 3: SMI test bus is for internal use only

Video Capture Unit

The Video Capture Unit captures incoming video data from the ZV Port and then stores the data into the frame buffer. The Video Capture Unit support several features to maintain display quality, and balance the capture rate:

- 2-tap, 3-tap, and 4-tap horizontal filtering
- 2 to 1 and 4 to 1 reduction for horizontal and vertical frame size
- YUV 4:2:2, YUV 4:2:2 with byte swap, RGB 5:5:5, and RGB 5:6:5
- Multiple frame skipping methods
- Interlaced data and non-interlaced data capture
- Single buffer and double buffer capture
- Cropping

SM731 uses the Video Processor block to display the captured data on the LCD, TV, or CRT display. The captured data can be displayed through Video Window I or Video Window II. The stretching, color interpolation, YUV-to-RGB conversion, and color key functions are performed in the Video Processor. SM731's Video Processor can simultaneously process captured video data and perform CD-ROM playback on two independent video windows.

SM731 also supports real-time video capture to the hard drive or system memory through PCI master mode or slave mode. In PCI bus master mode, SM731 uses the Drawing Engine's Host BLT and Host DMA functions to maximize performance.

Functional Description

SM731's Video Capture Unit supports the Video Port Extension (VPE) specification for video stream processing. This capture unit includes CLIP block, FILTER block, SHRINK block, and FIFO control block. Figure 9 and Figure 10 illustrate the SM731 Video Capture Block Diagram and Data Flow. The CLIP functional block is used to select the desired rectangles from the video stream to be captured. VPR40 register (Video Source Clipping Control) is used to define the upper left corner of the rectangle from the video source. VPR44 register (Video Source Capture Size Control) is used to define the height and width of the rectangle from the video source.

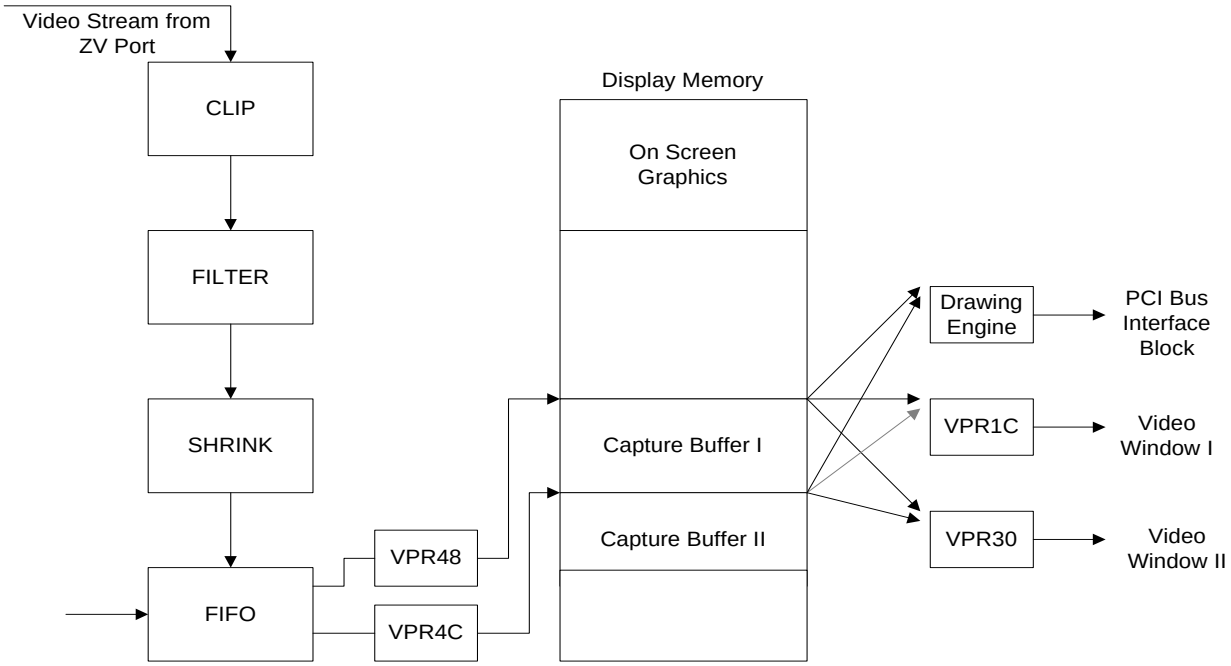


Figure 9: Video Capture Block Diagram

The FILTER functional block controls horizontal filtering logic. CPR00 (Capture Port Control) bit 21 and bit 20 are used to select 2 tap, 3 tap, and 4 tap filtering. The SHRINK functional block is used to not only reduce the storage area for both display memory and hard drive, but also increase performance of video capture and video playback. CPR00 bit 19 and 18 are used to enable vertical reduction, and bit 17 and bit 16 are used to enable horizontal reduction. With filter and shrink functions, SM731 is able to achieve high video capture performance and maintain optimal video playback quality.

CPR00 bit 13 to bit 11 are use to select 8 different frame skipping options in the event the capture rate is less than the incoming video stream. CPR00 bit 10 and bit 9 are used to support interlaced capture and double buffer capture. CPR00 bit 1 and bit 2 are used as control/status bits for Buffer I and Buffer II.

The captured data can be displayed on either Video Window I or Video Window II. The video capture driver needs to program VPR1C (or VPR30), Video Window I (or II) Source Start Address, with the same address value from Capture Port Buffer I or II Start Address register. VPR00 (Miscellaneous Graphics and Video Control) bit 24 may be used to automatically display the capture data on Video Window I without programming VPR1C register. This feature is independent of single buffer or double buffer mode.

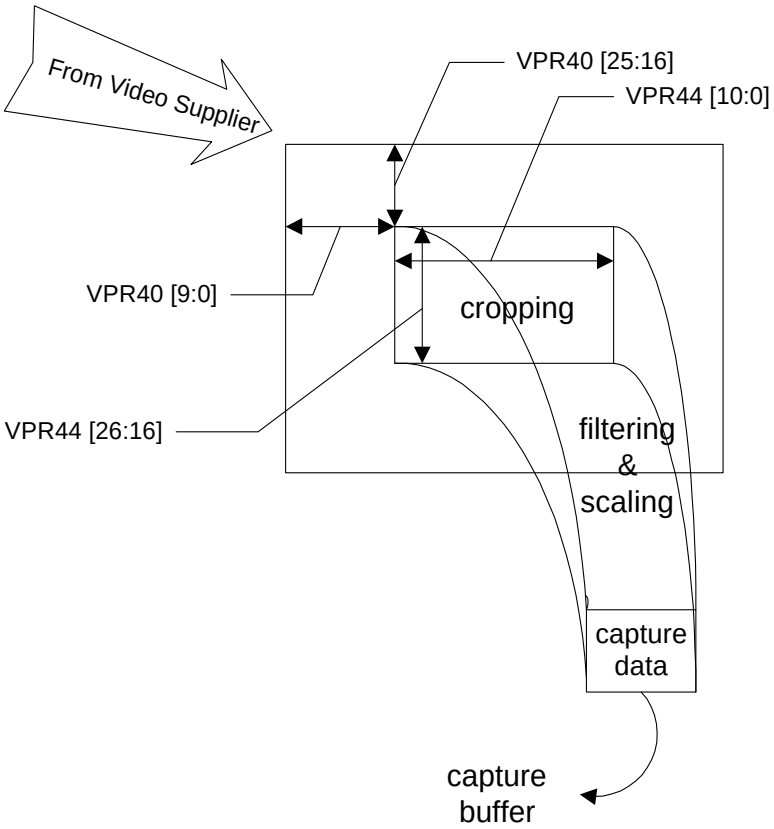


Figure 10: Video Capture Data Flow

Theory of Operation

Initialization

- Enable Video Capture (CPR00 bit 0 = 1)
- Preset Buffer I and Buffer II Status/Control bits (CPR00 [2:1] = 11b)
- Enable Drawing Engine (DPR0E bit 4 = 1)
- Select Host BLT Read Command function (DPR0E [3:0] =9h)
- Enable PCI bus master mode (SCR17 bit 6 = 1)
- Select Field Detection, VREF/HREF polarity, Vertical/Horizontal Reduction, Horizontal Filtering, Video Capture Input Data Format, Frame Skip, Interlaced/non-interlaced and other miscellaneous settings (CPR00, Capture Port Control Register)

Table 7: Bit Setting Summary for Video Capture

B1S	Buffer 1 Status/Control (CPR00 bit 1)
B2S	Buffer 2 Status/Control (CPR00 bit 2)
Continuous Capture	bit 8 = 0
Conditional Capture	bit 8 = 1
Single Buffer	bit 9 = 0
Double Buffer	bit 9 = 1
Non-interlaced Mode	bit 10 = 0
Interlaced Mode	bit 10 = 1

The Video Capture Unit supports the following types of capture modes:

- Single Buffer Mode with Continuous Capture
- Single Buffer Mode with Conditional Capture
- Double Buffer Mode with Continuous Capture
- Double Buffer Mode with Conditional Capture
- Interlace and Non-Interlaced Mode

A summary of each of the video capture modes follows:

- Single Buffer Mode with Continuous Capture

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
• Continuously capture incoming video data to capture buffer 1 • Independent of B1S and B2S bits	It is not recommended to use the Drawing Engine to transfer captured data from display memory to hard drive or system memory in this mode. This mode is used to view the captured data only.	• VPR00 bit 24 = 0 Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. • VPR00 bit 24 = 1 Captured data is automatically displayed on Video Window I.

- **Single Buffer Mode with Conditional Capture**

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
a) VCU monitors B1S bit b) If B1S = 1, start capture c) VCU will reset B1S to 0 after it completes a frame d) Go to step “a”	a) Test b) If B1S = 0, SW will activate the DE to transfer captured data from capture buffer 1 to hard drive or system memory c) DE will set B1S bit to 1 after it completes a frame d) Go to step "a”	• VPR00 bit 24 = 0 • Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. • VPR00 bit 24 = 1 • Captured data is automatically displayed on Video Window I

- Double Buffer Mode with Continuous Capture

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
• Continuously capture the incoming video data into capture buffer 1 or buffer 2 • Automatically switch from one buffer to the other when VCU completes a frame • Independent of B1S and B2S bits	It is not recommended to use DE to transfer captured data from display memory to hard drive or system memory in this mode. This mode is used to view the captured data only.	• VPR00 bit 24 = 0 Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. • VPR00 bit 24 = 1 Captured data is automatically displayed on Video Window I. If capture buffer 1 is used by VCU, Video Window I will display captured data from capture buffer 2

- Double Buffer Mode with Conditional Capture

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
a) VCU monitors B1S and B2S bits b) If B1S (or B2S) = 1, start video capture and store into capture buffer 1 (or buffer 2). c) VCU will reset B1S (or B2S) to 0 after it completes a frame d) VCU will continue video capture if B1S or B2S = 1 e) Go to step "a" if both bits = 0	a) SW monitors B1S or B2S bit b) If B1S (or B2S) = 0, SW will activate the DE to transfer captured data from capture buffer 1(or buffer 2) to hard drive or system memory c) DE will set B1S (or B2S) bit to 1 after it completes a frame d) DE will continuously transfer e) Data from capture buffer 1 or 2 if B1S or B2S = 0 f) Go to step "a " if both bits = 1	• VPR00 bit 24 = 0 Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. • VPR00 bit 24 = 1 Captured data is automatically displayed on Video Window I. If capture buffer 2 is used by VCU, Video Window I will display captured data from capture buffer 1.

- Interlaced Capture

CPR00 bits 10 are used to select the interlaced capture mode. In most of video capture applications, an interlaced video stream will be treated as non-interlaced video stream by dropping all even frames (CPR00[13:11] = 010b), or dropping all odd frames (CPR00[13:11] = 011). This approach will reduce artifacts when playing back the captured data. However, in some video capture applications, de-interlacing is needed to handle the incoming interlaced video stream.

For the de-interlacing case, CPR00 bit 10 needs to be set to 1 to enable interlaced capture for incoming interlaced video stream. The double buffer mode (CPR00 bit 9 = 1) needs to be turned on at the same time. Capture Buffer 1 and Capture Buffer 2 are combined together as a single buffer with one line offset. Figure 11 illustrates the capture buffer structure. The video capture driver will preset B1S and B2S bits to 1 to initialize the buffer 1 and 2 status/control bits. The Video Capture Unit will start video capture if any one of B1S and B2S = 1. After VCU fills capture buffer 1 and 2, both B1S and B2S bits are set to "0" by VCU. The video capture driver will activate Drawing Engine to transfer captured data in capture buffer 1 and 2 to system memory or hard drive when both B1S and B2S are "0". After the completion of the transfer, the Drawing Engine will set both B1S and B2S to "1". The Video Capture Unit then continues video capture and repeats the same protocol.

During video playback, the captured data can be displayed on either Video Window I or Video Window II. It is not recommended to display both even frame and odd frame for video playback. The video captured driver can program Video Window I (or II) Source Start Address Register and Video Window I (or II) Source Width and Offset Register in such a way that odd frame (or even frame) captured data will be dropped during video playback. The scaling, color interpolation, and YUV-to-RGB conversion functions can also be enabled at the same time.

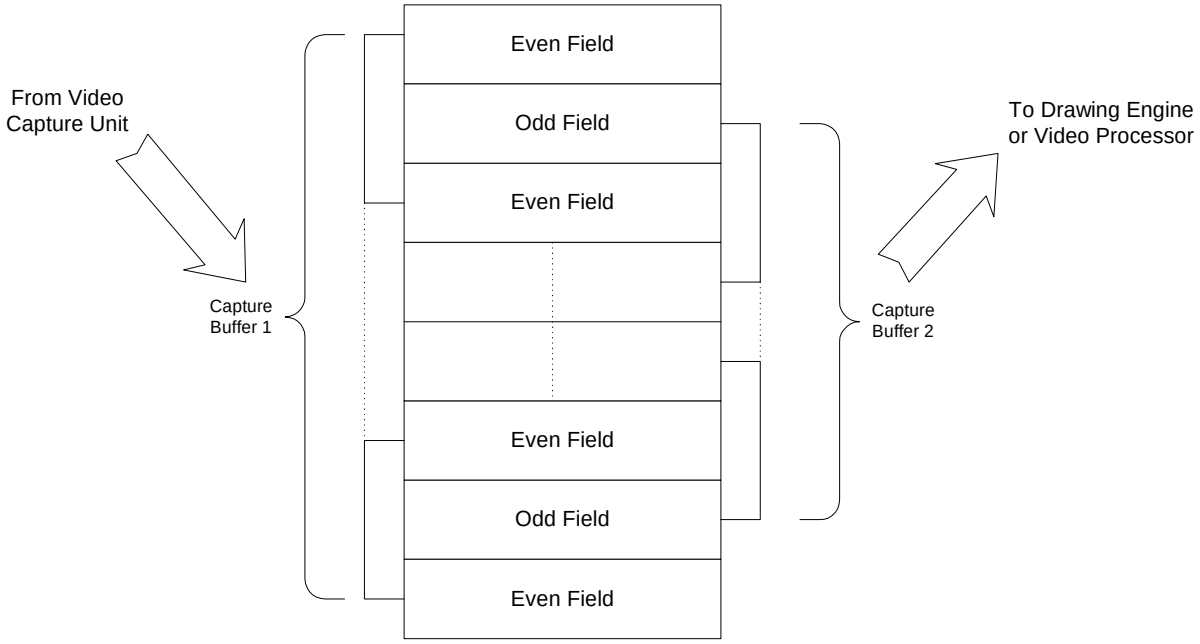


Figure 11: Capture Buffer Structure in Interlaced Mode

Chapter 9: Flat Panel Interface

The SM731 can directly drive LCD panels equipped with CMOS digital interface and/or panels with LVDS interface. There are two independent display controllers inside SM731: The Panel controller also referenced as the Primary Controller and the CRT Controller also referred to as the Secondary Controller. Because of this, SM731 is able to drive two screens with different images, from separate frame buffers and at independently programmable timing and resolution. Furthermore, the LCD panels can be programmed to display images from either controller, with some restrictions. See Section Display Processors.

The Digital Interface can drive data from either the Panel Controller or the CRT controller, just like the LVDS2 interface. The LVDS1 interface is hardwired to drive data from the Panel controller (primary display). If the digital interface and LVDS2 interface are both turned on to drive the single pixel panels, their data source has to be the same either from the Panel controller or CRT controller. There will be no restriction if only one interface is on for single pixel panel or LVDS2 is used for double pixel panel.

Digital Interface

The digital interface is 24 bit wide and can be programmed to drive 24 bpp or 18bpp displays. The image source, along with the corresponding control signals (syncs, shift clock and power control), is selectable between the Primary (FP) or Secondary (CRT) controllers through control bit FPR100[5].

FPR100[5] = 1, interface drives data and control signals from Panel controller (Primary).
FPR100[5] = 0, Interface drives data and control signals from CRT controller (Secondary).

Table 8: Digital Interface Pinout

Digital Interface Pinout	
FDATA [23:0]	Flat Panel Data Bits 23 to 0 for direct connection to 18 or 24 bbp panel or to external TMDS transceiver. These lines can be programmed to convey information from the Panel controller (primary display source) or the CRT controller (secondary display source). Single Pixel per clock mode support only. FDATA[23:22], FDATA[15:14] and FDATA[7:6] are driven low if panel type is set to 18 bpp.
FPHSYNC	Horizontal Sync signal from Panel controller (primary display source) or CRT controller (secondary source).
FPVSYNC	Vertical Sync signal from Panel controller (primary display source) or CRT controller (secondary source).
DE1	Display Enable signal from Panel controller (primary display source) or CRT controller (secondary source). This signal is used to indicate the active horizontal display time.
FPSCLK	Flat Panel Shift Clock. This is the pixel clock for Flat Panel Data.
FPEN2	Flat Panel Enable. This signal needs to become active after all panel voltages, clocks, and data are stable. This signal also needs to become inactive before any panel voltages or control signals are removed. FPEN is part of the VESA FPDI-1B specification. Panel controller or CRT controller can be timing source.
FPVDDEN2	Flat Panel VDD Enable. This signal is used to control LCD Panel power. Panel controller or CRT controller can be timing source.

Digital Interface Pinout	
FPVBIASEN2	Flat Panel Voltage Bias Enable. This signal is used to control LCD Bias power. Panel Controller or CRT Controller can be timing source.

Table 9: FPDATA Definition

FPDATA Definition		
Pin	18bpp, single pix/clk panel	24bpp, single pix/clk panel
FPDATA23	Drive low	R7 MSB
FPDATA22	Drive low	R6
FPDATA21	R5 MSB	R5
FPDATA20	R4	R4
FPDATA19	R3	R3
FPDATA18	R2	R2
FPDATA17	R1	R1
FPDATA16	R0 LSB	R0 LSB
FPDATA15	Drive low	G7 MSB
FPDATA14	Drive low	G6
FPDATA13	G5 MSB	G5
FPDATA12	G4	G4
FPDATA11	G3	G3
FPDATA10	G2	G2
FPDATA9	G1	G1
FPDATA8	G0 LSB	G0 LSB
FPDATA7	Drive low	B7 MSB
FPDATA6	Drive low	B6
FPDATA5	B5 MSB	B5
FPDATA4	B4	B4
FPDATA3	B3	B3
FPDATA2	B2	B2
FPDATA1	B1	B1
FPDATA0	B0 LSB	B0 LSB

LVDS Interfaces

The LVDS interfaces can be used to drive two independent panels, one displaying data from the Primary controller and the other displaying data from the Secondary controller. They can also be combined to drive a single, two pixels per clock, high resolution panel. Each LVDS block compresses 24 bits of RGB data and 4 bits of LCD timing into four differential

wire pairs, up to 392 MBytes per second at a maximum clock rate of 112 MHz. A fifth differential pair transmits the interface clock. This way, each LVDS block can drive one SXGA+ panel (1400x1050x24 @60Hz).

The LVDS1 Interface is hardwired to Panel Controller (Primary). It can be programmed to drive 18 or 24 bpp panels, and, if used in conjunction with the LVDS2 Interface, it can be used to drive a two channel, two pixels per clock panel of up to QXGA size (2048x1536).

Associated with the LVDS1 interface are the following control signals, whose timing source is always the Primary Controller: FPEN1, FPVDDEN1 and FPVBIASEN1.

Chapter 10: Miscellaneous Functions

This chapter describes functions of SM731 such as the Video ROM BIOS interface, VESA DPMS, and I^2C / VESA DDC2B.

Video BIOS ROM Interface

The Video BIOS contains code for chip power-on initialization, graphics mode setup, and various read/write routines to the frame buffer. The Video BIOS can be burned into a separate video BIOS EPROM (this is the typical case for add-in cards) or be integrated into the system BIOS ROM (this is the typical case for a motherboard graphics implementation).

To support separate video BIOS ROM access, BIOS address decode must be enabled by setting CSR30 (Expansion ROM Enable Base Address Register) bit 0 = 1. For implementations where video BIOS is integrated into the system BIOS ROM, BIOS address decode access must be disabled by clearing CSR30 bit 0.

Figure 12 shows the external video BIOS ROM configuration interface for SM731. The ~ROMEN (ROM Enable) signal from SM731 connects to the OE and CE signals of the BIOS ROM. Since video BIOS ROM address and data are shared with the video memory data (MD) lines, programmers must ensure that the memory bus is inactive when reading from the Video BIOS ROM. For this case, the Video BIOS ROM must be read out and shadowed (typically in system memory at C0000) immediately after reset. Direct physical access to the Video BIOS must then be disabled to prevent interference with ensuing graphics operations.

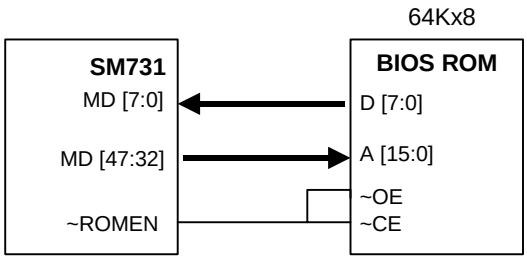


Figure 12: Video BIOS ROM Configuration Interface

VESA DPMS Interface

SM731 supports the VESA Display Power Management Signaling (DPMS) via direct programming PDR22 (LCD Panel Control Select Register) bits 5, 4, or through implementation of the chip's power down states. Table 10 shows the VESA DPMS states and methods for entering each of the DPMS states.

Table 10: DPMS Summary

DPMS State	HSYNC State	VSYNC State	RGB State	Direct Programming Method	Power Down State Method
ON	Pulses	Pulses	Active	PDR22 [5:4] = 00	-
Standby	No pulses	Pulses	Blank	PDR22 [5:4] = 01	Automatic Standby DPMS state when enter Standby mode
Suspend	Pulses	No pulses	Blank	PDR22 [5:4] = 10	CCR69[2]=0 selects Suspend DPMS state when in Sleep mode
OFF	No pulses	No pulses	Blank	PDR22 [5:4] = 11	CCR69[2]=1 selects OFF DPMS state when in Sleep mode

I^2C Bus or VESA DDC2B Interface

SM731 provides dual ports for I^2C-Bus through USR [3:0] I/O pins for various applications such as VESA's DDC2B monitor interface. It is recommended to use USR1 and USR0 as the primary port for SDA and SCL signals on I^2C Bus. USR3 and USR2 are reserved as a secondary port. GPR72 (User Defined Register 1) and GPR73 (User Defined Register 2) are defined to support I^2C/DDC2 bus protocol. SM731, as an I^2C master controller only, is designed to initiate a transfer, generate clock signal, and terminate a transfer to a slave I^2C component.

SM731's I^2C-Bus interface is designed to interface with NTSC/PAL decoders, EEPROMs, audio decoders, and others. The operation voltage of USR [3:0] I/O pins is controlled by VPVDD, which can be configured as 5V or 3.3V. Each of the USR [3:0] I/O pins has an internal pull-up resistor. To enable the data (SDA) and the clock (SCL) from SM731's primary port, bit 5 and bit 4 of GPR72 (3C5h index 72h) must be set as "11". To drive a logic "0" to SDA line (USR1) and SCL line (USR0), program GPR72 bit 1 and bit 0 to "0". The SDA and SCL can be read back from bit 3 and bit 2 of GPR72.

Figure 13 shows the basic I^2C-Bus protocol of SM731 as a master transmitter.

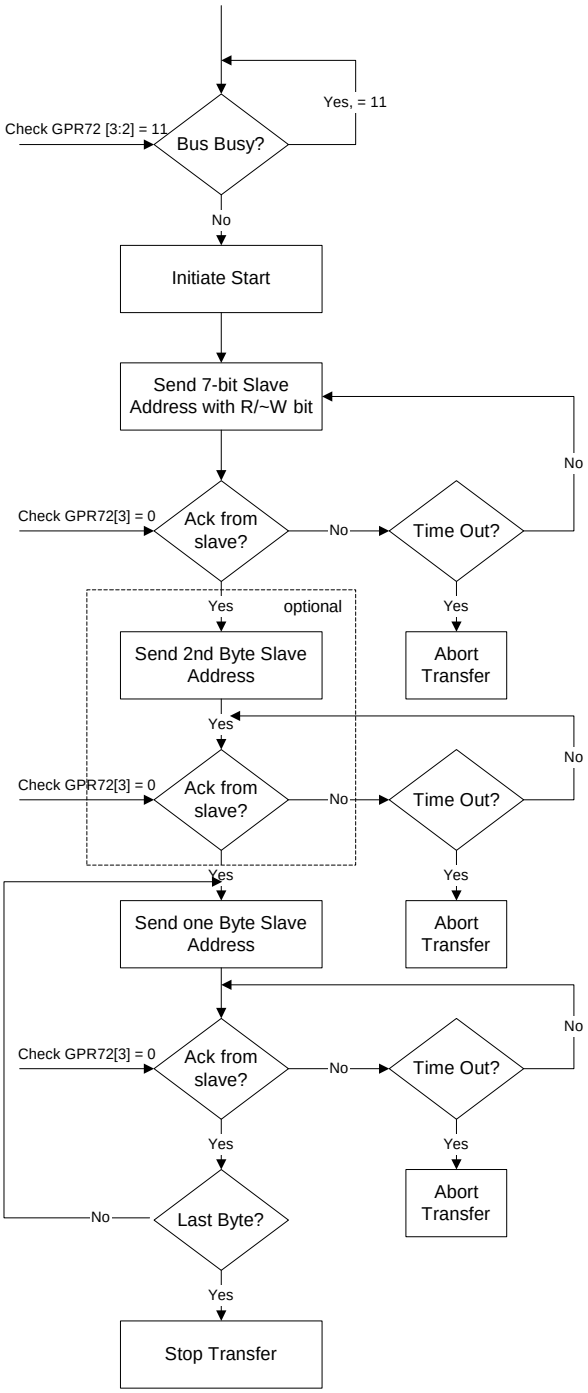


Figure 13: SM731 I²C Bus Protocol Flow Chart

Linear to tile address conversion for CPU access

In order to access the frame buffer in tile mode during the time application (software has no idea about the tile format in the memory), internal hardware has to make the address conversion to address to the right tile location. For additional information see Chapter 24: Video Capture Control Registers.

Chapter 11: Clock Synthesizers

SM731 integrates three programmable clock synthesizers for memory clock (MCLK), Video Clock 1 (VCLK), and Video Clock 2(VCLK2). VCLK1 is utilized for standard CRT only, LCD only, or CRT/LCD display modes for which the refresh rate for both devices is the same. VCLK2 may be utilized when Virtual Refresh mode is implemented - for this case, VCLK1 is utilized for panel timing and to clock the panel display block within SM731. VCLK2 may be utilized to clock the CRT interface independently for LCD/CRT display modes or to independently clock various functional blocks within the device to save power under LCD only display mode. Please see the Virtual Refresh discussion under the Power Management section for additional details regarding power saving capabilities under Virtual Refresh architecture.

Figure 14 illustrates the control logic for MCLK, VCLK, VCLK2. The figure also shows the clock generator module for WFIFO (WFIFOCLK), RFIFO (RFIFOCLK), RAM (RAMCLK), Video Capture (VCMCLK), Drawing Engine (DPMCLK), and Video Processor (VPCLK). TVCLK is used for an external analog TV encoder (this clock is either derived from 14.318MHz base clock - NTSC, or from separate 17.734480MHz clock source connected to input signal PALCLK - PAL).

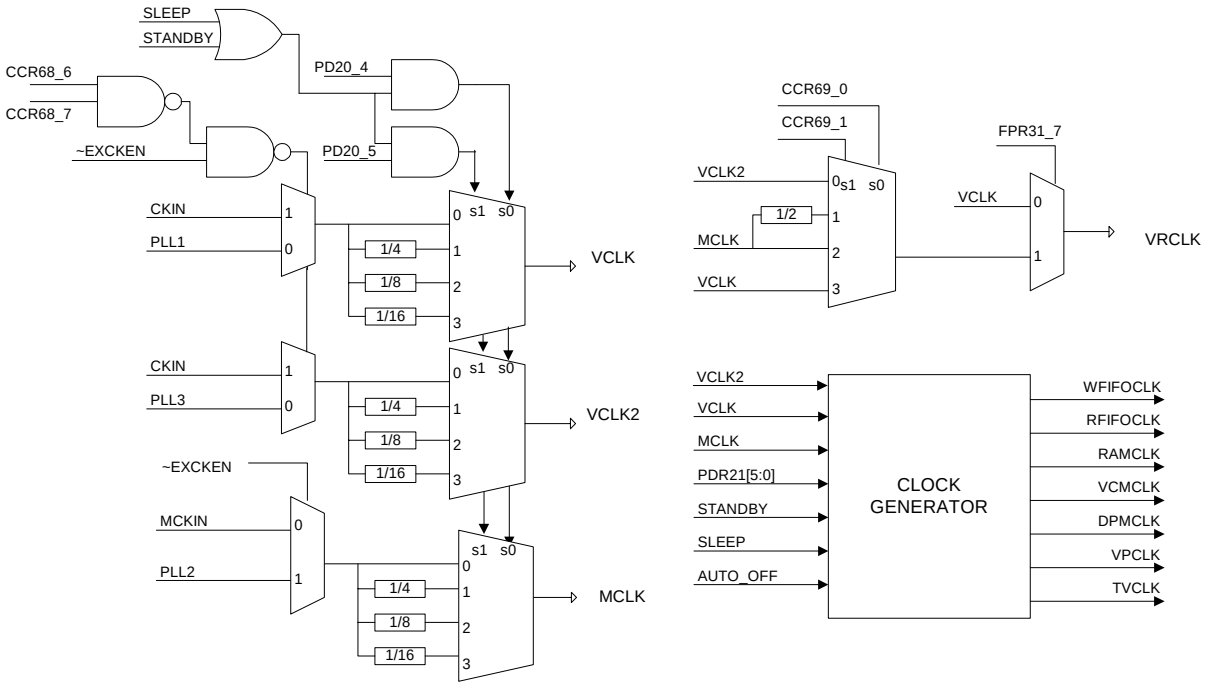


Figure 14: Clocks Generator Block Diagram

The VCLK PLL is programmed using the VCLK Numerator Register (VNR), CCR6C, and VCLK Denominator (VDR) and Post Scalar (PS) register, CCR6D. The VCLK frequency is based on the following equation:

$$VCLK = 14.31818\ MHz \times \frac{VNR}{VDR} \times \frac{1}{1+PS}$$

The post scalar is used to support VCLK frequencies which need a large VDR number. With PS enabled, the VDR number can be set to ½ of the original VDR number. This helps to reduce jitter and maintain accuracy.

The VCLK2 PLL is programmed using the VCLK2 Numerator Register (VCLK2NR), CCR6E, and VCLK Denominator (VCLK2DR) register CCR6F. The VCLK2 frequency is based on the following equation:

$$VCLK2 = 14.31818\ Mhz * \frac{VCLK2NR}{VCLK2DR}$$

Table 11: Recommended VNR and VDR values for common VCLK settings

Resolution Mode	Ref. Rate	VCLK (MHz)	VNR	VDR
640x480	60Hz	25Mhz	07h	82h
640x480	75Hz	31Mhz	16h	85h
640x480	85Hz	36Mhz	88h	9Bh
800x600	60Hz	40Mhz	27h	87h
800x600	75Hz	49Mhz	4Ch	8Bh
800x600	85Hz	56Mhz	37h	87h
1024x768	60Hz	65Mhz	29h	09h
1024x768	75Hz	78Mhz	0Bh	02h
1024x768	85Hz	94.5Mhz	21h	05h
1280x1024	60Hz	104Mhz	53h	0Bh
1280x1024	75Hz	134Mhz	2Fh	45h
1280x1024	85Hz	157Mhz	16h	42h
1400x1050	60Hz	122Mhz	4Dh	09h
1400x1050	75Hz	149MHz	49h	1Eh
1400x1050	85Hz	181Mhz	65h	08h
1600x1200	60Hz	161Mhz	22h	43h
1600x1200	75Hz	202Mhz	8Dh	4Ah
1600x1200	85Hz	229Mhz	A0h	4Ah

Notes:
1. VNR and VDR numbers are hard coded in VGA modes.
2. Post scalar enabled.

The MCLK PLL is programmed using the MCLK Numerator Register (MNR), CCR6A, and MCLK Denominator Register (MDR), CCR6B. MCLK frequency is based on the following equation:

$$MCLK = 14.31818\ MHz \times \frac{MNR}{MDR}$$

Chapter 12: Power Management

The SM731 supports three type of power management:

- **ACPI** - ACPI requirements as defined in the PCI Bus Management Interface Specification 1.0 (PPMI v1.0) and Display device Class Power Management Specification v1.0a.
- **Dynamic Power Management Control** - Silicon Motion's proprietary and pattern pending scheme to control the clock rate under different operational modes. The control mechanism provides control to the external voltage regulator to achieve power saving under normal operations.
- **Deep Sleep** - All PLL and pads are turned off.

ACPI

The SM731 supports D0-D3 modes of operation via the software programming of the Power Management Control/Status Register PMSCR[1:0]. As required by the PCI Bus Management Interface Specification; the PCI Configuration Space Status Register (offset 06h) bit 4 is set to "1" to indicate new capabilities have been defined for SM731. At offset 34h, the Cap_Ptr register, stores the offset of the new capabilities (this register is hardwired to 40h). The first byte at offset 40h has a value of 01h, which indicates a Power Management capability (supports D1 and D2 states in addition to the required D0 and D3 power states). The second byte has a value of 00h indicating the no additional new capability features. (Note: SM731 does not offer support for optional ~PME capabilities as defined in PPMI v1.0. Please refer to the PCI Bus Power Management Interface Specification 1.0 and Display Device Class Power Management Reference Specification v1.0a for additional details).

The SCR24_[0] has to be set to 1 to enable the ACPI function. In ACPI the D1 state (stand by mode), most clocks are shut down to only maintain the minimum operational modes such as screen refresh. In ACPI D2 and D3 states (suspend and sleep modes), all clocks are shut down. The DRAM enters the self refresh mode, and PDR20_[7] need to be set to 1 to enable these states. Display driver support for ACPI under Windows 98 and future versions of Windows NT will be provided by Silicon Motion in accordance with PC97 and PC98 requirements.

The CRT power management is controlled by the ACPI states according to the standards. The LCD power management and power sequencing are controlled by FPEN, FPVDD, and VBIAS control pins. Please refer to the flat panel register FPR100 for details.

ACPI Mode Sequence

- Set PDR24_[0] = 1 (ACPI enable)
- Set PDR20_[7]=1 (Enable Sleep Mode)
- Set PDR20_[6] = 1 (self DRAM refresh)
- Set SCR25_[1] = 1 To power down AGP4xpll.
- Set PDR21_[4] = 1 Shut off CRT pixel shift clock
- PDR20_[1] = 1 Turn off LCD panel data pains
- FPR100_[13:12] = 00 Power off LVDS 1 and 2 module
- Clock divider set up

PDR20_[5:4] = 11 - Enable clock divider in Sleep mode
CCR9E_[7:0] = 3F - Memory clock no divide, all other clocks divide 16

- Activate ACPI mode

Table 12: Interface Signals Sleep Mode States

Signal Name	Sleep Mode
Host Interface	
AD [31:0]	tri-state
C/ ~BE [3:0]	tri-state
PAR	tri-state
~FRAME	tri-state
~TRDY	tri-state
~IRDY	tri-state
~STOP	tri-state
~DEVSEL	tri-state
IDSEL	x
CLK	x
~RST	H
~REQ	tri-state
~GNT	x
~INTA	tri-state
Power Down Interface	
~PDOWN	L
~CLKRUN	open-collector
Clock Interface	
REFCLK/PALCLK	x
CKIN	x
LVDSCLK	tri-state
~EXCKEN	H
Memory Interface	
MA [11:0]	H
MD [63:0]	H or L (note 2)
~WE	H
~RAS	L
~CAS	L
~CS [1:0]	L
~DQM [7:0]	H
DSF	L
BA	H

Signal Name	Sleep Mode
SDCKEN	L (self-refresh), H (CAS-b-RAS)
SCK	depends on PLL
~ROMEN	H
Flat Panel Interface	
FDATA [23:0]	L
FPSCLK	L
FPEN	L
FPVDDEN	L
VBIASEN	L
LP/FHSYNC	L
FP/FVSYNC	L
CRT Interface	
R, G, B	0 V
CRTVSYNC	L
CRTHSYNC	L
Video Port Interface	
P [15:0]	L
PCLK	H
VREF	H
HREF	H
BLANK/TVCLK	H
General Purpose Registers/I^2C	
USR3	H
USR2	H
USR1/SDA	H
USR0/SCL	H
Test Mode Pins	
TEST [1:0]	L

Table 13: Gated Clock Trees

Clock Tree name	Control Register (1=disable unless noted)	Sleep	Standby
Video Capture	PDR21_[2]	Off	Off
CRT Video	PDR21_[0]	Off	Off
LCD Video	PDR21_[4]	Off	Off
LCD Wfifo	PDR21_[5]	Off	Off
2D Engine	PDR21_[1]	Off	No effect
Motion Comp	CCR66_[1]	Off	Off
3D Engine	CCR66_[0]	Off	Off
CRT DAC	PDR21_[7]	Off	Off
CRT CLUT	CCR66_[6]	Off	Off
LCD CLUT	CCR6_[7]	Off	Off
TV Encoder	CCR65_[5](1=enable)	Off	Off
TV YC DAC	CCR65_[6](1=enable)	Off	Off
TV SVHS DAC	CCR65_[7](1=enable)	Off	Off
CRT pix.Shift CLK	PDR21_[3]	No effect	No effect
PLL PwrDown Enb	PDR21_[6]	No effect	No effect

Dynamic Power Management Control (DPMC)

The DPMC is different from the ACPI power-down mode, and can be used to minimize power usage under normal operation without going to "sleep" mode. All the major functional blocks have their own gated clock tree which can be shut down independently via software control. The DPMC can also dynamically control the engine clock and memory clock rate to achieve power savings, and the clock rate adjustment is controlled by a look up table (register CCR94 - CCR9D). Depending on the state of the DPMC, the clock rate can be adjusted automatically. The DPMC has three states normal, save, and idle. These states depend on the AC power on/off, bus activity, and 3D engine on/off.

To enable the dynamic power management control

PDR23_[7]
0 = disable DPMC
1 = enable DPMC

DPMC interrupt

The "ACON" pin is a system provided input status control signal.
0 = "ACON" means the AC power is off. Saving battery (DC power) becomes important.
1 = "ACON" means the AC power is on.

Once the DPMC is enabled(PDR23_[7]=1) the SM731 can generate an interrupt by monitoring the ACON pin. When the ACON input pin status changes from 0->1 OR from 1->0 the interrupt will be software generated to control the DPMC.

DPMC interrupt control register bits

SCR1C_[1] - DPMC interrupt status bit

SCR1F_[5] - DPMC interrupt enable bit
0 = Disable DPMC interrupt
1 = Enable DPMC interrupt

SCR1F_[1] - DPMC interrupt mask bit:
0 = No interrupt mask
1 = Mask out DPMC interrupt

DPMC States

Once the DPMC is enabled, there are 3 states:

Normal state: if "ACON" status pin is 1, DPMC will stay (AC power on) in "Normal" state. DPMC will always stay in this state if PDR23_[7] = 0.

The engine clock rate is determined by:
CCR6A/CCR6B if 3D engine is OFF
(CCR6A - CCR98)/CCR6B if 3D engine is ON

The memory clock rate is determined by:
CCR63/CCR64 if 3D is OFF
(CCR63 - CCR99)/CCR64 if 3D is ON

PowerSave state: if "activity detection" detect no bus (AC power off) activities, DPMC will go to “PowerIdle" state. Otherwise the DPMC will stay in "PowerSave" state.

The engine clock rate is determined by:
(CCR6A - CCR94)/CCR6B if 3D engine is OFF
(CCR6A - CCR9A)/CCR6B if 3D engine is ON

The memory clock rate is determined by:
(CCR63 - CCR95)/CCR64 if 3D is OFF
(CCR63 - CCR9B)/CCR64 if 3D is ON

PowerIdle state: If "activity detection" detected bus (Bus idle) activity DPMC return to "PowerSave" state. Otherwise stay in "PowerIdle" state.

The engine clock rate is determined by:
(CCR6A - CCR96)/CCR6B if 3D engine is OFF
(CCR6A - CCR9C)/CCR6B if 3D engine is ON

The memory clock rate is determined by:
(CCR63 - CCR97)/CCR64 if 3D is OFF
(CCR63 - CCR9D)/CCR64 if 3D is ON

SM731 has control logic to monitor the host bus activities. The DPMC can be programmed to define how long it takes to wake up from idle states and what kind of bus activity detection should be monitored by DPMC for wake up as the following.

PDR23_[6:5]
00 = detect Memory write/read & IO write/read and capture enable
01 = detect memory write & IO write and capture enable
10 = detect memory write/read and capture enable
11 = detect IO write/read and capture enable

PDR23_[3:0] - Timer control to count number of VSYNC (CRT timing). If there is no bus activities in a specified period, the power management will enter "idle" mode.
0000 = Disable activity detection
0001 = 64 VSYNC
0010 = 128 VSYNC
0011 = 256 VSYNC
0100 = 512 VSYNC
0101 = 1K VSYNC
0110 = 2K VSYNC
0111 = 4K VSYNC
1000 = 8K VSYNC
1001 = 16K VSYNC
1010 = 32K VSYNC
1011 = 64K VSYNC
1100 = 128K VSYNC
1101 = 192K VSYNC
1110 = 256K VSYNC
1111 = 384K VSYNC

Activity output pin (P22)

There is an Activity output pin which can be used to control an external power regulator to adjust the core VDD to achieve power savings.

SCR18_[7]
0 = Select ~CLKRUN as input for pin P22. There is no Activity output for this case. This mode is considered an alternative to implementing ReduceOn. If the Activity pin is not available, see the appropriate app note for further details).

1 = Select Activity as output for pin P22. This Activity pin will always be low if “ACON” input pin is high; otherwise, the output will be controlled by CCR65_[4]:

0 = Output low status
1 = Output high status

Note: The Silicon Motion software implements this PIN as ReduceOn control pin which will control the external VDD power regulator. If the Activity is low, then the VDD will be 2.5V. If Activity is high, then the VDD will be dropped.

Deep Sleep Mode

After the SM731 ACPI mode is activated, the "deep sleep mode" can be used to further reduce the static current of the chip by shutting down all the internal PLLs and all AGP/PCI pads. The sequence of entering this mode should be:

ACPI => Deep Sleep Mode. Before exiting from the ACPI mode, the "deep sleep mode" must first be disengaged. To enter this mode, pull the "PWDOWN" pin to low (normally the pin is high by the internal pull up). PDR21_[6] = 1 has to be set to 1, before the pull PWDOWN pin to low.

Chapter 13: Motion Compensation Specification

Overview

The Motion Compensation block (MC) executes a series of instructions in a pipelined fashion. There is actually only one type of instruction with several flags that control the instruction execution. The MC instruction is similar to a CPU arithmetic instruction with three sources (imm - IMMediate operand, mrd - Memory ReaD and acc - ACCumulator) and one destination (mwr - Memory WRite). The main difference between standard CPU instructions and those used by the MC is that the MC instruction works on rectangular blocks of data instead of 8, 16, 32, or 64-bit integers.

The rectangular blocks of data (rectangles) used by the MC are 2-dimensional arrays containing 8-bit values. For the current implementation, the horizontal and vertical sizes (hsize and vsize) are limited to the following ranges: hsize = 8 or 16; vsize = 4 or 8. The MC requires one 128x16 SRAM for temporary storage of the input and output array values. It acts as a CPU accumulator.

The throughput of the MC pipeline is two pixels per cycle. Under worst case assumptions a MPEG-2 MP@ML picture will thus require 22 Mcycles/second.

Data Flow and External System Responsibilities

All instructions for motion compensation are generated by a software front-end and fed to the graphics controller via a standard software API. The instructions specify two different types of operations: (1) Memory accesses used for reading prediction data and writing reconstructed pels, and (2) Data processing operations used to combine predictions with the error terms generated by the IDCT operation.

The MC core handles all data processing operations required for motion compensation. The graphics memory controller handles the memory access operations. The memory controller must read the instructions generated by software, fetch prediction data, feed the data to the MC block and write the final reconstructed pels into the proper location.

MC Top Level Architecture

The top level architecture of the MC core is shown in Figure 15. It consists of a simplified quadrilinear filer (mc_qlf - this is the data path), a 128x16 dual port SRAM, and a controller (mc_ctl). The MC has four data busses: command (cmd), immediate operand (imm), memory read (mrd) and memory write (mwr).

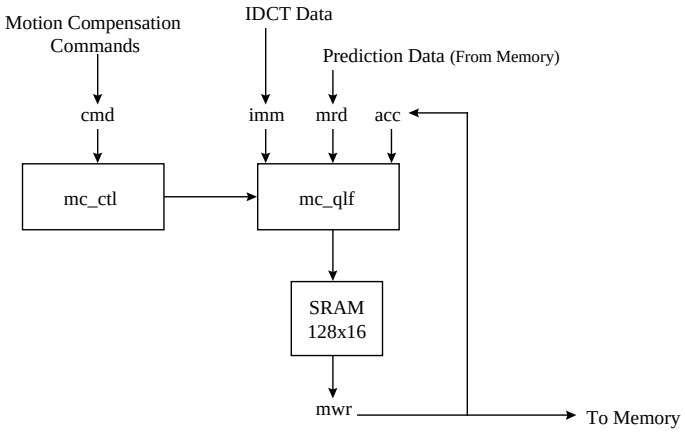


Figure 15: MC Top Level Architecture

In the current architecture all input and output busses are kept separate to offer the maximum processing throughput. Except for the command bus, all busses can operate continuously at one 16-bit or 18-bit value per cycle (two pixels/cycle). All busses use a rdy-ack protocol and can be stalled on any cycle.

For MPEG the IDCT output is fed through the imm bus and the prediction through the mrd bus. For bidirectionally interpolated macroblocks, first the forward prediction is read, half-pel interpolated, and stored in the 128x16 memory (block ACCumulator). Next, the backward prediction is read, half-pel interpolated, and added to both the acc (forward prediction) and imm (immediate or IDCT) data.

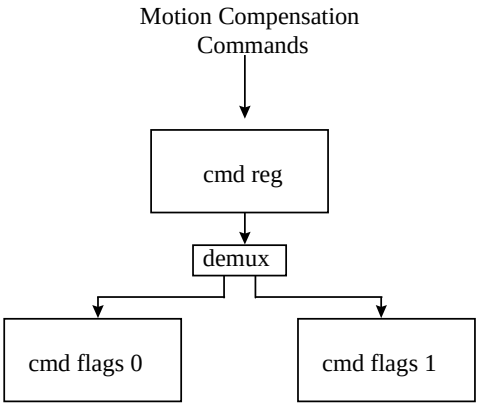


Figure 16: Control Block Diagram

Words from the cmd bus are loaded directly into the 16-bit cmd register as the command pipeline advances. The flags0 and flags1 registers each hold exactly one instruction each and together form a 2 instruction FIFO. One instruction is encoded as 2 or more 16-bit words, which means that it will take 2 or more pipeline advances before a flags register has accepted an entire instruction. Having 2 instructions queued at a time allows the MC to prepare an idle QLF pipeline with data ahead of time - before the current instruction has completed.

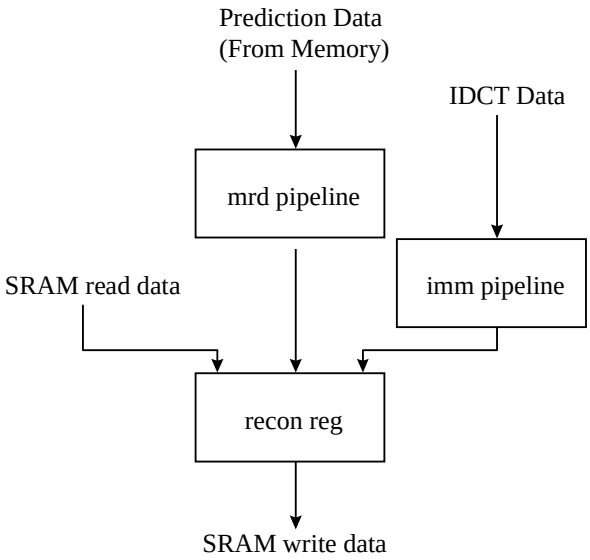


Figure 17: QLF Block Diagram

The Quadrilinear Filter consists of three pipelines, namely the acc, mrd, imm pipelines. The acc pipeline is not shown in block diagram because it consists of two stages external to the MC. The first stage is the synchronous SRAM read port while the second stage is a register that accepts SRAM read data. The width of this register matches the width of the reconstruction memory write back (mwr) data and is application dependent.

The mrd pipeline accepts prediction data from memory in a 16-bit wide format (2-pels). Pel alignment, horizontal half pel interpolation, and vertical half pel interpolation are handled in the pipeline.

The imm pipeline accepts IDCT data in a 18-bit (9-bit pel) or 16-bit (8-bit pel) format. The data is reformatted based on the flags in the current instruction.

Data from the three pipelines is combined and held in the reconstruction register. The data is added together, then saturated to values between 0 and 255. From this register the data is written to the local SRAM 16-bits (2 pels) at a time.

MC Instruction Format and Operation

Figure 19 shows the MC instruction format. The flags and parameters in the instructions are summarized in Table 14. All MC commands have the most significant bit (MSB) of word A set=1. Commands that have the MSB cleared=0, are intended for the memory controller or other control logic external to the MC. Currently, the only command with MSB=0 is used to indicate the end of stream:

	f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B	0	0	10000					0	0	0	00000					0

Figure 18: End Stream Instruction

This End Stream command can occur anywhere in a command stream and should trigger an end to the command stream transfer. After this instruction is encountered by hardware, communication would then take place between hardware and the driver to determine what step to take next. This command is intended for logic external to the MC but should also be passed on to the MC. The MC will see it as a Flush command and is required in order for the results from the last valid command to be written to memory.

The following table defines the format for MC instructions. Notice that the MSB of word A is set=1, indicating that this is an MC instruction.

	f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
A	1	-	ISL	IM8	MRD	IMM	ACC	MWR	THB	LHB	IH0	IH1	TVB	LVB	IV0	IV1
B	-	-	hsize [4:0]					HHP	-	-	vsize [4:0]					VHP
C	mrd_slot[1:0]		mrd_plane[1:0]		mrd_hadder [11:0]											
D	-			RVS	mrd_hadder [11:0]											
E	mrd_slot[1:0]		mrd_plane[1:0]		mrd_hadder [11:0]											
F	-			WVS	mrd_hadder [11:0]											

Figure 19: MC Instruction Format

Table 14: Instruction Flags and Parameters

Flag	Parameter	Meaning
ISL		Immediate Shift Left vs. sign extend left
IM8		IMmediate data 8-bits per pixel
MRD		Memory ReaD
IMM		IMMediate
ACC		ACCumulate
MWR		Memory WRite
THB		Two Horizontal Blocks
LHB		interLeaved Horizontal Blocks
IH0		Immediate operand for Horizontal block 0
IH1		Immediate operand for Horizontal block 1
TVB		Two Vertical Blocks
LVB		interLeaved Vertical Blocks
IV0		Immediate operand for Vertical block 0
IV1		Immediate operand for Vertical block 1
	hsize [4:0]	Horizontal SIZE
HHP		Horizontal Half Pel interpolation

Flag	Parameter	Meaning
	vsize [4:0]	Vertical SIZE
VHP		Vertical Half Pel interpolation
	mrd_slot [1:0]	Memory ReaD SLOT
	mrd_plane [1:0]	Memory ReaD PLANE
	mrd_haddr [11:0]	Memory ReaD Horizontal ADDRess
	mrd_vaddr [11:0]	Memory ReaD Vertical ADDRess
RVS	mrd_vstep	Memory ReaD Vertical STEP
	mwr_slot [1:0]	Memory WRite SLOT
	mwr_plane [1:0]	Memory WRite PLANE
	mwr_haddr [11:0]	Memory WRite Horizontal ADDRess
	mwr_vaddr [11:0]	Memory WRite Vertical ADDRess
RVS	mwr_vstep	Memory ReaD Vertical STEP

Each MC instruction consists of two, four or six 16-bit words. The first instruction, instruction A in Figure 19, contains the instruction flags. The second instruction contains the rectangle size. Depending on the flags in the first instruction, the remaining four instructions may or may not be present.

In instruction A, the most important flags are MRD, IMM, ACC, and MWR. These flags indicate what source operands are used and if the result should be stored to memory or to the accumulator (the 128x16 memory). All or none of these four flags can be set. If none of the source flags are set, the MC generates a rectangle of zeros.

If the MRD (Memory ReaD) flag is set, instructions C and D must be present. These instructions specify the address from which prediction data should be fetched. The memory slot (prediction slot) from which to read the data is given by the mrd_slot [1:0]. A slot contains one frame of video which can be broken down into two or three color planes: (Y, Cb, Cr) or (Y, Cb/Cr interleaved). Each color plane can be broken down into two fields. The top field is located in the even lines while the bottom field is located in the odd lines of the frame. The X-Y offset in the slot (frame) from which to fetch the data is given by the mrd_haddr [11:0} and mrd_vaddr [11:0]. The vertical step, mrd_vstep, indicates whether every line or every other line should be read from the slot. For frame prediction every line is read (mrd_vstep = 0) and for field prediction every other line is read (mrd_vstep = 1). The first line of a rectangle of prediction data is indicated by mrd_vaddr [11:0]. In field prediction (mrd_vstep = 1), which field the data must come from depends on the location the first line of the prediction rectangle. If that line is in the top field, then the data comes from the top field. Otherwise it comes from the bottom field.

The parameter mrd_plane (Memory ReaD PLANE) indicates which video plane is being processed (0=Y, 1=Cb, 2=Cr, 3=CbCr). For MPEG decompression the memory read plane, mrd_plane [1:0] and memorywrite plane, mwr_plane [1:0], are always equal. (Note: they are provided as different values to offer increased flexibility for other applications (read from one plane and write to a different plane).

If the MWR is set, instruction E and F must be present. These instructions specify the address to which the final computed pels should be written. Similar to the data read instructions, the write slot is indicated by mwr_slot [1:0]. The X-Y offset is indicated by mwr_haddr [11:0] and mdr_vaddr [11:0]. The mwr_vstep bit specifies whether or not to skip a line between successive rows written in the same way that the mrd_vstep does for the prediction data. In MPEG-2 decode, mwr_vstep setting reflects the motion type for the macroblock being processed.

In instruction B, if HHP is set, Horizontal Half Pel interpolation is performed and the mrd horizontal size shall be hsize pixels plus one. If VHP is set, Vertical Half Pel interpolation is performed and mrd vertical size shall be vsize rows plus one.

If the ACC flag is set, the MC adds the content of the ACCumulator (the 128x16 memory to be memory read data (if present).

If the IMM flag is set, the MC adds the immediate data, supplied on the imm bus, to the interpolated data, (mrd = acc)/2. The immediate data is the error term calculated by the IDCT. All the other nine flags have a meaning only if IMM is set.

IM8 indicates if the immediate data is only 8 bits wide. If IM8=0 the MC will accept IDCT data in a 9-bit per pixel format. MPEG-2 defines a range for IDCT data from -256 to =255 which is covered by a 9-bit two's complement number. A setting of IM8=1 indicates that the data is in an 8-bit per pixel format which approximates the full range. The ISL flag is used in conjunction with IM8 and differentiates between two 8-bit modes. ISL is ignored when IM8=0. 8-bit approximations allow data to be packed more efficiently into standard word widths. At issue is the sign bit. Intra-coded macroblocks never use the sign bit since values are restricted to the range of 0 to +255, while predicted to bidirectional IDCT values take the range of -256 to +255. For this reason, commands are separated into two different categories: intra-coded and non intra-coded.

If IM8=1 and ISL=0, the MC first determines the type of command currently being executed, then generates the sign bit based on the category. Intra-coded values are zero extended, while non intra-coded values are sign extended to the full 9 bits. Software that decodes the IDCT data must remove the sign bit in the intra-coded case while saturating the lower 7 bits and removing the 8th bit in the non intra-coded case. Non-intra coded data retains its sign bit since the saturation process results in a 8-bit twos complement number whose most significant bit represents its sign.

The IM8=1/ISL=0 setting will put an upper limit on the amount of correction that can be made to prediction data though. After the correction IDCT error terms can be no greater than =127 and no less than -128. As mentioned before, MPEG-2 specifies the range to be between +255 and -256. Under normal conditions values rarely exceed the smaller range since motion is relatively slow from picture to picture. When they do, it will be almost impossible for an observer to notice since the corrupted pels will be located in an area where a great deal of motion is occurring. In some rare cases though this range clipping can cause visible artifacts. They can be corrected though, with a second IMM data "pass". Instructions with settings of MRD=1, ACC=1 and IMM=1 calculate results as follows:

acc = (mrd+acc) / 2 = imm
Instructions with settings of MRD=0, ACC=1 and IMM=1 calculate results differently:

acc = acc + imm

This allows for a correction of IMM data terms that were saturated to the range of [-128, +127]. The first IMM pass would correct to this smaller range while the second pass would allow for a correction to a range of [-256 +254]. To reach a correction of +255, a third pass can be generated but would not be required very often.

If IM8=1 and ISL=1, the MC shifts the 8-bit IMM data left one bit before performing calculations with it. Intra coded an non-intra coded commands both treat the IMM data this way. Software must drop the least significant bit of the original 9-bit terms to convert to the format of the data required in this mode. This is the fastest way to generate 8-bit IMM data but will result in lower quality video. Images that contain large areas of a single color will suffer contour lines.

The remaining eight flags are needed to accommodate all possible combinations of coded_block_pattern and dct_type. The immediate data is present only if indicated by these flags. The term "reconstruction plane" in the following paragraphs refers to data that is written to the MC block's local SRAM as a result of a given command. Each reconstructed pel has a horizontal and vertical component that make up its position in the plane.

IH0 and IH1 indicate that the coded_block_pattern flag is set (IDCT data is present) for the one or two horizontal blocks that are processed. IH0 is used for the left most pels while IH1 is used for the right most. Pel locations in the reconstruction plane are assigned to one of the coded block pattern (cbp) bits, namely IH0, IH1, or IV1. IDCT data is only used in the reconstruction calculation for a given location when its cbp bit is 1. Otherwise, the IDCT data is either masked out or missing from the immediate data stream.

IV0 and IV1 are the cbp bits used when two vertical blocks are present. In MPEG terms, IV0 can be thought of as indicating that block Y2 is coded. IV1 can be thought of as indicating whether Y3 is coded. IDCT data is re-ordered to be combined with prediction data (MRD bus). For this reason, the cbp bits may not apply evenly to adjacent blocks as they do in the MPEG bitstream. Their assignment to locations in the reconstruction plane reflect the change in the order of the IDCT data.

TVB indicates that Two Vertical Block as are processed at the same time. If TVB is high, IH0 and IH1 are used for the top half of the rows while IV0 and IV1 are used for the bottom half. In the top half, whether IH0 and IH1 is used will be dependent on the horizontal reconstruction pel position, THB and LHB. The same is true of IV0 and IV1 in the bottom half. TVB is not an indicator of the number of vertical rows for a command. The vsize [3:0] bits indicate this. Although if TVB is high, vsize [3:0] bits indicate this. Although if TVB is high, vsize [3:0] is used to determine the vertical half-way point for a command.

LVB indicates that two Blocks are Vertically interLeaved. This is needed when frame prediction and field DCT type data are used in a frame picture. When LVB is high, the even rows in the reconstruction plane are assigned to IH0 and IH1 while the odd rows are assigned to IV0 and IV1.

For MPEG related applications, TVB and LVB will never both be set high. A command generator that sets them both will not cause a failure in the MC though. The result will be a union of the two modes. The top half of the rows will be interleaved while the bottom half will not. All of the bottom rows will be assigned to the IV0 and IV1 cbp bits.

THB indicates that Two Horizontal Blocks are processed at the same time. When THB is high, either IH0 and IV0 will be assigned to the left most half of a reconstruction row, while IH1 or IV1 will be used for the right most half. In the left half, whether IH0 and IV0 is used will be dependent on the row number, TVB and LVB. The same is true of IH1 and IV1 in the right half. THB is not an indicator of the number of horizontal pels in a row. The hsize [4:0] bits indicate this. Although if THB is high, hsize [4:0] is used to determine the half-way point in a row.

LHB indicates that two Blocks are Horizontally interLeaved. This is needed when chroma (Cb and Cr) is stored in a single plane to save memory bandwidth. When LHB is high, the upper 9 or 8 bits of the imm [17:0] bus are interpreted as a Cb IDCT pel and IH0 and IV0 is used as a mask while the lower 9 or 8 bits are interpreted as Cr with IH1 or IV1 as a mask. When a coded block pattern bit is 0 the corresponding immediate data is masked to 0 before being used in reconstruction calculations. Unlike non-interleaved cases, data for the pels masked to 0 must be present in the immediate data stream even though their values are thrown out. When LHB is set high, the THB bit is ignored. Setting both bits high has the same effect as setting LHB high and THB low.

Chapter 14: 3D Drawing Engine

SM731 incorporates a high end 3D drawing engine capable of rendering six million triangles and 250 million Texels per second. The engine itself along with the several pipelines it incorporates have been completely redesigned from Silicon Motion's previous 3D engine built inside Lynx3DM (SM720).

Architectural Delta from SM720

- Fast DMA engine
- 20-cycle setup engine
- Dual texel pipelines
- Tile based rasterization
- Enable single cycle tri-linear mip-map and anisotropic filtering
- Add color destination cache
- Add 32-bit frame and z/stencil buffer
- Reduce page break penalty

Functionality Delta from SM720

- Z clear value
- Single cycle multitexture
- Bump mapping
- W buffer
- W based fog
- Stencil planes (up to 8 planes)

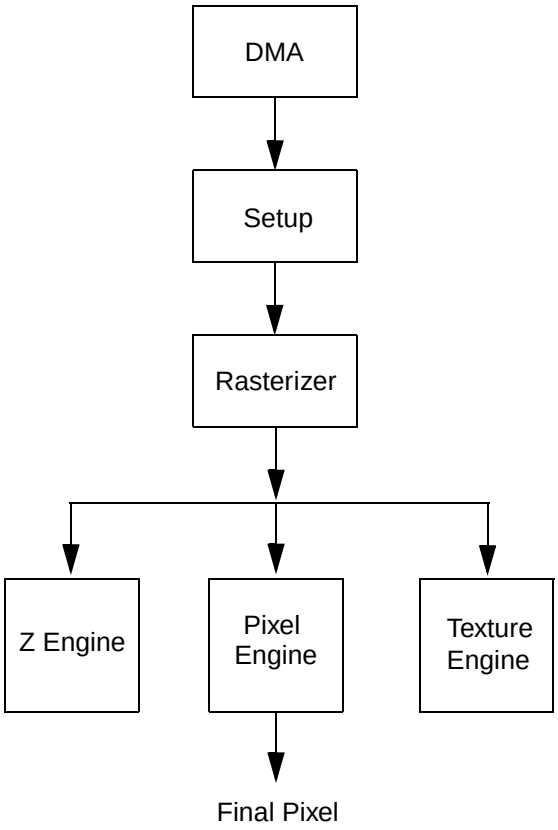


Figure 20: 3D Engine

DMA and Command Interpreter

SM731 incorporates a sophisticated DMA and command interpreter engine through which all data to and from the 3D engine flows. The software driver builds buffer structures in AGP memory containing all triangle data and commands for the 3D Engine. From there on, SM731 hardware gathers these buffers, processes, and conveys status information back to the driver.

Feature set

- Fast DMA engine
- Vertex buffer of 12 entries
- Supports flexible vertex format
- Supports vertex buffer
- Supports memory to memory blit
- Supports tiled memory to memory blit
- Accumulates and sends state changes to the entire 3D pipeline

Setup Engine

The Setup Engine completes a triangle parameter setup every 20 cycles. This gives 6 million triangles per second performance at 125 MHz. This performance is for a full featured triangle, i.e. a triangle with parameters: x, y, z, w, rs, gs, bs, as, rd, gd, bd, ad, s0, t0, s1, t1.

Feature Set

Primitive types supported:

- Triangle list
- Triangle strip
- Triangle fan

Functionality features:

- No Cull, cull cw, cull ccw
- Up to two sets of color components for diffused and specular colors
- A set of registers for flat shading
- Up to two sets of texture coordinates
- Texture coordinate wrapping. Wrapping is independent for each texture coordinate
- Screen space z
- Homogeneous space w

Rasterizer Engine

To improve memory interface performance, SM731 supports tile based rasterization.

Feature Set

- Tiled rasterization
- Supports clipping window
- Supports w, z
- Supports specular and diffuse lighting
- Supports two textures

Texture Engine

Two texture pipeline computes single pixel with two textures each clock cycle. The pipeline gives 250 Mtexels/second performance at 125 Mhz.

Feature Set

- Dual Texture pipeline
- Floating point s, t, w computation
- Supports point sample, bi-linear, and tri-linear mip-map
- Supports Bump mapping

- Supports texture compression

Supported texture formats:
- ARGB8888
- ARGB4444
- ARGB1555
- RGB565
- DXT1, 2, 3, 4 and 5

Pixel Engine

The Pixel Engine includes Texture Blending stages

Feature Set
- Efficient pixel pipeline
- Supports both diffuse and specular color components
- Supports 16-bit and 32-bit frame buffer formats
- Supports multi-texture blend functions
- Supports color key function
- Supports both vertex and table based fog
- Supports alpha test function
- Supports all D3D source and destination blend modes
- Supports dithering for 16-bit frame buffer format

Z Engine

SM731 Z Engine supports Stencil and Fog. One z/stencil/fog pipeline computes z, stencil and fog values for one pixels per cycle. This gives us 125 MP/s.

Feature Set
- Zero cycle Z buffer clear
- Supports either screen space z or w
- Supported z formats: 16 and 24 bit fixed point format
- Supported w formats: 16-bit fixed point format and 24-bit floating point format
- Supports up to 8 stencil planes
- Supports table based fog with table size of 256 x 8
- Z and stencil cache

Chapter 15: TV Encoder

The TV Encoder is an NTSC/PAL Composite Video/S-video Encoder. It receives RGB inputs and converts to digital video signals based on CCIR 624 format.

The input video signal of the TV Encoder is RGB 8-bit each. The sampling rate is corresponding to CCIR 601, Square pixel and 4Fsc (NTSC only).

The output video signals of the TV Encoder are Composite video signal and S-video signals of 10-bit each. These output signals are over-sampled by a double frequency clock called CLKX2. This feature helps to simplify external analog filtering.

The TV Encoder video timing is controlled by vertical sync and the horizontal sync input signals. The blank signal input is optional. If the blank signal input signal is pulled up, internal blanking control will be performed.

Macrovision 7.1.4 and closed captioning functions are included.

Key Feature Summary

- NTSC/PAL interlace mode digital video encoder
- Composite Video and S-Video digital output
- CCIR 601, Square pixel and 4Fsc (NTSC only) resolution RGB input
- Slave timing operation
- Interlace mode operation
- 2x over-sampling data output to simplify external analog filtering
- Selectable pedestal level OIRE/7.5IRE for NTSC
- Macrovision function (version 7.1.4)
- Closed captioning function

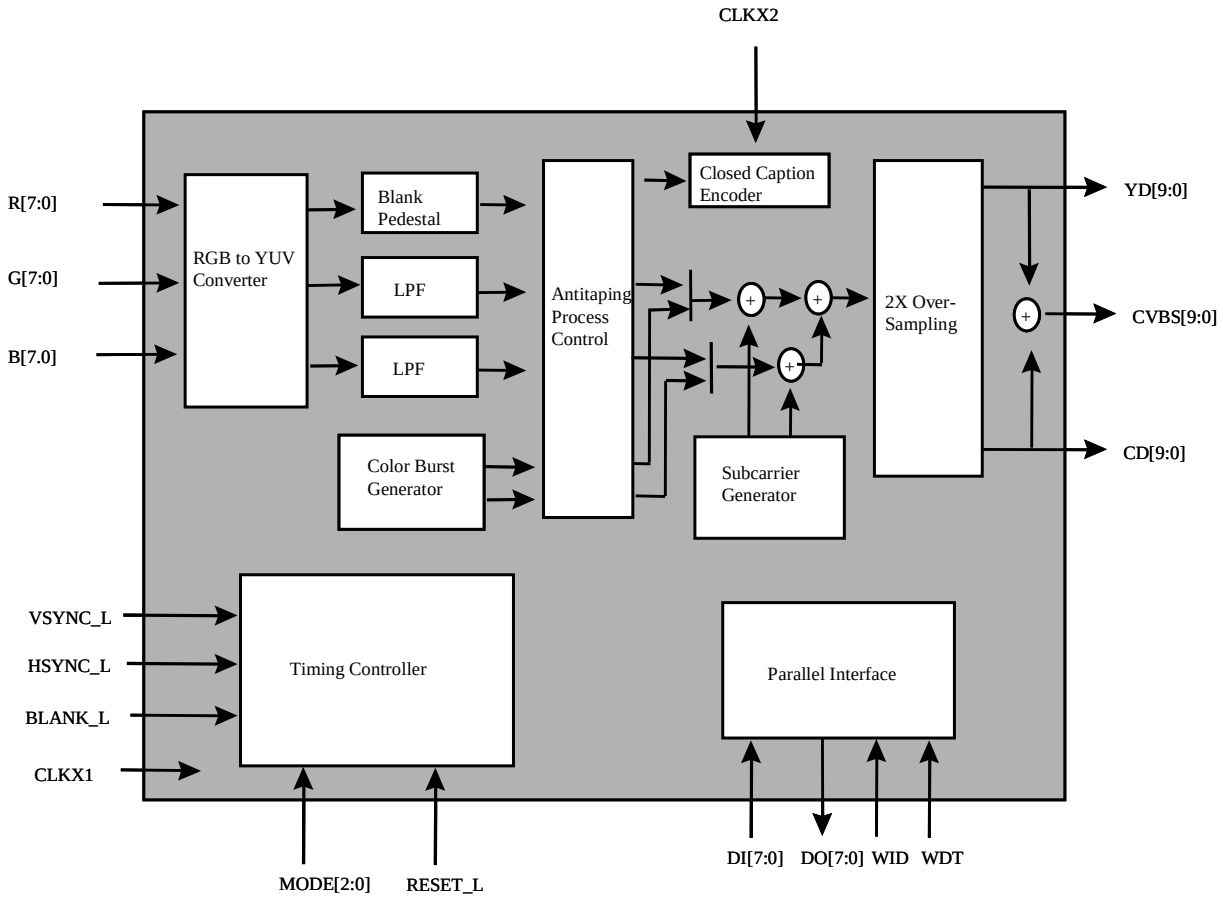


Figure 21: TV Encoder Block Diagram

Table 15: TV Encoder Block Interface Description

Excore-TV Encoder for SMI pin list

Pin name	Width	I/O	Description
R	8	I	4:4:4 sampled Red data This data should be synchronized to the CLKX1.
G	8	I	4:4:4 sampled Green data This data should be synchronized to the CLKX1.
B	8	I	4:4:4 sampled Blue data This data should be synchronized to the CLKX1.
VSYNC_L	8	I	Vertical sync input, active low This goes low during the vertical sync intervals.
HSYNC_L	1	I	Horizontal sync input, active low This goes low during the horizontal sync intervals.
BLANK_L	1	I	Composite blanking input, active low. This goes low during the composite blanking intervals. If this signal is low, the RGB input data will be masked.
CLKX1	1	I	Pixel rate clock input This clock should be free-running, and will be synchronized to the CLKX2.

Pin name	Width	I/O	Description
CLKX2	1	I	2X Pixel rate clock input This clock should be free-running.
MODE	3	1	Mode select When MR[7] is set to 1, the mode is controlled by these input pins, otherwise the mode register (MR) setting will be taken. 000: NTSC CCIR 100: PAL CCIR 001: NTSC Square Pixel 101: PAL Square pixel 010: NTSC 4Fsc
RESET_I	1	I	Reset input, active low
MV_EN	1	I	Macrovision function Enable
DI	8	I	Parallel I/F data input
DO	8	0	Parallel I/F data output
WID	1	I	Parallel I/F index strobe
WDT	1	I	Parallel I/F data strobe
CVBS	10	O	S-video Luminance data output
YD	10	O	Composite video data output
CD	10	O	S-video Chrominance data output

Function Descriptions

Video data input and sampling rate

The video input data is RGB. Each R, G, or B data is an 8-bit value. The range for the data is 0 to 255 respectively. The data is latched at positive edge of the CLKX1.

The TV Encoder supports the following sampling rates:

Table 16: TV Encoder Sampling Rates

Video Mode		Frequency	Total pixel/line	Total lines/frame
NTSC	CCIR 601	13.5 MHz	858	525
	Square pixel	12.27 MHz	780	525
	4Fsc	14.32 MHz	910	525
PAL	CCIR 601	13.5 MHz	864	625
	Square pixel	14.75 MHz	944	625

Macrovision Antitaping Process

The TV Encoder supports the Macrovision Antitaping process function (U7.01). Macrovision involves 3 functions which are the colorstripe process, Pseudo Sync/AGC pulses with sync pulse amplitude reduction and EOF back porch pulses. If the same line is assigned for closed captioning and the Macrovision process, all Macrovision functions at the line are disabled for the closed captioning function.

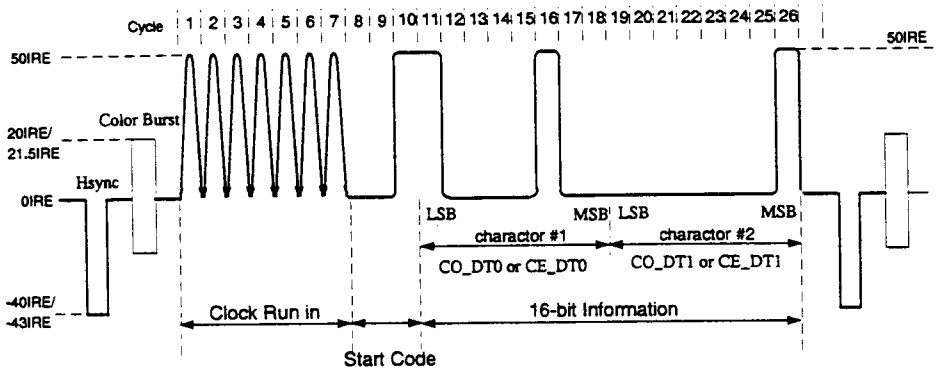
The color stripe process function is applied to the composite video output and the Chrominance signal output. This activated by MCR0[3] and controlled by MCR1 to MCR7 and MCR16 to MCR21. This function controls the color burst length and polarity. When this process is invoked during the burst blanking lines, no color burst signal is put. When the color burst length is assigned beyond the active video time, the color burst completes at the end of the blanking time. Active video data then starts. The blanking time is controlled by the BLANK-L input pin and internal blanking.

The Pseudo Sync/AGC pulse function is applied to the composite video output and the S-video Luminance output. The Pseudo Sync pulse is applied to the Luminance signal. The AGC pulses is a super-white positive going pulse. Both of these pulses are output after color burst signal. The Sync Pulse amplitude reduction changes the synchronizing level. This function is activated by MCR0[5] and MCR0[1:0], and controlled by MCR0[2], MCR8 to MCRI4.

The EOF back porch pulse function generates a high level signal immediately after the trailing edge of the H-sync pulse. The value is 100IRE for NTSC mode and 7OOmV for PAL mode. This function is activated by MCR0[4], and controlled by MCR[15].

Closed Captioning

The closed captioning function is applied to the Luminance data, and is shown at the composite video output and the S-video Luminance output as follows. The level and timing corresponds to the EIA standard EIA-608.



This function is controlled by the closed captioning registers. The closed captioned line is controlled as follows.

Table 17: Closed Captioning Lines

Video Mode	Odd field	Even field
NTSC	CCL + 4	CCL + 263 + 4
PAL	CCL + 1	CCL + 313 + 1

When the closed captioning function is enabled by the CCEN register, the captioning data will be placed on the assigned line. When there is new data, the TV Encoder outputs the new data. When there is no new data, a null code (80h) will be output.

The odd field and even field are controlled separately. When one of 2 odd (even) data registers is written, the TV Encoder recognizes new data for odd (even) field. The status bit OST(EST) is set to 1. For normal usage, the new data is written when the status bit is 1.

Table 18: Closed Captioning Odd Field Output Data

Enable	Status	1st Output Data	2nd Output Data
CCE[0] = 0	-	no data	no data
CCE[0] = 1	OST = 0	CO_DT0	CO_DT1
CCE[0] = 1	OST = 1	80 (hex)	80 (hex)

Table 19: Closed Captioning Even Field Output Data

Enable	Status	1st Output Data	2nd Output Data
CCE[0] = 0	-	no data	no data
CCE[0] = 1	EST = 0	CO_DT0	CE_DT1
CCE[0] = 1	EST = 1	80 (hex)	80 (hex)

Video data output and Over-sampling

The TV Encoder outputs composite video, Luminance and Chrorninance signals. These outputs have 10-bit each, and are 2X over-sampled by the double frequency clock designated CLKX2. This over-sampling simplifies external analog filtering. The output level and timing depend on the mode selected.

Synchronization

This TV Encoder operates in a slave mode. This means that the vertical sync and the horizontal sync are required for operation. The blanking signal is optional. The TV Encoder will calculate the composite blanking time using the sync information. If the blank signal BLANK-L is pulled up, input data at the blanking time will be masked by the internal blanking signal. When the blanking signal is controlled, it's possible to shorten the active time for the input data. The TV Encoder will mask the input data when the BLANK-L is low. The TV Encoder automatically detects the Odd/Even field by sync information.

Sub-carrier Generation

The sub-carrier is internally generated using CLKX1. Depending on the sampling rate, the TV Encoder will automatically calculate exact frequency. The sub-carrier phase is reset under the following conditions:

- RESET-L is low.
- The first field changes to field 1 after RESET- goes high.
- The first field changes to field 1 after the TV Encoder detects the mode change.
- When genlock control is on. For this case, the sub-carrier phase will be reset on every 4 fields for NTSC mode and 8 fields for PAL mode.

Parallel bus I/F

For internal register access, the parallel bus I/F is used. When the write index signal designated WID is high, the register address is latched. When the write data signal designated WDT is high, the data will be written to the latched address.

Chapter 16: Power On Configuration

SM731 Power-On Configurations

- Bit MD[63:0] and MA[11:0] have internal pull-up resistors on the I/O pads
- 0 = external pull-down resistor
- 1 = no external pull-down resistor

Table 20: Power On Configuration

Signal Name	Read/Write	Register Address	IO Address	Description
MD[37]	Config Only			PLL selection. This is a hardware test feature which is used for debug purpose only) Definition: pllvck = new,high performance pll pllvrck = existing pll from SM731 pllmck = existing pll from SM731 pllmck2 = new,high performance pll If MD[37] config = 1 (default) Vclk(video clock) = pllvck VrClk(LCD Panel clock) = pllvrck Mclk(Engine clock) = pllmck Mclk2(memory controller clock) = pllmck2 else Vclk(video clock) = pllvrck VrClk(LCD Panel clock) = pllvrck Mclk(Engine clock) = pllmck / 2 Mclk2(memory controller clock) = pllmck * See also definition of CCR67[3:2]
MD[36:35]	Config Only			Size of Base Memory selection 00=4MB 01=8MB 10=16MB 11=32MB
MD[34]	Config Only			Being used when only one Endian selected 0=Small Endian 1=Big Endian
MD[33]	Config Only			0=Only one Endian 1=Both Endian
MD[32]				Reserved
MD[31]	R/W	MCR76[7]	3c5.76	0=Reserved 1=Normal (default)
MD[30:25]				Reserved
MD[24]	R/W	MCR76[0]	3c5.76	0=SDRAM interface 1=Reserved

Signal Name	Read/Write	Register Address	IO Address	Description
MD[23]				0=AND with RESETN to reset the free running clock divider for simulation and testing 1=Normal (default)
MD[22}				Reserved
MBA[1]	Config Only			0=Enable C0000 EPROM access 1=Disable C0000 EPROM access
MBA[0]	Config Only			0=>PCI Config Reg54[2]=1=>AGP4X capable 1=>PCI Config Reg54[2]=0=>Not AGP4X capable
MA[11:8]	R/W	GPR70[3:0]	3c5.70	Panel ID 0000 = 640x480 TFT 0001 = 800x600 TFT 0010 = 1024x768 TFT 0011 = 1280x1024 TFT 0100 = 1600x1200 TFT
MA[7]	R/W			AGP pad configuration 0=For 1.5V AGP bus 1=For 3.3V AGP bus
MA[6]	R/W			LVDS interface 0 = 18 bit TFT 1 = 24 bit TFT
MA[5]	R/W			LVDS Panel 0 = MSB of R,G,B at TX3-+. For 24 bits LVDS 1 = LSB of R,G,B at Tx3-+. For 24 bits LVSDS (Hitachi type)
MA[4]	R/W			Panel Sequence 0 = Software panel on/off sequence 1 = Hardware panel on/off sequence
MA[3]	R/W			LVDS Configuration 0 = Use double LVDS configuration (two LVDS chips on panel side) 1 = Use single LVDS configuration (only single LVDS receiver on panel)
MA[2:1]	R/W			00=Reserved 01=Select non-LVDS panel as primary panel display 10=Select LVDS1 as primary panel display 11=Both LVDS1 and non-LVDS panel as primary panel display
MA[0]	R/W			Reserved for software purposes
MD[21:0]				Reserved

Note: For Windows XP, Windows NT, Windows 9X, and Windows Me, the setting for MD [36:35, 33] should be set at [111]. However, for Windows CE, the setting for MD [36:35, 33] should be set at [1,0,0].

Chapter 17: Register Overview & Usage

Register Types

There are three general types of registers used on the SM731:

PCI Configuration Registers

The PCI Configuration registers are listed in Chapter 18: PCI Configuration Space Registers and accessed via the standard PCI read/write protocols specified in the PCI specification.

Memory Mapped I/O Registers

All the I/O mapped registers within SM731 have been designed to be memory mapped as well. They are listed in Chapter 19: Standard VGA Registers and Chapter 20: Extended SMI IO Mapped Registers. “I/O” or “Memory” Mapping is selected through PCI configuration registers CSR04 bit 0 and bit 1.

- Access via “I/O” space is done by first writing the index value into the I/O register 3C4. Thereafter, the indexed register can be accessed via I/O read/write to I/O address 3C5

  Example: Register with Index 0/H
  I/O write 0/H to 3C4
  I/O read/write to/from 3C5

- The procedure to access these registers via “Memory” Mapped space is similar to “I/O” space; with the index register being moved to memory address 6C03C4 and access register to 6C03C5.

  Example: Register with Index 0/H
  Memory write 0/H to 6C03C4
  Memory read/write to/from 6C03C5

Memory Mapped Registers

All the advanced functions of SM731 are controlled through Memory Mapped registers. Such as the 2D and 3D motion compensation video registers, PCI bus master control registers, TV encoder registers and 3D registers. The following diagram illustrates the Memory Mapped register address assignment.

All the memory mapped registers can be accessed though the IO port 3cd & 3cf. As described by the following table.

3ce = 20	Address[7:0]
3ce = 21	Address[15:8]
3ce = 22	Address[23:16]
3ce = 23	Address[31:24] *
3ce = 24	Data[7:0]

3ce = 25	Data[15:8]
3ce = 26	Data[23:16]
3ce = 27	Data[31:24]
3ce = 28-2F	Activate Write/Read the IOAccess Command
3cf[7:4]	Reserved
3cf[3:0]	Byte Enable

* Address [31:30] Represent Different Ways of access
[31:30] = 2'b00: Linear Memory Map IO Access
[31:30] = 2'b01: Linear Memory Access

MMIO Write

Use IO write 3ce 20-27 to fill up the address and data. Use IO Write 3ce 28
Example: MMIO Address = 32'h00002800; Data = 32'haabbccdd; Byte Enable = 4'b0000

iowr_w(32'h3ce,32'h00000020);	// MMIO 20 word write
iowr_w(32'h3ce,32'h00002821);	// MMIO 21 word write
iowr_w(32'h3ce,32'h00000022);	// MMIO 22 word write
iowr_w(32'h3ce,32'h00000023);	// MMIO 23 word write
iowr_w(32'h3ce,32'h0000dd24);	// MMIO 24 word write
iowr_w(32'h3ce,32'h0000cc25);	// MMIO 25 word write
iowr_w(32'h3ce,32'h0000bb26);	// MMIO 26 word write
iowr_w(32'h3ce,32'h0000aa27);	// MMIO 27 word write
iowr_w(32'h3ce,32'h00000028);	// MMIO 28 with Byte Enable 4'b0000

MMIO Read

Use IO write 3ce 20-23 to fill up the address. Use IO Read with index 3ce=28 to activate and read 3ce 24-27 for data.
Example: MMIO Address = 32'h00002800

iowr_w(32'h3ce,32'h00000020);	// MMIO 20 word write
iowr_w(32'h3ce,32'h00002821);	// MMIO 21 word write
iowr_w(32'h3ce,32'h00000022);	// MMIO 22 word write
iowr_w(32'h3ce,32'h00000023);	// MMIO 23 word write
iowr_b(32'h3ce,32'h00000028);	// update 3ce index = 28
iord_b(32'h3cf,data);	// Execute IO Read. Don't care the data
iowr_b(32'h3ce,32'h00000024);	// MMIO 24 index write
iord_b(32'h3cf,data);	// MMIO Read Data[7:0]
iowr_b(32'h3ce,32'h00000025);	// MMIO 25 index write
iord_b(32'h3cf,data);	// MMIO Read Data[15:8]
iowr_b(32'h3ce,32'h00000026);	// MMIO 26 index write

iord_b(32'h3cf,data);	// MMIO Read Data[23:16]
iowr_b(32'h3ce,32'h00000027);	// MMIO 27 index write
iord_b(32'h3cf,data);	// MMIO Read Data[31:24]

Linear Memory Write

Use IO write 3ce 20-27 to fill up the address and data. Use IO Write 3ce 28
Example: Lmem Address = 32'h40002800; Data = 32'haabbccdd; Byte Enable = 4'b0000

iowr_w(32'h3ce,32'h00000020);	// MMIO 20 word write
iowr_w(32'h3ce,32'h00002821);	// MMIO 21 word write
iowr_w(32'h3ce,32'h00000022);	// MMIO 22 word write
iowr_w(32'h3ce,32'h00004023);	// MMIO 23 word write
iowr_w(32'h3ce,32'h0000dd24);	// MMIO 24 word write
iowr_w(32'h3ce,32'h0000cc25);	// MMIO 25 word write
iowr_w(32'h3ce,32'h0000bb26);	// MMIO 26 word write
iowr_w(32'h3ce,32'h0000aa27);	// MMIO 27 word write
iowr_w(32'h3ce,32'h00000028);	// MMIO 28 with Byte Enable 4'b0000

Linear Memory Read

Use IO write 3ce 20-23 to fill up the address. Use IO Read with index 3ce=28 to activate and read 3ce 24-27 for data.
Example: Lmem Address = 32'h40002800

iowr_w(32'h3ce,32'h00000020);	// MMIO 20 word write
iowr_w(32'h3ce,32'h00002821);	// MMIO 21 word write
iowr_w(32'h3ce,32'h00000022);	// MMIO 22 word write
iowr_w(32'h3ce,32'h00004023);	// MMIO 23 word write
iowr_b(32'h3ce,32'h00000028);	// update 3ce index = 28
iord_b(32'h3cf,data);	// Execute IO Read. Don't care the data
iowr_b(32'h3ce,32'h00000024);	// MMIO 24 index write
iord_b(32'h3cf,data);	// MMIO Read Data[7:0]
iowr_b(32'h3ce,32'h00000025);	// MMIO 25 index write
iord_b(32'h3cf,data);	// MMIO Read Data[15:8]
iowr_b(32'h3ce,32'h00000026);	// MMIO 26 index write
iord_b(32'h3cf,data);	// MMIO Read Data[23:16
iowr_b(32'h3ce,32'h00000027);	// MMIO 27 index write
iord_b(32'h3cf,data);	// MMIO Read Data[31:24]

I/O Mapped Register Mapped Summary

IBM VGA Sequencer Registers	Index 0-4
System Control Registers	Index 10-1F
Power Down Control Registers	Index 20-24
Memory Control Registers	Index 60-63
Clock or Power Down Control Registers in PPR Block	Index 63 - 6F, Index 94 - 9e
USR0-3 Ports Control Registers General Purpose Control Registers	Index 70-73
Scratch Registers	Index 74-75
Memory Control Registers	Index 76
Monitor Detect and CRT/TV DAC Test Registers	Index 7A-7D
CRT HWC Pop Icon Registers	Index 80-8D
CRT Pop Icon Registers	Index 90-93

Figure 22: I/O Port 3C4

IBM VGA CRTC Registers	Index 0-26
Extended CRTC Control Registers	Index 30-3C
Scratch Registers	Index 3D-3F
CRT Shadow Registers	Index 40-4D
TV Encoder Control Registers	Index 6X-8X
Screen Centering & Expansion Control	Index 90-9F; Index A0-AD

Figure 23: I/O Port 3?4

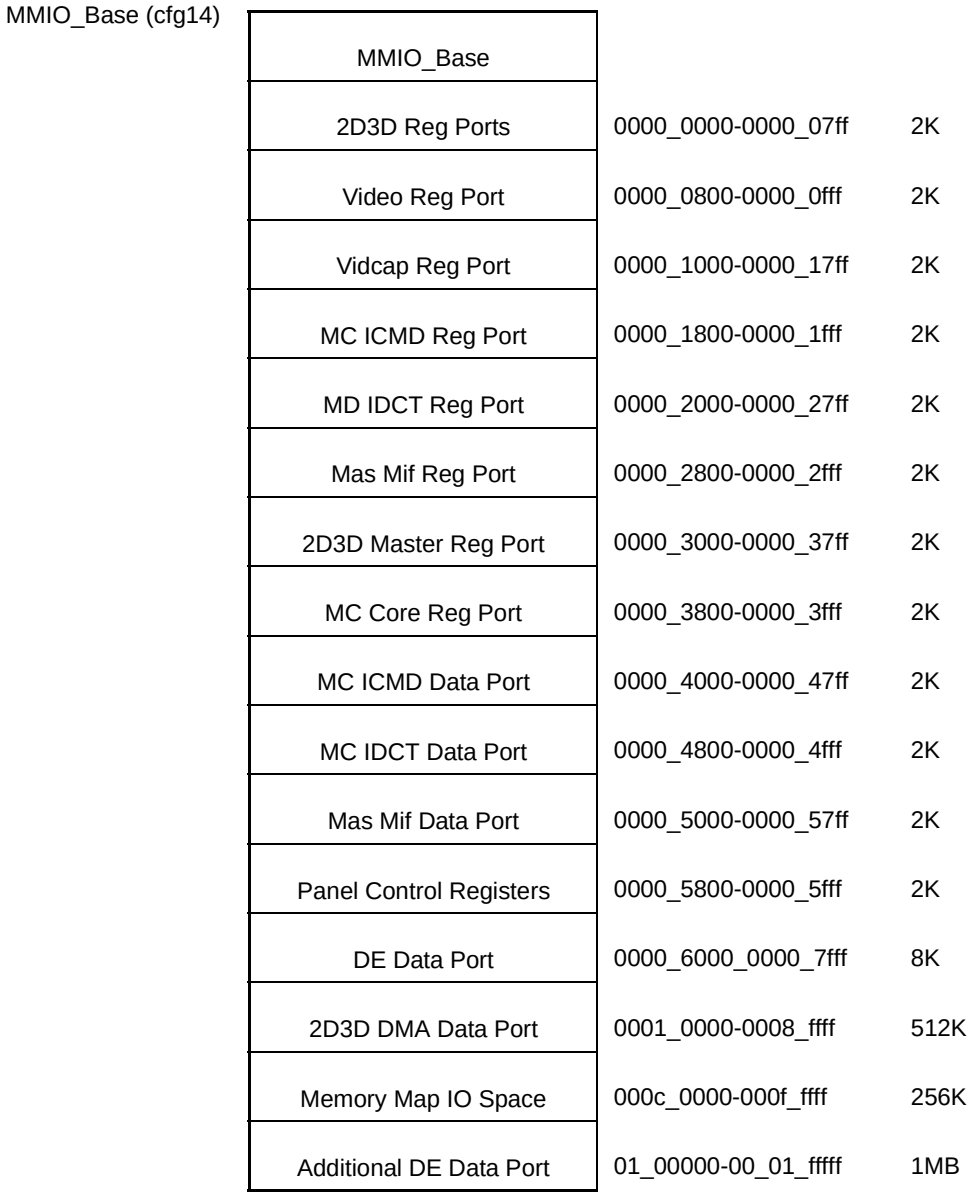


Figure 24: Memory Mapped Address Diagram

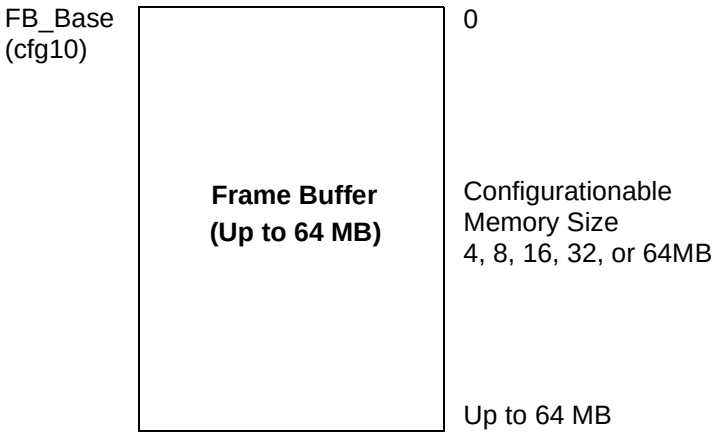


Figure 25: Frame Buffer Memory Space
(32MB for single endian, 64MB for bi-endian)

Chapter 18: PCI Configuration Space Registers

Table 21: PCI Configuration Registers Quick Reference

PCI Configuration Space Registers

The PCI specification defines the configuration space for auto-configuration (plug-and-play), device and memory relocation.

CSR00: Vendor ID and Device ID

Read Only Address: 00h
Power-on Default: 0730126Fh

This register specifies the vendor ID

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DEVICE ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VENDOR ID															

Bit 31:16 Device ID
These bits are hardwired to 0730h to identify the device as SM731.

Bit 15:0 Vendor ID
These bits are hardwired to 126Fh to identify as Silicon Motion®, Inc.

CSR04: Command and Status

Read/Write Address: 04h Note: Reserved bits are read only
Power-on Default: 02300000h

This register controls which types of PCI command cycles are supported by SM731.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPE	**R**		**DTA**	**R**	**DEVSEL**		**RESERVED**			**66C**	**NCD**	**RESERVED**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										**PSE**	**MWR**	**R**	**PBM**	**MS**	**IO**

Bit 31 (DPE) Data Parity Error Detected (Read Only)
0 = Correct
1 = Error Detected

Bit 30:29 Reserved

Bit 28 (DTA) Received Target Abort (Read Only)
0 = Correct
1 = Abort Detected

Bit 27 Reserved

Bit 26:25 (DEVSEL) Timing Select Medium (Read Only)

Bit 24:22 Reserved

Bit 21 66 MHz Capable (Read Only)

Bit 20 (NCD) New Capability Definition (Read Only)

Bit 19:6 Reserved

Bit 5 (PSE) Palette Snooping Enable (Read/Write)
0 = Disable
1 = Enable

Bit 4 (MWR) Memory Write and Invalidate Enable (Read/Write)
0 = Disable
1 = Enable

Bit 3 Reserved

Bit 2 (PBM) PCI Bus Master Enable (Read/Write)
0 = Disable
1 = Enable

Bit 1 (MS) Memory Space Access Enable (Read/Write)
0 = Disable
1= Enable

Bit 0 (IO) IO Space Access Enable (Read/Write)
0 = Disable
1 = Enable

CSR06: Status

Read Only Address: 06h
Power-on Default: 20h

This register controls device select timing status, detect parity status, and detects target abort status for SM731. In order to clear any bit of this register, you must write a "1" to that particular bit.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPE	**RESERVED**		**DTA**	**R**	**TS**		**RESERVED**								

Bit 31:16 Reserved

Bit 15 Detect Parity Error (DPE)

Bit 14:13 Reserved (R)

Bit 12 Detect Target Abort for Master Mode (DTA)

Bit 11 Reserved (R)

Bit 10:9 ~DEVSEL Timing Select (TS)
01 = medium speed (hardwired)

Bit 8:0 Reserved

CSR08: Revision ID and Class Code

Read Only Address: 08h
Power-on Default: 030000A0h

This register specifies the silicon revision ID and the Class Code that the silicon supports.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE CLASS CODE								**SUBCLASS CODE**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG LEVEL PROGRAMMING INTERFACE								**REVISION ID**							

Bit 31:24 Base Class Code
03h = for Video Controller

Bit 23:16 Subclass Code
00h = VGA

Bit 15:8 Register Level Programming Interface
00h = hardwired setting

Bit 7:0 Revision ID
For example, A0h = revision A; B0h = revision B

CSR0C: Latency Timer

Read Only Address: 0Dh
Power-on Default: 00h

This register specifies the latency timer that SM731 supports for burst master mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LATENCY TIMER								**RESERVED**							

Bit 31:16 Reserved

Bits 15:8 (LT) Latency Timer (Read/Write)
Default = 00h

Bit 7:0 Reserved

CSR10: Linear Frame Buffer Base Address Register

Read/Write Address: 10h (Note: Reserved bits are read only)
Power-on Default: 0000000h

This register specifies the PCI configuration space for address relocation

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LINEAR ADDRESSING MEMORY BASE						**RESERVED**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															**MSI**

Bit 31:26 Linear Addressing Memory Base Address. Memory segment allocated within 64 MB boundary
If 4 MB with One Endian:
Bit 25:22 = FBA (Read/Write)

If 8 MB with One Endian:
Bit 25:23 = FBA (Read/Write)
Bit 22 = 0b (Read Only)

If 16 MB with One Endian:
Bit 25:24 = FBA (Read/Write)
Bit 23:22 = 00b (Read Only)

If 32 MB with One Endian:
Bit 25 = FBA (Read/Write)
Bit 24:22 = 000b (Read Only)

If 4 MB with Big and Small Endian:
Bit 25:23 = FBA (Read/Write)
Bit 22 = 0b (Read Only)

If 8 MB with Big and Small Endian:

Bit 25:24 = FBA (Read/Write)
Bit 23:22 = 00b (Read Only)

If 16 MB with Big and Small Endian:
Bit 25 = FBA (Read/Write)
Bit 24:22 = 000b (Read Only)

If 32 MB with Big and Small Endian:
Bit [25:22] = 0000b (Read Only)

Bit 21:1 Linear Frame Buffer Base Address (Read Only)
Default = 000000h

Bit 0 (MB) Memory Base Read (Only)
Default = 0b

CSR14: Base Address Register for Memory Map Address

Read/Write Address: 14h (Note: Reserved bits are read only)
Power-on Default: 0000000h

This register specifies the PCI configuration space for address relocation

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LINEAR ADDRESSING MEMORY BASE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															**MB**

Bit 31:21 (FBA) Memory Map Address Base Address (R/W/R)
If One Endian:
Bit [31:21] = FBA (Read/Write)

If Big and Small Endian:
Bit [31:22] = FBA (Read/Write)
Bit [21] = 0b (Read Only)

Bit 20:1 (ABA) Memory Map Address Base Address (Read Only)
Default = 000000h

Bit 0 (MB) Memory Base (Read Only)
Default = 0b

CSR2C: Subsystem ID and Subsystem Vendor ID

Read Only Address: 2Ch
Power-on Default: 00000000h

This register specifies both the Subsystem device ID and the Subsystem Vendor ID.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SUBSYSTEM ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBSYSTEM VENDOR ID															

Bit 31:16 Subsystem ID. This System ID is written by the system BIOS during POST

Bit 15:0 Subsystem Vendor ID

CSR30: Expansion ROM Base Address

Read/Write Address: 30h
Power-on Default: 00000000h

This register specifies the expansion ROM base address. (Note: Reserved bits are read only.)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROM BASE ADDRESS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															**BIOS**

Bit 31:16 ROM Base Address. Memory segment allocated for BIOS ROM in 64KB boundary [15:0]

Bit 15:1 Reserved

Bit 0 BIOS Address Decode Enable. This bit is valid only if memory space access is enabled (CSR04 bit 1 = 1)
0 = Disable
1 = Enable

CSR34: Power Down Capability Pointer

Read Only Address: 34h
Power-on Default: 00000040h

This register contains the address where PCI power down management registers are located

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POWER DOWN CAPABILITY POINTER															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POWER DOWN CAPABILITY POINTER															

Bit 31:0 Capability pointer contains the address where the PCI Power Down Management Register is located.

CSR3C: Interrupt Pin and Interrupt Line

Read/Write Address: 3Ch
Power-on Default: 00000000h

This register specifies the PCI Interrupt Pin and Line.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERRUPT PIN (READ ONLY)								**INTERRUPT LINE (READ/WRITE)**							

Bit 31:16 Reserved

Bit 15:8 Interrupt Pin (Read only)

Bit 7:0 Interrupt Line (Read/write)

CSR40: Power Down Capability Register

Read Only Address: 40h
Power-on Default: 0601X001h

This register contains the address where PCI power down management Capabilities.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI POWER DOWN MANAGEMENT CAPABILITY (0601h)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT CAPABILITY POINTER LINK LIST								**PCI POWER DOWN MGMT CAPABILITY (01h)**							

Bit 31:16 PCI Power Down Management Capability = 0601h
Offset 2

Bit 15:8 If AGP Enabled:
Next Capability Pointer Link List = 50h
Offset 1
If PCI Only:
No More Extra Capability Pointer = 00h

Bit 7:0 PCI Power Down Management Capability ID= 01h
Offset 0

CSR44: Power Down Capability Data

Read/Write Address: 44h
Power-on Default: 00h

This register contains the address where PCI power down management Control, Status and Data are located.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA								**RESERVED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI POWER DOWN MGMT CONTROL/STATUS														**PDS**	

Bit 31:24 Data
Read Only. Offset 7

Bit 23:16 Reserved =00
Offset 6

Bit 15:2 PCI Power Down Management Control/Status
Offset 4

Bit 1:0 Power down management control and status
00 = Power Down Management State D0
01 = Power Down Management State D1
10 = Power Down Management State D2
11 = Power Down Management State D3

CSR50: AGP Capability Pointer

Read/Write Address: 50h
Power-on Default: 00200002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**MAJOR/MINOR REVISION**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT CAPABILITY POINTER								**AGP CAPABILITY ID**							

Bit 31:24 Reserved

Bit 23:16 Major/minor revision = 20h

Bit 15:8 Next capability pointer = 00h

Bit 7:0 AGP Capability ID = 02h

CSR54: AGP Status Pointer

Read Only Address: 54h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQUEST DEPTH								**RESERVED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**SBA**	**RESERVED**			**4GS**	**FWE**	**R**	**AGP4X**	**AGP2X**	**AGP1X**

Bit 31:24 Request Depth (= 0F)

Bit 23:10 Reserved

Bit 9 Side Bus Addressing Enabled (SBA) (= 1)

Bit 8:6 Reserved

Bit 5 4 GB Support (= 0)

Bit 4 Fast Write Enabled (= 0)

Bit 3 Reserved (R)

Bit 2 AGP4X Capable (Read Only)
1 If power-on configured MBA[0] = 0
0 If power-on configured MBA[0] = 1

Bit 1 AGP2X Capable (Read Only)
1 If SCR26[5] = 0
0 If SCR26[5] = 1

Bit 0 AGP1X Capable (Read Only)
1 If SCR26[4] = 0
0 If SCR24[4] = 1

CSR58: AGP Command Register

Read/Write Address: 58h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				**REQUEST DEPTH**				**RESERVED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**SBA**	**AGP**	**RESERVED**		**4GS**	**FWE**	**R**	**DATA RATE**		

Bit 31:28 Reserved (Maximum of 16 requests)

Bit 27:24 Request Depth

Bit 23:10 Reserved

Bit 9 Side Bus Addressing Enabled (SBA)
0 = Disable
1 = Enable

Bit 8 AGP Enabled
0 = Disable
1 = Enable

Bit 7:6 Reserved

Bit 5 4 GB Support

Bit 4 Fast Write Enabled

Bit 3 Reserved (R)

Bit 2:0 Data Rate
001 = 1X
010 = 2X
100 = 4X

Extended SMI Registers

LOCK: Extended Register Write Protect Control

Read/Write Address: 3C3h
Power-on Default: 00h

This register specifies write protect controls for the SMI extended registers. SMI extended registers are write-protected. In order to write to the SMI extended registers, one must write Bit [7:5] = 010b.

7	6	5	4	3	2	1	0
WPE			**RESERVED**				

Bit 7:5 Write Protect Enable (WPE)
101 = All SMI Extended registers are Write-Protected
010 = Enable writes to SMI Extended registers
Others = Maintain previous state

Bit 4:0 Reserved

Chapter 19: Standard VGA Registers

Table 22: Standard VGA Registers Quick Reference

Standard VGA Registers

In the following registers description, a '?' in an address stands for a hexadecimal value of either 'B' or 'D'. If Bit 0 of the Miscellaneous Output Register is set to 1, the address is based at 3Dxh for color emulation. If Bit 0 of the Miscellaneous Output Register is set to 0, the address is based at 3Bxh for monochrome emulation.

General Registers

MISC: Miscellaneous Output Register

Write Only Address: 3C2h
Read Only Address: 3CCh
Power-on Default: 00h

7	6	5	4	3	2	1	0
VSP	**HSP**	**OEM**	**R**	**VIDEO CLOCK**		**EVR**	**IO**

Bit 7 Vertical Sync Polarity Select (VSP)
0 = positive vertical sync polarity
1 = negative vertical sync polarity

Bit 6 Horizontal Sync Polarity Select (HSP)
0 = positive horizontal sync polarity
1 = negative horizontal sync polarity

Bit 5 Odd/Even Memory Page Select (OEM)
0 = Select lower 64K page of memory
1 = Select upper 64K page of memory

Bit 4 Reserved (R)

Bit 3:2 Video Clock Select
00 = Select 25.175MHz for 640 dots/line mode
01 = Select 28.322MHz for 720 dots/line mode
10 = Reserved (enable external clock source)
11 = Reserved (enable external clock source)

Bit 1 Enable Video RAM Access from CPU (EVR)
0 = Disable Video RAM access from CPU
1 = Enable Video RAM access from CPU

Bit 0 I/O Address Select (IO)
0 = Select monochrome mode. Address based at3Bxh.
1 = Select for color mode. Address based at 3Dxh

ISR0: Input Status Register 0

Read Only Address: 3C2h
Power-on Default: Undefined

7	6	5	4	3	2	1	0
CRT	**RESERVED**		**MDS**	**RESERVED**			

Bit 7 CRT Vertical Retrace Interrupt (CRT)
0 = Vertical Retrace Interrupt is cleared
1 = Vertical Retrace Interrupt is pending.

Bit 6:5 Reserved

Bit 4 Monitor Detect Status (MDS)
0 = Monochrome display is detected
1 = Color display is detected

Bit 3:0 Reserved

ISR1: Input Status Register 1

Read Only Address: 3?Ah
Power-on Default: Undefined

7	6	5	4	3	2	1	0
RESERVED		**COLOR PLANE**		**VRS**	**R**	**DISPLAY ENABLE**	

Bit 7:6 Reserved

Bit 5:4 Color Plane Diagnostics
These bits return two of the 8 video outputs VID0-VID7, as selected by Color Plane Enable Register [5:4]

Bit 3 Vertical Retrace Status (VRS)
0 = In display mode
1 = In vertical retrace mode

Bit 2:1 Reserved (R)

Bit 0 Display Enable
0 = In display mode
1 = Not in display mode. (it is either in horizontal or vertical retrace mode)

FCR: Feature Control Register

Write Only Address: 3?Ah
Read Only Address: 3CAh
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**VSC**	**RESERVED**		

Bit 7:4 Reserved

Bit 3 Vertical Sync Control
0 = VSYNC output is enabled
1 = VSYNC output is logical 'OR' of VSYNC and Vertical Display Enable

Bit 2:0 Reserved

Sequencer Register

SEQX: Sequencer Index Register

Read/ Write Address: 3C4h
Power-on Default: Undefined

7	6	5	4	3	2	1	0
RESERVED				**SEQUENCER ADDRESS/INDEX**			

Bit 7:4 Reserved

Bit 3:0 Sequencer Address/Index
The Sequencer address register is written with the index value of the sequencer register to be accessed.

SEQ00: Reset Register

Read/ Write Address: 3C5h, Index: 00h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED						**SR**	**AR**

Bit 7:2 Reserved

Bit 1 Synchronous Reset (SR)
0 = Sequencer is cleared and halted synchronously
1 = Normal operating mode

Bit 0 Asynchronous Reset (AR)
0 = Sequencer is cleared and halted asynchronously
1 = Normal operating mode

SEQ01: Clocking Mode Register

Read/ Write Address: 3C5h, Index: 01h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**SO**	**VS**	**DCS**	**SL**	**R**	**DC**

Bit 7:6 Reserved

Bit 5 Screen Off (SO)
0 = Normal operating mode
1 = Screen is turned off but SYNC signals remain active

Bit 4 Video Serial Shift Select (VS)
0 = Load video serializer every or every other character or clock, depending on Bit2 of this register.
1 = Load video serializer every 4th character clock

Bit 3 Dot Clock Select (DCS)
0 = Normal dot clock select by VCLK input frequency
1 = Dot clock is divided by 2 (320/360 pixel mode)

Bit 2 Shift Load (SL)
0 = Load video serializer every character or clock
1 = Load video serializer every other character or clock

Bit 1 Reserved (R)

Bit 0 8/9 Dot Clock (DC)
0 = 9 dot wide character clock
1 = 8 dot wide character clock

SEQ02: Enable Write Plane Register

Read/ Write Address: 3C5h, Index: 02h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**ENABLE WRITING**			

Bit 7:4 Reserved

Bit 3:0 Enable Writing to Memory Maps 3 through 0 (respectively)
0 = Disable writing to corresponding plane
1 = Enable writing to corresponding plane

SEQ03: Character Map Select Register

Read/ Write Address: 3C5h, Index: 03h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**SCM**	**SCMB**	**SCMA**	**SCMA**	**SCMB**	**SCMB**

Bit 7:6 Reserved

Bit 5,3,2 Select Character Map A (SCMA)

This value select the portion of plane 2 used to generate text character when bit 3 of this register = 0, according to the following table:

Bit 5,3,2	Font Table Location
000	First 8K of plane 2
100	Second 8K of plane 2
001	Third 8K of plane 2
101	Fourth 8K of plane 2
010	Fifth 8K of plane 2
110	Sixth 8K of plane 2
011	Seventh 8K of plane 2
111	Eighth 8K of plane 2

Bit 4,1,0 Select Character Map B (SCMB)

This value select the portion of plane 2 used to generate text character when bit 3 of this register = 1, according to the same table as character Map A

SEQ04: Memory Mode Register

Read/ Write Address: 3C5h, Index: 04h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**CM**	**SSA**	**EVM**	**R**

Bit 7:4 Reserved

Bit 3 Chained 4 Map (CM)
0 = Enable odd/even mode
1 = Enable Chain 4 mode. Uses the two lower bits of CPU address to select plane in video memory as follows:

MA1	MA0	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 Select Sequential Addressing Mode (SSA). This bit affects only CPU write data accesses into video memory. Bit 3 of this register must be 0 for this bit to be effective.
0 = Enable the odd/even addressing mode. Even addresses access planes 0 and 2, and odd addresses access plane 1 and 3
1 = Enable system to use a sequential addressing mode

Bit 1 Extended Video Memory Enable (EVM)
0 = Memory access restricted to 16/32K
1 = Enable extended video memory access. Allows complete memory access to 256K

Bit 0 Reserved (R)

CRTC Controller Registers

The CRTC registers are located at two locations in I/O address space. These registers are accessed by first writing to the index register (3?4h), then writing to the data register (3?5h). The I/O address is either 3Bxh or 3Dxh depending on bit 0 of the Miscellaneous Output Register at 3C2h.

CRTX: CRTC Controller Index Register

Read/Write Address: 3?4h
Power-on Default: 00h

This register is loaded with a binary value that indexes the CRTC controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED			CRTC ADDRESS INDEX				

Bit 7:5 Reserved

Bit 4:0 CRTC Address Index
These bits specify the CRTC register to be addressed. Its value is programmed in hexadecimal.

CRT00: Horizontal Total Register

Read/Write Address: 3?5h, Index 00h
Power-on Default: Undefined

This register defines the number of character clocks from HSYNC going active to the next HSYNC going active.

7	6	5	4	3	2	1	0
HORIZONTAL TOTAL							

Bit 7:0 Horizontal Total
This value = (number of character clocks per scan line) - 5.

CRT01: Horizontal Display End Register

Read/Write Address: 3?5h, Index 01h
Power-on Default: Undefined

This register defines the number of character clocks for one horizontal line active display. This register is locked when FPR33 (SC5h, index 33) bit 5 = 1. Please refer to FPR33 register.

7	6	5	4	3	2	1	0
HORIZONTAL DISPLAY ENABLE							

Bit 7:0 Horizontal Display Enable
This value = (number of character clocks during active display) - 1.

CRT02: Horizontal Blank Start Register

Read/Write Address: 3?5h, Index 02h
Power-on Default: Undefined

This register defines the number of character clocks at which horizontal ~Blank is asserted.

7	6	5	4	3	2	1	0
HORIZONTAL BLANK START							

Bit 7:0 Horizontal Blank Start
This value = character value at which ~Blank signal becomes active.

CRT03: Horizontal Blank End Register

Read/Write Address: 3?5h, Index 03h
Power-on Default: Undefined

This register defines the display enable skew and pulse width of ~Blank signal.

7	6	5	4	3	2	1	0
R	**DISPLAY ENABLE**		**HORIZONTAL BLANK END**				

Bit 7 Reserved

Bit 6:5 Display Enable Skew. These 2 bits define the display enable signal skew timing in relation to horizontal synchronization pulses.

DESKW1	DESKW0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0 Horizontal Blank End
Horizontal Blank End has a 6-bit value. This register contains the least significant 5-bits of this value. Bit 6 of this value is at CRTC index 05 bit 7.

CRT04: Horizontal Sync Pulse Start Register

Read/Write Address: 3?5h, Index 04h
Power-on Default: Undefined

This register is used to adjust screen position horizontally and to specify the position at which HSYNC is active.

7	6	5	4	3	2	1	0
HORIZONTAL SYNC PULSE START							

Bit 7:0 Horizontal Sync Pulse Start
This value = character clock count value at which HSYNC becomes active.

CRT05: End Horizontal Sync Pulse Register

Read/Write Address: 3?5h, Index 05h
Power-on Default: Undefined

This register defines the horizontal sync skew and pulse width of HSYNC signal.

7	6	5	4	3	2	1	0
HBE	**HSS**		**HORIZONTAL SYNC END**				

Bit 7 Horizontal Blank End Bit 5. This bit is End Horizontal Blank Bit 5. (HBE)

Bit 6:5 Horizontal Sync Skew. (HSS)
These 2-bits define the HSYNC signal skew timing in relation to horizontal synchronization pulses.

HSSKW1	HSSKW0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0 Horizontal Sync End
Horizontal Sync End has a 5-bit value. This value defines the character clock counter value at which HSYNC signal becomes inactive.

CRT06: Vertical Total Register

Read/Write Address: 3?5h, Index 06h
Power-on Default: Undefined

This register defines the number of scan lines from VSYNC going active to the next VSYNC going active. Vertical total has a 11-bit value. Bit 8 of this value is located at CRT07 bit 0. Bit 9 of this value is located at CRT07 bit 5. Bit 10 of this value is located at CRT30 bit 3.

7	6	5	4	3	2	1	0
VERTICAL TOTAL							

Bit 7:0 Vertical Total
Vertical Total has a 11-bit value. This register contains the least significant 8-bits of this value. This value = (number of scan lines from VSYNC going active to the next VSYNC) - 2. Bit 8 is in CRT07 bit 0. Bit 9 is in CRT 07 bit 5. Bit 10 is in CRT30 bit 3.

CRT07: Overflow Vertical Register

Read/ Write Address: 3?5h, Index: 07h
Power-on Default: Undefined

This register specifies the CRTC vertical overflow registers.

7	6	5	4	3	2	1	0
VSS	**VDE**	**VT**	**LC**	**VBS**	**VSS**	**VDE**	**VT**

Bit 7 Vertical Sync Start Bit 9 (VSS)

Bit 6 Vertical Display Enable End Bit 9. This bit is locked when FPR33 (SC5h, index 33) bit 5 = 1. Please refer to FPR33 register. (VDE)

Bit 5 Vertical Total Bit 9 (VT)

Bit 4 Line Compare Bit 8 (LC)

Bit 3 Vertical Blank Start Bit 8 (VBS)

Bit 2 Vertical Sync Start Bit 8 (VSS)

Bit 1 Vertical Display Enable End Bit 8. This bit is locked when FPR33 (SC5h, index 33) bit 5 = 1. (VDE)

Bit 0 Vertical Total Bit 8 (VT)

CRT08: Preset Row Scan Register

Read/Write Address: 3?5h, Index 08h
Power-on Default: Undefined

This register is used for panning and text scrolling.

7	6	5	4	3	2	1	0
R	**BYTE PLANNING**		**PRESET ROW SCAN COUNT**				

Bit 7 Reserved (R)

Bit 6:5 Byte Panning Control. These 2-bits controls the number of bytes to pan.

BPC1	BPC0	Operation
0	0	Normal
0	1	1 Byte left shift
1	0	2 Bytes left shift
1	1	3 Bytes left shift

Bit 4:0 Preset Row Scan Count
These bits preset the vertical row scan counter once after each vertical retrace. This counter is automatically incremented by 1 after each horizontal sync period. Once the maximum row scan count is reached, this counter is cleared. This is useful for smoothing vertical text scrolling.

CRT09: Maximum Scan Line Register

Read/Write Address: 3?5h, Index 09h
Power-on Default: Undefined

This register defines the maximum number of scan lines per character row and provides one scanning control and two overflow bits

7	6	5	4	3	2	1	0
EDS	**LC**	**VB**	**MAXIMUM SCAN LINE**				

Bit 7 Enable Double Scan (EDS)

0 = Normal Operating
1 = Enable Double Scan. The row scan counter is clocked at half of the horizontal scan rate.

Bit 6 Line Compare Register Bit 9 (LC)

Bit 5 Vertical Blank Start Register Bit 9 (VB)

Bit 4:0 Maximum Scan Line
This value equals to the total number of scan lines per character row - 1

CRT0A: Cursor Start Scan Line Register

Read/Write Address: 3?5h, Index 0Ah
Power-on Default: Undefined

This register defines the row scan of a character line at which the cursor begins and enable/disable cursor.

7	6	5	4	3	2	1	0
RESERVED		**EC**	**CURSOR START SCAN LINE**				

Bit 7:6 Reserved

Bit 5 Enable Cursor (EC)
0 = Cursor is on
1 = Cursor is off

Bit 4:0 Cursor Start Scan Line
This value equals to the starting cursor row within the character box. If this value is programmed with a value greater than the Cursor End Scan Line Register (3?5h, index 0Bh), no cursor will be displayed.

CRT0B: Cursor End Scan Line Register

Read/Write Address: 3?5h, Index 0Bh
Power-on Default: Undefined

This register defines the row scan of a character line at which the cursor begins and enable/disable cursor.

7	6	5	4	3	2	1	0
R	**CURSOR SKEW**		**CURSOR END SCAN LINE**				

Bit 7 Reserved (R)

Bit 6:5 Cursor Skew. These 2 bits defines the cursor delay skew, which moves the cursor to the right, in character clock.

CSKW1	CSKW0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0 Cursor End Scan Line
This value equals to the ending cursor row within the character box. If this value is programmed with a value less than the Cursor Start Scan Line Register (3?5h, index 0Ah), no cursor will be displayed.

CRT0C: Display Start Address High Register

Read/Write Address: 3?5h, Index 0Ch
Power-on Default: Undefined

This register defines the high order first address after a vertical retrace at which the display on the screen begins on each screen refresh. This value is a 19-bit value. Bit [18:16] are located in CRT30 bit [6:4]. Bit [7:0] are located in CRT0D.

7	6	5	4	3	2	1	0
DIPLAY START ADDRESS [15:8]							

Bit 7:0 Display Start Address [15:8]
This register is the high order byte of the address [15:8].

CRT0D: Display Start Address Low Register

Read/Write Address: 3?5h, Index 0Dh
Power-on Default: Undefined

This register defines the low order first address after a vertical retrace at which the display on the screen begins on each screen refresh. This value is a 19-bit value. Bit [18:16] are in CRT30 bit [6:4]. Bit [15:8] are in CRT0C.

7	6	5	4	3	2	1	0
START ADDRESS [7:0]							

Bit 7:0 Start Address [7:0]
This register is the low order byte of the address [7:0].

CRT0E: Cursor Location High Register

Read/Write Address: 3?5h, Index 0Eh
Power-on Default: Undefined

This register defines the high order cursor location address. This value is a 19-bit value along with CRT30 bit[6:4] are the high order bits of the address.

7	6	5	4	3	2	1	0
CURSOR LOCATION HIGH							

Bit 7:0 Cursor Location High
This register is the high order byte of the cursor location address.

CRT0F: Cursor Location Low Register

Read/Write Address: 3?5h, Index 0Fh
Power-on Default: Undefined

This register defines the low order cursor location address.

7	6	5	4	3	2	1	0
CURSOR LOCATION LOW							

Bit 7:0 Cursor Location Low
This register is the low order byte of the cursor location address.

CRT10: Vertical Sync Pulse Start Register

Read/Write Address: 3?5h, Index 10h
Power-on Default: Undefined

This register is used to adjust screen position vertically and to specify the position at which VSYNC is active. Bit 10 of this value is in CRT30 bit 0. Bit 9 of this value is in CRT07 bit 7. Bit 8 of this value is in CRT07 bit 2.

7	6	5	4	3	2	1	0
VERTICAL SYNC PULSE START							

Bit 7:0 Vertical Sync Pulse Start
Vertical Sync Start has a 11-bit value. This register contains the least significant 8 bits of this value. This value = number of scan lines at which VSYNC becomes active.

CRT11: Vertical Sync Pulse End Register

Read/Write Address: 3?5h, Index 11h
Power-on Default: 0xh.

This register is used to control vertical interrupt, vertical sync end CRT0-7 Write protect.

7	6	5	4	3	2	1	0
LW	**RCS**	**DVI**	**CVI**	**VERTICAL SYNC PULSE END**			

Bit 7 Lock writing to CRTC registers: CRT00-07. (LW)
0 = Enable writing to CRTC registers are
1 = Disable writing to CRTC registers, except CRT07 bit 4 (line compare)

Bit 6 Refresh Cycle Select (3/5) (RCS)
0 = 3 DRAM refresh cycles per horizontal scan line
1 = 5 DRAM refresh cycles per horizontal scan line

Bit 5 Disable Vertical Interrupt (DVI)
0 = vertical retrace interrupt enabled
1 = vertical retrace interrupt disabled

Bit 4 Clear Vertical Interrupt (CVI)
0 = vertical retrace interrupt is cleared
1 = vertical retrace interrupt. This allows an interrupt to be generated at the end of active vertical display.

Bit 3:0 Vertical Sync Pulse End
This value = number of scan lines at which VSYNC becomes inactive.

CRT12: Vertical Display End Register

Read/Write Address: 3?5h, Index 12h
Power-on Default: Undefined

This register defines the number of scan line where the display on the screen ends. Bit 10 of this value is in CRT30 bit 2. Bit 9 of this value is in CRT07 bit 6. Bit 8 of this value is in CRT07 bit 1. This register is locked when FPR33 (SC5h, index 33) bit 5 = 1. Please refer to FPR33 register.

7	6	5	4	3	2	1	0
VERTICAL DISPLAY END							

Bit 7:0 Vertical Display End
Vertical Display End has a 11-bit value. This register contains the least significant 8-bits of this value. This value = (number of scan lines during active display) - 1.

CRT13: Offset Register

Read/Write Address: 3?5h, Index 13h
Power-on Default: Undefined

7	6	5	4	3	2	1	0
LOGICAL SCREEN WIDTH							

This register defines the logical line width of the screen. The starting memory address for the next display row is larger than the current row by two (in byte mode), four (in word mode), or eight (in double word mode) times this offset.

Bit 7:0 Logical Screen Width
Logical Screen Width has a 10-bit value. This register contains the least significant 8-bits of this value. The addressing mode is specified by bit 6 of CRT14 and bit 3 of CRT17.

CRT14: Underline Location Register

Read/Write Address: 3?5h, Index 14h
Power-on Default: Undefined

This register defines the horizontal row scan position of underline and display buffer addressing modes.

7	6	5	4	3	2	1	0
R	**DWS**	**CS**	**UNDER LINE LOCATION**				

Bit 7 Reserved (R)

Bit 6 Double Word Mode Select (DWS)
0 = the memory address are byte or word addresses
1 = the memory address are double word addresses

Bit 5 Count by 4 Select (CS)
0 = the memory address counter depends on bit 3 of CRT17
1 = the memory address counter is incremented every four character clocks

Bit 4:0 Under Line Location
Under Line Location has a 5-bit value. This value = (scan line count of a character row on which an underline occurs) - 1.

CRT15: Vertical Blank Start Register

Read/Write Address: 3?5h, Index 15h
Power-on Default: Undefined

This register defines the number of scan lines at which vertical blank is asserted. Bit 10 of this value is in CRT30 bit 1. Bit 9 of this value is in CRT09 bit 5. Bit 8 of this value is in CRT07 bit 3.

7	6	5	4	3	2	1	0
VERTICAL BLANK START							

Bit 7:0 Vertical Blank Start
Vertical Blank Start has a 11-bit value. This register contains the least significant 8-bits of this value. This value = (scan line count at which vertical blank signal becomes active) - 1.

CRT16: Vertical Blank End Register

Read/Write Address: 3?5h, Index 16h
Power-on Default: Undefined

This register defines the number of scan lines at which vertical blank is de-asserted.

7	6	5	4	3	2	1	0
VERTICAL BLANK END							

Bit 7:0 Vertical Blank End
Vertical Blank End is a 8-bit value. This value = [(scan line count at which vertical blank signal becomes active) -1)] + (desired width of vertical blanking pulse in scan lines)

CRT17: CRT Mode Control Register

Read/Write Address: 3?5h, Index 17h
Power-on Default: Undefined

This register defines the controls for CRT mode.

7	6	5	4	3	2	1	0
HR	**BAS**	**AW**	**R**	**WS**	**HCS**	**EGA**	**CGA**

Bit 7 ~RST Hardware Reset for Horizontal and Vertical Sync (HR)
0 = horizontal and vertical sync outputs inactive
1 = horizontal and vertical sync outputs active

Bit 6 Byte Address Mode Select (BAS)
0 = word address mode. All memory address counter bits shift down by one bit and the MSB of the address counter appears on the LSB
1 = byte address mode

Bit 5 Address Wrap is useful in implementing CGA mode. (AW)
0 = In word address mode, memory address counter bit 13 appears on the memory address output signal of the CRT controller and the video memory address wraps around at 16KB.
1 = In word address mode, memory address counter bit 15 appears on the memory address output bit 0 signal of the CRTC controller.

Bit 4 Reserved (R)

Bit 3 Word Mode Select (WS)

0 = byte mode addressing is selected and memory address counter is clocked by the character clock input
1 = word mode addressing is selected and memory address counter is clocked by the character clock divided by two.

Bit 2 Horizontal Retrace Clock Select (HCS)
0 = select horizontal retrace clock rate
1 = select horizontal retrace clock rate divided by two.

Bit 1 EGA Emulation (EGA)
0 = Row scan counter bit 1 is replaced by memory address bit 14 during active display time
1 = Memory address bit 14 appear son the memory address output bit 14 signal of the CRT controller.

Bit 0 CGA Emulation (CGA)
0 = Row scan counter bit 0 is replaced by memory address bit 13 during active display time
1 = Memory address bit 13 appears on the memory address output bit 13 signal of the CRT controller.

CRT18: Line Compare Register

Read/Write Address: 3?5h, Index 18h
Power-on Default: Undefined

This register is used to implement a split screen function. When the scan line counter value is equal to the content of this register, the memory address counter is cleared to 0.

7	6	5	4	3	2	1	0
LINE COMPARE REGISTER							

Bit 7:0 Line Compare Register
This value = number of scan lines at which the screen is split into screen 1 and screen 2.

CRT22: Graphics Controller Data Latches Readback Register

Read Only Address: 3?5h, Index 22h
Power-on Default: Undefined

This register is used to read the CPU latches in the graphics controller.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER CPU DATA LATCHES							

Bit 7:0 Graphics Controller CPU Data Latches
Bits 1-0 of GR4 select the latch number N (3-0) of the CPU Latch.

CRT24: Attribute Controller Toggle Readback Register

Read Only Address: 3?5h, Index 24h

Power-on Default: Undefined

This register is used to provide access to the attribute controller toggle.

7	6	5	4	3	2	1	0
ACS	**RESERVED**						

Bit 7 Attribute Controller Index Select (ACS)
0 = the attribute controller reads or writes an index value on the next access
1 = the attribute controller reads or writes a data value on the next access

Bit 6:0 Reserved

CRT26: Attribute Controller Index Readback Register

Read Only Address: 3?5h, Index 26h
Power-on Default: Undefined

This register is used to provide access to the attribute controller index.

7	6	5	4	3	2	1	0
RESERVED		**VES**	**ATTRIBUTE CONTROLLER INDEX**				

Bit 7:6 Reserved

Bit 5 Video Enable Status (VES)

This bit provides status of the video display enable bit in Attribute Controller (3C0h) index bit 5.

Bit 4:0 Attribute Controller Index

This value is the attribute controller index data at 3C0h.

Graphics Controller Registers

The graphics controller registers are located at a two byte I/O address space. The registers are accessed by first writing an index to 3CEh and followed by writing a data to 3CFh.

GRXX: Graphics Controller Index Register

Read/Write Address: 3CEh
Power-on Default: Undefined

This register is loaded with a binary value that indexes the graphics controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED				**GRAPHICS CONTROLLER**			

Bit 7:4 Reserved

Bit 3:0 Graphics Controller Address Index
These bits specify the graphics controller register to be addressed. Its value is programmed in hexadecimal.

GRX00: Set/Reset Register

Read/Write Address: 3CFh, Index: 00h
Power-on Default: Undefined

This register represents the value written to all 8-bits of the corresponding memory planes when CPU executes a memory write in write mode 0.

7	6	5	4	3	2	1	0
RESERVED				**SET/RESET PLANE**			

Bit 7:4 Reserved

Bit 3:0 Set/Reset Plane3:0
In write mode 0, the set/reset data can be enabled on the corresponding bit of the bit of the Enable Set/Reset Data register. These bits become the color value for CPU memory write operations.

GRX01: Enable Set/Reset Register

Read/Write Address: 3CFh, Index: 01h.
Power-on Default: Undefined

This register enable the set/reset register in write mode 0.

7	6	5	4	3	2	1	0
RESERVED				**ENABLE SET/RESET PLANE**			

Bit 7:4 Reserved

Bit 3:0 Enable Set/Reset Plane3:0
In write mode 0, the enable set/reset bits allow writing to the corresponding planes with the data in set/reset register. A logical 0 disables the set/reset data in a plane, and that plane is written with the value of CPU write data.

GRX02: Color Compare Register

Read/Write Address: 3CFh Index: 02h.
Power-on Default: Undefined

This register is to used to compare with the CPU memory read data. This register works in conjunction with the Color Don't Care Register.

7	6	5	4	3	2	1	0
RESERVED				**COLOR COMPARE PLANE**			

Bit 7:4 Reserved

Bit 3:0 Color Compare Plane [3:0]
These bits represent the reference color used to compare each pixel in corresponding plane. A logical 1 is returned in each plane bit position when color matches.

GRX03: Data Rotate/ROP Register

Read/Write Address: 3CFhIndex: 03h.
Power-on Default: Undefined

This register is to used to control rotation and raster operations.

7	6	5	4	3	2	1	0
RESERVED			**ROS**		**ROTATE COUNT**		

Bit 7:5 Reserved

Bit 4:3 Raster Operations Select (ROS)
00 = No operation
01 = Logical AND with latched data
10 = Logical OR with latched data
11 = Logical XOR with latched data

Bit 2:0 Rotate Count
These bits specifies the number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0. To write non-rotated data, the CPU must present a count with 0.

GRX04: Read Plane Select Register

Read/Write Address: 3CFhIndex: 04h.
Power-on Default: Undefined

This register is selects which memory plane the CPU data is reading from in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored.

7	6	5	4	3	2	1	0
RESERVED						**READ PLANE**	

Bit 7:2 Reserved

Bit 1:0 Read Plane Select is as follows:
00 = Plane 0
01 = Plane 1
10 = Plane 2
11 = Plane 3

GRX05: Graphics Mode Register

Read/Write Address: 3CFhIndex: 05h.
Power-on Default: Undefined

This register is selects which memory plane the CPU data is reading from in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored.

7	6	5	4	3	2	1	0
R	**CS**	**OES**	**OEA**	**ERC**	**R**	**WRITING MODE**	

Bit 7 Reserved (R)

Bit 6 256 Color Shift Mode Select (CS)
0 = Enable bit 5 of this register to control loading of the shift registers.
1 = The shift registers are loaded in a manner that support the 256 color mode.

Bit 5 Odd/Even Shift Mode Select (OES)
0 = Normal shift mode
1 = The video shift registers are directed to format the serial data stream with even numbered bits from both planes on the even numbered planes and odd numbered bits from both planes on the odd planes.

Bit 4 Odd/Even Addressing Select (OEA)
0 = Normal addressing
1 = CGA Odd/even addressing mode is selected. Even CPU addresses access plane 0 and 2, while odd CPU addresses access plane 1 and 3.

Bit 3 Enable Read Compare (ERC)
0 = System read data from memory planes selected by read map select register (3CFh index 04h). This is called read mode 0.
1 = System read the results of logical comparison between the data in 4 memory planes selected by the Color Don't Care Register and the Color Compare Register. The results is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1.

Bit 2 Reserved (R)

Bit 1:0 Write Mode Select
00 = Write mode 0. Each of four video planes is written with CPU data rotated by the number of counts in rotate register. If Set/Reset register is enabled for any of the four planes, the corresponding planes is written with the data stored in the Set/Reset register.

01 = Write mode 1. Each of four video planes is written with CPU data in the processor latches. These latches are loaded during previous CPU read operations. Raster operation, rotate count, Set/Reset data, enable Set/Reset data and bit mask registers are ignored.

10 = Write mode 2. Video planes [3:0] are written with the value of CPU write data [3:0]. The 32-bit output from the four planes is then operated on by the Bit Mask register and the resulting data are written into the four planes. The Set/Reset, Enable Set/Reset and Rotate Count registers are ignored.

11 = Write mode 3. Each of the four video planes is written with 8-bit of the color value in the Set/Reset register for the corresponding plane. The bit-position-enable field is formed with the logical AND of the Bit Mask register and rotated CPU data. The Enable Set/Reset register is ignored.

GRX06: Graphics Miscellaneous Register

Read/Write Address: 3CFhIndex: 06h.
Power-on Default: Undefined

This register controls video memory addressing.

7	6	5	4	3	2	1	0
RESERVED				**MEMORY MAP**		**OES**	**GMS**

Bit 7:4 Reserved

Bit 3:2 Memory Map Mode. These bits control the address mapping of video memory into the CPU address space.
00 = A0000h to BFFFFh (128KB)
01 = A0000h to AFFFFh (64KB)
10 = B0000h to B7FFFh (32KB)
11 = B8000h to BFFFFh (32KB)

Bit 1 Odd/Even Mode Select (OES)
0 = CPU address bit A0 is the memory address bit MA0
1 = CPU address A0 is replaced by a higher order address bit. A0 is then used to select odd or even maps. A0=0, selects Map 2 or 0; A0 = 1, select Map 3 or 1.

Bit 0 Graphics Mode Select (GMS)
0 = Select Text mode
1 = Select Graphics mode

GRX07: Color Don't Care Plane Register

Read/Write Address: 3CFhIndex: 07h.
Power-on Default: Undefined

This register controls whether the corresponding bit of the Color Compare Register, GRX02, is to be ignored or used for color comparison. This register is used with GRX02 for Read Mode 1 accesses.

7	6	5	4	3	2	1	0
RESERVED				**COMPARE PLANE SELECT**			

Bit 7:4 Reserved

Bit 3:0 Compare Plane Select
0 = The corresponding color plane becomes a don't care plane when the CPU read from the video memory is performed in read mode 1.
1 = The corresponding color plane is used for color comparison with the data in the Color Compare Register, GRX02.

GRX08: Bit Mask Register

Read/Write Address: 3CFh, Index: 08h.
Power-on Default: Undefined

This register controls bit mask operations which applies simultaneously to all four maps. The data written into memory in this case is the data which was read in the previous cycle, and was stored in the processor latches. Any bit programmed to 1 allows unimpeded writes to the corresponding bits in the plane.

7	6	5	4	3	2	1	0
BIT MASK							

Bit 7:0 Bit Mask
0 = corresponding bit of each plane in memory is set to the corresponding bit in the processor latches.
1 = corresponding bit of each plane in memory is set as specified by other conditions.

Attribute Controller Registers

The attribute controller registers are located at the same byte I/O address for writing address and data. The Attribute Index Register has an internal flip-flop rather than an input bit to control the selection of the address and data registers. Reading the Input Status Register 1 at Port 3?Ah clears the flip-flop and selects the Address Register, which is read at address 3C1h and written at address 3C0h. Once the Address Register has been loaded with an index, the next write operation to 3C0h loads the Data Register. The flip-flop toggles between the Address and the Data Register after every write to address 3C0h, but does not toggle for reads from address 3C1h. Furthermore, the attribute controller index register is read at 3C0h, and the attribute controller data register is read at address 3C1h.

ATRX: Attribute Controller Index Register

Read/Write Address: 3C0h
Power-on Default: Undefined

This register is loaded with a binary value that indexes the attribute controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED		**PAS**	**ATTRIBUTE CONTROLLER ADDRESS**				

Bit 7:6 Reserved

Bit 5 Palette Address Source (PAS)
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers
1 = Enable internal color palette and normal video translation.

Bit 4:0 Attribute Controller Address
A binary value that points to the attribute controller register where data is to be written.

ATR00-0F: Palette Register

Read/Write Address: 3C1h/3C0h, Index 00h - 0Fh.
Power-on Default: Undefined

This register is loaded with a binary value that indexes the attribute controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED		**PALETTE COLORS**					

Bit 7:6 Reserved

Bit 5:0 Palette Colors
0 = corresponding pixel color is de-selected
1 = corresponding pixel color is enabled

ATR10: Attribute Mode Control Register

Read/Write Address: 3C1h/3C0h, Index: 10h.
Power-on Default: 00h

This register controls the attribute mode of the display function.

7	6	5	4	3	2	1	0
VID	**CS**	**PPE**	**R**	**BIS**	**LGC**	**MCE**	**TGM**

Bit 7 VID5, VID4 Select (VID)
0 = VID5 and VID4 palette register outputs are selected
1 = Color Select Register Port 3C1h/3C0h, Index 14h, bit 1 and bit 0 are selected for outputs.

Bit 6 256 Color Select (CS)
0 = Disable 256 color mode pixel width. PCLK rate = internal dot clock rate.

1 = Enable 256 color mode pixel width. PCLK rate = internal dot clock rate / 2

Bit 5 Pixel Panning Enable (PPE)
0 = Line compare will have no effect on the output of the pixel panning register
1 = Forces the output of the pixel panning register to 0 after matching line compare until VSYNC is active

Bit 4 Reserved (R)

Bit 3 Blinking and Intensity Select (BIS)
0 = Select background intensity from the text attribute byte.
1 = Select blink attribute in text modes

Bit 2 Line Graphics Character Enable (LGC)
0 = Forces the ninth dot to be the same color as the background in line graphics character codes.
1 = Enable special line graphics character codes.

Bit 1 Mono/Color Emulation (MCE)
0 = Select color display text attributes
1 = Select monochrome display text attributes

Bit 0 Text /Graphics Mode Select (TGM)
0 = Select text attribute control mode
1 = Select graphics control mode

ATR11: Overscan Color Register

Read/Write Address: 3C1h/3C0h, Index: 11h.
Power-on Default: 00h

This register controls the overscan or border color. This register will be locked if CRT3C register (3?5h, index 3Ch) bit 5 is set to 1. Please refer to CRT3C register for details.

7	6	5	4	3	2	1	0
OVERSCAN COLOR REGISTER							

Bit 7:0 OverScan Color register determines the overscan or border color displayed on the CRT screen.

ATR12: Color Plane Enable Register

Read/Write Address: 3C1h/3C0h, Index: 12h.
Power-on Default: 00h

This register enables the respective video memory color plan 0-3 and selects the video color outputs to be read back in the display status.

7	6	5	4	3	2	1	0
RESERVED		**VIDEO SATUS**		**COLOR PLANE ENABLE**			

Bit 7:6 Reserved

Bit 5:4 Video Status Multiplexer. These bits select two out of the 8 color outputs which can be read by the Input Status Register 1 at port 3?Ah, bit 5 and bit 4.

Color Plane Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID7

Bit 3:0 Color Plane Enable
0 = disable the corresponding color planes. Forces pixel bit to be 0 before it address palette.
1 = enables the corresponding color planes.

ATR13: Horizontal Pixel Panning Register

Read/Write Address: 3C1h/3C0h, Index: 13h.
Power-on Default: 00h

This register specifies the number of pixels to shift the display data horizontally to the left. Horizontal pixel panning is available in text and graphics modes.

7	6	5	4	3	2	1	0
RESERVED				**HORIZONTAL PIXEL PLANNING**			

Bit 7:4 Reserved

Bit 3:0 Horizontal Pixel Panning. These 4 bits determine the horizontal left shift of the video data in number of pixels. In the 9 pixel/character text mode, the output can be shifted a maximum shift of 8 pixels. In the 8 pixel/character text mode and all graphics modes, except for 256 color mode, a maximum shift of 7 pixels is allowed. In the 256 color mode, bit 0 of this register must be 0 resulting in only 4 panning positions per display byte. The panning is controlled as follows:

Bits 3:0	9 pixel/character	8 pixel/character	256 color modes
0000	1	0	0
0001	2	1	-
0010	3	2	1
0011	4	3	-
0100	5	4	2
0101	6	5	-
0110	7	6	3

0111	8	7	-
1000	0	-	-

ATR14: Color Select Register

Read/Write Address: 3C1h/3C0h, Index: 14h.
Power-on Default: 00h

This register specifies the high-order bits of video output when pixel padding is enable/disabled for 256 color modes.

7	6	5	4	3	2	1	0
RESERVED				**SC7/6**		**SC5/4**	

Bit 7:4 Reserved

Bit 3:2 Select Color 7 and Color 6 (SC7/6)
These are the two most significant bits of the 8 bits color value for video DAC. These are normally used in all modes except 256 color modes.

Bit 1:0 Select Color 5 and Color 4 (SC5/4)
These bits can be substituted for VID5 and VID4 from the palette registers to form the 8-bit color value for video DAC.

RAMDAC Registers

The section describes the RAMDAC registers. Special programming sequences are used to read or write data to and from the RAMDAC.

Writing data to DAC:

Write the color code to DAC Write Address Register at 3C8h.
Three bytes: Red, Green, Blue values are written into DAC Data Register at 3C9h.
Following the third write, the values are transferred to Color Lookup Table.

- The DAC Write Address Register is auto incremented by 1.

Reading data from DAC:

- Write the color code to DAC Read Address Register at 3C7h.
- Three bytes: Red, Green, Blue values are read from the DAC Data Register at 3C9h.

3C6: DAC Mask Register

Read/Write Address: 3C6h
Power-on Default: Undefined

This register is the pixel read mask register to select pixel video output.

7	6	5	4	3	2	1	0
DAC ADDRESS MASK							

Bit 7:0 DAC Address Mask
This field is the pixel mask for palette DAC. When a bit in this field is programmed to 0, the corresponding bit in the pixel data is ignored in looking up an entry I the Color Lookup Table. This register is initialized to FFh by the BIOS during a video mode set.

3C7W: DAC Address Read Register

Write Only Address: 3C7h
Power-on Default: Undefined

This register contains the pointer to one of the 256 palette data registers and is used when reading the color palette. A write to this register causes 11b to be driven out to the RAMDAC output.

7	6	5	4	3	2	1	0
DAC READ ADDRESS							

Bit 7:0 DAC Read Address
After a color code is written into this register, the chip will identifies that a DAC read sequence will occur. A read sequence consists of three consecutive byte reads from the RAMDAC data register at 3C9h.

3C7R: DAC Status Register

Read Only Address: 3C7h
Power-on Default: Undefined

This register specifies the DAC Status: read or write cycles.

7	6	5	4	3	2	1	0
RESERVED						**DAC STATUS**	

Bit 7:2 Reserved

Bit 1:0 DAC Status bits
00 = DAC write operation in progress
11 = DAC read operation in progress

3C8: DAC Address Write Register

Read/Write Address: 3C8h
Power-on Default: Undefined

This register contains the pointer to one of the 256 palette data registers and is during a palette load. A write to this register causes 11b to be driven out to the RAMDAC output.

7	6	5	4	3	2	1	0
DAC WRITE ADDRESS							

Bit 7:0 DAC Write Address
After a color code is written into this register, the chip identifies that a DAC write sequence will occur. A write sequence consists of three consecutive byte reads from the RAMDAC data register at 3C9h.

3C9: DAC Data Register

Read/Write Address: 3C9h
Power-on Default: Undefined

This register is the data port to read or write the contents of the location in the Color Lookup Table pointed to by the DAC Read Address or the DAC Write Address registers. An access to this register will cause 01b to be driven to RAMDAC outputs.

7	6	5	4	3	2	1	0
DAC READ/WRITE DATA							

Bit 7:0 DAC Read/Write Data
These read/write register bits store the Pixel data for the Palette DAC

Chapter 20: Extended SMI IO Mapped Registers

Table 23: Extended SMI IO Mapped Registers Quick Reference

Extended SMI Registers

This chapter describes the extended SMI registers including:

- System control registers
- Power down control register
- Memory control registers
- Clock control registers
- General purpose registers
- Popup-Icon and hardware cursor registers
- Extended CRT registers
- Shadow VGA registers

All extended SMI registers are accessed through 3C3h, 3C5h, or 3?5h address. (? = B for monochrome mode and D for color mode) or through their MMI0 location. In order to access extended SMI registers, one must unlock the extended SMI register by writing 010xxxxxb to Lock register (3C3h).

The name of the register consists of the index which the register resides in. For example, SCR10 can be accessed through index 10h of 3C5h.

System Control Registers

All system control registers are controlled by PCI system clock, rather than memory clock (MCLK) or video clock (VCLK). During SM731 power down (when MCLK and VCLK are shutdown), the system control registers can still be accessed through PCI bus.

SCR15: PCI Miscellaneous Control Register

Read Only Address: 3C5h, Index: 15h
Power-on Default: 00h

This register defines the various PCI control registers.

7	6	5	4	3	2	1	0
BRE	**ABORT**	**SDE**	**DEA**	**PCI**	**BIOS**	**XFER**	

Bit 7 PCI Burst Read Enable (BRE)
0 = Disable
1 = Enable. SCR17 bit 5 needs to be set to 1 in order for this bit to take effect. For example, if SCR17 bit 5 = 0, even this bit is set to 1, PCI burst read will not be enabled.

Bit 6 Abort 3D Engine (ABORT)
0 = 3D Engine Normal Operation
1 = Abort 3D Engine Activities

Bit 5 Software Abort Drawing Engine Enable (SDE)
0 = Normal
1 = Enable. This bit has no effect unless bit 4 is set to 1.

Bit 4 Drawing Engine Abort Enable (DEA)
0 = Normal
1 = Enable

Bit 3 PCI Configuration Space: Subsystem ID Lock Enable (PCI)
0 = Disable
1 = Enable

Bit 2 Full range for BIOS access (BIOS)

Bit 1:0 # of Double word transfer during burst read = for performance tuning purpose
00 = 2 3D-bit double words
01 = 4 3D-bit double words
IX = 8 3D-bit double words

SCR16: Status for Drawing Engine and Video Processor

Read Only Address: 3C5h, Index: 16h
Power-on Default: Undefined

This register specifies status of SM731 including Drawing Engine Status, Video Processor Status, and Drawing Engine FIFO Available.

7	6	5	4	3	2	1	0
GES	**VWI**	**VWII**	**DE**	**DEBS**	**3DEBS**	**VPR**	**VPRCB**

Bit 7 Graphics Engine Status (GES)
0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 6 Video Window I Status (VWI)
0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 5 Video Window II Status (VWII)
0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 4 Drawing Engine is Empty and Ready (DE
0 = Drawing Engine not empty
1 = Drawing Engine empty

Bit 3 2D Drawing Engine Busy Status (DEBS)
0 = Drawing Engine Idle
1 = Drawing Engine Busy

Bit 2 3D Engine Busy Status (3DEBS)
0 = 3D Engine Idle
1 = 3D Engine Busy

Bit 1 VPR53_7 (VPR)
SubPicture Status

0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 0 VPRcb_7

SCR17: General Graphics Command Register 1

Read/Write Address: 3C5h, Index: 17h
Power-on Default: 00h

This register specifies command controls for Memory Access Disable, PCI bus master status, PCI bus burst write and burst read enable, Big-Endian Swap mode Select, Direct 3D Data Buffer Select, Memory mapped access enable and BIOS ROM size select.

7	6	5	4	3	2	1	0
MAD	**PCI**	**PCI1**	**BESM**	**DIRECT3D**		**MMA**	**DLT**

Bit 7 Memory Access Disable when Drawing Engine Busy (MAD)
0 = Normal
1 = Disable memory access when Drawing Engine is busy

Bit 6 Start PCI Bus Master (PCI)
0 = Stop PCI
1 = Start PCI

Bit 5 PCI burst read and write enable. (PCI1)
0 = Disable
1 = Enable

Bit 4 Big Endian Swap Mode Select (BESM)

0 = Big Endian with byte swap

1 = Big Endian with word swap

	[31:24]	[23:16]	[15:8]	[7:0}
Before				
After	**[7:0]**	**[15:8]**	**[23:16]**	**[31:24]**

	[31:16]	[15:0]
Before		
After	**[15:0]**	**31:16]**

Bit 3:2 Direct3D Z-Buffer Data Select

00 = Normal (use all 32-bit data)

01 = Use low word [15:0]

10 = Use high word [31:16]

11 = Normal (use all 32-bit data)

Bit 1 Memory Mapped Aperture Select (MMA)
0 = Select Banking Aperture. No Memory Mapped registers access allowed.
1 = Select Memory Mapped Aperture

Bit 0 Disable Latency Timer (DLT)

0 = Normal
1 = Disable latency timer count

SCR18: General Graphics Command Register 2

Read/Write Address: 3C5h, Index: 18h
Power-on Default: 00h

This register specifies command control for aperture select, graphics modes select, 32/64 memory data path select and linear addressing mode enable.

7	6	5	4	3	2	1	0
SCLK	**ECLK**	**AS**	**GRAPHICS MODE**		**MDP**	**ERH**	**LMM**

Bit 7 Select ~CLKRUN or ACTIVITY (SCLK)
0 = Select ~CLKRUN as input for Pin 161
1 = Select ACITIVITY as output for Pin 161

Bit 6 Enable ~CLKRUN Function (ECLK)
0 = disable
1 = enable

Bit 5 Aperture Select. This bit is only valid in linear memory mode (bit 0 = 1) (AS)
0 = Select dual aperture. Allow 0A0000h-0AFFFFh and linear aperture to coexist.
1 = Select single aperture. Only linear aperture can be used.

Bit 4:3 Graphics Modes Select for Memory Access
00 = Standard VGA mode. The memory access only uses the lower 32-bit of the 64-bit internal memory bus. The memory address wraps after 256 KB.
01 = VESA Super VGA 16 color (4-bit) mode. The memory access only uses the low 32-bit of the 64-bit internal memory bus. The memory address does not wrap after 256 KB.
1x = Extended packed pixel graphics modes (8/16/24/32-bit). The memory access always use the internal 64-bit memory bus.

Bit 2 32/64 memory data path select. This bit is only valid in VGA or VESA Super VGA 16 color modes (bit 4 of this register = 0) (MDP)
0 = CPU access VGA memory. All host memory access goes through VGA aperture: 0A0000h - 0BFFFFh (controlled by 3CFh index 6 Bit [3:2]). The memory access only uses the low 32-bit of the 64-bit memory bus.
1 = CPU access graphics memory. All host memory access does not goes through VGA aperture. This bit is used to allow 64-bit memory access even in VGA or super VGA 16 color modes.
For example, when programming pop-up icon in VGA mode or VESA super VGA 16 color mode, one must set bit 2 = 1 and bit 4 = 0 of this register, in order to access full range of the display memory.

Bit 1 Enable Repeat Hardware Rotation BLT function (ERH)
0 = disable
1 = enable

Bit 0 Linear Memory Mode Enable (LMM)

0 = disable. Nonlinear addressing (banking) mode is selected, and MCR61 register will be used for memory bank select. Memory will be accessed according to 3CF index 6 Bit [3:2]:

3CF.6 Bit [3:2]	**Memory Range**
00	0A0000-0BFFFF
01	0A0000-0AFFFF
10	0B0000-0B7000
11	0B8000-0BFFFF

1 = enable. Linear memory mode is selected, and memory will be accessed according to the PCI base address register.

SCR19: Interrupt Enable and Mask I

Read/Write Address: 3C5h, Index: 19h
Power-on Default: 00h

This register specifies interrupt enables and interrupt masks for PCI master, Zoom Video Port, and Drawing Engine. Each interrupt mask will block out its particular interrupt when the interrupt mask is enabled. When the interrupt mask is disabled, the corresponding interrupt will be generated when its particular interrupt is enabled.

7	6	5	4	3	2	1	0
IEVGA	**PVBI**	**IEZVP**	**IEDE**	**R**	**PVBIM**	**IMZVP**	**IMDE**

Bit 7 Interrupt Enable for VGA (IEVGA)

Bit 6 Panel Vertical Blanking Interrupet (PVBI)
0= Disable
1 = Enable

Bit 5 Interrupt Enable for Zoom Video Port (IEZVP)
0 = Disable
1 = Enable

Bit 4 Interrupt Enable for 2D/3D Drawing Engine (IEDE)
0 = Disable
1 = Enable

Bit 3 Reserved

Bit 2 Panel Vertical Blanking Interrupt Mask (PVBIM)
0 = Disable
1 = Enable

Bit 1 Interrupt Mask for Zoom Video Port (IMZVP)
0 = Disable
1 = Enable

Bit 0 Interrupt Mask for 2D/3D Drawing Engine (IMDE)
0 = Disable
1 = Enable

SCR1A: Interrupt Status

Read Only Address: 3C5h, Index: 1Ah
Power-on Default: Undefined

This register specifies Interrupt Status of Drawing Engine, Video Port, PCI Master, and VGA. The interrupt enable and mask bits for these interrupts are located in SCR19 register, with the exception of VGA's enable and mask bits which reside within the VGA block.

7	6	5	4	3	2	1	0
ICMD	**IDCT**	**3D TE**	**VGA**	**HMCIS**	**PVBI**	**ZVP**	**DEI**

Bit 7 ICMD Interrupt Status (ICMD)
0 = No interrupt
1 = ICMD interrupt is detected

Bit 6 IDCT Interrupt Status (IDCT)

Bit 5 3D Texture Engine Interrupt Status (3D TE)
0 = No interrupt
1 = 3D Texture Engine interrupt detected

Bit 4 VGA Interrupt Status. VGA's interrupt enable and mask bits are in the VGA block. (VGA)
0 = No interrupt
1 = VGA Interrupt is detected

Bit 3 Host Memory Control Interrupt Status (HMCIS)
0 = No interrupt
1 = Master Control

Bit 2 Panel Vertical Blank Interrupt Status (PVBI)
0 = No interrupt detected
1 = Interrupt detected

Bit 1 Zoom Video Port Interrupt Status (ZVP)
0 = No interrupt
1 = Zoom Video Port Interrupt is detected

Bit 0 2D/3D Drawing Engine Interrupt Status (DEI)
0 = No interrupt
1 = Drawing Engine Interrupt is detected

SCR1B: Interrupt Status Enable and Mask II

Read Only: Address: 3C5h, Index: 1Bh
Power-on Default: 00h

7	6	5	4	3	2	1	0
ICMDIE	**IDCTIE**	**TEXTURE**	**HMCIE**	**ICMDIM**	**IDCTIM**	**TEXTURE**	**HMIMM**

Bit 7 ICMD Interrupt Enable (ICMDIE)
0 = Disable ICMD interrupt (hardware interrupt to system)
1 = Enable ICMD interrupt (hardware interrupt to system)

Bit 6 IDCT Interrupt Enable (IDCTIE)
0 = Disable IDCT interrupt (hardware interrupt to system)
1 = Enable IDCT interrupt (hardware interrupt to system)

Bit 5 Text 3D Interrupt Enable (TEXTURE)
0 = Disable Text 3D interrupt (hardware interrupt to system)
1 = Enable Text 3D interrupt (hardware interrupt to system)

Bit 4 Host Master Control Interrupt Enable (HMCIE)
0 = Disable Host Master interrupt (hardware interrupt to system)
1 = Enable Host Master interrupt (hardware interrupt to system)

Bit 3 ICMD Interrupt Mask (ICMDIM)
0 = Allow ICMD interrupt signal to be latched into interrupt register
1 = Will not allow ICMD interrupt signal to be into interrupt register

Bit 2 IDCT Interrupt Mask (IDCTIM)
0 = Allow IDCT interrupt signal to be latched into interrupt register
1 = Will not allow IDCT interrupt signal to be into interrupt register

Bit 1 Texture (TEXTURE)
0 = Allow Texture interrupt signal to be latched into interrupt register
1 = Will not allow Texture interrupt signal to be into interrupt register

Bit 0 Host Control Interrupt Mask Master (HCIMM)
0 = Allow Host Control interrupt signal to be latched into interrupt register
1 = Will not allow Host Control interrupt signal to be into interrupt register

SCR1C: Interrupt Status

Read Only: Address: 3C5h, Index: 1Ch
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**USR3**	**USR2**	**ACON**	**R**

Bit 7:4 Reserved

Bit 3 Usr3 Interrupt Status

Bit 2 Usr2 Interrupt Status

Bit 1 "ACON" pin status change interrupt status

Bit 0 Reserved

SCR1F: Interrupt Mask and Hardware Interrupt Enable

Read Only: Address: 3C5h, Index: 1Fh
Power-on Default: 00h

7	6	5	4	3	2	1	0
USR3	**USR2**	**API**	**R**	**USR3IM**	**USR2IM**	**APS**	**R**

Bit 7 Usr3 to enable system hardware interrupt
0 = Disable USR3 Pin as interrupt (default)
1 = Enable USR3 Pin as interrupt input

Bit 6 Usr2 to enable system hardware interrupt
0 = Disable USR3 Pin as interrupt (default)
1 = Enable USR3 Pin as interrupt input

Bit 5 "ACON" pin interrupt
0 = Disable "ACON" pin interrupt
1 = Enable "ACON" pin interrupt

Bit 4 Reserved

Bit 3 Usr3 Interrupt Mask

Bit 2 Usr2 Interrupt Mask

Bit 1 "ACON" pin status change interrupt
0 = No mask for "ACON" pin status change interrupt
1 = Mask out for "ACON" pin status change interrupt

Bit 0 Reserved

SCR24: Reserved

Read Only: Address: 3C5h, Index: 24h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**DEFAULT**		**RESERVED**			

Bit 7:6 Reserved

Bit 5:4 11 = Default

Bit 3:0 Reserved

SCR25: AGP PLL Control

Read/Write Address: 3C5h, Index: 25h
Power-on Default: 00h

This register controls the AGP4X clock

7	6	5	4	3	2	1	0
CLOCK DELAY		**BAND WIDTH**		**LC**	**BP**	**PD**	**XOR**

Bit 7:6 Programmable AGP4X clock delay
00: Delay 0 ns (default)
01: Delay 0.3 ns
10: Delay 0.6 ns
11: Delay 0.9 ns

Bit 5:4 4X PLL Band Width Control (PLL's bw_cntrl [1:0])
00: Loop BW = 1 MHz (default)
01: Loop BW = 2 MHz
11: Loop BW = 3 MHz
10: Reserved

Bit 3 Leading/lagging control (PLL's select input)
0: PLL output clock phase lagging input by ~500ps (default)
1: PLL output clock phase leading input by ~500 ps

Bit 2 Bypass PLL (PLL's test input)
0: PLL in normal operation output (default)
1: PLL in bypass mode, clk_out direct from clk_in

Bit 1 Power down the AGP PLL (PLL's power down input)
0: PLL power enable (default)
1: PLL in power down mode

Bit 0 Use XOR 4X clock (This is a mux selection outside the PLL)
0: 4X clock from PLL (default)
1: 4X clock from XOR

SCR26: AGP 2X/4X Control

Read/Write Address: 3C5h, Index: 26h
Power-on Default: 00h

This register is for controlling the voltage reference of the pad.

7	6	5	4	3	2	1	0
RESERVED		**READ BACK**		**HA**	**VOLTAGE REFERENCE**		

Bit 7:6 Reserved

Bit 5 This bit effects CSR54_[1] read back status
0 = CSR54_[1] read back 1 (AGP2X capable)
1 = CSR54_[1] read back 0 (not AGP2X capable)

Bit 4 This bit effect CSR54_[0] read back status
0 = CSR54_[0] read back 1 (AGP1X capable)
1 = CSR54_[0] read back 0 (not AGP1X capable)

Bit 3 This bit default to 0 is used for hardware adjustment purposes. Generally, for 3.3V AGP2X systems this bit is set to 0. For 1.5V AGP4X systems this bit is set to 1.
0 = Select hvreg to control ADSTB pad
1 = Select ADSTBN for differential pad configurations

Bit 2:0 Voltage reference control for PCICLK pad
000 = 00000001: Select HVref (40%*AGP3.3V=1.32V or 50%*AGP1.5V=.75V) (default)
001 = 00000010: Select 10% of VDDQ (3.3V) = .33V
010 = 00000100: Select 15% of VDDQ (3.3V) = .495V
011 = 00001000: Select 20% of VDDQ (3.3V) = .66V
100 = 00010000: Select 25% of VDDQ (3.3V) = .825V
101 = 00100000: Select 30% of VDDQ (3.3V) = .99V
110 = 01000000: Select 35% of VDDQ (3.3V) = 1.155V
111 = 10000000: Select 40% of VDDQ (3.3V) = 1.32V

Power Down Control Registers

The power down control registers are controlled by system clock only. The power down control registers can still be read or written by CPU even when internal PLL is off.

PDR20: Power Down Control for Memory, Flat Panel, PLL, and Video Port

Read/Write Address: 3C5h, Index: 20h
Power-on Default: 04h

This register defines the different power down control for Memory, Flat Panel Interface, PLL, and Video Port. This register can still be read or written by CPU even when PLL is off.

7	6	5	4	3	2	1	0
SM	**R**	**PLL POST DIVIDE**		**LVDS**	**VPO**	**FPI**	**DMI**

Bit 7 Sleep Mode

0 = Sleep mode disable
1 = Enable

Bit 6 Reserved

Bit 5:4 PLL post divider control
00 = All the PLL post dividers disabled
01 = All the PLL post dividers enabled
Each PLL post divider is controlled by CCR9E [7:0] respectively
1x = The PLL post dividers are enabled only if sleep or standby are active
Each PLL post divider is controlled by CCR9E [7:0] respectively

Bit 3 Tri-state LVDSCLK output pin. When ~EXCKEN = 0, Pin 159 (MCKIN) becomes an input pin. When ~EXCKEN = 1, Pin 159 (LVDSCLK) becomes an output pin. This register is only valid when ~EXCKEN = 1. This bit is used to test the silicon. (LVDS)
0 = Enable LVDSCLK output pin
1 = Tri-state LVDSCLK output pin

Bit 2 Tri-state Video Port Output. When this bit = 0, 20-bit outputs (R[7:2], G[7:2], B[7:2], BLANK, and PCLK) will be driven out. When Video Capture is enabled (CPR00 [0] = 1), video port output will be tri-stated automatically, except for BLANK/TVCLK output pin. This bit is used to test the silicon. (VPO)
0 = Enable output pins
1 = Tri-state output pins (default)

Bit 1 Tri-state Flat Panel Interface Output Pins. This bit is used to test the silicon (FPI)
0 = Enable output pins
1 = Tri-state output pins

Bit 0 Tri-state Display Memory Interface output pins. This bit can also be used to isolate SM731 from display memory. All display memory interface pins: control signals, output clock, data bus and address bus are tri-stated. This bit is used to test the silicon. (DMI)
0 = Enable display memory interface output pins
1 = Tri-state display memory interface output pins

PDR21: Functional Blocks Power Down Control

Read/Write Address: 3C5h, Index: 21h
Power-on Default: HA0h

This register is designed to achieve optimum power saving in operation mode. Special clock drivers are built-in to control major functional blocks independently. This power saving feature will not affect the graphics and video performance, or LCD display quality. This register could be read or written by CPU even when PLL is off.

7	6	5	4	3	2	1	0
MHZ	**PLLS**	**FBWO**	**PVC**	**PPR**	**ZVP**	**DE**	**VP**

Bit 7 Disable 135 MHz DAC (MHZ)
0 = Enable DAC

1 = Disable DAC

Bit 6 If “PWDOWN” pin is pulled low (deep sleep mode) then this bit controls all the internal PLLs
0 = Enable PLLs
1 = Disable PLLs

Bit 5 Disable LCD Frame Buffer Write Operation. This bit is used to shut-down the (FBWO)
64 x 8 LCD write FIFO and remove the display memory bus request for LCD frame buffer write from arbitration control.
This bit needs to be set to "1" in Dual View Mode -- displaying different graphics data on CRT (or TV) and LCD.
This bit should be set to "1" when LCD display is not enabled or when TFT is selected in standard refresh mode in order to obtain optimum power saving.
0 = Enable LCD frame buffer write
1 = Disable LCD frame buffer write

Bit 4 Panel video clock (PVC)
0 = Enable panel video clock (default)
1 = Disable panel video clock (VRCLK)

Bit 3 PPRVCLK shut off (PPR)
0 = Normal
1 = Shut off PPRVCLK. No pixels will be clocked out to the CRTDAC.

Bit 2 Disable Zoom Video Port. This bit is used when there is no external video source which is connected to the SM731. The SM731 will block input data from external video port, turn off the clock driver of ZV Port, and remove the ZV Port display memory bus request from memory controller. (ZVP)
0 = Enable Zoom Video Port
1 = Disable Zoom Video Port

Bit 1 Disable 2D/3D Drawing Engine. This bit is used to turn-off the 2D/3D drawing engine block. For optimum power saving, this bit should be set to "1" in standard VGA mode since 2D/3D drawing engine is not in use. (DE)
0 = Enable 2D/3D drawing engine
1 = Disable 2D/3D drawing engine

Bit 0 Disable Video Processor. This bit is used to turn-off the video processor block which includes graphics FIFO, V0FIFO, V1FIFO, horizontal/vertical color interpolation, YUV-to-RGB conversion, TV flicker reduction, HW pop-up icon, and related control logic. For optimum power saving, This bit could be set to "1" in standard VGA mode since video processor is not in use. (VP)
0 = Enable video processor
1 = Disable video processor

PDR22: DPMS Control Select

Read/Write Address: 3C5h, Index: 22h
Power-on Default: x0h

7	6	5	4	3	2	1	0
RESERVED		**DPMS CONTROL**		**RESERVED**			

Bit 7:6 Reserved

Bit 5:4 DPMS Control

	DPMS State	VSYNC	HSYNC
00 =	Normal	Pulses	Pulses
01 =	Standby	Pulses	No Pulse
10 =	Suspend	No Pulse	Pulses
11 =	Off	No Pulse	No Pulse

Bit 3:0 Reserved

PDR23: Dynamic Power Management Control Register

Read/Write Address: 3C5h, Index: 23h
Power-on Default: 00h

7	6	5	4	3	2	1	0
EDPC	**DM**		**R**	**TIMER CONTROL**			

Bit 7 Enable dynamic power control register (EDPC)
0 = Disable
1 = Enable

Bit 6:5 Detect memory write/read & IO write/read (DM)
00 = Detect memory write/read & IO write/read & capture enable
01 = Detect memory write & IO write & capture enable
10 = Detect memory write/read & capture enable
11 = Detect IO write/read & capture enable

Bit 4 Reserved (R)

Bit 3:0 Timer control to count number of VSYNC. If there is no bus activities in a specified period, the power management enters “idle” mode.
0000 = No bus activity detection
0001 = 64 VSYNC
0010 = 128 VSYNC
0011 = 256 VSYNC
0100 = 512 VSYNC
0101 = 1K VSYNC
0110 = 2K VSYNC
0111 = 4K VSYNC

1000 = 8K VSYNC
1001 = 16K VSYNC
1010 = 32K VSYNC
1011 = 64K VSYNC
1100 = 128K VSYNC
1101 = 192K VSYNC
1110 = 256K VSYNC
1111 = 384K VSYNC

PDR24: Power Down Register Select

Read/Write Address: 3C5h, Index: 24h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED							**(PDMS)**

Bit 7:1 Reserved

Bit 0 Power Down Mode Select (PDMS)
0 = VESA Compliance power down mode
1 = PCI power down Spec 1.0 compliance

Memory Control Registers

MCR60: Memory Control

Read/Write Address: 3C5h, Index: 60h
Power-on Default: 00h

This register specifies memory control for Memory Address Wrap Around, DRAM refresh, VGA to memory burst write, and synchronization. This register also includes RAMDAC Write/Read Command Pulse Width select.

7	6	5	4	3	2	1	0
R	**BWC**	**RAM**	**DVGA**	**VGAF**	**R**	**DDRR**	**DRC**

Bit 7 Reserved

Bit 6 Block Write Control (BWC)
0 = Block write enabled
1 = Block Write not enabled (default)

Bit 5 RAMDAC Write/Read Command Pulse Width Select (RAM)
0 = Command Pulse is 4 MCLK high and 12 MCLK low
1 = Command Pulse is 8 MCLK high and 24 MCLK low

Bit 4 Disable VGA to memory burst write (DVGA)
0 = Enable
1 = Disable

Bit 3 VGA FIFO Empty Level Request Select. VGA FIFO is 8 level deep. (VGAF)
0 = VGA FIFO request if VGA FIFO is two level empty
1 = VGA FIFO request if VGA FIFO is four level empty

Bit 2 Reserved (R)

Bit 1 Disable DRAM Refresh Request (DDRR)
0 = Enable
1 = Disable

Bit 0 DRAM Refresh Control (DRC)
0 = Normal DRAM refresh
1 = Force to 1 DRAM refresh per scan line

MCR61: Memory Bank Address High

Read/Write Address: 3C5h, Index: 61h
Power-on Default: 00h

This register specifies the high order memory bank address for non-linear addressing (or banking) mode (SCR18 bit 0 = 0).

7	6	5	4	3	2	1	0
MEMORY BANK ADDRESS HIGH							

Bit 7:0 Memory Bank Address High

Specifies the high-order address for memory access in non-linear addressing (or banking) mode. The host will take these bits append with address [15:0] to form a 22 bits address (4Mbyte).

MCR62: Memory Type and Timing Control

Read/Write Address: 3C5h, Index: 62h
Power-on Default: This is a power-on configurable register (by RESET)

SM731 supports internal memory. This register specifies the memory type and memory timing control. This register is power-on configurable by MD [7:0] of memory data bus.

7	6	5	4	3	2	1	0
MDS		**MDC**		**TBWC**	**TBPL**	**IMPD**	**IMR**

Bit 7:6 Memory DRAM size (MDS)
00 = 4 Mbyte

01 = 32 Mbyte
10 = 16 Mbyte
11 = 8 Mbyte (default)
(power on configuration MD [7:6])

Bit 5:4 Memory DRAM column size (MDC)
0x = 1K DRAM column
10 = 512 DRAM column
11 = 256 DRAM column (default)
(power on configuration MD [5:4])

Bit 3 TBWC - Internal Memory Block Write Cycle Time (TBWC)
0 = 1 MCLK
1 = 2 MCLK (default)
(power-on configuration MD [3])

Bit 2 Block Write to Precharge (TBPL)
0 = 4 MCLK
1 = 1 MCLK (default)
(power-on configuration MD [2])

Bit 1 Tras - Internal Memory Active to Precharge Delay (IMPD)
0 = 6 MCLK
1 = 7 MCLK (default)
(power-on configuration MD [1])

Bit 0 TRC - Internal Memory Refresh to Command Delay (IMR)
0 = 12 MCLK
1 = 10 MCLK (default)
(power-on configuration MD [0])

MCR76: Memory Type and Timing Control

Read/Write Address: 3C5h, Index: 76h
Power-on Default: This is a power-on configurable register (by RESET)

7	6	5	4	3	2	1	0
EIM	**FMR**	**FDRA**	**R**	**MBS**	**R**	**DE**	**R**

Bit 7 Enable Internal Memory (EIM)
0 = Reserved
1 = Normal (default)
(power on configuration MD [31])

Bit 6 Force Memory Reset (FMR)
0 = Force memory reset
1 = Normal (default)
(power on configuration MD [30])

Bit 5 Force Dram Remain in Active State (FDRA)
0 = Force Dram in Active State
1 = Normal (default)
(power on configuration MD [29])

Bit 4 Reserved

Bit 3 Memory Bank Selection (MBS)
0 = 2 bank
1 = 4 bank

Bit 2 Reserved

Bit 1 DLL Enable (DE)
0 = DLL not enabled
1 = DLL enabled (default)
(power-on configuration MD [25])

Bit 0 Reserved

Clock Control Registers

CCR63: Memory Controller Clock Numerator Register

Read/Write Address: 3C5h, Index: 63h
Power-on Default: 0c

This register specifies the 8-bit numerator value of MCLK2 PLL frequency (MNR).

7	6	5	4	3	2	1	0
8-BIT MCLK2 PLL							

Bit 7:0 Specify the 8-bit numerator value to calculate the selected MCLK2 PLL frequency.

CCR64: Memory Controller Clock Denominator Register

Read/Write Address: 3C5h, Index: 64h
Power-on Default: 02h

This register specifies the 6-bit denominator value of MCLK2 PLL frequency (MDR).

7	6	5	4	3	2	1	0
6-BIT MCLK2 PLL							

Bit 7 Divide by 2 Post Scaler (PS)
0 = Normal

1 = Post Scaler Enabler

Bit 6 VCO select
0 = Select VCO for frequency range 20-120 MHz
1 = Select VCO for frequency higher than 120 MHz

Bit 5:0 Specify the 6-bit denominator value to calculate the selected MCLK frequency. The power-on default of this register is 20h.

CCR65: TV Encoder Control Register

Read/Write Address: 3C5h, Index: 65h
Power-on Default: 00h

This register specifies the various TV controls.

7	6	5	4	3	2	1	0
SVHS	**CVBS**	**TVEE**	**ERO**	**CRRC**	**LVDS2**	**LVDS1**	**VRCK**

Bit 7 SVHS TV enable (SVHS)
0 = SVHS TV off
1 = SVHS TV on

Bit 6 CVBS TV enable (CVBS)
0 = CVBS TV off
1 = CVBS TV on

Bit 5 TV Encoder Enable (TVEE)
0 = Disable TV Encoder (TVCLK disable)
1 = Enable TV Encoder

Bit 4 Enable ReduceOn (ERO)
Level 2 if activity pin is used.
0 = Normal
1 = VDD drop

Bit 3 Color RAM read control (CRRC)
0 = Read from CRT color RAM
1 = Read from LCD color RAM

Bit 2 LVDS2 clock polarity control
0 = Normal
1 = Inverted

Bit 1 LVDS1 clock polarity control
0 = Normal
1 = Inverted

Bit 0 LCD video clock (VRCK) jitter ejection control
0 = No jitter ejection from outside chip
1 = Jitter ejection enabled. SPNLCKOUT pin output the panel control clock source and SPNLCKIN pin feedback the clock with jitter control.

CCR66: RAM Control and Function On/Off Register

Read/Write Address: 3C5h, Index: 66h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RWCB1		**RWCB2**		**CRT RAM**		**MCE**	**DEE**

Bit 7:6 RAM Write Control Bits (RWCB1)

0	0	Both RAM ON*~
1	0	LCD RAM OFF
0	1	CRT RAM OFF
1	1	Both RAM OFF

Bit 5:4 RAM Write Control Bits (RWCB2)

0	0	Write both RAM (CRT/LCD)
1	0	Write CRT RAM only
0	1	Write LCD RAM only
1	1	Reserve

Bit 3:2 CRT RAM 8/6 Bits and Gamma Control

0	0	6-bits RAM
1	0	8-bits RAM
x	1	Gamma correct ON

Bit 1 Motion Comp Enable (MCE)
1 = Disable MComp*~
0 = Enable MComp
Include MCCLK off

Bit 0 3D DrawEng Enable (DEE)
1 = Disable 3DEng*~
0 = Enable 3DEng
Include 3DMCLK and 3DMCLKB off

CCR67: For Test Purpose Only

Read/Write Address: 3C5h, Index: 67h
Power-on Default: 00h

7	6	5	4	3	2	1	0
VSYNC		**VSYNC2**	**VSYNC3**	**PLL SELECTION**		**PLL TESTING**	

Bit 7:6 11 = The internal Vsync counter increment by toggle CCR67[5] otherwise the internal Vsync counter toggled by Vsync from CRT control.

Bit 5 Toggle this bit will increment the internal Vsync counter if bit [7:6] = 11 (VSYNC2)

Bit 4 Vsync counter (VSYNC3)
0 = Normal
1 = The Vsync counter becomes the shift register for testing purposes

Bit 3:2 PLL selection
The following tables illustrate controls for the Memory Clock, Engine Clock, CRT Video Clock, and Panel Video Clock. Config[37] is the power on memory data[37] configuration bit with default high.

Config[37]	CCR67[3:2]	Engine Clock Output	Memory Clock Output
1	0	ccr6a/ccr6b	ccr63/ccr64*
1	1	ccr6a/ccr6b	ccr63/ccr64 x 4**
0	00	ccr6a/ccr6b div 2	ccr6a/ccr6b
0	01	ccr6a/ccr6b div 2	agp4xclk (266MHz)
0	11	ccr6a/ccr6b	agp4xclk/2 (133 MHz)
0	10	ccr6a/ccr6b	ccr6a/ccr6b

PwrConfig[37]	CRT VideoClock	PanelVideoClock
1	ccr6c/ccr6d	ccr6e/ccr6f*
0	ccr6e/ccr6f	ccr6e/ccr6f

* Note: This should be the default setting for normal operation.
** Note: When PwrConfig[37] and ccr67[2] = 1 the 4xpll is power on. Otherwise it is power off. The ccr67[2] needs to be set to 1, prior ccr67[3] set to 1, or ccr67[3] needs to be set to 0 before ccr67[2] is set to 0.

Bit 1:0 For PLL testing purposes or can be used for external panel link or LVDS clock
00 = PprVclk goes to XMCK pad
01 = Inverted PprVclk goes to XMCK pad
10 = VrClk2x goes to XMCK pad
11 = Inverted VrClk2x goes to XMCK pad

CCR68: Clock Control 1

Read/Write Address: 3C5h, Index: 68h
Power-on Default: 40h

This register is used to select clock frequencies and pulse-width control.

7	6	5	4	3	2	1	0
VCLKF		**ISO**	**CLK**	**SELECT VCLK**		**SELECT MCLK**	

Bit 7:6 Select VCLK frequency based on the following table (VCLKF)

Bit [7:6]	~EXCKEN	VCLK frequency
00	1	VCLK is selected from VGA 3C2h register
01	1	VCLK is selected from programmable VCLK registers: CCR6C and CCR6D
10	1	VCLK is selected from 17.734 MHz
11	1	VCLK is selected from 14.131818 MHz
xx	0	VCLK is selected from CKIN input

Bit 5 Enable ISO standard at VGA modes. This bit is designed to increase the CRT screen refresh rate to ISO standard at VGA modes. This bit is used only when CCR68 bit [7:6] = 00b. (ISO)
0 = Standard VGA frequency which controlled by 3C2h bit [3:2]
1 = ISO frequency which selected by 3C2h bit [3:2]

CCR68 Bit 5	3C2h Bit [3:2]	VCLK frequency
0	00	25.180 MHz
0	01	28.325 MHz
1	00	31.500 MHz
1	01	35.484 MHz

Bit 4 Select 8-dot character clock and disable dot clock divided by 2 function. This bit is used when LCD or TV is selected (determined by FPR31 [2:0]). When this bit set to "1", the bit 3 and bit 0 setting of VGA Clocking Mode Register will be ignored. (CLK)
0 = Character clock and dot clock are controlled by VGA clocking mode register
1 = Select 8-dot character clock and non-divided by 2 dot clock

Bit 3:2 Select VCLK high pulse width
00 = default value
01 = reduce 1 ns high time
10 = increase 1 ns high time
11 = increase 2 ns high time

Bit 1:0 Select MCLK high pulse width
00 = default value
01 = reduce 1 ns high time
10 = increase 1 ns high time
11 = increase 2 ns high time

CCR69: Clock Control 2

Read/Write Address: 3C5h, Index: 69h
Power-on Default: 80h

This register is used to select Virtual Refresh clock frequency, DRAM refresh clock frequency during sleep mode and standby mode, and HSYNC & VSYNC control during sleep mode.

7	6	5	4	3	2	1	0
TVCLK	**TDSS**	**LVDSCLK**		**DRAM**	**SHVSM**	**SELECT VRCLK**	

Bit 7:6 Select the LCD Video clock high pulse width. The definition is similar to CCR68 [1:0], except for the LCD Video clock.

Bit 5:4 Select MCLK2 clock high pulse width. This definition is similar to CCR68 [3:2], except for the MCLK2.

Bit 3 This bit becomes read only for the read back AC power on states
0 = AC power is off
1 = AC power is on

Bit 2 Select HSYNC and VSYNC during Sleep Mode. (PDR20 bit 7 = 1). This bit is used to support VESA DPMS during Sleep Mode. SM731 will automatically support VESA DPMS Standby Mode during its internal Standby Mode. (SHVSM)

Bit 2	DPMS STATE	HSYNC	VSYNC
0	Suspend	Pulses	No Pulses
1	Off	No Pulses	No Pulses

Bit 1:0 LCD video clock
00 = LCD video clock is controlled by the LCD video clock PLL
01 = LCD video clock is from the MCLK
10 = LCD video clock is from the MCLK, divide by 2
11 = Same as bit [1:0] = 00

CCR6A: MCLK Numerator Register

Read/Write Address: 3C5h, Index: 6Ah
Power-on Default: 0Ch

This register specifies the 8-bit numerator value of MCLK frequency (MNR).

7	6	5	4	3	2	1	0
8-BIT MCLK							

Bit 7:0 Specify the 8-bit numerator value to calculate the selected MCLK frequency. The power-on default of this register is 0Ch.

CCR6B: MCLK Denominator Register

Read/Write Address: 3C5h, Index: 6Bh
Power-on Default: 02h

This register specifies the 6-bit denominator value of MCLK frequency (MDR).

7	6	5	4	3	2	1	0
6-BIT MCLK							

Bit 7 Divide by 2 post scalar.
0 = Disable
1 = Enable

Bit 6 VCO Select
0 = Select VCO for frequency range 20MHz to 120MHz
1 = Select VCO for frequency higher than120MHz

Bit 5:0 Specify the 6-bit denominator value to calculate the selected MCLK frequency. The power-on default of this register is 20h. Along with CCR6A, the default frequency is set to 40.27 MHz.

CCR6C: VCLK Numerator Register

Read/Write Address: 3C5h, Index: 6Ch
Power-on Default: 04h

This register specifies the numerator value of VCLK frequency (VNR).

7	6	5	4	3	2	1	0
VCLK FREQUENCY							

Bit 7:0 Specify the numerator value to calculate the selected VCLK frequency. The power-on default setting of this register is 04h.

CCR6D: VCLK Denominator Register

Read/Write Address: 3C5h, Index: 6Dh
Power-on Default: 02h

This register specifies the 6-bit denominator.

7	6	5	4	3	2	1	0
PS	**VCO**	**VCLK FREQUENCY [6]**					

Bit 7 Divide by 2 post scalar.
0 = Disable
1 = Enable

Bit 6 VCO Select
0 = Select VCO for frequency range 20MHz to 120MHz
1 = Select VCO for frequency higher than120MHz

Bit 5:0 Specify the 6-bit denominator value to calculate the selected VCLK frequency. The power-on default setting of this register is 02h.

CCR6E: Panel Clock Numerator Register

Read/Write Address: 3C5h, Index: 6Eh
Power-on Default: 06h

This register specifies the 8-bit numerator value of VCLK2 frequency (VRCLK).

7	6	5	4	3	2	1	0
8-BIT VRCLK FREQUENCY							

Bit 7:0 Specify the 8-bit numerator value to calculate the selected VRCLK frequency.

CCR6F: Panel Clock Denominator Register

Read/Write Address: 3C5h, Index: 6Fh
Power-on Default: 02h

This register specifies the 6-bit denominator value of VRCLK frequency.

7	6	5	4	3	2	1	0
PS	**VCO**	**6-BIT VRCLK FREQUENCY**					

Bit 7 Divide by 2 post scalar.
0 = Disable
1 = Enable

Bit 6 VCO Select
0 = Select VCO for frequency range 20MHz to 120MHz
1 = Select VCO for frequency higher than120MHz

Bit 5:0 Specify the 6-bit denominator value to calculate the selected VRCLK frequency.

CCR78: Scratch Register I

Read/Write Address: 3C5h, Index: 78h
Power-on Default: xxh

7	6	5	4	3	2	1	0
SCRATCH REGISTER							

Bit 7:0 Scratch Register

CCR79: Scratch Register 2

Read/Write Address: 3C5h, Index: 79h
Power-on Default: xxh

7	6	5	4	3	2	1	0
SCRATCH REGISTER							

Bit 7:0 Scratch Register

CCR7A-CCR7C: TV and RAMDAC Testing Power

Read/Write Address: 3C5h, Index: 7Ah-7Ch
Power-on Default: 00h

7	6	5	4	3	2	1	0
TV AND RAMDAC TESTING POWER ON RESET = 00							

Bit 7:0 TV and RAMDAC testing power on reset = 00

Note: See Appendix E for further details.

CCR7D: Control Registers for TV and RAMDAC Testing

Read/Write Address: 3C5h, Index: 7Dh
Power-on Default: 00h

7	6	5	4	3	2	1	0
TV	**SVHS**	**CVBS**	**MD**	**VCLK**	**MCLK**	**R**	**CRT**

Bit 7 TV Detect (TV)
0 = Normal operation
1 = Use CCR7A, CCR7B, and CCR7C data to check for TV detect

Bit 6 Read only for SVHS Detect (SVHS)

Bit 5 Read only for CVBS detect (CVBS)

Bit 4 Monitor Detect (MD)
0 = Normal operation
1 = Use CCR7A, CCR7B, and CCR7C data to check for monitor detect

Bit 3 External VCLK
0 = Normal operation
1 = Enable external VCLK

Bit 2 External MCLK
0 = Normal operation
1 = Enable external MCLK

Bit 1 Reserved

Bit 0 CRT/Panel Simul Mode Control Register Bit (CRT)
0 = Select CrtRgb data to drive the CRTDAC
CrtVsync, CrtHsync is going through the DPMS logic to drive the CRTVSYNC and CRTHSLYNC output
1 = Select FpData to drive the CRTDAC
FpVsync, FpHsync is going through the DPMS logic to drive the CRTVSYNC and CRTHSYNC output

Note: See Appendix E for further details.

CCR94: MCK PLL Numerator Adjustment

Read/Write Address: 3C5h, Index: 94h
Power-on Default: 00h

In “powersaving” mode and 3D is off CCR6A value is reduced by subtracting CCR94 to control MCK PLL’s numerator.

7	6	5	4	3	2	1	0
MCK PLL NUMERATOR ADJUSTMENT							

Bit 7:0 MCK PLL Numerator Adjustment

CCR95: MCK2 PLL Numerator Adjustment

Read/Write Address: 3C5h, Index: 95h
Power-on Default: 00h

In “powersaving” mode and 3D is off CCR63 value is reduced by subtracting CCR95 to control MCK2 PLL’s numerator.

7	6	5	4	3	2	1	0
MCK2 PLL NUMERATOR ADJUSTMENT							

Bit 7:0 MCK2 PLL Numerator Adjustment

CCR96: MCK PLL Numerator Adjustment 2

Read/Write Address: 3C5h, Index: 96h
Power-on Default: 00h

In “poweridle” mode and 3D is off CCR6A value is reduced by subtracting CCR96 to control MCK PLL’s numerator.

7	6	5	4	3	2	1	0
MCK PLL NUMERATOR ADJUSTMENT							

Bit 7:0 MCK PLL Numerator Adjustment

CCR97: MCK2 PLL Numerator Adjustment 2

Read/Write Address: 3C5h, Index: 97h
Power-on Default: 00h

In “poweridle” mode and 3D is off CCR63 value is reduced by subtracting CCR97 to control MCK2 PLL’s numerator.

7	6	5	4	3	2	1	0
MCK2 PLL NUMERATOR ADJUSTMENT							

Bit 7:0 MCK2 PLL Numerator Adjustment

CCR98: MCK PLL Numerator Adjustment 3

Read/Write Address: 3C5h, Index: 98h
Power-on Default: 00h

In “powernormal” mode and 3D is on CCR6A value is reduced by subtracting CCR98 to control MCK PLL’s numerator.

7	6	5	4	3	2	1	0
MCK PLL NUMERATOR ADJUSTMENT							

Bit 7:0 MCK PLL Numerator Adjustment

CCR99: MCK2 PLL Numerator Adjustment 3

Read/Write Address: 3C5h, Index: 99h
Power-on Default: 00h

In “powernormal” mode and 3D is on CCR63 value is reduced by subtracting CCR99 to control MCK2 PLL’s numerator.

7	6	5	4	3	2	1	0
MCK2 PLL NUMERATOR ADJUSTMENT							

Bit 7:0 MCK2 PLL Numerator Adjustment

CCR9A: MCK PLL Numerator Adjustment 4

Read/Write Address: 3C5h, Index: 9Ah

Power-on Default: 00h

In “powersaving” mode and 3D is on CCR6A value is reduced by subtracting CCR9A to control MCK PLL’s numerator.

7	6	5	4	3	2	1	0
MCK PLL NUMERATOR ADJUSTMENT							

Bit 7:0 MCK PLL Numerator Adjustment

CCR9B: MCK2 PLL Numerator Adjustment 4

Read/Write Address: 3C5h, Index: 9Bh
Power-on Default: 00h

In “powersaving” mode and 3D is on CCR63 value is reduced by subtracting CCR9B to control MCK2 PLL’s numerator.

7	6	5	4	3	2	1	0
MCK2 PLL NUMERATOR ADJUSTMENT							

Bit 7:0 MCK2 PLL Numerator Adjustment

CCR9C: MCK PLL Numerator Adjustment 5

Read/Write Address: 3C5h, Index: 9Ch
Power-on Default: 00h

In “poweridle” mode and 3D is on CCR6A value is reduced by subtracting CCR9C to control MCK PLL’s numerator.

7	6	5	4	3	2	1	0
MCK PLL NUMERATOR ADJUSTMENT							

Bit 7:0 MCK PLL Numerator Adjustment

CCR9D: MCK2 PLL Numerator Adjustment 5

Read/Write Address: 3C5h, Index: 9Dh
Power-on Default: 00h

In “poweridle” mode and 3D is on CCR63 value is reduced by subtracting CCR9D to control MCK2 PLL’s numerator.

7	6	5	4	3	2	1	0
MCK2 PLL NUMERATOR ADJUSTMENT							

Bit 7:0 MCK2 PLL Numerator Adjustment

CCR9E: PLL Post Divider Control

Read/Write Address: 3C5h, Index: 9Eh
Power-on Default: 00h

The post divider is also controlled by PDR20[5:4]. Refer to PDR20[5:4] for the definition.

7	6	5	4	3	2	1	0
M2CLK PLL		**MCLK PLL**		**VRCLK PLL**		**VLK PLL**	

Bit 7:6 Output divide for M2CLK PLL
00 = No divide for M2CLK PLL output
01 = M2CLK PLL output divide by 4
10 = M2CLK PLL output divide by 8
11 = M2CLK PLL output divide by 16

Bit 5:4 Output divide for MCKPLL
00 = No divide for MCLK PLL output
01 = MCLK PLL output divide by 4
10 = MCLK PLL output divide by 8
11 = MCLK PLL output divide by 16

Bit 3:2 Output divide for VRCLK PLL
00 = No divide for VRCLK PLL output
01 = VRCLK PLL output divide by 4
10 = VRCLK PLL output divide by 8
11 = VRCLK PLL output divide by 16

Bit 1:0 Output divide for VCLK PLL
00 = No divide for VCLK PLL output
01 = VCLK PLL output divide by 4
10 = VCLK PLL output divide by 8
11 = VsCLK PLL output divide by 16

General Purpose Registers

GPR70: Scratch Pad Register 1

Read/Write Address: 3C5h, Index: 70h
Power-on Default: Undefined except for bit [3:0] which are power-on configurable (by RESET)

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD REG BITS				**PRIMARY PANEL ID**			

Bit 7:4 Scratch pad register bits. This register can be used as general purpose bits.

Bit 3:0 Primary panel ID
0000 = 640 x 480 TFT
0001 = 800 x 600 TFT
0010 = 1024 x 768 TFT
0011 = 1280 x 1024 TFT
0100 = 1600 x 1200 TFT

GPR71: Scratch Pad Register 2

Read/Write Address: 3C5h, Index: 71h
Power-on Default: Undefined

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD 2 REGISTER							

Bit 7:0 Scratch Pad 2 register. This register can be used as general purpose scratch bits.

GPR72: User Defined Register 1 for DDC2/ I2C

Read/Write Address: 3C5h, Index: 72h
Power-on Default: 00h

This register is used for user defined registers: USR1/SDA and USR0/SCL. The SDA and SCL can be used for VESA DDC2 / I2C serial communication port.

7	6	5	4	3	2	1	0
RESERVED		**EUSR1**	**EUSR0**	**USR1S**	**USR0S**	**USR1W**	**USR0W**

Bit 7:6 Reserved

Bit 5 Enable USR1/SDA Port (EUSR1)
0 = Disable use of bit 1 of this register
1 = Enable use of bit 1 of this register

Bit 4 Enable USR0/SCL Port (EUSR0)
0 = Disable use of bit 0 of this register
1 = Enable use of bit 0 of this register

Bit 3 USR1/SDA Status (Read only). This bit can be used for DDC2/I2C Data. (USR1S)
0 = pin USR1/SDA is low
1 = pin USR1/SDA is tri-stated

Bit 2 USR0/SCL Status (Read only). This bit can be used for DDC2/I2C Clock. (USR0S)
0 = pin USR0/SCL is low

1 = pin USR0/SCL is tri-stated

Bit 1 USR1/SDA Write. Pin 131 can be used for DDC2/I2C Data. When pin USR1/SDA is tri-stated, other devices may drive this line. The actual state of the pin USR1/SDA is read via bit 3 of this register. (USR1W)
0 = pin USR1/SDA is driven low
1 = pin USR1/SDA is tri-stated

Bit 0 USR0/SCL Write. Pin 132 can be used for DDC2/I2C Clock. When pin USR0/SCL is tri-stated, other devices may drive this line. The actual state of the pin USR0/SCL is read via bit 2 of this register. (USR0W)0 = pin USR0/SCL is driven low
1 = pin USR0/SCL is tri-stated

Note: See Appendix D for further details.

GPR73: User Defined Register 2

Read/Write Address: 3C5h, Index: 73h
Power-on Default: 00h

This register can be used to control user programmable outputs: USR2 and USR3 pins.

7	6	5	4	3	2	1	0
RESERVED		**USR3P**	**USR2P**	**USER3**	**USER2**	**USR3W**	**USR2W**

Bit 7:6 Reserved

Bit 5 Enable USR3 Port (USR3P)
0 = Disable use of bit 1 of this register
1 = Enable use of bit 1 of this register

Bit 4 Enable USR2 Port (USR2P)
0 = Disable use of bit 0 of this register
1 = Enable use of bit 0 of this register

Bit 3 USER3 Status (Read only) (USER3)
0 = pin USR3 is low
1 = pin USR3 is tri-stated

Bit 2 USER2 Status (Read only) (USER2)
0 = pin USR2 is low
1 = pin USR2 is tri-stated

Bit 1 USR3 Write. When pin USR3 is tri-stated, other devices may drive this line. The actual state of the pin USR3 is read via bit 3 of this register. (USR3W)
0 = pin USR3 is driven low
1 = pin USR3 is tri-stated

Bit 0 USR2 Write. When pin USR2 is tri-stated, other devices may drive this line. The actual state of the pin USR2 is read via bit 2 of this register. (USR2W)
0 = pin USR2 is driven low
1 = pin USR2 is tri-stated

GPR74: Scratch Pad Register 3

Read/Write Address: 3C5h, Index: 74h
Power-on Default: Undefined

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD 3 REGISTER							

Bit 7:0 Scratch Pad 3 register. This register can be used as general purpose scratch bits.

GPR75: Scratch Pad register 4

Read/Write Address: 3C5h, Index: 75h
Power-on Default: Undefined

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD 4 REGISTER							

Bit 7:0 Scratch Pad 4 register. This register can be used as general purpose scratch bits.

Pop-up Icon and Hardware Cursor Registers

PHR80: Pop-up Icon and Hardware Cursor Pattern Location Low

Read/Write Address: 3C5h, Index: 80h
Power-on Default: Undefined

This register specifies the low 8 bits of the address for pop-up icon and Hardware Cursor Pattern Location, which is a 11-bit register. The high order 3 bits are specified in the PHR81 [2:0] register.

7	6	5	4	3	2	1	0
POP-UP ICON AND HARDWARE CURSOR PATTERN							

Bit 7:0 Pop-up Icon and Hardware Cursor Pattern Location Low. The PHR80 and PHR81 [2:0] registers allocate 2KB off-screen memory within the maximum 4MB of physical memory. The lower 1KB is used to store Pop-up Icon image. The upper 1KB is used to store Hardware Cursor image

PHR81: Hardware Cursor Enable & PI/HWC Pattern Location High

Read/Write Address: 3C5h, Index: 81h
Power-on Default: 0xh

This register specifies the hardware cursor enable and the high-order 3 bits of the address for pop-up icon and Hardware Cursor Pattern Location, which is a 11-bit register. The low order 8 bits are specified in the PHR80 register.

7	6	5	4	3	2	1	0
HCE	**R**	**POP-UP ICON**					

Bit 7 Hardware Cursor Enable (HCE)
0 = Disable (default)
1 = Enable

Bit 6 Reserved (R)

Bit 5:0 Pop-up Icon and Hardware Cursor Pattern Location High. The PHR80 and PHR81 [2:0] registers allocate 2KB off-screen memory within the maximum 32MB of physical memory. The lower 1KB is used to store Pop-up Icon image. The upper 1KB is used to store Hardware Cursor image.

Pop-up Icon Registers

POP82: Pop-up Icon Control

Read/Write Address: 3C5h, Index: 82h
Power-on Default: 00h

This register specifies the control for pop-up icon.

7	6	5	4	3	2	1	0
PUIE	**PUIZE**	**RESERVED**					

Bit 7 Pop-up Icon Enable (PUIE)
0 = Disable
1 = Enable

Bit 6 Pop-up Icon Zoom Enable (PUIZE)
0 = Normal. (Pop-up Icon size is 64x64x2)
1 = zoom up the Pop-up Icon size by 2. (Pop-up Icon size is 128x128x2)

Bit 5:0 Reserved

POP83: Reserved

Read/Write Address: 3C5h, Index: 83h
Power-on Default: Undefined

This register is reserved.

7	6	5	4	3	2	1	0
RESERVED							

Bit 7:0 Reserved

POP84: Pop-up Icon Color 1

Read/Write Address: 3C5h, Index: 84h
Power-on Default: Undefined

This register specifies the color1 for pop-up icon.

7	6	5	4	3	2	1	0
POP-UP ICON COLOR1							

Bit 7:0 Pop-up icon color1.

POP85: Pop-up Icon Color 2

Read/Write Address: 3C5h, Index: 85h
Power-on Default: Undefined

This register specifies the color2 for pop-up icon.

7	6	5	4	3	2	1	0
POP-UP ICON COLOR2							

Bit 7:0 Pop-up icon color2.

POP86: Pop-up Icon Color 3

Read/Write Address: 3C5h, Index: 86h
Power-on Default: Undefined

This register specifies the color3 for pop-up icon.

7	6	5	4	3	2	1	0
POP-UP ICON COLOR3							

Bit 7:0 Pop-up icon color3.

POP90: Pop-up Icon Start X - Low

Read/Write Address: 3C5h, Index: 90h
Power-on Default: Undefined

This register specifies Pop-up icon location X start [7:1]. The pop icon can only be moved in X direction by increments of 2 pixels. Bit [0] has no effect

7	6	5	4	3	2	1	0
POP-UP ICON X START [7:0]							**NE**

Bit 7:1 Pop-up icon X start [7:1]

Bit 0 Has no effect (NE)

POP91: Pop-up Icon Start X - High

Read/Write Address: 3C5h, Index: 91h
Power-on Default: Undefined

This register specifies Pop-up icon location X start [11:8]

7	6	5	4	3	2	1	0
RESERVED					**POP-UP ICON X START**		

Bit 7:3 Reserved

Bit 2:0 Pop-up icon X start [10:8]

POP92: Pop-up Icon Start Y - Low

Read/Write Address: 3C5h, Index: 92h
Power-on Default: Undefined

This register specifies Pop-up icon location Y start [7:0]

7	6	5	4	3	2	1	0
POP-UP ICON Y START							

Bit 7:0 Pop-up icon Y start [7:0]

POP93: Pop-up Icon Start Y - High

Read/Write Address: 3C5h, Index: 93h
Power-on Default: Undefined

This register specifies Pop-up icon location Y start [11:8]

7	6	5	4	3	2	1	0
RESERVED					**POP-UP ICON Y START**		

Bit 7:3 Reserved

Bit 2:0 Pop-up icon Y start [10:8]

Hardware Cursor Registers

HCR88: Hardware Cursor Upper Left X Position - Low

Read/Write Address: 3C5h, Index: 88h
Power-on Default: 00h

This register specifies the lower 8-bit upper left X position for hardware cursor.

7	6	5	4	3	2	1	0
HARDWARE CURSOR X POSITION LOW ORDER							

Bit 7:0 Hardware Cursor X position low order 8 bits. The high order 3 bits are in HCR89[2:0].

HCR89: Hardware Cursor Upper Left X Position- High

Read/Write Address: 3C5h, Index: 89h
Power-on Default: 00h

This register specifies the upper left X position for hardware cursor.

7	6	5	4	3	2	1	0
RESERVED				**HCUL**	**HCXP**		

Bit 7:4 Reserved

Bit 3 Hardware Cursor Upper Left X Position Boundary Select (HCUL)
0 = hardware cursor is within the screen left side boundary. {HCR89[2:0], HCR88[7:0]} specify the X position of the hardware cursor from the left side boundary.
1 = hardware cursor is partially or totally outside of the left side screen boundary. HCR88 [4:0] specify how many pixels of the hardware cursor are outside the left side screen boundary.

Bit 2:0 Hardware Cursor X position high-order 3 bits. The low order 8 bits are specified in the HCR88 register. (HCXP)

HCR8A: Hardware Cursor Upper Left Y Position - Low

Read/Write Address: 3C5h, Index: 8Ah
Power-on Default: 00h

This register specifies the upper left Y position for hardware cursor.

7	6	5	4	3	2	1	0
HARDWARE CURSOR Y POSITION LOW ORDER							

Bit 7:0 Hardware Cursor Y position low order 8 bits. The high order 3 bits are in HCR8B [2:0].

HCR8B: Hardware Cursor Upper Left Y Position - High

Read/Write Address: 3C5h, Index: 8Bh
Power-on Default: 00h

This register specifies the upper left Y position for hardware cursor.

7	6	5	4	3	2	1	0
RESERVED				**HCUL**	**HCYP**		

Bit 7:4 Reserved

Bit 3 Hardware Cursor Upper Left Y Boundary Select (HCUL)
0 = hardware cursor is within the screen top side boundary. {HCR8B[2:0], HCR8A[7:0]} specify the Y position of the hardware cursor from the top side boundary.
1 = hardware cursor is partially or totally outside of the top side screen boundary. HCR8A [4:0] specify how many pixels of the hardware cursor are outside the top side screen boundary.

Bit 2:0 Hardware Cursor Y position high-order 3 bits. The low order 8 bits are specified in the HCR8A register. (HCYP)

HCR8C: Hardware Cursor Foreground Color

Read/Write Address: 3C5h, Index: 8Ch
Power-on Default: 00h

This register specifies the foreground color for hardware cursor. Hardware Cursor is always in 24-bit color. The 24-bit color is the expansion of 3:3:2 RGB into 8:8:8 RGB color.

7	6	5	4	3	2	1	0
HARDWARE CURSOR FOREGROUND COLOR							

Bit 7:0 Hardware Cursor foreground color
This register defines 3:3:2 8-bit RGB of the Hardware Cursor foreground color.

HCR8D: Hardware Cursor Background Color

Read/Write Address: 3C5h, Index: 8Dh
Power-on Default: 00h

This register specifies the background color for hardware cursor. Hardware Cursor is always in 24-bit color. The 24-bit color is the expansion of 3:3:2 RGB into 8:8:8 RGB color.

7	6	5	4	3	2	1	0
HARDWARE CURSOR BACKGROUND COLOR							

Bit 7:0 Hardware Cursor background color
This register defines 3:3:2 8-bit RGB of the Hardware Cursor background color.

Extended CRT Control Registers

CRT30: CRTC Overflow and Interlace Mode Enable

Read/Write Address: 3?5h, Index: 30h
Power-on Default: 00h

This register specifies the CRTC overflow registers and Interlace Mode Enable.

7	6	5	4	3	2	1	0
IME	**CRT DISPLAY**			**CVTR**	**CVDER**	**CVBS**	**CVRS**

Bit 7 Interlace Mode Enable (IME)
0 = Disable
1 = Enable

Bit 6:4 Bit [18:16] of the CRT display starting address. The lower order 16-bit are located in CRTC register index 0Ch and 0Dh.

Bit 3 Bit 10 of the CRT vertical total register. The lower bit [9:0] are defined in CRTC register index 07h and 06h. (CVTR)

Bit 2 Bit 10 of the CRT vertical display end register. The lower bit [9:0] are defined in CRTC register index 12h and 07h. (CVDER)

Bit 1 Bit 10 of the CRT vertical blank start. The lower bit [9:0] are defined in CRTC register index 15 h, 09h, and 07h. (CVBS)

Bit 0 Bit 10 of the CRT vertical retrace start. The lower bit [9:0] are defined in CRTC register index 10h and 07h. (CVRS)

CRT31: Interlace Retrace

Read/Write Address: 3?5h, Index: 31h
Power-on Default: 00h

This register specifies when vertical retrace begins. This register is only valid if interlace mode is enabled (CRT30 Bit 7 = 1).

7	6	5	4	3	2	1	0
SPECIFIY # CHARACTER UNITS IN HORIZONTAL TIMING							

Bit 7:0 Specify the number of character units in horizontal timing when vertical retrace begins.

CRT32: TV Vertical Display Enable Start

Read/Write Address: 3?5h, Index: 32h
Power-on Default: 00h

This register specifies the vertical display enable start for TV timing.

7	6	5	4	3	2	1	0
TV VERTICAL DISPLAY ENABLE							

Bit 7:0 When CRT vertical count = CRT32 [7:0], TV vertical display enable become active.

CRT33: TV Vertical Display Enable End - High

Read/Write Address: 3?5h, Index: 33h
Power-on Default: 00h

This register specifies the vertical display enable end for TV timing. This register is a 11-bit register. The lower 8-bit of this register resides in CRT34.

7	6	5	4	3	2	1	0
ITE	**HBE**		**VBE**		**CRT VERTICAL COUNT**		

Bit 7 Interlace Timing Enable for double scan modes (i.e.: mode 13, etc.) (ITE)
0 = Disable
1 = Enable

Bit 6:5 Bit [7:6] of Horizontal Blank End. Bit 5 is located in bit 7 of CRTC register, 3?5h, index 5. Bit [4:0] is located in CRTC register, 3?5h, index 3. (HBE)

Bit 4:3 Bit [9:8] of Vertical Blank End. Bit [7:0] of Vertical Blank End is located in CRTC register, 3?5h, index 16. (VBE)

Bit 2:0 When CRT vertical count = {CRT33 [2:0],CRT34 [7:0]}, TV vertical display enable becomes inactive.

CRT34: TV Vertical Display Enable End - Low

Read/Write Address: 3?5h, Index: 34h
Power-on Default: 00h

This register specifies the vertical display enable end for TV timing.

7	6	5	4	3	2	1	0
CRT VERTICAL COUNT							

Bit 7:0 When CRT vertical count = {CRT33 [2:0],CRT34 [7:0]} TV vertical display enable becomes inactive.

CRT35: Vertical Screen Expansion DDA Control Constant - Low

Read/Write Address: 3?5h, Index: 35h
Power-on Default: 00h

This register specifies bit [7:0] the DDA control constant (DDACC) which is used for vertical screen expansion in VGA modes. Bit [9:8] of the DDACC is located in CRT36.

To enable vertical screen expansion in VGA graphics modes, one needs to program the DDA control constant (DDACC) equal to:

$$\text{DDACC} = \frac{1024 * \text{actual vertical size}}{\text{expanded vertical size}}$$

To enable vertical expansion in VGA text mode, one must program DDACC [2:0] = # of times the last character row should be repeated.

7	6	5	4	3	2	1	0
VERTICAL SCREEN EXPANSION							

Bit 7:0 This register defines the lower 8 bits of the vertical screen expansion DDA control constant. The upper 2 bits of the DDACC register is located in CRT36. For VGA text modes, only the lower [2:0] are valid.

CRT36: Vertical Screen Expansion DDA Control Constant - High

Read/Write Address: 3?5h, Index: 36h
Power-on Default: 00h

This register the vertical screen expansion DDA control constant lower 8 bits.

7	6	5	4	3	2	1	0
RESERVED						**VSE**	

Bit 7:2 Reserved

Bit 1:0 This register defines bit [9:8] of the vertical screen expansion DDA control constant. The lower 8-bit are located in CRT35. (VSE)

CRT37: Hardware/VGA Test Selection/Display Control

Read/Write Address: 3?5h, Index: 37h
Power-on Default: 00h

7	6	5	4	3	2	1	0
VGA TEST BUS			**VGA**	**HVDE**	**DISPLAY CONTROL**		

Bit 7:5 VGA test bus selection. These bits select groups of VGA signals to test the bus. This is for testing purposes only

Bit 4 This is used for VGA testing only. Should default to 0. (VGA)
0 = In non VGA mode, the display enable and blank signal is 1 character clock (plus 3 pixel clocks) earlier compared with VGA mode.
1 = In non VGA mode, the display enable and blank signal matches with VGA mode timing

Bit 3 Horizontal and vertical display enable (HVDE)
0 = Normal
1 = Lock horizontal and vertical display enable shadow registers

Bit 2:0 Display control
000 = CRT display only
001 = LCD display is on. CRT shadow registers are locked
010 = CRT display only
011 = CRT & LCD display. CRT shadow registers are locked
100 = TV display
101 = TV & LCD display
110 = In legal setting
111 = In legal setting

CRT38: Extra Horizontal Timing Control

Read/Write Address: 3?5h, Index: 38h
Power-on Default: 00h

7	6	5	4	3	2	1	0
LS	**RESERVED**			**VB**	**HS**	**HB**	**HT**

Bit 7 Lock Shadow (LS)
0 = Normal (default)
1 = Lock all shadow registers including CRT33 Bit [6:3]

Bit 6:4 Reserved

Bit 3 Vertical blank end bit [10] (VB)

Bit 2 Horizontal sync start bit [8] (HS)

Bit 1 Horizontal blank end bit [8] (HB)

Bit 0 Horizontal total bit [8] (HT)

CRT39: Scratch Register

Read/Write Address: 3?5h, Index: 39h
Power-on Default: 00h

7	6	5	4	3	2	1	0
SCRATCH REGISTER							

Bit 7:0 Scratch register

CRT3A: TV Total Timing Control for the Internal TV Encoder

Read/Write Address: 3?5h, Index: 3Ah
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**HSYNC**			**DOT CLOCKS**		

Bit 7:6 Reserved

Bit 5:3
00 = Normal
01 = HSYNC delayed by one pixel clock
02 = HSYNC delayed by two pixel clock
03 = HSYNC delayed by three pixel clock
04 = HSYNC delayed by four pixel clock
05 = HSYNC delayed by five pixel clock

Bit 2:0
07 = One character clock contains 7 dot clocks
06 = One character clock contains 6 dot clocks
05 = One character clock contains 5 dot clocks
04 = One character clock contains 4 dot clocks
03 = One character clock contains 3 dot clocks
02 = One character clock contains 2 dot clocks
01 = One character clock contains 1 dot clocks
00 = One character clock contains 0 dot clocks

For example, to program 910 pixel horizontal total for 4fc NTSC TV mode:

Program CRT horizontal total register to be 109 character clock
Program 3?4 index 3A bit [2:0] = 06
The actual total number of characters per horizontal line is 109 + 5 = 114
The horizontal total in pixel clock is: 113 x 8 + 6 = 910

CRT3B: Miscellaneous Lock Register I

Read/Write Address: 3?5h, Index: 3Bh
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED FOR VGA HARDWARE TESTING							

Bit 7:0 Reserved for VGA Hardware testing

CRT3C: Miscellaneous Lock Register II

Read/Write Address: 3?5h, Index: 3Ch
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**BSS**	**VGALC**	**BLINKING LOGIC**		**BLINK RATE**	

Bit 7:6 Reserved VGA hardware debug test bus selection

Bit 5 Blanking signal selection (BSS)
0 = The blanking signal sent to RAMDAC is reversed active display. Outside of active display the blanking is active (black color). The border color register has no effect.
1 = The blank signal sent to RAMDAC is the normal blank signal from CRT. When both the blank and dispen are inactive the border color is displayed.

Bit 4 VGA line compare register (CRT09 [6] and CRT07 [4]) force (VGALC)
0 = normal (default)
1 = Enable. Force line compare [9:8] to be high. The original line compare control bits [9:8] have no effect. This register is used for Japanese DOS hardware scrolling compatibility purpose.

Bit 3:2 For testing blinking logic text mode
Bit [2] = 1 enable test mode
Bit [3] = 1 for blank to act

Bit 1:0 Select LCD character/cursor blink rate in text modes
00 = Character/cursor blink every 16 frames
01 = Character/cursor blink every 32 frames
1x = Character/cursor blink every 64 frames

CRT3D Scratch Register Bits

Read/Write Address: 3?5h, Index: 3Dh
Power-on Default:

7	6	5	4	3	2	1	0
SCRATCH REGISTER BITS							

Bit 7:0 Scratch Register Bit

CRT3E: Scratch Register Bits

Read/Write Address: 3?4h, Index: 3Eh
Power-on Default: 00h

7	6	5	4	3	2	1	0
SCRATCH REGISTER BITS							

Bit 7:0 Scratch Register Bits

CRT3F: Scratch Register Bits

Read/Write Address: 3?4h, Index: 3Fh
Power-on Default: 00h

7	6	5	4	3	2	1	0
SCRATCH REGISTER BITS							

Bit 7:0 Scratch Register Bits

CRT9E: Expansion/Centering Control Register 2

Read/Write Address: 3?4h, Index: 9Eh
Power-on Default: 00h

7	6	5	4	3	2	1	0
FE	**HSCRT**	**HSRW**	**VE**	**VC**	**VEE**	**VCE**	**HCE**

Bit 7 Font expansion control bit (FE)
This bit is effective if the following is true: CRT9E_[4] = 0 and the text mode plus the vertical expansion is on and CRT09_[4:0] < H0F
0 = The font vertical expansion will repeat the last character row
1 = The font vertical expansion will insert lines (with screen background color) between the last scan line of the current character row and the first scan of the next character row.

Bit 6 Horizontal shadow register selection for CRT timing control (HSCRT)
0 = There are two sets of horizontal shadow registers (primary and secondary). The selection switch is at the beginning of the vsync. If CR9F_[0] or CR9F [1] is equal to 1 the second set is selected. If these registers are not equal to 1 then the primary set is selected.
1 = To force the selection of the second set of horizontal shadow register

Bit 5 Horizontal shadow register read/write selection (HSRW)

The following register update are effected
SVR40_[7:0] - Horizontal total shadow
SVR41_[7:0] - Horizontal blank start shadow
SVR42_[4:0] - Horizontal blank end shadow
SVR44_[7] - Horizontal blank end bit 5 shadow
CRT33_[6:5] - Horizontal blank end bit 7 & 6
SVR43_[7:0] - Horizontal sync start shadow
SVR44_[4:0] - Horizontal sync end
CRT9F_[0] - 10 dots expansion
CRT9F_[1] - 12 dots expansion

These registers have two sets - primary and secondary.
Bit 5=0: The primary registers are selected for W/R and control crt
Bit 5=1: The secondary registers are selected for W/R and control crt

Bit 4 Vertical expansion DDA value selection (VE)
0 = Vertical expansion will select the DDA value from the DDA look up table (3?4.35&36). This bit has no effect if bit 2 of this register = 0.
1 = Vertical expansion will select the DDA value from the DDA look up table (3?4.90-91B).

Bit 3 Vertical centering offset value selection (VC)
0 = Select vertical centering offset value from vertical center offset register (3?4, Index A6). This bit has no effect if bit 1 of this register = 0
1 = Select vertical centering offset value from a look-up table (look up by vdispend)

Bit 2 Vertical expansion enable selection (VEE)
0 = Vertical expansion disable
1 = Vertical expansion enable

Bit 1 Vertical centering enable selection (VCE)
0 = Vertical centering disable
1 = Vertical centering enable

Bit 0 Horizontal centering enable selection (HCE)
0 = Horizontal centering disable
1 = Horizontal centering enable

CRT9F: Expansion/Center Control Register 1

Read/Write Address: 3?4h, Index: 9Fh
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**HT**	**16DOT**	**CC12**	**CC10**

Bit 7:4 Reserved

Bit 3 For hardware testing only (HT)
0 = VGA mode use non divide by 2 video clock. Extended VGA mode use divide by 2 video clock
1 = Reserved for 16 dot expansion. Should set to 0.

Bit 2 Blank pixel
0 = Normal
1 = In 10 dots expansion mode, this bit if set to 1 will insert blank pixels between characters in VGA text modes.

Bit 1 12 dot expansion (CC12)
0 = 12 dots expansion disabled
1 = Character clock expand to 12 dots regardless of bit 0 of this register

Bit 0 10 dot expansion (CC10)
0 = 10 dots expansion
1 = Character clock expand to 10 dots

CRT90-9B Vertical DDA Look Up Table & CRTA0-A5: Vertical Centering Offset Look Up Table

Read/Write Address: 3?4, Index A0h-A5h
Power-on Default: 00h

3?4.90								**3?4.91**								**3?4.A0**					
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	5	4	3	2	1	0
FIELD 3								**FIELD 2**								**FIELD 1**					

Field 3: This field compared with Vdisp_end (3?4.12 bit_[7:2])

Field 2: This field is selected DDA value if field 3 compares

Field 1: This field is selected vertical centering offset value if field 3 compares. The actual offset value = 3?4.A0_[5:0] x 4

The vertical expansion/centering using look up table is enabled only if the following conditions are true: CR9E_[3:1] = 111; if the compare fails to match with any entry, the value from 3?4.A6 will be used for vertical centering and the 3?4.35&36 will be used for DDA.

The following register groups behave the same:

3?4.92; 3?4.93; 3?4.A1
3?4.94; 3?4.95; 3?4.A2

3?4.96; 3?4.97; 3?4.A3
3?4.98; 3?4.99; 3?4.A4
3?4.9A; 3?4.9B; 3?4.A5

CRTA0-A5: Vertical Centering Offset Look Up Table

Read/Write Address: 3?4, Index A0h-A5h
Power-on Default: 00h

3?4.90								3?4.91								3?4.A0					
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	5	4	3	2	1	0
FIELD 3								FIELD 2								FIELD 1					

Field 3: This field compared with Vdisp_end (3?4.12 bit_[7:2])

Field 2: This field is selected DDA value if field 3 compares

Field 1: This field is selected vertical centering offset value if field 3 compares. The actual offset value = 3?4.A0_[5:0] x 4

The vertical expansion/centering using look up table is enabled only if the following conditions are true: CR9E_[3:1] = 111; if the compare fails to match with any entry, the value from 3?4.A6 will be used for vertical centering and the 3?4.35&36 will be used for DDA.

The following register groups behave the same:

3?4.92; 3?4.93; 3?4.A1
3?4.94; 3?4.95; 3?4.A2
3?4.96; 3?4.97; 3?4.A3
3?4.98; 3?4.99; 3?4.A4
3?4.9A; 3?4.9B; 3?4.A5

CRTA6: Vertical Centering Offset Register

Read/Write Address: 3?4, Index: A6h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		LINE SHIFT DOWN					

Bit 7:6 Reserved

Bit 5:0 Specifies how many lines the screen image will shift down. This register will have no effect if 3?4.9E bit_[1]=1

CRTA7: Horizontal Centering Offset Register

Read/Write Address: 3?4h, Index: A7h
Power-on Default: 00h

7	6	5	4	3	2	1	0
R	**CHARACTER UNIT SHIFT RIGHT**						

Bit 7 Reserved (R)

Bit 6:0 Specifies how many character units the screen image will shift to the right. This register has no effect if 3?4.9E BIT_[0] = 0.

0 = Use to specify how many character units the screen image will shift to the right to center position. The horizontal screen centering look up table has no effect.

1 = To enable horizontal shift look up table (CRT9E_[0] has to be 1). One of the table entry will be select and the value in the entry specifies how many character units the screen image will shift to the right center position.

The selection of the look up is as follows:
IF CRT01_[7:1] = CRTA8_[6:0] control screen centering. Else if CRT01_[7:1] = CRTAA_[6:0], CRTAB_[6:0] control screen centering. Else if CRT01_[7:1] = CRTAC_[6:0], CRTAD_[6:0] control screen centering. Else CRA7_[6:0] will be used as default to control screen centering.

CRTA8-AD: Horizontal Screen Centering Look Up Table

Read/Write Address: 3?4, Index A8h-Adh
Power-on Default: 00h

7	6	5	4	3	2	1	0
R	**HORIZONTAL SCREEN CENTERING LOOK UP TABLE**						

Bit 7: Reserved

Bit 6:0 Horizontal Screen Centering Look Up Table

Shadow VGA Registers

The Shadow VGA Registers are designed to control CRT, LCD and TV timing, and maintain VGA compatibility. SM731 shadows 12 VGA CRT registers. When these shadow registers are unlocked, the CPU I/O write operation can write into both standard CRT registers and shadow registers through standard VGA CRTC I/O location. When these shadow registers are locked, the CPU I/O write can only write into the standard CRT registers through CRTC I/O location. These 12 shadow registers also have specific I/O location which is not controlled by Shadow Lock/Unlock Register.

SVR40 - Horizontal Total	SVR45 - Vertical Total	SVR4A - Overflow (bit 7, 6,5, 3, 2, 1,and 0)
SVR41 - Start Horizontal Blanking	SVR46 - Start Vertical Blank	SVR4B - Maximum Scan Line (bit 5 only)
SVR42 - End Horizontal Blanking	SVR47 - End Vertical Blank	SVR4C - Horizontal Display End
SVR43 - Start Horizontal Retrace	SVR48 - Vertical Retrace Start	SVR4D - Vertical Display End
SVR44 - End Horizontal Retrace	SVR49 - Vertical Retrace End	

Automatic Lock/Unlock Scheme for Shadow Registers

There are two ways to access shadow registers. One is through standard VGA CRTC I/O location when CRT is the only selected display. These VGA CRT I/O write operations will write to both standard VGA CRT registers and shadow registers. The other way to access shadow registers is through their dedicated I/O locations. The shadow registers can only be read through their dedicated I/O locations.

When LCD or TV display is selected, the shadow registers will be automatically locked. The VGA CRT I/O write operation will write only to the standard VGA CRT registers. The shadow registers have to be accessed from their dedicated I/O location. This approach will reduce programming difficulty and maintain VGA compatibility.

SVR40: Shadow VGA Horizontal Total

Read/Write Address: 3?5h, Index: 40h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Total register.

7	6	5	4	3	2	1	0
SHADOW VGA HORIZONTAL TOTAL							

Bit 7:0 Defines the total character count minus 5 characters per horizontal scan line. This register only depends on the resolution of LCD, not the type of LCD.

SVR41: Shadow VGA Horizontal Blank Start

Read/Write Address: 3?5h, Index: 41h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Blank Start register.

7	6	5	4	3	2	1	0
SHADOW VGA HORIZONTAL BLANK							

Bit 7:0 When the horizontal character = SVR41 [7:0], shadow VGA horizontal blank become active.

SVR42: Shadow VGA Horizontal Blank End

Read/Write Address: 3?5h, Index: 42h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Blank End register.

7	6	5	4	3	2	1	0
R	**SDES**		**SHADOW VGA HORIZONTAL BLANK INACTIVE**				

Bit 7 Reserved (R)

Bit 6:5 Shadows display enable skew control (SDES)

Bit 4:0 When the horizontal character = {SVR44 [7],SVR42 [4:0]}, shadow VGA horizontal blank become inactive.

SVR43: Shadow VGA Horizontal Retrace Start

Read/Write Address: 3?5h, Index: 43h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Retrace Start register.

7	6	5	4	3	2	1	0
SHADOW VGA HORIZONTAL RETRACE INACTIVE							

Bit 7:0 When the horizontal character = SVR43 [7:0], shadow VGA horizontal retrace become active.

SVR44: Shadow VGA Horizontal Retrace End

Read/Write Address: 3?5h, Index: 44h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Retrace End register.

7	6	5	4	3	2	1	0
SVHB	**SHRD**		**SHADOW VGA HORIZONTAL RETRACE INACTIVE**				

Bit 7 When the horizontal character = {SVR44 [7],SVR41 [4:0]}, shadow VGA horizontal blank become inactive. (SVHB)

Bit 6:5 Shadows horizontal retrace delay (SHRD)

Bit 4:0 When the horizontal character = SVR44 [4:0], shadow VGA horizontal retrace become inactive.

SVR45: Shadow VGA Vertical Total

Read/Write Address: 3?5h, Index: 45h
Power-on Default: 00h

This register shadows VGA CRT Vertical Total register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL TOTAL							

Bit 7:0 Shadows the least significant 8 bits of 11 bits count of raster scan lines for display frame.

SVR46: Shadow VGA Vertical Blank Start

Read/Write Address: 3?5h, Index: 46h
Power-on Default: 00h

This register shadows VGA CRT Vertical Blank Start register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL BLANK START							

Bit 7:0 Shadows the least significant 8-bit of the 11-bit VGA CRT vertical blank start register.

SVR47: Shadow VGA Vertical Blank End

Read/Write Address: 3?5h, Index: 47h
Power-on Default: 00h

This register shadows VGA CRT Vertical Blank End register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL BLANK END							

Bit 7:0 Shadows the least significant 8-bit VGA CRT vertical blank end register.

SVR48: Shadow VGA Vertical Retrace Start

Read/Write Address: 3?5h, Index: 48h
Power-on Default: 00h

This register shadows VGA CRT Vertical Retrace Start register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL RETRACE START							

Bit 7:0 Shadows the least significant 8-bit of the 11-bit vertical retrace start register.

SVR49: Shadow VGA Vertical Retrace End

Read/Write Address: 3?5h, Index: 49h
Power-on Default: 00h

This register shadows VGA CRT Vertical Retrace End register.

7	6	5	4	3	2	1	0
RESERVED				**SHADOW VGA/CRT VERTICAL RETRACE**			

Bit 7:4 Reserved

Bit 3:0 Shadows bit [3:0] of VGA CRT vertical retrace end register.

SVR4A: Shadow VGA Vertical Overflow

Read/Write Address: 3?5h, Index: 4Ah
Power-on Default: 00h

This register shadows VGA CRT Vertical Overflow register.

7	6	5	4	3	2	1	0
SVRS9	**SVDE9**	**SVTB9**	**R**	**SVBS**	**SVRS8**	**SVDE8**	**SVTB8**

Bit 7 Shadows vertical retrace start bit 9 (SVRS9)

Bit 6 Shadow vertical display enable bit 9 (3?5h, index 7 [6]). When CRT37[3] = 1, can only access this bit through 3?5h, index 4Ah. (SVDE9)

Bit 5 Shadows vertical total bit 9 (SVTB9)

Bit 4 Reserved (R)

Bit 3 Shadows vertical blank start bit 8 (SVBS)

Bit 2 Shadows vertical retrace start bit 8 (SVRS8)

Bit 1 Shadow vertical display enable bit 8 (3?5h, index 7 [1]). When CRT37[3] = 1, can only access this bit through 3?5h, index 4Ah. (SVDE8)

Bit 0 Shadows vertical total bit 8 (SVTB8)

SVR4B: Shadow VGA Maximum Scan Line

Read/Write Address: 3?5h, Index: 4Bh
Power-on Default: 00h

This register shadows VGA CRT Maximum Scan Line register.

7	6	5	4	3	2	1	0
SSP		**SVBS**	**RESERVED**				

Bit 7:6 Shadow 3C2 bit_[7:6] for sync polarity (SSP)

Bit 5 Shadows vertical blank start bit 9 (SVBS)

Bit 4:0 Reserved

SVR4C: Shadow VGA Horizontal Display End

Read/Write Address: 3?5h, Index: 4Ch
Power-on Default: 00h

This register shadows VGA CRT Horizontal Display end.

7	6	5	4	3	2	1	0
SHADOW HORIZONTAL DISPLAY END							

Bit 7:0 Shadows Horizontal Display End register (3?5h, index 01). When CRT37[3] = 1, it locks access to this register only through 3?5h, index 4Ch.

SVR4D: Shadow VGA Vertical Display End

Read/Write Address: 3?5h, Index: 4Dh
Power-on Default: 00h

This register shadows VGA CRT Vertical Display end.

7	6	5	4	3	2	1	0
SHADOW VERTICAL DISPLAY END							

Bit 7:0 Shadows Vertical Display End register [7:0] (3?5h, index 12) When CRT37[3] = 1, it locks access to this register only through 3?5h, index 4Dh.

Chapter 21: Flat Panel Processor Registers

Table 24: Extended SMI Registers Quick Reference

Video Processor Control Registers

SM731 integrates a concurrent Flat Panel processor. It can support 2 independent video windows using hardware scaling for any size of video windows at any location of the screen display. The Flat Panel Processor Control Registers can only be accessed through memory-mapped.

FPR00: Miscellaneous Graphics and Video Control

Read/Write Address: 5800h
Power-on Default: 00000000h

This register specifies the controls for graphics and video window I/II. (where x = don't care)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DOFF	**R**	**R**	**FIELD**	**R**	**EBOB**	**R**	**CVWI**	**RESERVED**			**GDT**	**GDE**	**GDF**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TVWS	**VWIIC**	**R**	**VWIIT**	**VWIIE**	**VWIIF**			**VWIC**	**VWIL**		**VWIT**	**VWIE**	**VWIF**		

Bit 31 Display Off (DOFF)
0 = Display On
1 = Display Off (except POP UP ICON)

Bit 30 Reserved (R) (must be 0)

Bit 29 Reserved (R)

Bit 28 Current display field (FIELD) (read only)
0 = Current display even field
1 = Current display odd field

Bit 27 Reserved (R)

Bit 26 Enable BOB display (EBOB)
0 = Disable
1 = Enable

Bit 25 Reserved

Bit 24 Select video window I source start address same as video capture buffer start address. This bit is used to automatically display captured data on video window I without programming video window I source start address register (SVWI).
0 = Normal. Video window I source start address is from FPR1C register.
1 = Video window I source start address is equal to capture port buffer I source start address (FPR48) or capture port buffer II source start address (FPR4C). If single buffer is selected for video capture, video window I source start address is equal to capture port buffer I source address. If double buffer is selected for video capture and capture port buffer I is busy, video window I source start address is equal to capture port buffer II source address.

Bit 23:21 Reserved

Bit 20 Graphic Data in Tile format (GDT)
0 = Normal format
1 = Tile format

Bit 19 Graphic Enable (GDE)
0 = Disable
1 = Enable

Bit 18:16 Graphics Data Format (GDF)
000 = 8-bit index
001 = 15 -bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = Reserved
11x = Reserved

Bit 15 Top Video Window Select (TVWS)
0 = Video window I is on top
1 = Video window II is on top

Bit 14 Color Key Enable for Video Window II (CKEII)
0 = Disable
1 = Enable

Bit 13 Reserved (R)

Bit 12 Video Window II Data in Tile format (VWIIT)
0 = Normal format
1 = Tile format

Bit 11 Video Window II Enable (VWIIE)
0 = Disable
1 = Enable

Bit 10:8 Video Window II Format (VWFII)
000 = 8-bit index
001 = 15-bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = 8-bit 3-3-2 RGB
110 = YUV 4:2:2
111 = YUV 4:2:0 (UV interleave)

Bit 7 Color Key Enable for Video Window I (CKEI)
0 = Disable
1 = Enable

Bit 6:5 Video Window I Line of Filtering (VWIL)
00 = 1 line
01 = 2 line
1x = 4 line (data format cannot be YUV 4:2:0 and bit 29 must set to 1)

Bit 4 Video Window I Data in Tile format (VWIT)
0 = Normal format
1 = Tile format

Bit 3 Video Window I Enable (VWIE)
0 = Disable
1 = Enable

Bit 2:0 Video Window I Format (VWIF)
000 = 8-bit index
001 = 15-bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = 8-bit 3-3-2 RGB
110 = YUV 4:2:2
111 = YUV 4:2:0 (UV interleave)

FPR04: Color Keys

Read/Write Address: 5804h
Power-on Default: Undefined

This register specifies color keys for the two video windows

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**VIDEO WINDOW II COLOR KEY INDEX**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**VIDEO WINDOW I COLOR KEY INDEX**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II COLOR KEY [15:8]								**VIDEO WINDOW II COLOR KEY [7:0]**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I COLOR KEY [15:8]								**VIDEO WINDOW I COLOR KEY [7:0]**							

	8-bit color mode	**16-bit color mode**[1]
Bit 31:24	Reserved	Video Window II Color Key [15:8]
Bit 23:16	Video Window II Color Key Index	Video Window II Color Key [7:0]

Bit 15:8 Reserved Video Window I Color Key [15:8]

Bit 7:0 Video Window I Color Key Index Video Window I Color Key [7:0]

Note[1]: for 24-bit or 32-bit color mode, software will need to repack the color key data into RGB - 5:6:5 (16-bit) format.

FPR08: Color Key Masks

Read/Write Address: 5808h
Power-on Default: Undefined

This register specifies color key masks for the two video window.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II COLOR KEY MASK															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I COLOR KEY MASK															

Bit 31:16 Video Window II Color Key Mask
0 = Disable color mask
1 = Enable color mask

Bit 15:0 Video Window I Color Key Mask
0 = Disable color mask
1 = Enable color mask

FPR0C: Data Source Start Address for Extended Graphics Modes

Read/Write Address: 580Ch
Power-on Default: Undefined

This register specifies data source start address for extended graphics modes

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GDSB	**RESERVED**									**GDSSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GDSSA															

Bit 31 Graphic Data Status Bit (GDSB)

Bit 30:22 Reserved

Bit 21:0 Graphics Data Source Starting Address, in 64-bit segment (GDSSA)

FPR10: Data Source Width and Offset for Extended Graphics Modes

Read/Write Address: 5810h
Power-on Default: Undefined

This register specifies data source data line width and offset address for extended graphics modes.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**GRAPHICS DATA SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**GRAPHICS DATA START ADDRESS OFFSET**									

Bit 31:26 Reserved

Bit 25:16 Graphics Data Source data line width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Graphics Data Start Address Offset, in 64-bit segment

FPR14: Video Window I Left and Top Boundaries

Read/Write Address: 5814h
Power-on Default: Undefined

This register specifies left and top boundary for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW I TOP BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW I LEFT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video window I, top boundary

Bit 15:11 Reserved

Bit 10:0 Video window I, left boundary

FPR18: Video Window I Right and Bottom Boundaries

Read/Write Address: 5818h
Power-on Default: Undefined

This register specifies right and bottom boundary for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					VIDEO WINDOW I BOTTOM BOUNDARY										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					VIDEO WINDOW I RIGHT BOUNDARY										

Bit 31:27 Reserved

Bit 26:16 Video window I, bottom boundary

Bit 15:11 Reserved

Bit 10:0 Video window I, right boundary

FPR1C: Video Window I Source Start Address

Read/Write Address: 581Ch
Power-on Default: Undefined

This register specifies video start address for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWIS	RESERVED									VWISS					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWISS															

Bit 31 Video Window I Status Bit (VWIS)

Bit 30:22 Reserved

Bit 21:0 Video Window I source start address for, in 64-bit segment. (VWISS)

FPR20: Video Window I Source Width and Offset

Read/Write Address: 5820h
Power-on Default: Undefined

This register specifies video source data line width and offset address for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						VIDEO WINDOW I SOURCE DATA LINE									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						VIDEO WINDOW I SOURCE ADDRESS									

Bit 31:26 Reserved

Bit 25:16 Video Window I Source Data Line Width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Video Window I Source Address Offset, in 64-bit segment

FPR24: Video Window I Stretch Factor

Read/Write Address: 5824h
Power-on Default: 00000000h

This register specifies video horizontal and Vertical stretch factor for video window I. For optimal display quality, we recommend destination to source ratio to be maximum of 4:1. The two high bytes of this register can be used to enable the "Bob" function.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II INITAL ODD FIELD								**VIDEO WINDOW II INITIAL EVEN FIELD**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I HORIZONTAL STRETCH								**VIDEO WINDOW I VERTICAL STRETCH**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor

Bit 15:8 Video Window 1 Horizontal Stretch Factor (W1HSF)

note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W1HSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Video Window 1 Vertical Stretch Factor (W1VSF)
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W1VSF = \frac{Source}{Destination} * 256$$

FPR28: Video Window II Left and Top Boundaries

Read/Write Address: 5828h
Power-on Default: Undefined

This register specifies left and top boundary for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW II TOP BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW II LEFT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video Window II, Top Boundary

Bit 15:11 Reserved

Bit 10:0 Video Window II, Left Boundary

FPR2C: Video Window II Right and Bottom Boundaries

Read/Write Address: 582Ch
Power-on Default: Undefined

This register specifies right and bottom boundary for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW II BOTTOM BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW II RIGHT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video Window II, Bottom Boundary

Bit 15:11 Reserved

Bit 10:0 Video Window II, Right Boundary

FPR30: Video Window II Source Start Address

Read/Write Address: 5830h
Power-on Default: Undefined

This register specifies video start address for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWIIS	**RESERVED**									**VWIIDS**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIIDS															

Bit 31 Video Window II Status Bits (VWIIS)

Bit 30:22 Reserved

Bit 21:0 Video Window II Data Source Starting Address (VWIIDS)

FPR34: Video Window II Source Width and Offset

Read/Write Address: 5834h
Power-on Default: Undefined

This register specifies video source data line width and offset address for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**VIDEO WINDOW II SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**VIDEO WINDOW II SOURCE ADDRESS**									

Bit 31:26 Reserved

Bit 25:16 Video Window II Source Data Line Width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Video Window II Source Address Offset, in 64-bit segment

FPR38: Video Window II Stretch Factor

Read/Write Address: 5838h/3?5h, Index f8, f9, fa, fb
Power-on Default: 00000000h

This register specifies video horizontal and Vertical stretch factor for video window II. For optimal display quality, we recommend destination to source ratio to be maximum of 4:1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II INITAL ODD FIELD								**VIDEO WINDOW II INITIAL EVEN FIELD**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II HORIZONTAL STRETCH								**VIDEO WINDOW II VERTICAL STRETCH**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor

Bit 15:8 Video Window II Horizontal Stretch Factor (W2HSF)

note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W2HSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Video Window II Vertical Stretch Factor (W2VSF)
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W2VSF = \frac{Source}{Destination} * 256$$

FPR3C: Graphics and Video Control II

Read/Write: Address: 583Ch
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHF1								**SHF0**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**CKCS**	**SBE**	**SF**		**SE**	**EVWII UVS**	**RESERVED**		**EVWII HB**	**EVWI UVS**	**R**	**EVWI VB**	**EVWI HB**

Bit 31:24 Sub Picture horizontal filter 1 (SHF1)

Bit 23:16 Sub Picture horizontal filter 0 (SHF0)

Bit 15:13 Reserved

Bit 12 Color Key Control Sub-Picture (CKCS)
0 = Disable
1 = Enable*
* Only 8-bit and 16-bit sub-picture data format supported

Bit 11 Sub-Picture bi-linear enable (SBE)
0 = Disable
1 = Enable

Bit 10:9 Sub-Picture data format (SF)
00 = 8-bit alpha blending format (alpha_[3:0], color_[3:0])
01 = 16-bit alpha blending format (alpha_[7:0], color_[7:0])
1x = 32-bit alpha blending format (alpha_[7:0], color_[23:0])

Bit 8 Sub-Picture Enable (SE)
0 = Disable
1 = Enable

Bit 7 Video Window II UV Swap enable (EVWIIUVS)
0 = Disable
1 = Enable

Bit 6:5 Reserved

Bit 4 Video window II horizontal bi-linear enable (EVWIIHB)
0 = Disable
1 = Enable

Bit 3 Video Window I UV Swap enable (EVWIUVS)
0 = Disable
1 = Enable

Bit 2 Reserved

Bit 1 Video window I vertical bi-linear enable (EVWIVB)
0 = Disable
1 = Enable

Bit 0 Video window I horizontal bi-linear enable (EVWIHB)
0 = Disable
1 = Enable

FPR40: Sub Picture Scale Factor

Read/Write Address: 5840h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SUB PICTURE INITIAL ODD FIELD VERTICAL								**SUB PICTURE INITAL EVEN FIELD VERTICAL**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE HORIZONTAL SCALE FACTOR								**SUB PICTURE VERTICAL SCALE FACTOR**							

Bit 31:24 Sub Picture Initial Odd Field Vertical Scale Factor

Bit 23:16 Sub Picture Initial Even Field Vertical Scale Factor

Bit 15:8 Sub Picture Horizontal Scale Factor $GHSF = \frac{Source}{Destination} * 256$

Bit 7:0 Sub Picture Vertical Scale Factor $GVSF = \frac{Source}{Destination} * 256$

FPR44: Sub Picture Scale Factor LSB

Read/Write Address: 5844h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SUB PICTURE INITIAL ODD FIELD VERTICAL LSB								**SUB PICTURE INITAL EVEN FIELD VERTICAL LSB**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE HORIZONTAL SCALE FACTOR LSB								**SUB PICTURE VERTICAL SCALE FACTOR LSB**							

Bit 31:24 Sub Picture Initial Odd Field Vertical Scale Factor LSB

Bit 23:16 Sub Picture Initial Even Field Vertical Scale Factor LSB

Bit 15:8 Sub Picture Horizontal Scale Factor LSB GHSF = $\frac{\text{Source}}{\text{Destination}}$ * 65536

Bit 7:0 Sub Picture Vertical Scale Factor LSB GVSF = $\frac{\text{Source}}{\text{Destination}}$ * 65535

FPR48: Video Window I Chroma Data Source Starting Address

Read/Write Address: 5848h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VIDEO WINDOW I CHROMA DATA SOURCE**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I CHROMA DATA SOURCE															

Bit 31:22 Reserved

Bit 21:0 Video Window I Chroma Data Source Starting Address

FPR4C: Video Window II Chroma Data Source Starting Address

Read/Write Address: 584Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VIDEO WINDOW II CHROMA DATA SOURCE**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II CHROMA DATA SOURCE															

Bit 31:22 Reserved

Bit 21:0 Video Window II Chroma Data Source Starting Address

FPR50: Sub-Picture Data Source Starting Address

Read/Write Address: 5850h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**SUB-PICTURE DATA SOURCE**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB-PICTURE DATA SOURCE															

Bit 31:22 Reserved

Bit 21:0 Sub-picture Data Source Starting Address

FPR54: FIFO Priority Control

Read/Write Address: 5854h
Power-on Default: 07216543h

This register specifies FIFO priority controls for graphics, Flat Panel Read Frame Buffer FIFO1, Video Window I, Video Window II, Flat Panel Write Frame Buffer, Capture Window and Flat Panel Read Frame Buffer FIFO2. Graphics FIFO has the highest priority and Flat Panel Read FIFO2 has the lowest priority as default.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															

Bit 31:0 Reserved (must be 0)

FPR58: FIFO Empty Request level Control

Read/Write Address: 5858h
Power-on Default: 00004444h

This register specifies FIFO empty request level for graphics FIFO, Video Window I, and Video Window II. At the specified empty FIFO level, FIFO request will be generated. Default FIFO empty levels are all 6 or more empty. For LCD Read FIFO1/FIFO2 and LCD Write FIFO request level controls, they are located in FPR4A register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**S FIFO**			**R**	**VWII FIFO**			**R**	**VWI FIFO**			**R**	**GFIFO**		

Bit 31:15 Reserved

Bit 14:12 Sub Picture FIFO Empty request level Select (S FIFO)
00x = 2 or more empty
010 = 2 or more empty

011 = 3 or more empty
100 = 4 or more empty (default)
101 = 5 or more empty
11x = 6 or more empty

Bit 7 Reserved (R)

Bit 10:8 Video Window II FIFO Empty request level Select (VWII FIFO)
000 = 2 or more empty
001 = 4 or more empty
010 = 5 or more empty
011 = 6 or more empty
100 = 7 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

Bit 7 Reserved (R)

Bit 6:4 Video Window I FIFO Empty request level Select (VWI FIFO)
000 = 2 or more empty
001 = 4 or more empty
010 = 5 or more empty
011 = 6 or more empty
100 = 7 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

Bit 3 Reserved (R)

Bit 2:0 Graphics FIFO Empty request level Select (GFIFO)
000 = 2 or more empty
001 = 4 or more empty
010 = 5 or more empty
011 = 6 or more empty
100 = 7 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

FPR5C: YUV to RGB Conversion Constant

Read/Write Address: 585Ch
Power-on Default: EDEDEDh
This register specifies the YUV to RGB conversion constant.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LUMA Y ADJUSTMENT								**RED CONVERSION CONSTANT**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN CONVERSION CONSTANT								**BLUE CONVERSION CONSTANT**							

Bit 31:24 Luma Y Adjustment

Bit 23:16 Red Conversion Constant

Bit 15:8 Green Conversion Constant

Bit 7:0 Blue Conversion Constant

FPR60: Current Scan Line Position

Read Only Address: 5860h
Power-on Default: Undefined

This register specifies the current scan line position.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**CURRENT SCAN LINE**										

Bit 31:11 Reserved

Bit 10:0 Current Scan Line. This register returns the number for current scan line.

FPR64: Signature Analyzer Control and Status

Read/Write Address: 5864h
Power-on Default: Undefined

This register specifies controls and status for signature analyzer as well as the analyzer signature.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ANALYZER SIGNATURE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												**SAE**	**SAR**	**SASS**	

Bit 31:16 Analyzer Signature. These bits are Ready Only.

Bit 15:4 Reserved

Bit 3 Signature Analyzer Enable/Stop. Software needs to set this bit = 1 as a "ENABLE" control bit in order to enable signature analyzer. Once the analysis is completed, the hardware will reset this bit = 0 as a "STOP" status bit. (SAE)
0 = Stop (analysis is completed)
1 = Enable (analysis is in progress)

Bit 2 Signature Analyzer Reset/Normal. Software needs to set this bit = 1 as a (SAR)
"RESET" control bit to reset signature shift register to "0" before turning on signature analyzer. In the next vertical sync pulse after bit 3 and bit 2 have been set to "11", bit 2 will be automatically reset to "0" as a "NORMAL" status bit.
0 = Normal (disable reset to signature analyzer)
1 = Reset (enable reset to signature analyzer)

Bit 1:0 Signature Analyzer Source Select. These bits selects the input source for the signature analyzer. (SASS)
00 = Source is Red output from Multimedia RAMDAC
01 = Source is Green output from Multimedia RAMDAC
1x = Source is Blue output from Multimedia RAMDAC

FPR68: Video Window I Scale Factor LSB

Read/Write Address: 5868h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWI INITIAL ODD FIELD VERTICAL LSB								**VWI INITAL EVEN FIELD VERTICAL LSB**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWI HORIZONTAL SCALE FACTOR LSB								**VWI VERTICAL SCALE FACTOR LSB**							

Bit 31:24 Video Window I Initial Odd Field Vertical Scale Factor LSB

Bit 23:16 Video Window I Initial Even Field Vertical Scale Factor LSB

Bit 15:8 Video Window I Horizontal Scale Factor LSB GHSF = $\frac{\text{Source}}{\text{Destination}}$ * 65536

Bit 7:0 Video Window I Vertical Scale Factor LSB GVSF = $\frac{\text{Source}}{\text{Destination}}$ * 65535

FPR6C: Video Window II Scale Factor LSB

Read/Write Address: 586Ch
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWII INITIAL ODD FIELD VERTICAL LSB								**VWII INITAL EVEN FIELD VERTICAL LSB**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWII HORIZONTAL SCALE FACTOR LSB								**VWII VERTICAL SCALE FACTOR LSB**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor LSB

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor LSB

Bit 15:8 Video Window II Horizontal Scale Factor LSB GHSF = $\frac{\text{Source}}{\text{Destination}}$ * 65536

Bit 7:0 Video Window II Vertical Scale Factor LSB GVSF = $\frac{\text{Source}}{\text{Destination}}$ * 65535

FPR70: Sub Picture Color Look Up Register 0

Read/Write Address: 5870h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 0**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 0															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 0

FPR74: Sub Picture Color Look Up Register 1

Read/Write Address: 5874h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 1**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 1															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 1

FPR78: Sub Picture Color Look Up Register 2

Read/Write Address: 5878h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 2															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 2

FPR7C: Sub Picture Color Look Up Register 3

Read/Write Address: 587Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 3**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 3															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 3

FPR80: Sub Picture Color Look Up Register 4

Read/Write Address: 5880h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 4**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 4															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 4

FPR84: Sub Picture Color Look Up Register 5

Read/Write Address: 5884h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 5**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 5															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 5

FPR88: Sub Picture Color Look Up Register 6

Read/Write Address: 5888h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 6**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 6															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 6

FPR8C: Sub Picture Color Look Up Register 7

Read/Write Address: 588Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 7**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 7															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 7

FPR90: Sub Picture Color Look Up Register 8

Read/Write Address: 5890h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 8**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 8															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 8

FPR94: Sub Picture Color Look Up Register 9

Read/Write Address: 5894h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 9**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 9															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 9

FPR98: Sub Picture Color Look Up Register A

Read/Write Address: 5898h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP A**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP A															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register A

FPR9C: Sub Picture Color Look Up Register B

Read/Write Address: 589Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								SUB PICTURE COLOR LOOK UP B							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP B															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register B

FPRA0: Sub Picture Color Look Up Register C

Read/Write Address: 58A0h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								SUB PICTURE COLOR LOOK UP C							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP C															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register C

FPRA4: Sub Picture Color Look Up Register D

Read/Write Address: 58A4h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								SUB PICTURE COLOR LOOK UP D							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP D															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register D

FPRA8: Sub Picture Color Look Up Register E

Read/Write Address: 58A8h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								SUB PICTURE COLOR LOOK UP E							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP E															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register E

FPRAC: Sub Picture Color Look Up Register F

Read/Write Address: 58ACh
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								SUB PICTURE COLOR LOOK UP F							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP F															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register F

FPRB0: Sub Picture Top/Left Boundary

Read/Write 58B0h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					SUB PICTURE TOP BOUNDARY										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SUB PICTURE LEFT BOUNDARY										

Bit 31:27 Reserved

Bit 26:16 Sub Picture Top Boundary

Bit 15:11 Reserved

Bit 10:0 Sub Picture Left Boundary

FPRB4: Sub Picture Bottom/Right Boundary

Read/Write Address: 58B4h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					SUB PICTURE BOTTOM BOUNDARY										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SUB PICTURE RIGHT BOUNDARY										

Bit 31:27 Reserved

Bit 26:16 Sub Picture Bottom Boundary

Bit 15:11 Reserved

Bit 10:0 Sub Picture Right Boundary

FPRB8: Sub Picture Source Data Address Offset and Line Width

Read/Write Address: 58B8h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						SUB PICTURE SOURCE DATA LINE									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SUB PICTURE SOURCE DATA ADDRESS OFFSET									

Bit 31:26 Reserved

Bit 25:16 Sub Picture Source Data Line Width

Bit 15:10 Reserved

Bit 9:0 Sub Picture Source Data Address Offset

FPRC0: Data Source Last Start Address for Extended Graphics Modes

Read/Write Address: 58C0h
Power-on Default: 3FFFFF

This register specifies data source last starting address for extended graphics modes. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**GRAPHICS DATA SOURCE**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRAPHICS DATA SOURCE															

Bit 31:22 Reserved

Bit 21:0 Graphics Data Source Last Starting Address, in 64-bit segment

FPRC4: Data Source Last Start Address for Video Window I

Read/Write Address: 58C4h
Power-on Default: 3FFFFF

This register specifies data source last starting address for video window I. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VIDEO WINDOW I SOURCE**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I SOURCE															

Bit 31:22 Reserved

Bit 21:0 Video Window I Source Last Starting Address, in 64-bit segment

FPRC8: Data Source Last Start Address for Video Window II

Read/Write Address: 58C8h
Power-on Default: 3FFFFF

This register specifies data source last starting address for video window II. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VIDEO WINDOW II SOURCE**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II SOURCE															

Bit 31:22 Reserved

Bit 21:0 Video Window II Source Last Starting Address, in 64-bit segment (VWIISLSA)

FPRCC: Chroma Last Start Address for Video Window I

Read/Write Address: 58CCh
Power-on Default: 3FFFFF

This register specifies chroma last starting address for video window I. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VIDEO WINDOW I CHROMA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I CHROMA															

Bit 31:22 Reserved

Bit 21:0 Video Window I Chroma Last Starting Address, in 64-bit segment

FPRD0: Chroma Last Start Address for Video Window II

Read/Write Address: 58D0h
Power-on Default: 3FFFFF

This register specifies data source last starting address for video window II. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VIDEO WINDOW II CHROMA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II CHROMA															

Bit 31:22 Reserved

Bit 21:0 Video Window II Chroma Last Starting Address, in 64-bit segment

FPRD4: Horizontal Filter for Video Window I

Read/Write: Address: 58D4h
Power-on Default: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**VIDEO WINDOW I HORIZONTAL FILTER 2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I HORIZONTAL FILTER 1								**VIDEO WINDOW I HORIZONTAL FILTER 0**							

Bit 31:24 Reserved

Bit 23:16 Video Window I horizontal filter 2

Bit 15:8 Video Window I horizontal filter 1

Bit 7:0 Video Window I horizontal filter 0

FPRD8: Vertical Filter for Video Window I

Read/Write: Address: 58D8h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW I VERTICAL FILTER 3								**VIDEO WINDOW I VERTICAL FILTER 2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I VERTICAL FILTER 1								**VIDEO WINDOW I VERTICAL FILTER 0**							

Bit 31:24 Video Window I vertical filter 3

Bit 23:16 Video Window I vertical filter 2

Bit 15:8 Video Window I vertical filter 1

Bit 7:0 Video Window I vertical filter 0

FPRDC: Horizontal Filter for Video Window II

Read/Write: Address: 58DCh
Power-on Default: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**VIDEO WINDOW II HORIZONTAL FILTER 2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II HORIZONTAL FILTER 1								**VIDEO WINDOW II HORIZONTAL FILTER 0**							

Bit 31:24 Reserved

Bit 23:16 Video Window II horizontal filter 2

Bit 15:8 Video Window II horizontal filter 1

Bit 7:0 Video Window II horizontal filter 0

FPRE0: Data Source Last Start Address for Sub Picture

Read/Write Address: 58E0h
Power-on Default: 3FFFFF

This register specifies data source last starting address for sub picture. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**SUB PICTURE SOURCE**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE SOURCE															

Bit 31:22 Reserved

Bit 21:0 Sub Picture Source Last Starting Address, in 64-bit segment

FPRE4: Video Window I Source Odd Field Start Address

Read/Write Address: 58E4h
Power-on Default: Undefined

This register specifies video odd field start address for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VIDEO WINDOW I ODD FIELD**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I ODD FIELD															

Bit 31:22 Reserved

Bit 21:0 Video Window I odd field source start address for, in 64-bit segment.

FPRE8: Video Window I Odd Field Chroma Data Source Starting Address

Read/Write Address: 58E8h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VIDEO WINDOW I ODD FIELD CHROMA DATA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I ODD FIELD CHROMA DATA															

Bit 31:22 Reserved

Bit 21:0 Video Window I Odd Field Chroma Data Source Starting Address

FPREC: Data Source Odd Field Last Start Address for Video Window I

Read/Write Address: 58ECh
Power-on Default: 3FFFFF

This register specifies odd field data source last starting address for video window I. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										VIDEO WINDOW I ODD FIELD					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I ODD FIELD															

Bit 31:22 Reserved

Bit 21:0 Video Window I Odd Field Source Last Starting Address, in 64-bit segment

FPRF0: Odd Field Chroma Last Start Address for Video Window I

Read/Write Address: 58F0h
Power-on Default: 3FFFFF

This register specifies odd field chroma last starting address for video window I. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										VIDEO WINDOW I ODD FIELD CHROMA					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I ODD FIELD CHROMA															

Bit 31:22 Reserved

Bit 21:0 Video Window I Odd Field Chroma Last Starting Address, in 64-bit segment

Flat Panel Registers

FPR100: Panel Interface Selection Controls

Read/Write Address: 5900h
Power-on Default: 00000000h

This registers specifies the different types of flat panel controls.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PANEL ADJ		**PHPS**	**PSHS**	**PP ON/OFF 1**		**PP ON/OFF 0**		**RESERVED**		**CHPS**	**CSHS**	**CP ON/OFF 1**		**CP ON/OFF 0**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L2I	**L2DS**	**L2EN**	**LIEN**	**LIDB**	**L1I**	**MSEL**	**R**	**LIPEN**	**LIPI**	**FCS**	**R**	**HSP**	**VSP**	**CKP**	**TFT**

Bit 31:30 Panel HSync Adjustment
00: No adjustment
01: Move HSync 2 pixel clock ahead
10: Move HSync 4 pixel clock ahead
11: Move HSync 6 pixel clock ahead

Bit 29 For Panel Timing Panel only. (PHPS)
0 = LCD power sequence
1 = Bypass hardware power sequence for the Fpdata. If select software power sequence, this bit will not function

Bit 28 For Panel Timing Panel only (PSHS)
Select Hardware or Software LCD auto-power ON/OFF sequence during display switching in operation or power down modes. This bit can be used to select two different ways to turn ON/OFF LCD panel. For special programming sequence, please refer to the Power Down Management chapter of this data book.
0 = Select software LCD power sequencing
1 = Select hardware LCD power sequencing

Bit 27:26 For Panel Timing Panel only
Panel ON/OFF timing select. These two bits are used to control the time period from VBIASEN to LCD control signals. These two bits are only valid when LCD H/W auto-power ON/OFF sequence is selected.
00 = 1 vertical frame
01 = 2 vertical frame
10 = 4 vertical frame
11 = 8 vertical frame

Bit 25:24 For Panel Timing Panel only
Panel ON/OFF timing select. These two bits are used to control the time period from FPVDDENto LCD control signals. These two bits are only valid when LCD H/W auto-power ON/OFF sequence is selected.
00 = 1 vertical frame
01 = 2 vertical frame
10 = 4 vertical frame
11 = 8 vertical frame

Bit 23:22 Reserved (R)

Bit 21 For CRT Timing Panel only. (CHPS)
0 = LCD power sequence
1 = Bypass hardware power sequence for the Fpdata. If select software power sequence, this bit will not function

Bit 20 For CRT Timing Panel only (CSHS)
Select Hardware or Software LCD auto-power ON/OFF sequence during display switching in operation or power down modes. This bit can be used to select two different ways to turn ON/OFF LCD panel. For special programming sequence, please refer to the Power Down Management chapter of this data book.
0 = Select software LCD power sequencing
1 = Select hardware LCD power sequencing

Bit 19:18 For CRT Timing Panel only
Panel ON/OFF timing select. These two bits are used to control the time period from VBIASEN to LCD control signals. These two bits are only valid when LCD H/W auto-power ON/OFF sequence is selected.
00 = 1 vertical frame
01 = 2 vertical frame
10 = 4 vertical frame
11 = 8 vertical frame

Bit 17:16 For CRT Timing Panel only
Panel ON/OFF timing select. These two bits are used to control the time period from FPVDDEN to LCD control signal. These two bits are only valid when LCD H/W auto-power ON/OFF sequence is selected.
00 = 1 vertical frame
01 = 2 vertical frame
10 = 4 vertical frame
11 = 8 vertical frame

Bit 15 LVDS2 Panel Interface (L2I)
0 = 18 bit panel
Tx2: DE, FP, LP, B5, B4, B3, B2.
Tx1: B1, B0, G5, G4, G3, G2, G1.
Tx0: G0, R5, R4, R3, R2, R1, R0.
Txclk: Clock

1 = 24 bit panel
Refer to Bit 9 setting

Bit 14 LVDS2 Data Select (L2DS)
0 = CRT Data
1 = Panel Data

Bit 13 LVDS2 enable bit. (L2EN)
0 = Disable
1 = Enable

Bit 12 LVDS1 enable bit. (LIEN)
0 = Disable
1 = Enable

Bit 11 LVDS1 is using for double pixel panel. (LIDB)
0 = Single pixel
1 = Double pixel

Bit 10 LVDS1 Panel Interface (L1I)
0 = 18 bit panel
Tx2: DE, FP, LP, B5, B4, B3, B2
Tx1: B1, B0, G5, G4, G3, G2, G1
Tx0: G0, R5, R4, R3, R2, R1, R0
Txclk: Clock

1 = 24 bit panel
Refer to Bit 9 setting

Bit 9 LVDS Panel Manufacture select (MSEL)
0 = Normal
Tx3: NC, B7, B6, G7, G6, R7, R6
Tx2: DE, FP, LP, B5, B4, B3, B2
Tx1: B1, B0, G5, G4, G3, G2, G1
Tx0: G0, R5, R4, R3, R2, R1, R0
Txclk: Clock

1 = Hitachi
Tx3: NC, B1, B0, G1, G0, R1, R0
Tx2: DE, FP, LP, B7, B6, B5, B4
Tx1: B3, B2, G7, G6, G5, G4, G3
Tx0: G2, R7, R6, R5, R4, R3, R2
Txclk: Clock

Bit 8 Reserved (R)

Bit 7 Panel 1 without LVDS enable bit. (LIPEN)
1 = Enable
0 = Disable

Bit 6 Panel 1 interface type select without LVDS. (L1PI)
0 = 18-bit 6-bit per R, G, B
1 = 24-bit 8-bit per R, G, B

Bit 5 Panel 1 Data Select (FCS)
0 = CRT Data
1 = Panel Data

Bit 4 Reserved (R)

Bit 3 Panel 1 HSYNC phase select. (HSP)
0 = Normal
1 = Inverted HSYNC

Bit 2 Panel 1 VSYNC phase select. (VSP)
0 = Normal
1 = Inverted VSYNC

Bit 1 TFT FPSCLK1 Clock Phase Select. To adjust TFT flat panel data timing, user may wish to change the TFT FPSCLK1 phase by inverting the TFT FPSCLK1. (CKP)
0 = Normal
1 = Inverted clock

Bit 0 Color LCD type select. (TFT)
0 = Color TFT
1 = reserved

FPR104: WFIFO, LCDRAM, Line Buffer DDA Controls

Read/Write Address: 5904h
Power-on Default:Bit 31-24 are power-on configured by MD[15:8]. Others are power-on default to zero.

This registers specifies the different control signals for WFIFO, LCDRAM, LBUFFER and DDA modules.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POC	**R**	**RESERVED**						**RESERVED**						**PVD**	**VDP**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HDP	**R**	**VAC**	**VDDA**	**HAC**	**HDDA**	**LFR**	**LFE**	**LCD1**	**LCD2**	**EAL**	**WATERMARK**		**PI**	**WIFIFO**	**ES**

Bit 31 Power-on configured by MA [7] (POC)
0= 1.5V AGP pad
1 = 3.3V AGP pad

Bit 30 Reserved

Bit 29:24 Reserved for software use with power-on configured by MA [5:0]

Bit 23:18 Reserved

Bit 17 Panel vertical display enable probing (PVD)
1 = on
0 = off

Bit 16 Vertical Duplicate Pixel Enable (VDP)
1 = enable
0 = disable

Bit 15 Horizontal Duplicate Pixel Enable. (HDP)
1 = enable
0 = disable

Bit 14 Reserved (R)

Bit 13 Vertical Auto-centering enable (VAC)
1 = enable
0 = disable

Bit 12 Vertical DDA enable (VDDA)
1 = enable
0 = disable

Bit 11 Horizontal Auto-centering enable (HAC)
1 = enable
0 = disable

Bit 10 Horizontal DDA enable (HDDA)
1 = enable
0 = disable

Bit 9 Line FIFO RAM ON/OFF (LFR)
1 = off
0 = on

Bit 8 Line FIFO enable (LFE)
1 = enable
0 = disable

Bit 7 LCD RAM 8/6 bits (LCD1)
0 = 6 bits.
1 = 8 bits.

Bit 6 LCD RAM Gamma On (LCD2)
1 = enable
0 = disable

Bit 5 Enable Abort line factor (EAL)
1 = enable
0 = disable

Bit 4:3 WFIFO water mark
00 = 4 more
01 = 8 more
1x = 12 more

Bit 2 Zero out data except popup icon (PI)
0 = No zero out data
1 = zero out data except popup icon

Bit 1 WFIFO input data
0 = from CRT
1 = from Panel

Bit 0 Encode select (ES)
0 = Reserved
1 = RGB 5:6:5

FPR108: WFIFO Start Address

Read/Write Address: 5908h
Power-on Default: 00000000h

WFIFO Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**STARTING ADDRESS [21:0]**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STARTING ADDRESS [21:0]															

Bit 31:22 Reserved

Bit 21:0 Starting Address [21:0]

FPR10C: WFIFO Off-Set Address

Read/Write Address: 590Ch
Power-on Default: 00000000h

WFIFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**LINE OFFSET ADDRESS [9:0]**									

Bit 31:10 Reserved

Bit 9:0 Line offset address [9:0]

FPR110: LCD Horizontal Display Enable Horizontal Total

Read/Write Address: 5910h
Power-on Default: 00000000h

Panel control Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							**HORIZONTAL DISPLAY**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							**HORIZONTAL TOTAL**								

Bit 31:25 Reserved

Bit 24:16 Horizontal Display character count [8:0}

Bit 15:9 Reserved

Bit 8:0 Horizontal Total character count [8:0]

FPR114: HSync Pulse Width, VSync Pulse Width & Horizontal Sync Start

Read/Write Address: 5914h
Power-on Default: 00000000h

Panel control Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESRVED			**HSYNC PULSE**					**RESERVED**			**VSYNC PULSE**				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							**HORIZONTAL SYNC START CHARACTER COUNT**								

Bit 31:29 Reserved

Bit 28:24 HSYNC pulse width in # of character clocks

Bit 23:21 Reserved

Bit 20:16 VSYNC pulse width in # of HSYNCs

Bit 15:9 Reserved]

Bit 8:0 Horizontal sync start character count [8:0]

FPR118: Vertical Display Count and Vertical Total Count

Read/Write Address: 5918h
Power-on Default: 00000000h

Panel control Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VERTICAL DISPLAY COUNT**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VERTICAL TOTAL COUNT**										

Bit 31:27 Reserved

Bit 26:16 Vertical Display Count [10:0]

Bit 15:11 Reserved

Bit 10:0 Vertical Total Count [10:0]

FPR11C: Jitter Control

Read/Write Address: 591Ch
Power-on Default: 00000000h

Panel control Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							**JCE**	**R**	**FPSCLK2 DELAY**			**R**	**FPSCLK1 DELAY**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VERTICAL SYNC START**										

Bit 31:25 Reserved

Bit 24 Jitter Control Enable (JCE)

Bit 23 Reserved

Bit 22:20 Panel 1 FPSCLK2 Clock delay control
000 = normal
001 = FPSCLK2 delays by 1 unit of clock
010 = FPSCLK2 delays by 2 unit of clock
011 = FPSCLK2 delays by 3 unit of clock
100 = FPSCLK2 delays by 4 unit of clock
101 = FPSCLK2 delays by 5 unit of clock
110 = FPSCLK2 delays by 6 unit of clock
111 = FPSCLK2 delays by 7 unit of clock

Bit 19 Reserved

Bit 18:16 Panel 1 FPSCLK1 Clock delay control
000 = normal
001 = FPSCLK1 delays by 1 unit of clock
010 = FPSCLK1 delays by 2 unit of clock
011 = FPSCLK1 delays by 3 unit of clock
100 = FPSCLK1 delays by 4 unit of clock
101 = FPSCLK1 delays by 5 unit of clock
110 = FPSCLK1 delays by 6 unit of clock
111 = FPSCLK1 delays by 7 unit of clock

Bit 15:11 Reserved

Bit 10:0 Vertical Sync Start [10:0]

FPR120: Panel Power Down Control Register

Read/Write Address: 5920
Power-on Default: 00030000h

Panel control Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**PHVS**	**CHVS**	**RESERVED**						**PDF**	**CDF**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRT TIMING FPEN TO FPVBIASEN								**PANEL TIMING FPEN TO FPVBIASEN**							

Bit 31:26 Reserved

Bit 25 For Panel Timing Panel only (PHVS)
Sync. Counter select for power down sequence
0 = Vsync
1= Hsync

Bit 24 For CRT Timing Panel only (CHVS)
Sync. Counter select for power down sequence
0 = Vsync
1= Hsync

Bit 23:18 Reserved

Bit 17 Panel Timing Screen Off. (PDF)
Power On Default value for this bit is 1.
0 = Screen On.
1 = Screen Off.

Bit 16 CRT Timing Screen Off. (CDF)
Power On Default value for this bit is 1.
0 = Screen On.
1 = Screen Off.

Bit 15:8 CRT Timing Panel
Panel ON/OFF timing select. These 8 bits are used to control the time period from FPEN to FPVBIASEN. These 8 bits are only valid when LCD H/W auto-power ON/OFF sequence is selected.

Bit 7:0 Panel Timing
Panel ON/OFF timing select. These 8 bits are used to control the time period from FPEN to FPVBIASEN. These 8 bits are only valid when LCD H/W auto-power ON/OFF sequence is selected.

FPR124: Horizontal DDA Table Line 0

Read/Write Address: 5924
Power-on Default: 00000000h

Horizontal DDA Table Line 0 (This register is used when the horizontal display value does not compare to FPR128 or FPR130)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FHD	**RESERVED**								**HORIZONTAL AUTO CENTERING VALUE**						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HORIZONTAL DDA VALUE															

Bit 31 Force to use this register as horizontal center value and DDA value without compare display value
0 = use compare
1 = force to use this register

Bit 30:23 Reserved

Bit 22:16 Horizontal auto-centering value [6:0]

Bit 15:0 Horizontal DDA Value [15:0]

FPR128: Horizontal DDA Table Line 1

Read/Write Address: 5928
Power-on Default: 00000000h

Horizontal DDA Table Line 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	**HORIZONTAL DISPLAY VALUE**							**R**	**HORIZONTAL AUTO CENTERING VALUE**						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HORIZONTAL DDA VALUE															

Bit 31 Reserved

Bit 30:24 Hdisp value [6:0]

Bit 23 Reserved

Bit 22:16 Horizontal auto-centering value [6:0]

Bit 15:0 Horizontal DDA Value [15:0]

FPR12C: Horizontal DDA Table Line 2

Read/Write Address: 593C
Power-on Default: 00000000h

Horizontal DDA Table Line 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	**HORIZONTAL DISPLAY VALUE**							**R**	**HORIZONTAL AUTO CENTERING VALUE**						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HORIZONTAL DDA VALUE															

Bit 31 Reserved

Bit 30:24 Hdisp value [6:0]

Bit 23 Reserved

Bit 22:16 Horizontal auto-centering value [6:0]

Bit 15:0 Horizontal DDA Value [15:0]

FPR130: Horizontal DDA Table Line 3

Read/Write Address: 5930
Power-on Default: 00000000h

Horizontal DDA Table Line 3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	**HORIZONTAL DISPLAY VALUE**							**R**	**HORIZONTAL AUTO CENTERING VALUE**						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HORIZONTAL DDA VALUE															

Bit 31 Reserved

Bit 30:24 Hdisp value [6:0]

Bit 23 Reserved

Bit 22:16 Horizontal auto-centering value [6:0]

Bit 15:0 Horizontal DDA Value [15:0]

FPR134: Vertical DDA Table Line 0

Read/Write Address: 5934
Power-on Default: 00000000h

Vertical DDA Table Line 0 (This register is used when the vertical display value did not compare to FPR138 or FPR154)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FVD	**RESERVED**						**VERTICAL AUTO CENTERING VALUE**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL DDA VALUE															

Bit 31 Force to use this register as the vertical center value and DDA value without compare display value
0 = use compare.
1 = force to use this register.

Bit 30:25 Reserved

Bit 24:16 Vertical auto-centering value [8:0] (# of line)

Bit 15:0 Vertical DDA Value [15:0]

FPR138: Vertical DDA Table Line 1

Read/Write Address: 5938
Power-on Default: 00000000h

Vertical DDA Table Line 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTICAL DISPLAY VALUE							**VERTICAL AUTO CENTERING VALUE**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL DDA VALUE															

Bit 31:25 Vdisp value [6:0]

Bit 24:16 Vertical auto-centering value [8:0] (# of lines)

Bit 15:0 Vertical DDA Value [15:0]

FPR13C: Vertical DDA Table Line 2

Read/Write Address: 593C
Power-on Default: 00000000h

Vertical DDA Table Line 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTICAL DISPLAY VALUE							**VERTICAL AUTO CENTERING VALUE**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL DDA VALUE															

Bit 31:25 Vdisp value [6:0]

Bit 24:16 Vertical auto-centering value [8:0] (# of lines)

Bit 15:0 Vertical DDA Value [15:0]

FPR140: Vertical DDA Table Line 3

Read/Write Address: 5940
Power-on Default: 00000000h

Vertical DDA Table Line 3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTICAL DISPLAY VALUE							**VERTICAL AUTO CENTERING VALUE**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL DDA VALUE															

Bit 31:25 Vdisp value [6:0]

Bit 24:16 Vertical auto-centering value [8:0] (# of lines)

Bit 15:0 Vertical DDA Value [15:0]

FPR144: Vertical DDA Table Line 4

Read/Write Address: 5944
Power-on Default: 00000000h

Vertical DDA Table Line 4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTICAL DISPLAY VALUE							**VERTICAL AUTO CENTERING VALUE**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL DDA VALUE															

Bit 31:25 Vdisp value [6:0]

Bit 24:16 Vertical auto-centering value [8:0] (# of lines)

Bit 15:0 Vertical DDA Value [15:0]

FPR148: Vertical DDA Table Line 5

Read/Write Address: 5948
Power-on Default: 00000000h

Vertical DDA Table Line 5

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTICAL DISPLAY VALUE							**VERTICAL AUTO CENTERING VALUE**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL DDA VALUE															

Bit 31:25 Vdisp value [6:0]

Bit 24:16 Vertical auto-centering value [8:0] (# of lines)

Bit 15:0 Vertical DDA Value [15:0]

FPR14C: Vertical DDA TAble Line 6

Read/Write Address: 594C
Power-on Default: 00000000h

Vertical DDA Table Line 6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTICAL DISPLAY VALUE							**VERTICAL AUTO CENTERING VALUE**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL DDA VALUE															

Bit 31:24 Vdisp value [6:0]

Bit 24:16 Vertical auto-centering value [8:0] (# of lines)

Bit 15:0 Vertical DDA Value [15:0]

FPR150: Vertical DDA Table Line 7

Read/Write Address: 5950
Power-on Default: 00000000h

Vertical DDA Table Line 7

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTICAL DISPLAY VALUE							**VERTICAL AUTO CENTERING VALUE**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL DDA VALUE															

Bit 31:25 Vdisp value [6:0]

Bit 24:16 Vertical auto-centering value [8:0] (# of lines)

Bit 15:0 Vertical DDA Value [15:0]

FPR154: Vertical DDA Table Line 8

Read/Write Address: 5954
Power-on Default: 00000000h

Vertical DDA Table Line 8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VERTICAL DISPLAY VALUE							**VERTICAL AUTO CENTERING VALUE**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTICAL DDA VALUE															

Bit 31:25 Vdisp value [6:0]

Bit 24:16 Vertical auto-centering value [8:0] (# of lines)

Bit 15:0 Vertical DDA Value [15:0]

FPR158: Hardware Cursor X and Y Position

Read/Write Address: 5958
Power-on Default: 00000000h

Hardware Cursor Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				**HWC X POSITION HIGH AND LOW**											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**HWC Y POSITION HIGH AND LOW**											

Bit 31:28 Reserved

Bit 27:16 HWC X position high [3:0] and HWC position low [7:0]

Bit 15:12 Reserved

Bit 11:0 HWC Y position high [3:0] and HWC position low [7:0]

FPR15C: Pop-up Icon Pattern, Background, and Foreground Color

Read/Write Address: 595C

Power-on Default: 00000000h

Hardware Cursor FG/BG Color Register. HWC and Pop-up icon pattern.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HCE	**R**	**POP-UP ICON/HWC PATTERN HIGH**						**POP-UP ICON/HWC PATTERN LOW**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWC BACKGROUND COLOR								**HWC FOREGROUND COLOR**							

Bit 31 HWC enable (HCE)
1 = Enable
0 = Disable

Bit 30 Reserved

Bit 29:24 Pop-up icon/HWC Pattern High [5:0]

Bit 23:16 Pop-up icon/HWC Pattern Low [7:0]

Bit 15:8 HWC Background Color [7:0]

Bit 7:0 HWC Foreground Color [7:0]

FPR160: Pop-up Icon Enable X & Y Position

Read/Write Address: 5960
Power-on Default: 00000000h

Pop-up Icon Control Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**X POSITION HIGH**			**X POSITION LOW**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**PE**	**PZ**	**R**	**Y POSITION HIGH**			**Y POSITION LOW**							

Bit 31:27 Reserved

Bit 26:24 X Position High [2:0]

Bit 23:16 X Position Low [7:0]

Bit 15:14 Reserved

Bit 13 Pop-up icon enable (PE)
1 = Enable
0 = Disable

Bit 12 Pop-icon Zoom (PZ)
0 = normal
1 = Zoom up size by 2

Bit 11 Reserved (R)

Bit 10:8 Y Position High [2:0]

Bit 7:0 Y Position Low [7:0]

FPR164: Pop-up Icon Color Table

Read/Write Address: 5964
Power-on Default: 00000000h

Pop-up Icon Color Table

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**POP-UP ICON COLOR III**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POP-UP ICON COLOR II								**POP-UP ICON COLOR I**							

Bit 31:24 Reserved

Bit 23:16 Pop-icon Color III

Bit 15:8 Pop-icon Color II

Bit 7:0 Pop-icon Color I

Chapter 22: CRT Processor Registers

Table 25: Memory Mapped Video Registers Quick Reference

Note: Some VPR registers can be accessed using memory mapped register space, or can be accessed using I/O mapped register space. Please see register descriptions for detailed information.

Video Processor Control Registers

SM731 integrates a concurrent video processor. It can support 2 independent video windows using hardware scaling for any size of video windows at any location of the screen display. The Video Processor Control Registers specify the control registers for Video Processor. The Video Processor Control Registers can only be accessed through memory-mapped.

VPR00: Miscellaneous Graphics and Video Control

Read/Write Address: 0800h
Power-on Default: 00000000h

This register specifies the controls for graphics and video window I/II. (where x = don't care)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DOFF	**R**	**ESP**	**FIELD**	**R**	**EBOB**	**ESD**	**CVWI**	**RESERVED**			**GDT**	**GDE**	**GDF**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TVWS	**VWIIC**	**R**	**VWIIT**	**VWIIE**	**VWIIF**			**VWIC**	**VWIL**		**VWIT**	**VWIE**	**VWIF**		

Bit 31 Display Off (DOFF)
0 = Display On
1 = Display Off (except POP UP ICON)

Bit 30 Reserved (R) (must be 0)

Bit 29 Enable Single Pixel (ESP)
0 = double pixel through video pipe
1 = Single pixel through video pipe

Bit 28 Current display field (FIELD) (read only)
0 = Current display even field
1 = Current display odd field

Bit 27 Reserved (R)

Bit 26 Enable BOB display (EBOB)
0 = Disable
1 = Enable

Bit 25 Enable separate data (video) to DAC/TV and graphic data to write FIFO. This bit needs to also be set to allow flicker reduction for TV display in index-color mode. (ESD)
0 = Disable
1 = Enable

Bit 24 Select video window I source start address same as video capture buffer start address. This bit is used to automatically display captured data on video window I without programming video window I source start address register (SVWI).
0 = Normal. Video window I source start address is from VPR1C register.
1 = Video window I source start address is equal to capture port buffer I source start address (VPR48) or capture port buffer II source start address (VPR4C). If single buffer is selected for video capture, video

window I source start address is equal to capture port buffer I source address. If double buffer is selected for video capture and capture port buffer I is busy, video window I source start address is equal to capture port buffer II source address.

Bit 23:21 Reserved

Bit 20 Graphic Data in Tile format (GDT)
0 = Normal format
1 = Tile format

Bit 19 Graphic Enable (GDE)
0 = Disable
1 = Enable

Bit 18:16 Graphics Data Format (GDF)
000 = 8-bit index
001 = 15 -bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = Reserved
11x = Reserved

Bit 15 Top Video Window Select (TVWS)
0 = Video window I is on top
1 = Video window II is on top

Bit 14 Color Key Enable for Video Window II (CKEII)
0 = Disable
1 = Enable

Bit 13 Reserved (R)

Bit 12 Video Window II Data in Tile format (VWIIT)
0 = Normal format
1 = Tile format

Bit 11 Video Window II Enable (VWIIE)
0 = Disable
1 = Enable

Bit 10:8 Video Window II Format (VWFII)
000 = 8-bit index
001 = 15-bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = 8-bit 3-3-2 RGB
110 = YUV 4:2:2
111 = YUV 4:2:0 (UV interleave)

Bit 7 Color Key Enable for Video Window I (CKEI)
0 = Disable
1 = Enable

Bit 6:5 Video Window I Line of Filtering (VWIL)
00 = 1 line
01 = 2 line
1x = 4 line (data format cannot be YUV 4:2:0 and bit 29 must set to 1)

Bit 4 Video Window I Data in Tile format (VWIT)
0 = Normal format
1 = Tile format

Bit 3 Video Window I Enable (VWIE)
0 = Disable
1 = Enable

Bit 2:0 Video Window I Format (VWIF)
000 = 8-bit index
001 = 15-bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = 8-bit 3-3-2 RGB
110 = YUV 4:2:2
111 = YUV 4:2:0 (UV interleave)

VPR04: Color Keys

Read/Write Address: 0804h
Power-on Default: Undefined

This register specifies color keys for the two video windows

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**VIDEO WINDOW II COLOR KEY INDEX**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**VIDEO WINDOW I COLOR KEY INDEX**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II COLOR KEY [15:8]								**VIDEO WINDOW II COLOR KEY [7:0]**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I COLOR KEY [15:8]								**VIDEO WINDOW I COLOR KEY [7:0]**							

	8-bit color mode	16-bit color mode[1]
Bit 31:24	Reserved	Video Window II Color Key [15:8]
Bit 23:16	Video Window II Color Key Index	Video Window II Color Key [7:0]
Bit 15:8	Reserved	Video Window I Color Key [15:8]
Bit 7:0	Video Window I Color Key Index	Video Window I Color Key [7:0]

Note[1]: for 24-bit or 32-bit color mode, software will need to repack the color key data into RGB - 5:6:5 (16-bit) format.

VPR08: Color Key Masks

Read/Write Address: 0808h
Power-on Default: Undefined

This register specifies color key masks for the two video window.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II COLOR KEY MASK															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I COLOR KEY MASK															

Bit 31:16 Video Window II Color Key Mask
0 = Disable color mask
1 = Enable color mask

Bit 15:0 Video Window I Color Key Mask
0 = Disable color mask
1 = Enable color mask

VPR0C: Data Source Start Address for Extended Graphics Modes

Read/Write Address: 080Ch
Power-on Default: Undefined

This register specifies data source start address for extended graphics modes

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GDSB	**RESERVED**									**GDSSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GDSSA															

Bit 31 Graphic Data Status Bit (GDSB)

Bit 30:22 Reserved

Bit 21:0 Graphics Data Source Starting Address, in 64-bit segment (GDSSA)

VPR10: Data Source Width and Offset for Extended Graphics Modes

Read/Write Address: 0810h
Power-on Default: Undefined

This register specifies data source data line width and offset address for extended graphics modes.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**GRAPHICS DATA SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**GRAPHICS DATA START ADDRESS OFFSET**									

Bit 31:26 Reserved

Bit 25:16 Graphics Data Source data line width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Graphics Data Start Address Offset, in 64-bit segment

VPR14: Video Window I Left and Top Boundaries

Read/Write Address: 0814h
Power-on Default: Undefined

This register specifies left and top boundary for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW I TOP BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW I LEFT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video window I, top boundary

Bit 15:11 Reserved

Bit 10:0 Video window I, left boundary

VPR18: Video Window I Right and Bottom Boundaries

Read/Write Address: VP_Base+18h
Power-on Default: Undefined

This register specifies right and bottom boundary for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW I BOTTOM BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW I RIGHT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video window I, bottom boundary

Bit 15:11 Reserved

Bit 10:0 Video window I, right boundary

VPR1C: Video Window I Source Start Address

Read/Write Address: VP_Base+1Ch
Power-on Default: Undefined

This register specifies video start address for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWIS	**RESERVED**									**VWISS**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWISS															

Bit 31 Video Window I Status Bit (VWIS)

Bit 30:22 Reserved

Bit 21:0 Video Window I source start address for, in 64-bit segment. (VWISS)

VPR20: Video Window I Source Width and Offset

Read/Write Address: VP_Base+20h
Power-on Default: Undefined

This register specifies video source data line width and offset address for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**VIDEO WINDOW I SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**VIDEO WINDOW I SOURCE ADDRESS**									

Bit 31:26 Reserved

Bit 25:16 Video Window I Source Data Line Width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Video Window I Source Address Offset, in 64-bit segment

VPR24: Video Window I Stretch Factor:

Read/Write Address: VP_Base+24h
Power-on Default: 00000000h

This register specifies video horizontal and Vertical stretch factor for video window I. For optimal display quality, we recommend destination to source ratio to be maximum of 4:1. The two high bytes of this register can be used to enable the "Bob" function.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II INITAL ODD FIELD								**VIDEO WINDOW II INITIAL EVEN FIELD**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I HORIZONTAL STRETCH								**VIDEO WINDOW I VERTICAL STRETCH**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor

Bit 15:8 Video Window 1 Horizontal Stretch Factor (W1HSF)

note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W1HSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Video Window 1 Vertical Stretch Factor (W1VSF)
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W1VSF = \frac{Source}{Destination} * 256$$

VPR28: Video Window II Left and Top Boundaries

Read/Write Address: VP_Base+28h
Power-on Default: Undefined

This register specifies left and top boundary for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW II TOP BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW II LEFT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video Window II, Top Boundary

Bit 15:11 Reserved

Bit 10:0 Video Window II, Left Boundary

VPR2C: Video Window II Right and Bottom Boundaries

Read/Write Address: VP_Base+2Ch
Power-on Default: Undefined

This register specifies right and bottom boundary for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW II BOTTOM BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW II RIGHT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video Window II, Bottom Boundary

Bit 15:11 Reserved

Bit 10:0 Video Window II, Right Boundary

VPR30: Video Window II Source Start Address

Read/Write Address: VP_Base+30h
Power-on Default: Undefined

This register specifies video start address for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWIIS	**RESERVED**									**VWIIDS**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIIDS															

Bit 31 Video Window II Status Bits (VWIIS)

Bit 30:22 Reserved

Bit 21:0 Video Window II Data Source Starting Address (VWIIDS)

VPR34: Video Window II Source Width and Offset

Read/Write Address: VP_Base+34h
Power-on Default: Undefined

This register specifies video source data line width and offset address for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**VIDEO WINDOW II SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**VIDEO WINDOW II SOURCE ADDRESS**									

Bit 31:26 Reserved

Bit 25:16 Video Window II Source Data Line Width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Video Window II Source Address Offset, in 64-bit segment

VPR38: Video Window II Stretch Factor

Read/Write Address: VP_Base+38h/3?5h, Index f8, f9, fa, fb
Power-on Default: 00000000h

This register specifies video horizontal and Vertical stretch factor for video window II. For optimal display quality, we recommend destination to source ratio to be maximum of 4:1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II INITAL ODD FIELD								**VIDEO WINDOW II INITIAL EVEN FIELD**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II HORIZONTAL STRETCH								**VIDEO WINDOW II VERTICAL STRETCH**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor

Bit 15:8 Video Window II Horizontal Stretch Factor (W2HSF)

note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W2HSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Video Window II Vertical Stretch Factor (W2VSF)
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W2VSF = \frac{Source}{Destination} * 256$$

VPR3C: Graphics and Video Control II

Read/Write: Address: VP_Base+3Ch
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHF1								**SHF0**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**CKCS**	**SBE**	**SF**		**SE**	**EVWII UVS**	**RESERVED**		**EVWII HB**	**EVWI UVS**	**R**	**EVWI VB**	**EVWI HB**

Bit 31:24 Sub Picture horizontal filter 1 (SHF1)

Bit 23:16 Sub Picture horizontal filter 0 (SHF0)

Bit 15:13 Reserved

Bit 12 Color Key Control Sub-Picture (CKCS)
0 = Disable
1 = Enable*
* Only 8-bit and 16-bit sub-picture data format supported

Bit 11 Sub-Picture bi-linear enable (SBE)
0 = Disable
1 = Enable

Bit 10:9 Sub-Picture data format (SF)
00 = 8-bit alpha blending format (alpha_[3:0], color_[3:0])
01 = 16-bit alpha blending format (alpha_[7:0], color_[7:0])
1x = 32-bit alpha blending format (alpha_[7:0], color_[23:0])

Bit 8 Sub-Picture Enable (SE)
0 = Disable
1 = Enable

Bit 7 Video Window II UV Swap enable (EVWIIUVS)
0 = Disable
1 = Enable

Bit 6:5 Reserved

Bit 4 Video window II horizontal bi-linear enable (EVWIIHB)
0 = Disable
1 = Enable

Bit 3 Video Window I UV Swap enable (EVWIUVS)
0 = Disable
1 = Enable

Bit 2 Reserved

Bit 1 Video window I vertical bi-linear enable (EVWIVB)
0 = Disable
1 = Enable

Bit 0 Video window I horizontal bi-linear enable (EVWIHB)
0 = Disable
1 = Enable

VPR40: Sub Picture Scale Factor

Read/Write Address: VP_Base+40h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SUB PICTURE INITIAL ODD FIELD VERTICAL								**SUB PICTURE INITAL EVEN FIELD VERTICAL**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE HORIZONTAL SCALE FACTOR								**SUB PICTURE VERTICAL SCALE FACTOR**							

Bit 31:24 Sub Picture Initial Odd Field Vertical Scale Factor

Bit 23:16 Sub Picture Initial Even Field Vertical Scale Factor

Bit 15:8 Sub Picture Horizontal Scale Factor

$$GHSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Sub Picture Vertical Scale Factor

$$GVSF = \frac{Source}{Destination} * 256$$

VPR44: Sub Picture Scale Factor LSB

Read/Write Address: VP_Base+44h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SUB PICTURE INITIAL ODD FIELD VERTICAL LSB								**SUB PICTURE INITAL EVEN FIELD VERTICAL LSB**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE HORIZONTAL SCALE FACTOR LSB								**SUB PICTURE VERTICAL SCALE FACTOR LSB**							

Bit 31:24 Sub Picture Initial Odd Field Vertical Scale Factor LSB

Bit 23:16 Sub Picture Initial Even Field Vertical Scale Factor LSB

Bit 15:8 Sub Picture Horizontal Scale Factor LSB

$$GHSF = \frac{Source}{Destination} * 65536$$

Bit 7:0 Sub Picture Vertical Scale Factor LSB

$$GVSF = \frac{Source}{Destination} * 65535$$

VPR48: Video Window I Chroma Data Source Starting Address

Read/Write Address: VP_Base+48h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VWICSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWICSA															

Bit 31:22 Reserved

Bit 21:0 Video Window I Chroma Data Source Starting Address (VWICSA)

VPR4C: Video Window II Chroma Data Source Starting Address

Read/Write Address: VP_Base+4Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VWIICSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIICSA															

Bit 31:22 Reserved

Bit 21:0 Video Window II Chroma Data Source Starting Address (VWIICSA)

VPR50: Sub-Picture Data Source Starting Address

Read/Write Address: VP_Base=50h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**SUB-PICTURE DATA SOURCE**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB-PICTURE DATA SOURCE															

Bit 31:22 Reserved

Bit 21:0 Sub-picture Data Source Starting Address

VPR54: FIFO Priority Control

Read/Write Address: VP_Base+54h
Power-on Default: 07216543h

This register specifies FIFO priority controls for graphics, Flat Panel Read Frame Buffer FIFO1, Video Window I, Video Window II, Flat Panel Write Frame Buffer, Capture Window and Flat Panel Read Frame Buffer FIFO2. Graphics FIFO has the highest priority and Flat Panel Read FIFO2 has the lowest priority as default.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**FPR FIFO2**			**R**	**CWFIFO**			**R**	**FPW FIFO**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**VWII FIFO**			**R**	**VWI FIFO**			**R**	**FPR FIFO1**			**R**	**GFIFO**		

Bit 31:27 Reserved (must be 0)

Bit 26:24 Flat Panel Read FIFO2 priority select (FPR FIFO2
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)

100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last) (default)

Bit 23 Reserved (R)

Bit 22:20 Capture Window FIFO priority select (CWFIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd) (default)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

Bit 19 Reserved (R)

Bit 18:16 Flat Panel Write FIFO priority select (FPW FIFO)
000 = request is off
001 = highest priority (1st) (default)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

Bit 15 Reserved (R)

Bit14:12 Video Window II FIFO priority select (VWII FIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th) (default)
111 = lowest priority (last)

Bit 11 Reserved (R)

Bit 10:8 Video Window I FIFO priority select (VWI FIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th) (default)

110 = next priority (6th)
111 = lowest priority (last)

Bit 7 Reserved (R)

Bit 6:4 Flat Panel Read FIFO1 priority select (FPR FIFO1)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th) (default)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

Bit 3 Reserved

Bit 2:0 Graphics FIFO priority select (GFIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd) (default)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

VPR58: FIFO Empty Request level Control

Read/Write Address: VP_Base+58h
Power-on Default: 00004444h

This register specifies FIFO empty request level for graphics FIFO, Video Window I, and Video Window II. At the specified empty FIFO level, FIFO request will be generated. Default FIFO empty levels are all 6 or more empty. For LCD Read FIFO1/FIFO2 and LCD Write FIFO request level controls, they are located in FPR4A register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**S FIFO**			**R**	**VWII FIFO**			**R**	**VWI FIFO**			**R**	**GFIFO**		

Bit 31:15 Reserved

Bit 14:12 Sub Picture FIFO Empty request level Select (S FIFO)
00x = 2 or more empty
010 = 2 or more empty
011 = 3 or more empty
100 = 4 or more empty (default)

101 = 5 or more empty
11x = 6 or more empty

Bit 7 Reserved (R)

Bit 10:8 Video Window II FIFO Empty request level Select (VWII FIFO)
000 = 2 or more empty
001 = 4 or more empty
010 = 5 or more empty
011 = 6 or more empty
100 = 7 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

Bit 7 Reserved (R)

Bit 6:4 Video Window I FIFO Empty request level Select (VWI FIFO)
000 = 2 or more empty
001 = 4 or more empty
010 = 5 or more empty
011 = 6 or more empty
100 = 7 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

Bit 3 Reserved (R)

Bit 2:0 Graphics FIFO Empty request level Select (GFIFO)
000 = 2 or more empty
001 = 4 or more empty
010 = 5 or more empty
011 = 6 or more empty
100 = 7 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

VPR5C: YUV to RGB Conversion Constant

Read/Write Address: VP_Base+5Ch
Power-on Default: EDEDEDh
This register specifies the YUV to RGB conversion constant.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LUMA Y ADJUSTMENT								**RED CONVERSION CONSTANT**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN CONVERSION CONSTANT								**BLUE CONVERSION CONSTANT**							

Bit 31:24 Luma Y Adjustment

Bit 23:16 Red Conversion Constant

Bit 15:8 Green Conversion Constant

Bit 7:0 Blue Conversion Constant

VPR60: Current Scan Line Position

Read Only Address: VP_Base+60h
Power-on Default: Undefined

This register specifies the current scan line position.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**CURRENT SCAN LINE**										

Bit 31:11 Reserved

Bit 10:0 Current Scan Line. This register returns the number for current scan line.

VPR64: Signature Analyzer Control and Status

Read/Write Address: VP_Base+64h
Power-on Default: Undefined

This register specifies controls and status for signature analyzer as well as the analyzer signature.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ANALYZER SIGNATURE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												**SAE**	**SAR**	**SASS**	

Bit 31:16 Analyzer Signature. These bits are Ready Only.

Bit 15:4 Reserved

Bit 3 Signature Analyzer Enable/Stop. Software needs to set this bit = 1 as a "ENABLE" control bit in order to enable signature analyzer. Once the analysis is completed, the hardware will reset this bit = 0 as a "STOP" status bit. (SAE)
0 = Stop (analysis is completed)
1 = Enable (analysis is in progress)

Bit 2 Signature Analyzer Reset/Normal. Software needs to set this bit = 1 as a (SAR)
"RESET" control bit to reset signature shift register to "0" before turning on signature analyzer. In the next vertical sync pulse after bit 3 and bit 2 have been set to "11", bit 2 will be automatically reset to "0" as a "NORMAL" status bit.
0 = Normal (disable reset to signature analyzer)
1 = Reset (enable reset to signature analyzer)

Bit 1:0 Signature Analyzer Source Select. These bits selects the input source for the signature analyzer. (SASS)
00 = Source is Red output from Multimedia RAMDAC
01 = Source is Green output from Multimedia RAMDAC
1x = Source is Blue output from Multimedia RAMDAC

VPR68: Video Window I Scale Factor LSB

Read/Write Address: VP_Base+68h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWI INITIAL ODD FIELD VERTICAL LSB								**VWI INITAL EVEN FIELD VERTICAL LSB**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWI HORIZONTAL SCALE FACTOR LSB								**VWI VERTICAL SCALE FACTOR LSB**							

Bit 31:24 Video Window I Initial Odd Field Vertical Scale Factor LSB

Bit 23:16 Video Window I Initial Even Field Vertical Scale Factor LSB

Bit 15:8 Video Window I Horizontal Scale Factor LSB

$$GHSF = \frac{Source}{Destination} * 65536$$

Bit 7:0 Video Window I Vertical Scale Factor LSB

$$GVSF = \frac{Source}{Destination} * 65535$$

VPR6C: Video Window II Scale Factor LSB

Read/Write Address: VP_Base+6ch
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWII INITIAL ODD FIELD VERTICAL LSB								**VWII INITAL EVEN FIELD VERTICAL LSB**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWII HORIZONTAL SCALE FACTOR LSB								**VWII VERTICAL SCALE FACTOR LSB**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor LSB

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor LSB

Bit 15:8 Video Window II Horizontal Scale Factor LSB

$$GHSF = \frac{Source}{Destination} * 65536$$

Bit 7:0 Video Window II Vertical Scale Factor LSB

$$GVSF = \frac{Source}{Destination} * 65535$$

VPR70: Sub Picture Color Look Up Register 0

Read/Write Address: VP_Base+70h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 0**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 0															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 0

VPR74: Sub Picture Color Look Up Register 1

Read/Write Address: VP_Base+74h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 1**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 1															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 1

VPR78: Sub Picture Color Look Up Register 2

Read/Write Address: VP_Base+78h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 2															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 2

VPR7C: Sub Picture Color Look Up Register 3

Read/Write Address: VP_Base+7Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 3**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 3															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 3

VPR80: Sub Picture Color Look Up Register 4

Read/Write Address: VP_Base+80h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 4**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 4															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 4

VPR84: Sub Picture Color Look Up Register 5

Read/Write Address: VP_Base+84h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 5**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 5															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 5

VPR88: Sub Picture Color Look Up Register 6

Read/Write Address: VP_Base+88h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 6**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 6															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 6

VPR8C: Sub Picture Color Look Up Register 7

Read/Write Address: VP_Base+8Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 7**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 7															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 7

VPR90: Sub Picture Color Look Up Register 8

Read/Write Address: VP_Base+90h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 8**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 8															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 8

VPR94: Sub Picture Color Look Up Register 9

Read/Write Address: VP_Base+94h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP 9**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP 9															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register 9

VPR98: Sub Picture Color Look Up Register A

Read/Write Address: VP_Base+98h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP A**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP A															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register A

VPR9C: Sub Picture Color Look Up Register B

Read/Write Address: VP_Base+9Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP B**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP B															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register B

VPRA0: Sub Picture Color Look Up Register C

Read/Write Address: VP_Base+A0h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP C**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP C															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register C

VPRA4: Sub Picture Color Look Up Register D

Read/Write Address: VP_Base+A4h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SUB PICTURE COLOR LOOK UP D**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP D															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register D

VPRA8: Sub Picture Color Look Up Register E

Read/Write Address: VP_Base+A8h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								SUB PICTURE COLOR LOOK UP E							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP E															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register E

VPRAC: Sub Picture Color Look Up Register F

Read/Write Address: VP_Base+ACh
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								SUB PICTURE COLOR LOOK UP F							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUB PICTURE COLOR LOOK UP F															

Bit 31:24 Reserved

Bit 23:0 Sub Picture Color Look Up Register F

VPRB0: Sub Picture Top/Left Boundary

Read/Write Address: VP_Base+B0h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					SUB PICTURE TOP BOUNDARY										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SUB PICTURE LEFT BOUNDARY										

Bit 31:27 Reserved

Bit 26:16 Sub Picture Top Boundary

Bit 15:11 Reserved

Bit 10:0 Sub Picture Left Boundary

VPRB4: Sub Picture Bottom/Right Boundary

Read/Write Address: VP_Base+B4h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**SUB PICTURE BOTTOM BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**SUB PICTURE RIGHT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Sub Picture Bottom Boundary

Bit 15:11 Reserved

Bit 10:0 Sub Picture Right Boundary

VPRB8: Sub Picture Source Data Address Offset and Line Width

Read/Write Address: VP_Base+B8h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**SUB PICTURE SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**SUB PICTURE SOURCE DATA ADDRESS OFFSET**									

Bit 31:26 Reserved

Bit 25:16 Sub Picture Source Data Line Width

Bit 15:10 Reserved

Bit 9:0 Sub Picture Source Data Address Offset

VPRC0: Data Source Last Start Address for Extended Graphics Modes

Read/Write Address: VP_Base+C0h
Power-on Default: 3FFFFF

This register specifies data source last starting address for extended graphics modes. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**GDSLSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GDSLSA															

Bit 31:22 Reserved

Bit 21:0 Graphics Data Source Last Starting Address, in 64-bit segment (GDSLSA)

VPRC4: Data Source Last Start Address for Video Window I

Read/Write Address: VP_Base+C4h
Power-on Default: 3FFFFF

This register specifies data source last starting address for video window I. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VWISLSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWISLSA															

Bit 31:22 Reserved

Bit 21:0 Video Window I Source Last Starting Address, in 64-bit segment (VWISLSA)

VPRC8: Data Source Last Start Address for Video Window II

Read/Write Address: VP_Base+C8h
Power-on Default: 3FFFFF

This register specifies data source last starting address for video window II. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VWIISLSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIISLSA															

Bit 31:22 Reserved

Bit 21:0 Video Window II Source Last Starting Address, in 64-bit segment (VWIISLSA)

VPRCC: Chroma Last Start Address for Video Window I

Read/Write Address: VP_Base+CCh
Power-on Default: 3FFFFF

This register specifies chroma last starting address for video window I. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VWICLSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWICLSA															

Bit 31:22 Reserved

Bit 21:0 Video Window I Chroma Last Starting Address, in 64-bit segment (VWICLSA)

VPRD0: Chroma Last Start Address for Video Window II

Read/Write Address: VP_Base+D0h
Power-on Default: 3FFFFF

This register specifies data source last starting address for video window II. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VWIICLSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIICLSA															

Bit 31:22 Reserved

Bit 21:0 Video Window II Chroma Last Starting Address, in 64-bit segment (VWIICLSA)

VPRD4: Horizontal Filter for Video Window I

Read/Write: Address: VP_Base+D4h
Power-on Default: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**VWIHF2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIHF1								**VWIHF0**							

Bit 31:24 Reserved

Bit 23:16 Video Window I horizontal filter 2 (VWIHF2)

Bit 15:8 Video Window I horizontal filter 1 (VWIHF1)

Bit 7:0 Video Window I horizontal filter 0 (VWIHF0)

VPRD8: Vertical Filter for Video Window I

Read/Write: Address: VP_Base+D8h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VWIVF3								**VWIVF2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIVF1								**VWIVF0**							

Bit 31:24 Video Window I vertical filter 3 (VWIVF3)

Bit 23:16 Video Window I vertical filter 2 (VWIVF2)

Bit 15:8 Video Window I vertical filter 1 (VWIVF1)

Bit 7:0 Video Window I vertical filter 0 (VWIVF0)

VPRDC: Horizontal Filter for Video Window II

Read/Write: Address: VP_Base+DCh
Power-on Default: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**VWIIHF2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIIHF1								**VWIIHF0**							

Bit 31:24 Reserved

Bit 23:16 Video Window II horizontal filter 2 (VWIIHF2)

Bit 15:8 Video Window II horizontal filter 1 (VWIIHF1)

Bit 7:0 Video Window II horizontal filter 0 (VWIIHF0)

VPRE0: Data Source Last Start Address for Sub Picture

Read/Write Address: VP_Base+E0h
Power-on Default: 3FFFFF

This register specifies data source last starting address for sub picture. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**SSLSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSLSA															

Bit 31:22 Reserved

Bit 21:0 Sub Picture Source Last Starting Address, in 64-bit segment (SSLSA)

VPRE4: Video Window I Source Odd Field Start Address

Read/Write Address: VP_Base+E4h
Power-on Default: Undefined

This register specifies video odd field start address for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VWIOSS**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIOSS															

Bit 31:22 Reserved

Bit 21:0 Video Window I odd field source start address for, in 64-bit segment. (VWIOSS)

VPRE8: Video Window I Odd Field Chroma Data Source Starting Address

Read/Write Address: VP_Base+E8h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VWIOCSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIOCSA															

Bit 31:22 Reserved

Bit 21:0 Video Window I Odd Field Chroma Data Source Starting Address (VWIOCSA)

VPREC: Data Source Odd Field Last Start Address for Video Window I

Read/Write Address: VP_Base+ECh
Power-on Default: 3FFFFF

This register specifies odd field data source last starting address for video window I. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VWIOSLSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIOSLSA															

Bit 31:22 Reserved

Bit 21:0 Video Window I Odd Field Source Last Starting Address, in 64-bit segment (VWISLSA)

VPRF0: Odd Field Chroma Last Start Address for Video Window I

Read/Write Address: VP_Base+F0h
Power-on Default: 3FFFFF

This register specifies odd field chroma last starting address for video window I. When the current line starting address equal or greater then the last start address, the current line starting address will remain the same until next vertical sync.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										**VWIOCLSA**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIOCLSA															

Bit 31:22 Reserved

Bit 21:0 Video Window I Odd Field Chroma Last Starting Address, in 64-bit segment (VWIOCLSA)

Chapter 23: 2D Drawing Engine Registers

Table 26: Drawing Engine & Capture Control Registers Quick Reference

Drawing Engine Control Registers

The Drawing Engine supports various drawing functions, including Bresenham line draw, short stroke line draw, BITBLT, rectangle fill, HOSTBLT, Rotation Blit, and others. Hardware clipping is supported by 4 registers, DPR2C-DPR32, which defines a rectangular clipping area.

The drawing engine supports two types of format for its source and destination locations. One can specify location formats in X-Y coordinate, where the upper left corner of the screen is defined to be (0,0); this method is referred as X-Y addressing. Also, one can specify the location format based on its position in the display memory sequentially from the first pixel of the visible data; this method is referred as DE linear addressing. To select DE linear addressing, one must set DPR1E bit [3:0] = 1111.

All Drawing Engine control registers can be accessed via memory-mapped.

DPR00: Source Y or K2

Read/Write Address: DP_Base+00h
Power-on Default: Undefined

This register specifies the 12-bit Source Y position in x-y addressing mode, or low-order source address in DE linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify the 14-bit for K2 constant of Bresenham line when DPR0E bit [3:0] = 0111b to select Bresenham line command function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOURCE Y FOR X-Y ADDRESSING															

Bit 15:0 Source Y for X-Y addressing. In 24-bit packed modes, Source Y needs to be multiplied by 3.
OR
High-order source address SA[23:12] for DE linear addressing. Low-order 12-bit are in DPR02.

Bresenham Line (DPR0E bit [3:0] = 0111b)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**AXIAL DIAGONAL CONSTANT (K2)**													

Bit 15:14 Reserved

Bit 13:0 Axial Diagonal Constant (K2) = 2 * (min(|dx|,|dy|) - max(|dx|,|dy|))

DPR02: Source X or K1

Read/Write Address: DP_Base+02h
Power-on Default: Undefined

This register specifies the 12-bit Source X position in x-y addressing mode, or low-order source address in linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify the 14-bit for K1 constant of Bresenham line when DPR0E bit [3:0] = 0111b to select Bresenham line command function. For HOSTBLT write

command function (when DPR0E bit [3:0] = 1000b), this register is also used to specify the 5-bit HOST mono source for alignment.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**SOURCE X FOR X-Y ADDRESSING**												

Bit 15:13 Reserved

Bit 12:0 Source X for X-Y addressing mode. In 24-bit packed modes, Source X needs to be multiplied by 3.
OR
Low-order source address SA [11:0] for DE linear addressing mode. Higher order 12-bit are in DPR00.

Note: For 24-bit color pattern, Xs = (PatXs * 3) LOGIC_OR (Yd[2:0] *3, shift 3 bits to left)
For 32-bit color pattern, Xs = (PatXs) LOGIC_OR (Yd[2:0], shift 3 bits to left)

Bresenham Line (DPR0E bit [3:0] = 0111b)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**AXIAL STEP CONSTANT K1**													

Bit 15:14 Reserved

Bit 13:0 Axial Step Constant (K1) = 2 * min (|dx|, |dy|)

HOSTBLT Write (DPR0E bit [3:0] = 1000b)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											**HMSA**				

Bit 15:5 Reserved

Bit 4:0 Host mono source alignment for 8, 16, or 32-bit color modes. For 24-bit color mode, software needs to adjust for alignment. (HMSA)

DPR04: Destination Y or Start Y

Read/Write Address: DP_Base+04h
Power-on Default: Undefined

This register specifies the 12-bit Destination Y position in x-y addressing mode or higher-order destination address for DE linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify Vector Y start address for Bresenham Line when DPR0E bit [3:0] = 0111b to select Bresenham line command function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESTINATION Y OR START Y															

		Bresenham Line (DPR0E bit [3:0] = 0111b
Bit 15:0	Destination Y for X-Y addressing. In 24-bit packed modes, Destination Y needs to be multiplied by 3. OR High-order 12 bits destination address DA[23:12] for DE linear addressing.	Vector Y start address

DPR06: Destination X or Start X

Read/Write Address: DP_Base+06h
Power-on Default: Undefined

This register specifies 12-bit Destination X position in x-y addressing mode or low-order 12-bit destination address in DE linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify Vector X start address for Bresenham Line when DPR0E bit [3:0] = 0111b to select Bresenham line command function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**DESTINATION X OR START X**												

Bit 15:13 Reserved

		Bresenham Line (DPR0E bit [3:0] = 0111b
Bit 12:0	Destination X for X-Y addressing. In 24-bit packed modes, Destination X needs to be multiplied by 3. OR Low-order 12 bits destination address DA[11:0] for DE linear addressing.	Vector X start address

DPR08: Dimension Y or Error Term

Read/Write Address: DP_Base+08h
Power-on Default: Undefined

This register specifies the rectangle height or Dimension Y in pixels. When Bresenham line command function is selected (DPR0E bit [3:0] = 0111b), this register specifies the Vector Error Term. When Short Stroke Line command function is selected (DPR0E bit [3:0] = 0110b), this register specifies the short stroke line length for non-horizontal short stroke line

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**DIMENSION Y OR ERROR TERM**												

		Short Stroke (DPR0E bit [3:0] = 0110b)	**Bresenham Line (DPR0E bit [3:0] = 0111b)**
Bit 15:13	Reserved	Reserved	Reserved
Bit 12:0	Dimension Y	Short Stroke Length if not a horizontal line (≠ 0° or ≠ 180°)	(ET)*

* Vector Error Term is determined based on the following logic:
ET = 2 * min (|dx|,|dy|) - max (|dx|,|dy|) if starting X > ending X.
ET = 2 * min (|dx|,|dy|) - max (|dx|,|dy|) -1 if starting X <= ending X.

DPR0A: Dimension X or Vector Length

Read/Write Address: DP_Base+0Ah
Power-on Default: Undefined

This register specifies the rectangle width or Dimension X in pixels. When Bresenham line command function is selected (DPR0E bit [3:0] = 0111b), this register specifies the Vector Length. When Short Stroke Line command function is selected (DPR0E bit [3:0] = 0110b), this register specifies the short stroke line length for horizontal short stroke line.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**DIMENSION X OR VECTOR LENGTH**												

Bit 15:13 Reserved

	.	**Bresenham Line (DPR0E bit [3:0] = 0111b)**	**Short Stroke (DPR0E bit [3:0] = 0110b)**
Bit 12:0	Dimension X. In 24-bit packed mode, Dimension X needs to be multiplied by 3. (note: Dimension Y does not need to be multiplied by 3)	Vector Length = Dmax + 1.Where Dmax is the dimension of Vector length which is on the major axis. Major axis is determined to be the axis which has longer length.	Short Stroke Length for horizontal short stroke line. (= 0° or = 180°)

DPR0C: ROP and Miscellaneous Control

Read/Write Address: DP_Base+0Ch
Power-on Default: Undefined

This register specifies the ROP2/ROP3 select, ROP2 source select, mono data format, pixel control, and 3 ROP operands.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROP	**ROPS**	**MDS**		**ERR**	**MPC**	**PCTS**	**TE**	**ROP3 RESERVED**				**ROP CODE**			

Bit 15 ROP2 or ROP3 select (ROP)
0 = select ROP3
1 = select ROP2

Bit 14 ROP2 source select. This bit is only valid when bit 15 of this register is set to "1". (ROPS)
0 = ROP2 source is not pattern
1 = ROP2 source is pattern

Bit 13:12 Mono Data Select. Mono data format is used to optimize font performance. Driver selects particular mono data format for particular font sizes. (MDS)

00 = No packed mono data
01 = Mono data packed at 8-bit
10 = Mono data packed at 16-bit
11 = Mono data packed at 32-bit

Bit 11 Enable Repeat Rotation BLT. This bit is only valid when DPR0E[3:0] = 1011b. (ERR)
0 = disable
1 = enable

Bit 10 Matching Pixel Control. This bit is only valid when transparency is enabled (bit 8 of this register = 1) (MPC)
0 = Matching pixel is opaque
1 = Matching pixel is transparent

Bit 9 Pixel Control Transparency Select (PCTS)
0 = Source controls transparency
1 = Destination controls transparency

Bit 8 Transparency Enable (TE)
0 = disable
1 = enable

Bit 7:4 ROP3 code[1] Reserved

Bit 3:0 ROP3 code[1] ROP2 code[2]

Notes:
[1] 3 Operands 256 operations ROP codes table reference listed below. For details on ROP codes, please refer to the Microsoft's device driver adaptation guide.

ROP3 Code	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pattern	1	1	1	1	0	0	0	0
Source	1	1	0	0	1	1	0	0
Destination	1	0	1	0	1	0	1	0

[2] 2 Operands 16 operations ROP codes table listed below:

ROP2 Code	Bit 3	Bit 2	Bit 1	Bit 0
Zero	0	0	0	0
~(D+ S)	0	0	0	1
D * ~S	0	0	1	0
~ S	0	0	1	1
S * ~D	0	1	0	0
~D	0	1	0	1

ROP2 Code	Bit 3	Bit 2	Bit 1	Bit 0
D * S	1	0	0	0
~(D ⊕ S)	1	0	0	1
D	1	0	1	0
D + ~S	1	0	1	1
S	1	1	0	0
S + ~D	1	1	0	1

ROP2 Code	Bit 3	Bit 2	Bit 1	Bit 0
D ⊕ S	0	1	1	0
~(D * S)	0	1	1	1

ROP2 Code	Bit 3	Bit 2	Bit 1	Bit 0
D + S	1	1	1	0
One	1	1	1	1

DPR0E: Drawing Engine Commands and Control

Read/Write Address: DP_Base+0Eh
Power-on Default: Undefined (except for Bit 15 and Bit 12 = 0)

This register specifies the drawing engine command and control registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEA	**PS**	**DUE**	**DEQS**	**SSL**	**BMA**	**XYS**		**GSE**	**HBSC**	**PSB**	**DECE**	**COMMAND FUNCTIONS**			

Bit 15 Drawing Engine Activate (DEA)
0 = Idle (Power-on default = 0)
1 = Start Activate Drawing Engine

Bit 14 Pattern Select (PS)
0 = mono pattern
1 = color pattern

Bit 13 Destination X Update Enable (DUE)

0 = Do not update destination X on completion of a drawing engine function
1 = Update destination X on completion of a drawing engine function

Bit 12 Drawing Engine Quick Start Enable. If this bit is set, drawing engine will be activated right after dimension X is provided. One does not need to activate the drawing engine by setting bit 15 = 1 if quick start is already enabled. (DEQS)
0 = disable (Power-on default = 0)
1 = enable

Bit 11 Direction for Short Stroke Line and BITBLT For diagonal and vertical line, this bit needs to be set to "0". (SSL)

Bit 11	Short Stroke Line Direction	BITBLT Direction
0	not horizontal	Left to Right
1	horizontal	Right to Left

Bit 10 Bresenham Major Axis (Y) (BMA)
0= major axis is X
1= major axis is Y. For vertical line, this bit needs to be set.

Bit 9:8 X-Step and Y-Step (XYS)
00 = 0 degree transform

01 = 90 degree (CW90)
11 = 180 degree
10 = 270 degree (CCW90)

Bit 7 Graphics Stretch Enable (only for Y direction) (GSE)
0 = disable
1 = enable

Bit 6 HOST BITBLT Source Color Select (HBSC)
0 = Source is color
1 = Source is monochrome

Bit 5 Last Pixel Select for Bresenham line (PSB)
0 = Vector not draw last pixel
1 = Vector draw last pixel

Bit 4 Drawing Engine Capture Enable (DECE)
0 = Normal Operation. No HOSTBLT capture operation.
1 = Enable HOSTBLT Read capture operation

Bit 3:0 Command Functions
0000 = BITBLT
0001 = Rectangle Fill
0010 = De-tile BITBLT (Screen → Screen)
0011 = Trapezoid Pattern Fill
0100 = Alpha Blending BITBLT
0101 = Run Length Encoding (RLE) Strip Draw
0110 = Short Stroke
0111 = Bresenham Line Draw
1000 = Host BLT Write
1001 = Host BLT Read
1010 = Host BLT Write from Left_Bottom
1011 = Rotation BLT
1100 = Reserved
1101 = Reserved
1110 = Reserved
1111 = DMA Texture Load

DPR10: Source Row Pitch

Read/Write Address: DP_Base+10h
Power-on Default: Undefined

This register specifies the source row offset in pixel unit for 8/16/32-bit color modes. In 24-bit color mode, source row offset needs to be multiplied by 3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**SOURCE ROW OFFSET**												

Bit 15:13 Reserved

Bit 12:0 Source Row Offset. In 24-bit color mode, source row offset needs to be multiplied by 3.

DPR12: Destination Row Pitch

Read/Write Address: DP_Base+12h
Power-on Default: Undefined

This register specifies the destination row offset in pixel unit for 8/16/32-bit color modes. In 24-bit color mode, destination row offset needs to be multiplied by 3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**DESTINATION ROW OFFSET**												

Bit 15:13 Reserved

Bit 12:0 Destination Row Offset. In 24-bit color mode, destination row offset needs to be multiplied by 3.

DPR14: Foreground Colors

Read/Write Address: DP_Base+14h
Power-on Default: Undefined

The register specifies the foreground graphics color for 8-bit color (DPR1E bit [5:4] = 00b), 16-bit color (DPR1E bit [5:4] = 01b), and 24-bit color (DPR1E bit [5:4] = 11b) modes.

8-bit color mode

31	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**FOREGROUND COLOR**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR HIGH BYTE								**FOREGROUND COLOR LOW BYTE**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**FOREGROUND COLOR RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR GREEN								**FOREGROUND COLOR BLUE**							

32-Bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOREGROUND ALPHA								**FOREGROUND COLOR RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR GREEN								**FOREGROUND COLOR BLUE**							

	8-bit color mode	**16-bit color mode**	**24-bit color mode**	**32-bit color mode**
Bit 31:24	Reserved	Reserved	Reserved	Alpha Component
Bit 23:16	Reserved	Reserved	Foreground Color Red	Foreground Color Red
Bit 15:8	Reserved	Foreground Color High Byte	Foreground Color Green	Foreground Color Green
Bit 7:0	Foreground Color 8-bit index	Foreground Color Low Byte	Foreground Color Blue	Foreground Color Blue

DPR18: Background Colors

Read/Write Address: DP_Base+18h
Power-on Default: Undefined

The register specifies the background graphics color for 8-bit color (DPR1E bit [5:4] = 00), 16-bit color (DPR1E bit [5:4] = 01), and 24-bit color (DPR1E bit [5:4] = 11) modes.

Note: in monochrome transparency mode (font operation), the background color needs to be programmed to equal to the invert of foreground color in DPR14.

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**BACKGROUND COLOR**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR HIGH BYTE								**BACKGROUND COLOR GREEN**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**BACKGROUND COLOR RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR GREEN								**BACKGROUND COLOR BLUE**							

	8-bit color mode	16-bit color mode	24-bit color mode	32-bit color mode
Bit 31:24	Reserved	Reserved	Reserved	Background Alpha
Bit 23:16	Reserved	Reserved	Background Color Red	Background Color Red
Bit 15:8	Reserved	Background Color High Byte	Background Color Green	Background Color Green
Bit 7:0	Background Color 8-bit index	Background Color Low Byte	Background Color Blue	Background Color Blue

DPR1C: Stretch Source Height Y

Read/Write Address: DP_Base+1Ch
Power-on Default: Undefined

This register specifies the height of source block for stretch BITBLT.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SOURCE Y DIMENSION FOR STRETCH BLT**											

Bit 15:12 Reserved

Bit 11:0 Source Y dimension for stretch BLT. (only for Y direction)

DPR1E: Drawing Engine Data Format and Location Format Select

Read/Write Address: DP_Base+1Eh
Power-on Default: Undefined

The register specifies drawing engine source & destination locations select and data format.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**XY**	**PATTERN START Y**			**PATTERN START X**				**R**	**DEDF**		**DRAWING ENG LOCATION**			

Bit 15 Reserved (R)

Bit 14 Pattern XY Overwrite Select (XY)
0 = Normal. Drawing Engine uses Bit [13:8] as pattern address only when it is in linear addressing mode (Bit [3:0] = 1111b]
1 = Overwrite. Drawing Engine uses Bit [13:8] as pattern address no matter what addressing mode it is in.

Bit 13:11 Pattern Start Y Address (Yd [2:0]). This address is only valid if Bit 14 = 1 or Bit [3:0] = 11xxb (linear addressing).

Bit 10:7 Pattern Start X Address (Xd [2:0]). This address is only valid if Bit 14 = 1 or Bit [3:0] = 11xxb (linear addressing). It is based on the top left corner of screen as (0,0) coordinate address. Rotation is needed

for pattern source if Xd is non-zero. All 4 bits (bit 10:7) are used at 24bpp. Only 3 bits (bit 9:7) are used at 8, 16, and 32 bpp.

Bit 6 Reserved

Bit 5:4 Drawing Engine Data Format (DEDF)
00 = 8-bit per pixel
01 = 16-bit per pixel
10 = 32-bit per pixel
11 = 24-bit per pixel (24-bit packed)

Bit 3:0 Drawing Engine Locations (Source and Destination) Format Select. The drawing engine supports two types of format for its source and destination locations. One can specifies location format in X-Y coordinate, where the upper left corner of the screen is defined to be (0,0); this method is referred as X-Y addressing. Also, one can specifies the location format based on its position in the display memory sequentially from the first pixel of the visible data; this method is referred as DE linear addressing. This register selects the pixel width for X-Y addressing and DE linear addressing.
1111 = DE linear addressing
else = XY screen width depends on DPR3C register

DPR20: Color Compare

Read/Write Address: DP_Base+20h
Power-on Default: Undefined

The register specifies the color compare for 8-bit color (DPR1E bit [5:4] = 00), 16-bit color (DPR1E bit [5:4] = 01), and 24-bit color (DPR1E bit [5:4] = 11) modes.
Note, in monochrome transparency mode for font operations, the color compare needs to be programmed to equal to the foreground color in DPR14.

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**COLOR COMPARE 8-BIT INDEX**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE HIGH BYTE								**COLOR COMPARE LOW BYTE**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**COLOR COMPARE RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE GREEN								**COLOR COMPARE BLUE**							

	8-bit color mode	16-bit color mode	24-bit color mode
Bit 31:24	Reserved	Reserved	Reserved
Bit 23:16	Reserved	Reserved	Color Compare Red
Bit 15:8	Reserved	Color Compare High Byte	Color Compare Green
Bit 7:0	Color Compare 8-bit index	Color Compare Low Byte	Color Compare Blue

DPR24: Color Compare Masks

Read/Write Address: DP_Base+24h
Power-on Default: Undefined

The register specifies the color compare mask for 8-bit color (DPR1E bit [5:4] = 00), 16-bit color (DPR1E bit [5:4] = 01), and 24-bit color (DPR1E bit [5:4] = 11) modes.

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**COLOR COMPARE 8-BIT INDEX**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE MASK HIGH BYTE								**COLOR COMPARE MASK LOW BYTE**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**COLOR COMPARE MASK RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE MASK GREEN								**COLOR COMPARE MASK BLUE**							

	8-bit color mode	16-bit color mode	24-bit color mode
Bit 31:24	Reserved	Reserved	Reserved
Bit 23:16	Reserved	Reserved	Color Compare Mask Red
	8-bit color mode	**16-bit color mode**	**24-bit color mode**
Bit 15:8	Reserved	Color Compare Mask High Byte	Color Compare Mask Green
Bit 7:0	Color Compare Mask 8-bit index	Color Compare Mask Low Byte	Color Compare Mask Blue

DPR28: Bit Mask

Read/Write Address: DP_Base+28h
Power-on Default: Undefined

The register specifies the Bit Mask for 8-bit color (DPR1E bit [5:4] = 00) and 16-bit color (DPR1E bit [5:4] = 01) modes.

8-bit color mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**BIT MASK 8-BIT INDEX**							

16-bit color mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT MASK HIGH BYTE								**BIT MASK LOW BYTE**							

	8-bit color mode	**16-bit color mode**
Bit 15:8	Reserved	Bit Mask High Byte
Bit 7:0	Bit Mask 8-bit index	Bit Mask Low Byte

DPR2A: Byte Mask Enable

Read/Write Address: DP_Base+2Ah
Power-on Default: Undefined

The register specifies the byte mask enable register for 64-bit datapath.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTE MASK FOR 64-BIT DATAPATH															

Bit 15:0 Byte Mask for 128-bit datapath. Each bit enables the corresponding byte data.
0 = disable write
1 = enable write

DPR2C: Scissors Left and Control

Read/Write Address: DP_Base+2Ch
Power-on Default: Undefined

The register specifies the Scissors left boundary and control registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**SBS**	**SE**	**SCISSORS BOUNDARY LEFT**												

Bit 15 Reserved (R)

Bit 14 Scissors Boundary Select (SBS)
0 = Write disable outside the Scissors boundary
1 = Write disable inside the Scissors boundary

Bit 13 Scissors Enable (SE)
0 = disable
1 = enable

Bit 12:0 Scissors Boundary Left. In 24-bit color mode, the scissors boundary left position needs to be multiplied by 3.

DPR2E: Scissors Top

Read/Write Address: DP_Base+2Eh
Power-on Default: Undefined

The register specifies the scissors top boundary.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCISSORS BOUNDARY TOP															

Bit 15:0 Scissors Boundary Top. In 24-bit color mode, the scissors boundary top position needs to be multiplied by 3.

DPR30: Scissors Right

Read/Write Address: DP_Base+30h
Power-on Default: Undefined

The register specifies the right boundary.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**SCISSORS BOUNDARY RIGHT**												

Bit 15:13 Reserved

Bit 12:0 Scissors Boundary Right. In 24-bit color mode, the scissors boundary right position needs to be multiplied by 3.

DPR32: Scissors Bottom

Read/Write Address: DP_Base+32h
Power-on Default: Undefined

The register specifies the bottom boundary.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCISSORS BOUNDARY BOTTOM															

Bit 15:0 Scissors Boundary Bottom. In 24-bit color mode, the scissors boundary bottom position = scissors boundary top position DPR2E [11:0] + height of the clipping window.

DPR34: Mono Pattern Low

Read/Write Address: DP_Base+34h
Power-on Default: Undefined

The register specifies the monochrome pattern lower double word. It is 32-bit access only. The higher 32-bit are in DPR38.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MONO PATTERN TOP 4 LINES															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MONO PATTERN TOP 4 LINES															

Bit 31:0 Mono pattern top 4 lines. Line 3 data is located in the most significant byte where as line 0 data is located in the least significant bye.

DPR38: Mono Pattern High

Read/Write Address: DP_Base+38h
Power-on Default: Undefined

The register specifies the monochrome pattern higher double word. It is 32-bit access only. The lower 32-bit are in DPR34.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MONO PATTERN LAST 4 LINES															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MONO PATTERN LAST 4 LINES															

Bit 31:0 Mono pattern last 4 lines. Line 7 data is located in the most significant byte where as line 4 data is located in the least significant bye.

DPR3C: XY Addressing Destination & Source Window Widths

Read/Write Address: DP_Base+3Ch
Power-on Default: Undefined

The register specifies the XY width for source and destination window.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				**DESTINATION WINDOW WIDTH IN PIXEL**											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SOURCE WINDOW WIDTH IN PIXEL**											

Bit 31:28 Reserved

Bit 27:16 Destination Window width in pixel for XY addressing mode (max. = 4096 pixel)

Bit 15:12 Reserved

Bit 11:0 Source Window width in pixel for XY addressing mode (max. = 4096 pixel)

DPR40: Source Base Address

Read/Write Address: DP_Base+40h
Power-on Default: Undefined

The register specifies the Source base address in 64-bit unit (8 byte unit).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**SOURCE BASE ADDRESS**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOURCE BASE ADDRESS															

Bit 31:24 Reserved

Bit 23:0 Source Base address

DPR44: Destination Base Address

Read/Write Address: DP_Base+44h
Power-on Default: Undefined

The register specifies the destination base address in 64-bit (8-byte) unit.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**DESTINATION BASE ADDRESS**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESTINATION BASE ADDRESS															

Bit 31:24 Reserved

Bit 23:0 Destination Base address

DPR48: Alpha Value for Blending Bitblt

Read/Write Address: DP_Base+48h
Power-on Default: Undefined

The register specifies the bottom boundary.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**ALPHA VALUE**							

Bit 15:8 Reserved

Bit 7:0 Alpha Value used in Alpha Blending Bitblt
Color = (Src * Alpha + (255 - Alpha) * Dst) * 257/64K

Chapter 24: Video Capture Control Registers

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Capture Processor Control Registers

The Capture Processor Control Registers specify the control registers for Capture Processor The Capture Processor Control Registers can only be accessed through memory-mapped.

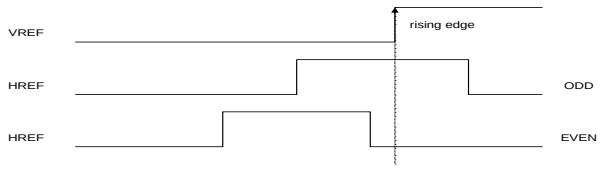
CPR00: Capture Port Control

Read/Write Address: CP_Base+00h
Power-on Default: 00h
This register specifies the capture port which can be used for video capture and video playback.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							**FDMS**	**VREF**	**HREF**	**EHF**		**EVR**		**EHR**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDI		**FSE**			**IDCE**	**DBE**	**CC**	**FIS**	**IS**	**CBS**	**CFO**	**VIS**	**BUF2**	**BUF1**	**VCE**

Bit 31:25 Reserved

Bit 24 Field Detect Method Select (FDMS)
0 = Falling edge of VSYNC
1 = Rising edge of VSYNCt



Bit 23 VREF Polarity (VREF)
0 = "High" active
1 = "Low" active

Bit 22 HREF Polarity (HREF)
0 = "High" active
1 = "Low" active

Bit 21:20 Enable Horizontal Filtering (EHF)
00 = no filtering
01 = 2-tap filtering
10 = 3-tap filtering
11 = 4-tap filtering

Bit 19:18 Enable Vertical Reduction (EVR)
00 = no reduction
01 = 2 to 1 reduction
10 = 4 to 1 reduction
11 = reserved

Bit 17:16 Enable Horizontal Reduction (EHR)
00 = no reduction
01 = 2 to 1 reduction
10 = 4 to 1 reduction
11 = reserved

Bit 15:14 Video Capture Input Data Format (VDI)
00 = YUV 4:2:2
01 = YUV 4:2:2 (with byte swapping)
10 = RGB 5:5:5
11 = RGB 5:6:5

Bit 13:11 Frame Skip Enable (FSE)
000 = no skip
001 = skip every other frame
010 = skip even frame
011 = skip odd frame
100 = capture 2 and skip 1 frame
101 = capture 3 and skip 1 frame
110 = capture 1 and skip 2 frame
111 = capture 1 and skip 3 frame

Bit 10 Interlace Data Capture Enable (IDCE)
0 = Disable (non-interlace)
1 = Enable (interlace data. even field will be captured into buffer1 and odd field will be captured into buffer2) When this bit is set to 1, double buffer mode needs to be also enabled (bit 9 =1).

Bit 9 Double Buffer Enable (DBE)
0 = Disable. Use buffer1 addressed by VPR48.
1 = Enable. Use buffer1 and buffer2 addressed by VPR48 and VPR4C.

Bit 8 Capture Control (CC)
0 = Continuous Capture
1 = Conditional Capture. Capture is controlled by bit 1 or bit 2 of this register.

Bit 7 Field Input Status (Read Only) (FIS)
0 = even field
1 = odd field

Bit 6 Interlace Status (Read Only) (IS)
0 = non-interlace
1 = interlace

Bit 5 Current Buffer Status (Read Only) (CBS)
0 = Buffer 1 is the current buffer used
1 = Buffer 2 is the current buffer used

Bit 4 Current Frame Capture Status (Read Only) (CFO)
0 = Skip the current frame
1 = Capture the current frame

Bit 3 VSYNC Input Status (Read Only) (VIS)
0 = VSYNC pulse is inactive
1 = VSYNC pulse is active

Bit 2 Buffer 2 Status/Control Bit. This bit is used for software to read back the status of the current frame. Software needs to preset this bit to 1 when programming the Buffer 2 starting address in VPR4C. This bit can be set by drawing engine, and it can also be reset by video capture unit. If continuous capture is selected (bit 8 =0), this bit will be ignored. (BUF2)
0 = Idle or Capture has completed
1 = Capture in progress

Bit 1 Buffer 1 Status/Control Bit. This bit is used for software to read back the status of the current frame. Software needs to preset this bit to 1 when programming the Buffer 1 starting address in VPR48. This bit can be set by drawing engine, and it can also be reset by video capture unit. If continuous capture is selected (bit 8 =0), this bit will be ignored. (BUF1)
0 = Idle or Capture has completed
1 = Capture in progress

Bit 0 Video Capture Enable. When Video Capture is enabled, all video port I/O pins except for "BLANK" pin will become input pins only. This bit can also be accessed through I/O register space 3?5, index FF, bit [0]. (VCE)
0 = Disable
1 = Enable

CPR04: Video Source Clipping Control

Read/Write Address: CP_Base+04h
Power-on Default: Undefined

This register specifies top and left clipping of video source.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**VIDEO SOURCE TOP CLIPPING**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**VIDEO SOURCE LEFT CLIPPING**									

Bit 31:26 Reserved

Bit 25:16 Video Source Top Clipping, # of line to drop

Bit 15:10 Reserved

Bit 9:0 Video Source Left Clipping, # of pixel to drop

CPR08: Video Source Capture Size Control

Read/Write Address: CP_Base+08h
Power-on Default: Undefined

This register specifies video source capture size.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO SOURCE HEIGHT**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO SOURCE WIDTH**										

Bit 31:27 Reserved

Bit 26:16 Video Source Height

Bit 15:11 Reserved

Bit 10:0 Video Source Width

CPR0C: Capture Port Buffer I Source Start Address

Read/Write Address: CP_Base+0Ch
Power-on Default: Undefined

This register specifies video source start address for Buffer I of Capture Port.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											**CAPTURE PORT I**				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE PORT I															

Bit 31:21 Reserved

Bit 20:0 Capture Port Buffer I source start address, in 64-bit segment

CPR10: Capture Port Buffer II Source Start Address

Read/Write Address: CP_Base+10h
Power-on Default: Undefined

This register specifies video source start address for Buffer II of Capture Port.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											**CAPTURE PORT II**				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE PORT II															

Bit 31:21 Reserved

Bit 20:0 Capture Port Buffer II source start address, in 64-bit segment.

CPR14: Capture Port Source Offset Address

Read/Write Address: CP_Base+14h
Power-on Default: Undefined

This register specifies video source offset address for Capture Port.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**CAPTURE PORT SOURCE**										

Bit 31:11 Reserved

Bit 10:0 Capture Port Source Address Offset, in 64-bit segment

CPR18: Capture FIFO Empty Request level Control

Read/Write Address: CP_Base+18h
Power-on Default: 00000006h

This register specifies Capture FIFO empty request level. At the specified empty FIFO level, FIFO request will be generated. Default FIFO empty levels are all 6 or more empty.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													**CAPTURE WINDOW**		

Bit 31:3 Reserved

Bit 2:0 Capture Window FIFO Empty request level Select
000 = 2 or more empty
001 = 3 or more empty
010 = 4 or more empty
011 = 5 or more empty
100 = 6 or more empty
101 = 8 or more empty
110 = 10 or more empty (default)
111 = 12 or more empty

CPR1C: Reserved (Internal Use)

Read/Write Address: CP_Base+1Ch
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															

Bit 31:0 Reserved

Linear to Tile Address Conversion For CPU Access

In order to access the frame buffer in tile mode during the time application software has no idea about the tile format in the memory. Internal hardware has to make the address conversion to address to the right tile location.

CPR20: Tile Conversion Setting

Read/Write Address: CP_Base+20h
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										**RESOLUTION**			**PS**	**TM**	**EL**

Bit 31:6 Reserved

Bit 5:3 Resolution
000 = 640 x 480
001 = 800 x 600
010 = 1024 x 768
011 = 1280 x 1024
100 = 1600 x 1200
Else = reserved

Bit 2 Pixel Size (PS)
0 = 16 bits per pixel
1 = 32 bits per pixel

Bit 1 Tile Mode (TM)
0 = Read/Write in linear mode.
1 = Read/Write in tile mode.

Bit 0 Enable Linear to Tile Conversion (EL)
0 = Disable Tile Conversion (Default)
1 = Enable Tile Conversion

CPR24: Start-End Address

Read/Write Address: CP_Base+24h
Power-on Default: 00h

Start/end address of the range needed to do tile conversion.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	**END ADDRESS**														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**START ADDRESS**														

Bit 31 Reserved (R)

Bit 30:16 End Address in 1K-byte as a unit (=Byte Address_[24:10])

Bit 15 Reserved

Bit 14:0 Start Address in 1K-byte as a unit (=Byte Address_[24:10])

Chapter 25: PCI/AGP DMA Control Registers

Table 28: Motion Comp Video Registers Quick Reference

Motion Comp Bus Master CMD Control Registers

MCR00: Motion Comp Enable

Read/Write Address: MCR_Base + Offset
Power-On Default:

7	6	5	4	3	2	1	0
RESERVED							**MCE**

Bit 7:1 Reserved

Bit 0 Motion Comp Enable (MCE)

MCR04: Slot 0 Y Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT0 Y DATA**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT0 Y DATA															

Bit 31:20 Reserved

Bit 19:0 Slot0, Y Data Source Starting Address

MCR08: Slot1 Y Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT1 Y DATA**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT1 Y DATA															

Bit 31:20 Reserved

Bit 19:0 Slot1, Y Data Source Starting Address

MCR0C: Slot2 Y Data Source

Read/Write Address: MCR_Base + Offset

Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT2 Y DATA**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT2 Y DATA															

Bit 31:20 Reserved

Bit 19:0 Slot2, Y Data Source Starting Address

MCR10: Slot3 Y Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT3 Y DATA**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT3 Y DATA															

Bit 31:20 Reserved

Bit 19:0 Slot3, Y Data Source Starting Address

MCR14: Slot0 UV Interleave Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT0 UV INTERLEAVE**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT0 UV INTERLEAVE															

Bit 31:20 Reserved

Bit 19:0 Slot0, UV Interleave Data Source Starting Address

MCR18: Slot1 UV Interleave Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT1 UV INTERLEAVE**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT1 UV INTERLEAVE															

Bit 31:20 Reserved

Bit 19:0 Slot1, UV Interleave Data Source Starting Address

MCR1C: Slot2 UV Interleave

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT2 UV INTERLEAVE**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT2 UV INTERLEAVE															

Bit 31:20 Reserved

Bit 19:0 Slot2, UV Interleave Data Source Starting Address

MCR20: Slot3 UV Interleave Data Source

Read/Write Address: MCR_Base + Offset
Power-On Default:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SLOT3 UV INTERLEAVE**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOT3 UV INTERLEAVE															

Bit 31:20 Reserved

Bit 19:0 Slot3, UV Interleave Data Source Starting Address

MCR24: Y Data Source Line Offset

Read/Write Address: MCR_Base + Offset
Power-On Default:

7	6	5	4	3	2	1	0
OFFSET							

Bit 8:0 Y Data Source Line Offset (row pitch)

MCR28: UV Interleave Data Source Line Offset

Read/Write Address: MCR_Base + Offset
Power-On Default:

7	6	5	4	3	2	1	0
UV INTERLEAVE DATA SOURCE LINE OFFSET							

Bit 8:0 UV Interleave Data Source Line Offset (row pitch)

Motion Compensation ICMD Control Registers

Table of Entry Register

Read/Write Address: ICMD_Reg_Base + Offset
Offset 0:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLE OF ENTRY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLE OF ENTRY														**DC**	**LL**

Bit 31:2 Table of Entry Address

Bit 1 Don’t Care (DC)

Bit 0 Link List Bit (LL)
1 = more table of entries
0 = end of table of entry

Physical Address Register

Read/Write Address: ICMD_Reg_Base + Offset
Offset 4:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHYSICAL DATA MEMORY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICAL DATA MEMORY														**DON'T CARE**	

Bit 31:2 Physical Data Memory Address

Bit 1:0 Don't Care

Blocksize Register

Read/Write Address: ICMD_Reg_Base + Offset
Offset 8:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
READ ONLY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLOCK SIZE															

Bit 31:16 Read Only

Bit 15:0 Block size

Entire Transfer Size of 32-Bit Data

Read/Write Address: ICMD_Reg_Base + Offset
Offset C:
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMI	**PMD**	**DON'T CARE**												**ETS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETS															

Bit 31 Enable Master Interface (EMI)

Bit 30 Use of physical memory data address instead of table entry address during master request phase (PMD)

Bit 29:18 Don't Care

Bit 17:0 Entire Transfer Size (ETS)

Transfer Size Remaining

Read/Write Address: ICMD_Reg_Base + Offset
Offset 10: Read Only
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DON'T CARE														**RTS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTS															

Bit 31:18 Don't Care

Bit 17:0 Remaining transfer size including all blocks (RTS)

Motion Compensation IDCT Control Registers

Table of Entry Register

Read/Write Address: IDCT_Reg_Base + Offset
Offset 0:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLE OF ENTRY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLE OF ENTRY														**DC**	**LL**

Bit 31:2 Table of Entry Address

Bit 1 Don't Care (DC)

Bit 0 Link List Bit (LL)
1 = more table of entries
0 = end of table of entry

Physical Address Register

Read/Write Address: IDCT_Reg_Base + Offset
Offset 4:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHYSICAL DATA MEMORY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICAL DATA MEMORY														**DON'T CARE**	

Bit 31:2 Physical Data Memory Address

Bit 1:0 Don't Care

Blocksize Register

Read/Write Address: IDCT_Reg_Base + Offset
Offset 8:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
READ ONLY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLOCK SIZE															

Bit 31:16 Read Only

Bit 15:0 Block size

Entire Transfer Size of 32-Bit Data

Read/Write Address: IDCT_Reg_Base + Offset
Offset C:
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMI	**PMD**	**DON'T CARE**												**ETS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETS															

Bit 31 Enable Master Interface (EMI)

Bit 30 Use of physical memory data address instead of table entry address during master request phase (PMD)

Bit 29:18 Don't Care

Bit 17:0 Entire Transfer Size (ETS)

Transfer Size Remaining

Read/Write Address: IDCT_Reg_Base + Offset
Offset 10: Read Only
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DON'T CARE														**RTS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTS															

Bit 31:18 Don't Care

Bit 17:0 Remaining transfer size including all blocks (RTS)

Host Master Control Registers

Table of Entry Register

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 0:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLE OF ENTRY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLE OF ENTRY														**DC**	**LL**

Bit 31:2 Table of Entry Address

Bit 1 Don't Care (DC)

Bit 0 Link List Bit (LL)
1 = more table of entries
0 = end of table of entry

Physical Address Register

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 4:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHYSICAL DATA MEMORY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICAL DATA MEMORY														**DON'T CARE**	

Bit 31:2 Physical Data Memory Address

Bit 1:0 Don't Care

Blocksize Register

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 8:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
READ ONLY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLOCK SIZE															

Bit 31:16 Read Only

Bit 15:0 Block size

Entire Transfer Size of 32-Bit Data

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset C:
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMI	**PMD**	**DON'T CARE**												**ETS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETS															

Bit 31 Enable Master Interface (EMI)

Bit 30 Use of physical memory data address instead of table entry address during master request phase (PMD)

Bit 29:18 Don't Care

Bit 17:0 Entire Transfer Size (ETS)

Transfer Size Remaining

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 10: Read Only
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DON'T CARE														**RTS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTS															

Bit 31:18 Don't Care

Bit 17:0 Remaining transfer size including all blocks (RTS) Motion Compensation ICMD Control Registers

Starting Address

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 14:
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**STARTING ADDRESS**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STARTING ADDRESS															

Bit 31:20 Reserved

Bit 19:0 Starting Address for Master Transfer

Width and Offset

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 18:
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**WIDTH FOR MASTER TRANSFER**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**OFFSET FOR MASTER TRANSFER**									

Bit 31:26 Reserved

Bit 25:16 Width for Master Transfer

Bit 15:10 Reserved

Bit 9:0 Offset for Master Transfer

Plane Selection

Read/Write Address: Host Master Control_Reg_Base + Offset
Offset 1C:
Power-on Default: 00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													**EY**	**EU**	**EV**

Bit 31:3 Reserved

Bit 2 Enable Y-Plane Transfer

Bit 1 Enable U-Plane Transfer

Bit 0 Enable V Plane Transfer

Texture 3D Bus Master Control Registers

Table of Entry Register

Read/Write Address: Text3D_Reg_Base + Offset
Offset 0:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLE OF ENTRY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLE OF ENTRY														**DC**	**LL**

Bit 31:2 Table of Entry Address

Bit 1 Don’t Care (DC)

Bit 0 Link List Bit (LL)
1 = more table of entries
0 = end of table of entry

Physical Address Register

Read/Write Address: Text3D_Reg_Base + Offset
Offset 4:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHYSICAL DATA MEMORY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICAL DATA MEMORY														**DON'T CARE**	

Bit 31:2 Physical Data Memory Address

Bit 1:0 Don't Care

Blocksize Register

Read/Write Address: Text3D_Reg_Base + Offset
Offset 8:
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
READ ONLY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLOCK SIZE															

Bit 31:16 Read Only

Bit 15:0 Block size

Entire Transfer Size of 32-Bit Data

Read/Write Address: Text3D_Reg_Base + Offset
Offset C:
Power-on Default: 00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EMI	**PMD**	**DON'T CARE**												**ETS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETS															

Bit 31 Enable Master Interface (EMI)

Bit 30 Use of physical memory data address instead of table entry address during master request phase (PMD)

Bit 29:18 Don’t Care

Bit 17:0 Entire Transfer Size (ETS)

Transfer Size Remaining

Read/Write Address: Text3D_Reg_Base + Offset
Offset 10: Read Only
Power-on Default: XXh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DON’T CARE														**RTS**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTS															

Bit 31:18 Don’t Care

Bit 17:0 Remaining transfer size including all blocks (RTS)

Chapter 26: TV Encoder Registers

Table 29: TV Encoder Registers Quick Reference

Summary of Registers	Page
Common Register	
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Closed Captioning Line Number Register	26 - 3
Closed Captioning 1st and 2nd byte Data for Odd Field	26 - 3
Closed Captioning 1st and 2nd byte Data for Even Field	26 - 4
Closed Captioning Status Register	26 - 4

TV Decoder Register Descriptions

The following are the descriptions for each registers.

Common Register

Mode Register

Read/Write Address: 60h
Power-on Default: 00h

This register controls main function as follows.

7	6	5	4	3	2	1	0
DON'T CARE		**GL**	**OV**	**BL**	**VIDEO MODE**		

Bit 7:6 Don't Care. These Bits are permanently set to logic 0

Bit 5 Genlock control (GL)
This Bit controls genlock On/Off. When the genlock is on, sub-carrier is aligned by the horizontal sync for every four or eight fields.
0: On
1: Off

Bit 4 Override control (OV)
This Bit switches the video mode select source.
0: Mode pins are selected
1: Mode register Bits are selected

Bit 3 Blank Level control (BL)
This Bit switches are the black setup level
0: Black level is 7.5 IRE
1: Black level is 0 IRE

Bit 2:0 Video Mode select
These Bits switch the video mode when (OV) is 1.
000: NTSC CCIR
001: NTSC Square Pixel
010: NTSC 4Fsc
100: PAL CCIR
101: PAL Square pixel

Closed Captioning Registers

Closed Captioning Enable Register

Read/Write Address: 61h
Power-on Default: 00h

This register controls the closed captioning function On/Off as follows. If this function is enabled and a new data is not written (the field status is 1), a null data (80 hex) will be output.

7	6	5	4	3	2	1	0
DON'T CARE						**CCE**	

Bit 7:2 Don't Care. These Bits are permanently set to logic 0

Bit 1:0 Closed captioning enable (CCE)
These Bits control the closed captioning On/Off for each field
00: Disable
01: Enable Odd field only
10: Enable Even field only
11: Enable both fields

Closed Captioning Line Number Register

Read/Write Address: 62h
Power-on Default: 11h

This register controls closed captioning line number as follows:

7	6	5	4	3	2	1	0
DON'T CARE			**CLOSED CAPTIONING LINE NUMBER**				

Bit 7:5 Don't Care. These Bits are permanently set to logic 0

Bit 4:0 Closed Captioning Line Number Select
These Bits set the line number for the closed captioning data.
For NTSC mode, the actual line number will be CCL + 4 and CCL +263 +4
For PAL mode, the actual line number will be CCL +1 and CCL + 313+1

Closed Captioning 1st and 2nd byte Data for Odd Field

Read/Write Address: 63h
Power-on Default: 00h

7	6	5	4	3	2	1	0
CLOSED CAPTIONING 1st BYTE ODD FIELD							

Bit 7:0 Closed Captioning 1st Byte Odd Field

Read/Write Address: 64h
Power-on Default: 00h

7	6	5	4	3	2	1	0
CLOSED CAPTIONING 2nd BYTE ODD FIELD							

Bit 7:0 Closed Captioning 2nd Byte Odd Field

The value at Closed Captioning 1st byte will be output as a 1st closed captioning data of the odd filed, and the value at Closed Captioning 2nd byte will be output as a 2nd one. When one of these bytes is written, the odd status Bit OST will be cleared.

Closed Captioning 1st and 2nd byte Data for Even Field

Read/Write Address: 65h
Power-on Default: 00h

7	6	5	4	3	2	1	0
CLOSED CAPTIONING 1st BYTE EVEN FIELD							

Bit 7:0 Closed Captioning 1st Byte Even Field

Read/Write Address: 66h
Power-on Default: 00h

7	6	5	4	3	2	1	0
CLOSED CAPTIONING 2nd BYTE EVEN FIELD							

Bit 7:0 Closed Captioning 2nd Byte Even Field

The value at Closed Captioning 1st byte will be output as a 1st closed captioning data of the even filed, and the value at Closed Captioning 2nd byte will be output as a 2nd one. When one of these bytes is written, the even status Bit EST will be cleared.

Closed Captioning Status Register

Read Only Address: 67h
Power-on Default: 03h

This register shows the closed captioning status of each field. If these Bits are set to 1, existed data was sent out, and suitable for writing a new data to each closed captioning data registers. These Bits are cleared on new data writing for each field

7	6	5	4	3	2	1	0
DON'T CARE						**OST**	**EST**

Bit 7:2 Don't Care. These Bits are permanently set to logic 0

Bit 1 Closed Captioning Odd filed status (OST)
This Bit shows the odd field status. When set to 1, the data was sent out.
0: The data is not sent
1: The data is sent and ready for writing next data

Bit 0 Closed Captioning Even Field Status (EST)
This Bit shows the even field status. When set to 1, the data was sent out.
0: The data is not sent
1: The data was sent and ready for writing next data.

Chapter 27: 3D Registers

Table 30: 3D Registers

ADDR	REGISTER NAME	COMMENT
100	Device 0	
104	Primitive Type	
108	ZW_Reg	
10C	Stencil_Reg	
110	Z_Init_Value	
114	Pixel_Reg	
118	Texture_factor	
11C	Fog Color	
120	FB_ZB_Stride	
124	Z Base Address	In QDW unit
128	3D Display Address	3D Display Address
12C	DrawBufferBaseAddr	In QDW (128-bit)
130	Clip Top_Left	
134	Clip Bottom_Right	
138	Window Size	
13C	ZW Norm_1	Wnear for W buf;
140	ZW Norm_2	(2^n - 1)/ (Wfar - Wnear), n=16 scale value when in Z buf
144	Fog Norm_1	W1
148	Fog Norm_2	255/(W2 - W1)
150		
154		
158		
15C		
160	*Text0_Bump_EnvReg	
164	Text0_Bump_EnvMat	
168	Text0_Border_Color	
16C	Text0 Color Key1	
170	Text0 Color Key2	
174	Text0_Blend_Reg	
178	T0_Lod_TextID	
17C	Text0_Register	
180	T0_Lvl0_Base	[31] AGP [30] Flush Cache [24:0] in 128_byte
184	T0_Lvl1_Base	
188	T0_Lvl2_Base	
18C	T0_Lvl3_Base	
190	T0_Lvl4_Base	
194	T0_Lvl5_Base	
198	T0_Lvl6_Base	
19C	T0_Lvl7_Base	
1A0	T0_Lvl8_Base	
1A4	T0_Lvl9_Base	
1A8	T0_Lvl10_Base	
1AC		
1B0	Text1_Bump_EnvReg	
1B4	Text1_Bump_EnvMat	
1B8	Text1_Border_Color	
1BC	Text1 Color Key1	
1C0	Text1 Color Key2	
1C4	Text1_Blend_Reg	
1C8	T1_Lod_TextID	
1CC	Text1_Register	
1D0	T1_LVl0_Base	[31] AGP [30] Flush Cache
1D4	T1_LVl1_Base	
1D8	T1_LVl2_Base	

ADDR	REGISTER NAME	COMMENT
1DC	T1_LVl3_Base	
1E0	T1_LVl4_Base	
1E4	T1_LVl5_Base	
1E8	T1_LVl6_Base	
1EC	T1_LVl7_Base	
1F0	T1_LVl8_Base	
1F4	T1_LVl9_Base	
1F8	T1_LVl0_Base	
1FC		

Table 1: Vertex Registers

ADDR	BIT_[31:0]	VERTEX 0 REGISTER		ADDR	BIT_[31:0]	VERTEX 1 REGISTER	COMMENTS
400	32	X0		500	32	X1	IEEE Floating point
404	32	Y0		504	32	Y1	"
408	32	Z0		508	32	Z1	"
40C	32	W0 Perspective Correction		50C	32	W1 Perspective Correction	"
410	32	Diffuse Color		510	32	Diffuse Color	ARGB8888
414	32	Specular Color		514	32	Specular Color	ARGB8888
418	32	U0_1st		518	32	U0_1st	IEEE floating point
41C	32	V0_1st		51C	32	V0_1st	"
420	32	U0_2nd		520	32	U0_2nd	"
424	32	V0_2nd		524	32	V0_2nd	"
458	1	Go at [0]		558	1	Go at [0]	

ADDR	BIT_[31:0]	VERTEX 2 REGISTER	COMMENTS
600	32	X0	IEEE Floating point
604	32	Y0	"
608	32	Z0	"
60C	32	W0 Perspective Correction	"
610	32	Diffuse Color	ARGB8888
614	32	Specular Color	ARGB8888
618	32	U0_1st	IEEE floating point
61C	32	V0_1st	"
620	32	U0_2nd	"
624	32	V0_2nd	"
658	1	Go at [0]	

Table 31: Global Fog Look up Table (700-7FF)

GLOBAL FOG FACTOR - LOOK UP TABLE	
DPR700[31:0]	Fog3210
DPR704[31:0]	Fog7654
……..	
DPR7FC[31:0]	Last 4 fogs (FF,FE,FD & FC)

Table 32: 3D Registers Quick Reference

Device 0 Register (100)

Write Only Address: DP_Base + 100h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														**EPC**	**RPC**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRT	**RESERVED**		**SRAM**	**PE**	**FBE**	**ZCXY**	**ZCWB**	**ZTE**	**DBTE**	**CRT**	**PDA**	**PE**	**ZMAP**	**ZIE**	**ZCF**

Bit 31:18 Reserved

Bit 17 Enable performance counter (EPC)

Bit 16 Reset performance counter (RPC)

Bit 15 Select CRT VSYNC for flip control (CRT)
0 = Select LCD VSync (default)
1 = Select CRT VSync

Bit 14:13 Reserved

Bit 12 Enable internal SRAM self test. Status report at Device 1 status register

Bit 11 PE cache write back ahead enable

Bit 10 Flip block enable (FBE)

Bit 9 Z cache XY shift 4 bits enable (ZCXY)

Bit 8 Z cache write back ahead enable (ZCWB)

Bit 7 Z tile enable (ZTE)

Bit 6 Draw buffer tile enable (DBTE)

Bit 5 CRT display address use 3D display address (CRT)

Bit 4 Panel display address use 3D display address (PDA)

Bit 3 PE cache flush (texture cache flush = → move to texture base bit [30]) (PE)

Bit 2 Z map bypass (ZMAP)
0 = Normal, zero cycle z op
1 = Bypass

Bit 1 Z initial enable (ZIE)

Bit 0 Z cache flush (ZCF)

Primitive Register (104)

Write Only Address: DP_Base + 104h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			**EDGE FLAG**			**DL**	**VERTEX TYPE**			**PRIMITIVE TYPE**				**CULL TYPE**	

Bit 31:13 Reserved

Bit 12:10 *Edge Flag
000: no draw
001: V0
010: V1
100: V2
111: All
Else: Reserved

Bit 9 *Draw Line (DL)
0: X Major
1: Y Major

Bit 8:6 *Vertex Buffer Type

Bit 5:2 *Primitive Type

Bit 1:0 Cull Type
00: No Cull
01: CW
10: CCW
11: Reserved

ZW_Reg (108)

Write Only Address: DP_Base + 108h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											**Z BIAS**				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STENCIL WRITE MASK								**WB**	**ZE**	**DBF**		**ZCE**	**ZCF**		

Bit 31:21 Reserved

Bit 20:16 Z Bias

Bit 15:8 Stencil Write Mask

Bit 7 Use W Buffer (WB)
0: use Z buffer
1: use W buffer

Bit 6 Z Update Enable (ZE)

Bit 5:4 Depth Buffer Format (DBF)
00: 16 bit Z only, no stencil
01: 32_bit, 24 bits Z and 8 bits stencil

Bit 3 Z Compare Enable (ZCE)
0: Disable Z
1: Enable Z compare

Bit 2:0 Z Compare Function (ZCF)
000:Never
001:Less
010:Equal
011:LessEqual
100:Greater
101:Not Equal
110:GreaterEqual
111:Always

Note: Z supports 1) 16_bit fixed point without stencil. 2) 24_bit fixed point with 8_bit stencil.
W supports 1) 16_bit fixed point wo stencil. 2) 24_bit floating point with 8_bit stencil.

Stencil Register (10C)

Write Only Address: DP_Base + 10Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STENCIL MASK								**STENCIL REFERENCE REGISTER**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**STENCIL PASS**			**R**	**STENCIL Z FAIL**			**R**	**STENCIL FAIL**			**SCE**	**SCF**		

Bit 31:24 Stencil Mask

Bit 23:16 Stencil Reference Register

Bit 15 Reserved (R)

Bit 14:12 Stencil Pass Operations
000: Keep
001: Zero
010: Replace
011: Increment saturate
100: Decrement saturate
101: Invert
110: Increment
111: Decrement

Bit 11 Reserved (R)

Bit 10:8 Stencil Z Fail Operations

Bit 7 Reserved (R)

Bit 6:4 Stencil Fail Operations

Bit 3 Stencil Compare Enable (SCE)

Bit 2:0 Stencil Compare Function (SCF)
000: Never
001: Less
010: Equal
011: Less equal
100: Greater
101: Not equal
110: Greater equal
111:Always

Z/W Initial Value (110)

Write Only Address: DP_Base + 110h
Power-on Default: Undefined

For 24-bit Z fix point

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STENCIL PLANES								**FIX POINT Z**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIX POINT Z															

Bit 31:24 Stencil Planes

Bit 23:0 Fix Point Z

For 16-bit Z fix point

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIXED POINT INITIAL Z VALUE															

Bit 31:16 Reserved

Bit 15:0 Fixed Point Initial Z Value

For 24-bit Floating W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STENCIL PLANES								**FLOATING POINT W**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLOATING POINT W															

Bit 31:24 Stencil Planes

Bit 23:0 Floating Point W (SE8M15)

For 16-bit Fix Point W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIXED POINT W															

Bit 31:16 Reserved

Bit 15:0 Fixed Point W value

Note: Stencil only supported in 24bit Z or W

Pixel Register (114)

Write Only Address: DP_Base + 114h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PROCESS ID				**RESERVED**		**PCE**	**SE**	**FBF**		**SM**		**SOURCE BLENDING**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESTINATION BLENDING				**ABE**	**ALPHA TEST**			**RESERVED**				**ATE**	**DE**	**TFT**	**FE**

Bit 31:28 Process ID

Bit 27:26 Reserved

Bit 25 Perspect Correct Enable (PCE)
When this bit set to 0, Setup Engine will force W = 1.

Bit 24 Specular Enable (SE)

Bit 23:22 Frame Buffer Format (FBF)
00: RGB565
01: ARGB1555
10: ARGB4444
11: ARGB8888

Bit 21:20 Shade Mode (SM)
00: Flat
01: Gouraud
10: Phong
11: Reserved

Bit 19:16 Source Blending Factor

0000	ZERO	0x0
0001	ONE	0x1
0010	SRCCOLOR	0x2
0011	INVSRCCOLOR	0x3
0100	SRCALPHA	0x4
0101	INVSRCALPHA	0x5
0110	DESTALPHA	0x6
0111	INVDESTALPHA	0x7
1000	DESTCOLOR	0x8
1001	INVDESTCOLOR	0x9
1010	SRCALPHASAT	0xA
1011	BOTHSRCALPHA	0xB
1100	BOTHINVSRCALPHA	0xC

Bit 15:12 Destination Blending Factor

Bit 11 Alpha Blend Enable (ABE)

Bit 10:8 Alpha Test Function

000	NEVER	0x0
001	LESS	0x1
010	EQUAL	0x2
011	LESSEQUAL	0x3
100	GREATER	0x4
101	NOTEQUAL	0x5
110	GREATEREQUAL	0x6
111	ALWAYS	0x7

Bit 7:4 Reserved

Bit 3 Alpha Test Enable (ATE)

Bit 2 Dithering Enable (DE)

Bit 1 Table Fog Type (TFT)
0: Vertex Fog
1: Table Fog

Bit 0 Fog Enable (FE)

Texture Factor (118)

Write Only Address: DP_Base + 118h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALPHA								**RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN								**BLUE**							

Bit 31:24 Alpha - to be used in pixel blending

Bit 23:16 Red

Bit 15:8 Green

Bit 7:0 Blue

Fog Color (11C)

Write Only Address: DP_Base + 11Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PROCESS ID				**RESERVED**		**PCE**	**SE**	**FBF**		**SM**		**SOURCE BLENDING**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESTINATION BLENDING				**ABE**	**ALPHA TEST**			**RESERVED**				**ATE**	**DE**	**TFT**	**FE**

Bit 31:24 Alpha Reference Value

Bit 23:0 RGB

FB_ZB Stride Register (120)

Write Only Address: DP_Base + 120h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRAME BUFFER STRIDE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z BUFFER STRIDE															

Bit 31:16 Frame Buffer Stride

Bit 15:0 Z Buffer Stride

Z Base Address (124)

Write Only Address: DP_Base + 124h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS IN QDW															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE ADDRESS IN QDW															

Bit 31:0 Base Address in QDW (128-bit) unit

3D Display Address (128)

Write Only Address: DP_Base + 128h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
3D BASE DISPLAY ADDRESS IN QDW															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3D BASE DISPLAY ADDRESS IN QDW															

Bit 31:0 3D Display Address in QDW (128-bit) unit

Draw Buffer Base Address (12C)

Write Only Address: DP_Base + 12Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DRAW BUFFER BASE ADDRESS IN QDW															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRAW BUFFER BASE ADDRESS IN QDW															

Bit 31:0 Draw Buffer Base Address in QDW (128-bit) unit

Clip Top Left Register (130)

Write Only Address: DP_Base + 130h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLIP TOP REGISTER															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLIP LEFT REGISTER															

Bit 31:16 Clip Top Register

Bit 15:0 Clip Left Register

Clip Bottom Right Register (134)

Write Only Address: DP_Base + 134h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLIP BOTTOM REGISTER															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLIP RIGHT REGISTER															

Bit 31:16 Clip Bottom Register

Bit 15:0 Clip Right Register

Window Size (138)*

Write Only Address: DP_Base + 138h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		**HEIGHT**													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**WIDTH**													

Bit 31:30 Reserved

Bit 29:16 Height

Bit 15:14 Reserved

Bit 13:0 Width

ZW Norm_1 (13C)

Write Only Address: DP_Base + 13Ch
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
32-BIT FLOATING POINT WNEAR IN W BUFFER															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32-BIT FLOATING POINT WNEAR IN W BUFFER															

Bit 31:0 32-bit floating point Wnear in W buffer (internal use unsigned 24-bit float);

ZW Norm_2 (140)

Write Only Address: DP_Base + 140h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZW NORM_2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZW NORM_2															

Bit 31:0 = (2^n - 1)/(Wfar - Wnear) if W buffer
= Z scale when in Z buffer
in floating point

Note: Wnorm = (W - ZW_Norm_1) * ZW_Norm_2;
To make the better resolution in W buffer

Fog Norm_1 (144)

Write Only Address: DP_Base + 144h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W1 IN FLOATING POINT															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W1 IN FLOATING POINT															

Bit 31:0 W1 in floating point

Fog Norm_2 (148)

Write Only Address: DP_Base + 148h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOG NORM_2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOG NORM_2															

Bit 31:0 = 255/(W2 - W1)

Note: Fog_LUT_index = (W - Fog_Norm_1) * (Fog_Norm_2);

Text_Bump_Env (160 & 1B0)

Write Only Address: DP_Base + 160h; DP_Base + 1B0h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															

Bit 31:0 Reserved

Text_Bump_Env_Mat (164 & 1B4)

Write Only Address: DP_Base + 164h; DP_Base + 1B4h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BUMPENVMAT11								**BUMPENVMAT10**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUMPENVMAT01								**BUMPENVMAT00**							

Bit 31:24 BumpEnvMat11

Bit 23:16 BumpEnvMat10

Bit 15:8 BumpEnvMat01

Bit 7:0 BumpEnvMat00

Texture Border Color (168 & 1B8)

Write Only Address: DP_Base + 168h; DP_Base + 1B8h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALPHA								**RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN								**BLUE**							

Bit 31:24 Alpha

Bit 23:16 Red

Bit 15:8 Green

Bit 7:0 Blue

Texture Color Key 1 (16C & 1BC)

Write Only Address: DP_Base + 16C; DP_Base + 1BCh
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALPHA								**RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN								**BLUE**							

Bit 31:24 Alpha

Bit 23:16 Red

Bit 15:8 Green

Bit 7:0 Blue

Texture Color Key 2 (170 & 1C0)

Write Only Address: DP_Base + 170h; DP_Base + 1C0h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALPHA								**RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN								**BLUE**							

Bit 31:24 Alpha

Bit 23:16 Red

Bit 15:8 Green

Bit 7:0 Blue

Texture Blending Register (174 & 1C4)

Write Only Address: DP_Base + 174h; DP_Base + 1C4h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	**ACM**		**ACS**			**ACMF**		**ACS1**			**COLOR BLEND**				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**AMS**		**AAS**			**AMS1**		**AAS1**			**ALPHA BLEND OPERATION**				

Bit 31 Reserved (R)

Bit 30:29 Argument2 Color Modifier selection; Second set of argument selection (ACM)
- 00 No modify
- 01 Color Replicate
- 10 Complement
- 11 Reserved

Bit 28:26 Argument 2 Color selection (ACS)
- 000 Diffuse color
- 001 Previous stage output
- 010 Texture
- 011 Texture factor from Reg 118
- 100 Specular
- else Reserved

Bit 25:24 Argument1 Color Modifier selection; First set of argument selection (ACMF)

Bit 23:21 Argument1 Color selection (ACS1)

Bit 20:16 Color Blend Operation

00000	Disable	
00001	Select Argument1	
00010	Select Argument2	
00011	Multiply;	Arg1 * Arg2
00100	Multiply 2X;	(Arg1 * Agr2) * 2
00101	Multiply 4X;	(Arg1 * Arg2) * 4
00110	ADD;	Arg1 + Arg2
00111	Add Signed;	Arg1 + Arg2 - 0.5
01000	Add Signed 2X	(arg1 + Arg2 - 0.5) << 1

01001	Subtract;	Arg1 - Arg2
01010	Add Smooth	Arg1 + Arg2 - Arg1*Agr2
01011	Blend Diffuse Alpha;	Arg1*AlphaD + Arg2*(1 - AlphaD)
01100	Blend Texture Alpha;	Blend the arguments with texture alpha
01110	Blend Factor Alpha;	Blend the arguments with factor (morphing) alpha
01111	Blend Texture PM;	Arg1 + Arg2*(1 - Alpha)
10000	Pre-modulate;	Modulate this texture stage with next texture stage
10001	Modulate Alpha Add Color;	Arg1RGB + Arg1A * Arg2RGB
10010	Modulate Color Add Alpha	Arg1RGB * Arg2RGB + Arg1A
10011	Modulate Inverted Alpha Add Color;	(1 - Arg1A)*Arg2RGB + Arg1RGB
10100	Modulate Inverted Color Add Alpha;	(1 - Arg1RGB)*Arg2RGB + Arg1A
10101	Bump Environment Map Without Luminance	
10110	Bump Environment Map With Luminance	
10111	Dot Product 3;	Arg1R*Arg2R + Arg1G*Agr2G + Arg1B*Arg2B

Bit 15 Reserved (R)

Bit 14:13 Argument2 Alpha Modifier selection (AMS)

Bit 12:10 Argument2 Alpha selection (AAS)

Bit 9:8 Argument1 Alpha Modifier selection (AMS1)

Bit 7:5 Argument1 Alpha selection (AAS1)

Bit 4:0 Alpha Blend Operation

00000	Disable	
00001	Select Argument1	
00010	Select Argument2	
00011	Multiply;	Arg1 * Arg2
00100	Multiply 2X;	(Arg1 * Agr2) * 2
00101	Multiply 4X;	(Arg1 * Arg2) * 4
00110	ADD;	Arg1 + Arg2
00111	Add Signed;	Arg1 + Arg2 - 0.5
01000	Add Signed 2X;	(arg1 + Arg2 - 0.5) << 1
01001	Subtract	Arg1 - Arg2
01010	Add Smooth	Arg1 + Arg2 - Arg1*Agr2
01011	Blend Diffuse Alpha;	Arg1*AlphaD + Arg2*(1 - AlphaD)
01100	Blend Texture Alpha;	Blend the arguments with texture alpha
01110	Blend Factor Alpha;	Blend the arguments with factor (morphing) alpha
01111	Blend Texture PM;	Arg1 + Arg2*(1 - Alpha)
10000	Pre-modulate;	$Arg1_A$
10001	Modulate Alpha Add Color;	$Alpha_D$
10010	Modulate Color Add Alpha	$Alpha_D$
10011	Modulate Inverted Alpha Add Color;	$Alpha_D$
10100	Modulate Inverted Color Add Alpha;	$Alpha_D$
10101	Reserved	
10110	Reserved	
10111	Dot Product 3;	$Alpha_D$

Text0_Lod_TextID (178) & Text1_Lod_TextID (1C8)

Write Only Address: DP_Base + 178h; DP_Base + 1C8
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**LOD BIAS (S + 4.5)**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEXTURE ID								**MAXIMUM TEXTURE**				**MINIMUM TEXTURE**			

Bit 31:26 Reserved

Bit 25:16 Lod Bias (S + 4.5)

Bit 15:8 Texture ID

Bit 7:4 Maximum Texture Level - Start Level (Base Level in OpenGL)
When LOD < Maximum Texture Level, LOD = Maximum Texture Level.

Bit 3:0 Minimum Texture Level - Clamp Level (called Max Level in OpenGL)

Text0_Reg (17C) & Text1_Reg (1CC)

Write Only Address: DP_Base + 17Ch; DP_Base + 1CC
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CKE	**CKB**	**RESERVED**			**ME**	**MF**	**MIN FILTER**		**MAG FILTER**			**TEXTURE COLOR FORMAT**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE V				**SIZE U**				**PS**	**AMV**		**AMU**		**WV**	**WU**	**TE**

Bit 31 Color Key Enable (CKE)

Bit 30 Color Key Blend Enable (CKB)

Bit 29:27 Reserved

Bit 26 Mipmap Enable (ME)

Bit 25 Mipmap Filter
0: point - select one map
1: linear - linear between map

Bit 24:23 Minification Filter
00: point

01: linear
10: Anisotropic
11: reserved

Bit 22:20 Magnification Filter
000: point
001: linear
010: anisotropic
011 to 111: reserved

Bit 19:16 Texture Color Format
0000: ARGB8888
0001: ARGB4444
0010: ARGB1555
0011: RGB565
0100: Reserved
0101: DXT1
0110: DXT2
0111: DXT3
1000: DXT4
1001: DXT5
Else: reserved

Bit 15:12 Size V; 2^V

Bit 11:8 Size U; 2^U

Bit 7 Point Sample Floor (PS)

Bit 6:5 Address Mode V (AMV)
00: border color
01: wrap
10: clamp
11: mirror

Bit 4:3 Address Mode U (AMU)
00: border color
01: wrap
10: clamp
11: mirror

Bit 2 Wrap V (WV)

Bit 1 Wrap U (WU)

Bit 0 Texture0 Enable (TE)

Text0_Texture Level 0 Base Address (180) & Text1_Texture Level 0 Base Address(1D0)

Write Only Address: DP_Base + 180h; DP_Base + 1D0h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AGP	**FC**	**RESERVED**					**BASE ADDRESS**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE ADDRESS															

Bit 31 AGP/Local (AGP)
0: Local memory
1: AGP memory

Bit 30 Flush Cache (FC)
0: Normal operation
1: Invalidate the texture in the cache.

Note: when set flush cache, it will generate an one clock pulse to flush the cache, and reset this bit back to 0 after the clock pulse.

Bit 29:25 Reserved

Bit 24:0 Base address in unit of 128_byte

Texture Level 1 Base Address (184 & 1D4)

Write Only Address: DP_Base + 184h; DP_Base + 1D4h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AGP	**RESERVED**						**BASE ADDRESS**								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE ADDRESS															

Bit 31 AGP/Local (AGP)
0 = Word memory
1 = AGP memory

Bit 30:25 Reserved

Bit 24:0 Base address in unit of 128-byte

Texture Level 2 Base Address (188 & 1D8)

Write Only Address: DP_Base + 188h; DP_Base + 1D8h
Power-on Default: Undefined

Description same as *Texture Level 1 Base Address (184 & 1D4)*.

Texture Level 3 Base Address (18C & 1DC)

Write Only Address: DP_Base + 18Ch; DP_Base + 1DCh
Power-on Default: Undefined

Description same as *Texture Level 1 Base Address (184 & 1D4)*.

Texture Level 4 Base Address (190 & 1E0)

Write Only Address: DP_Base + 190h; DP_Base + 1E0h
Power-on Default: Undefined

Description same as *Texture Level 1 Base Address (184 & 1D4)*.

Texture Level 5 Base Address (194 & 1E4)

Write Only Address: DP_Base + 194h; DP_Base + 1E4h
Power-on Default: Undefined

Description same as *Texture Level 1 Base Address (184 & 1D4)*.

Texture Level 6 Base Address (198 & 1E8)

Write Only Address: DP_Base + 198h; DP_Base + 1E8h
Power-on Default: Undefined

Description same as *Texture Level 1 Base Address (184 & 1D4)*.

Texture Level 7 Base Address (19C & 1EC)

Write Only Address: DP_Base + 19Ch; DP_Base + 1ECh
Power-on Default: Undefined

Description same as *Texture Level 1 Base Address (184 & 1D4)*.

Texture Level 8 Base Address (1A0& 1F0)

Write Only Address: DP_Base + 1A0h; DP_Base + 1F0h
Power-on Default: Undefined

Description same as *Texture Level 1 Base Address (184 & 1D4)*.

Texture Level 9 Base Address (1A4 & 1F4)

Write Only Address: DP_Base + 1A4h; DP_Base + 1F4h
Power-on Default: Undefined

Description same as *Texture Level 1 Base Address (184 & 1D4)*.

Chapter 28: 2D3D DMA Registers

2D 3D Address Space Arrangement:
000 - 0FF : 2D & DMA Shadow registers
100 - 3FF : 3D Registers
400 - 4FF : Vertex 0 registers
500 - 5FF : Vertex 1 registers
600 - 6FF : Vertex 2 registers
700 - 7FF : Global Fog registers 256X8 (=64x32)
10000 - 8FFFF : DMA Slave Write Port

Addr	Bit_[31:0]	2D
0	13+14	Xs_K1,Ys_K2
4	13+14	Xd,Yd
8	13+14	DimX,DimY_ET
C	16+16	Cmd_ctl,ROP
10	13+13	D_pitch,S_pitch
14	32	Fgc
18	24	Bgc
1C	15+12	ps_xy,stretch_h
20	24	Compare_color
24	24	CC_mask
28	8+16	Bytemask, Bitmask
2C	13+14	Clip_T,Clip_L
30	13+13	Clip_B,Clip_R
34	32	mono_pattern_low
38	32	Mono_pattrn_high
3C	13+13	D_xywid,S_xywid
40	1+24	S_base

Addr	Bit_[31:0]	DMA Shadow Reg	Comments
80	32	DMA Start Address	Shared with 3000
84	32	Write Back Address	Shared with 3004
88	32	Total Transfer Size	Shared with 3008
8C	32	DMA Address Mask	For Circular DMA Buffer 300C Addr&!Mask | Start_addr&Mask
90	28	Sleep Counter	Loop Header activate DMA when count reach 0
94	32		
98	32		
9C	32		
A0	32	AGP Write Back Data Register	Write Back Data_[31:0] Read Thru 3020
A4	32		" WB Data_[63:32] - R3024
A8	32		" WB Data_[95:64] - R3028
AC	32		" WB Data_[127:96] - R302C
B0	32		
B4	32		
B8	32		
BC	32		
C0			

Addr	Bit_[31:0]	2D
44	1+24	D_base
48	8	Alpha for Bitblt
4C		
50		
54		
58		
5C		
60		
64		
68		
6C		
70		
74		
78		

Addr	Bit_[31:0]	DMA Shadow Reg	Comments
C4			
C8			
CC			
D0			
D4			
D8			
DC			
E0			
E4			
E8			
EC			
F0			
F4			
F8			
FC			

Address	Bit	Function	Comment
3000	31:0	DMA Start Address [27:0] in Quad Dword unit	Share with 2D reg_80
3004	31:0	Write Back Address [27:0] in Quad Dword unit	With data at Reg_A0
3008	31:0	Total Transfer Size in QDWORD	[21:0]: size in Qdword
[27:26]: Write Back Req			
[30:28]: Req Water Mark			
[31]: activate DMA			
300C	27:0	DMA Address Mask	AGP_addr = addr&mask | start_addr&!mask;
3010	31:0	Sleep Counter	Read Only, Write Thru 90
301C	31:0	2nd DMA AGP Start Address	Read Only, Write Thru 9C
3020	31:0	Write Back Data [31:0]	
3024	31:0	" [63:32]	
3028	31:0	" [95:64]	
302C	31:0	" [127:96]	
3030	31:0		
3034	31:0		
3038	31:0		

Address	Bit	Function	Comment
303C	31:0		
3040	31:0		
3044	31:0		
3048	31:0		
304C	31:0		
3050	31:0		

Table 33: Summary of 2D 3D DMA Registers

DMA Start Address (3000)

Read/Write Address: PCI_Base + 3000h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				**DMA START ADDRESS**											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA START ADDRESS															

Bit 31:28 Reserved

Bit 27:0 DMA start address in quad double word as a unit

DMA Write Back Address (3004)

Read/Write Address: PCI_Base + 3004h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				**DMA WRITE BACK**											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA WRITE BACK															

Bit 31:28 Reserved

Bit 27:0 DMA write back address in quad double word as a unit

Total Transfer Size (3008)

Read/Write Address: PCI_Base + 3008h
Power-on Default: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMA	**RESERVED**			**WB**		**RESERVED**				**TOTAL TRANSFER SIZE IN QUAD DWORD**					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOTAL TRANSFER SIZE IN QUAD DWORD															

Bit 31 DMA
1 = Activate DMA
0 = DMA IDLE - after DMA complete, this bit will be reset to 0 by hardware

Bit 30:28 Reserved

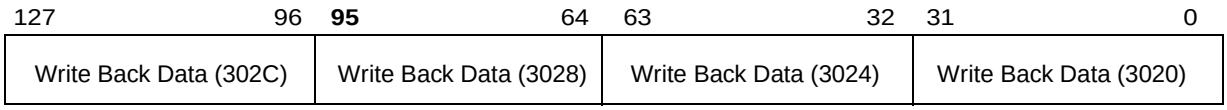
Bit 27:26 Write Back (WB)
00 = No Write Back
01 = Reserved
1x = Write Back 128-bit "

Bit 25:22 Reserved

Bit 21:0 Total Transfer Size in Quad Dword. Total could transfer 64MB DMA data.

Write Back Data (3020 - 302C)

Read Only Address:
Power-on Default:



Bit 127:96 Write Back Data (302C)

Bit 95:64 Write Back Data (3028)

Bit 63:32 Write Back Data (3024)

Bit 31:0 Write Back Data (3020)

Performance Monitoring Registers (3054 - 3060) - internal use only

Read Only Address: PCI_Base + 3054h...3060h
Power-on Default: Undefined

Control by programming the Device0 register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														**EPC**	**RPC**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															

Bit 31:18 Reserved

Bit 17 Device0: Enable the performance count. (EPC)

Bit 16 Device0: Reset the performance counter (RPC)

Bit 15:0 Reserved

Device 1 Status (3064) - Internal use only

Read Only Address: PCI_Base + 3064h
Power-on Default: Undefined

Control by programming the Device0 register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												**ZCM**	**ZC**	**PC**	**SB**

Bit 31:4 Reserved

Bit 3 Zero Cycle Map (ZCM)
0: Zero Cycle Map Test fail or Not Test
1: Zero Cycle Map SRAM test pass

Bit 2 Z Cache (ZC)
0: Z Cache Test fail or Not Test
1: Z Cache SRAM test pass

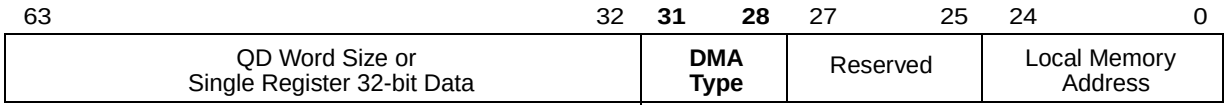
Bit 1 Pixel Cache (PC)
0: Pixel Cache Test fail or Not Test
1: Pixel Cache SRAM test pass

Bit 0 Status Bits (SB)
0: Status bits 14C_[6:1] invalid
1: Status bits 14C_[6:1] valid

Note: To initiate the Internal SRAM self test by program Device0(100)_[12] to 1
Bit [3:0] Valid only when 100_[12] = 1

DMA Data Header Specification

Generic Format



QDWord Size [63:32] - total transfer size in Quad Dword or 32 register data

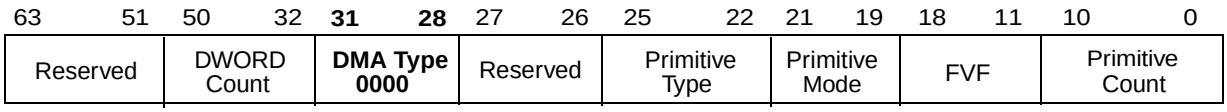
Bit 31:28 **DMA Type**
0000: 3D Primitive Data

0001: 2D3D Command - Consecutive registers with 64-bit header and pairs of DWORD registers
0010: Texture Data - host data loading to local memory linearly
0011: Device Status Test Command
0100: Loading of Single Register
0101: Reserved
0110: Reserved
0111: 2D Hbltw Data
1000: Write Back Header
1110: Loop DMA with Sleep Counter DMA Activation
1111: Dummy Header - will be trash out at parser
Else: Reserved for future expansion

Bit 27:25 Reserved

Bit 24:0 Local Memory Address - each unit is 128-bit address space in local memory

Primitive Data Header (Type=0000)



DWORD Count [50:32]: Total number of Dword count for all vertex registers follow this header

Bit 25:22 Primitive Type
4'b0000: PRIMTYPE_POINTS
4'b0001: PRIMTYPE_INDEXEDLINELIST
4'b0010: PRIMTYPE_LINELIST
4'b0011: PRIMTYPE_LINESTRIP
4'b0100: PRIMTYPE_INDEXEDLINESTRIP
4'b0101: PRIMTYPE_LINELIST_IMM
4'b1000: PRIMTYPE_TRIANGLELIST
4'b1001: PRIMTYPE_INDEXEDTRIANGLELIST
4'b1010: PRIMTYPE_INDEXEDTRIANGLELIST2
4'b1011: PRIMTYPE_TRIANGLESTRIP
4'b1100: PRIMTYPE_INDEXEDTRIANGLESTRIP
4'b1101: PRIMTYPE_TRIANGLEFAN
4'b1110: PRIMTYPE_INDEXEDTRIANGLEFAN
4'b1111: PRIMTYPE_TRIANGLEFAN_IMM

Bit 21:19 Primitive Mode
3'b000: PRIMMODE_IMMEDIATE
3'b001: PRIMMODE_VTX_BUFFER
3'b010: PRIMMODE_VTX_INDEXBUF
3'b011: PRIMMODE_INDEX_BUF

Bit 18 FVF Reserved - XYZ always on

Bit 17 0 = rhW off(not included in vertex file)
1 = rhW on

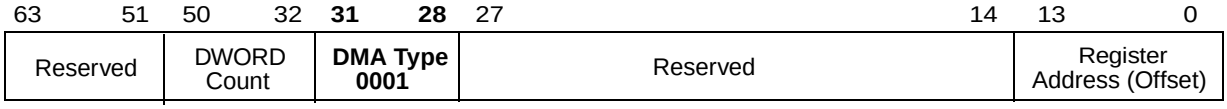
Bit 16 0 Diffuse off(not included in vertex file)
1 Diffuse on

Bit 15 0 = Specular off(not included in vertex file)
1 = Specular on

Bit 14:11 Number of Textures (UnVn)

Bit 10:0 Primitive Count: Number of Triangles (no function in hardware)

2D3D Command Pair (Type=0001)

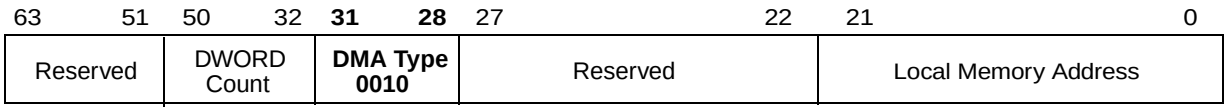


Consecutive registers pair.

64-bit Register data followed this header will be loaded into hardware in order of Low Dword then High Dword.

DWORD Count does not include header.

Texture Data (Type=0010)

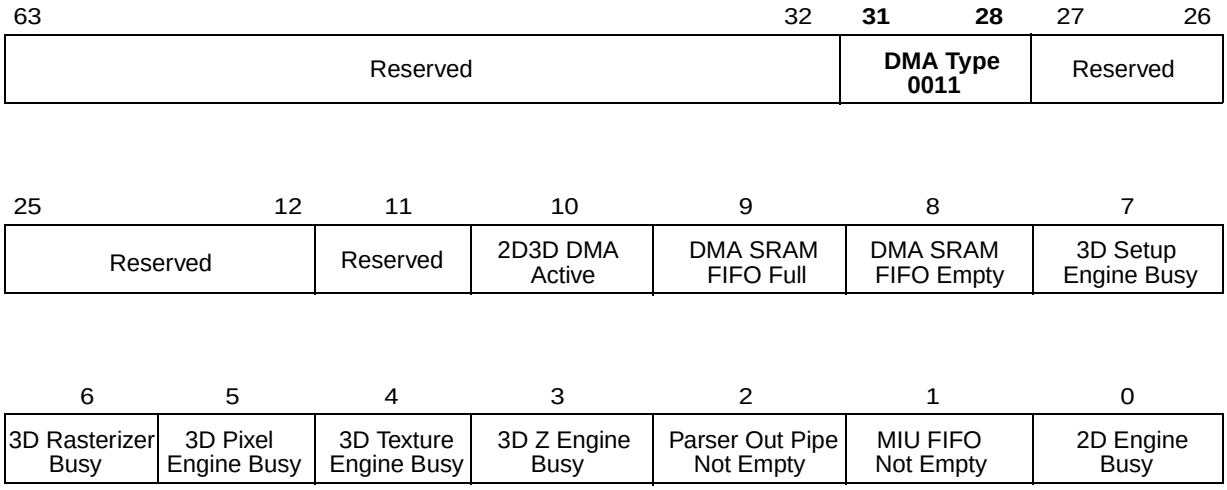


Host data loading to local memory linearly

Local Memory Address 22 bits at Quad DWORD as unit, could address up to 64MB.

QDWord Size 19 bits could transfer up to 8MB -1 size in a DMA buffer.

Status Test Register (Type=0011)



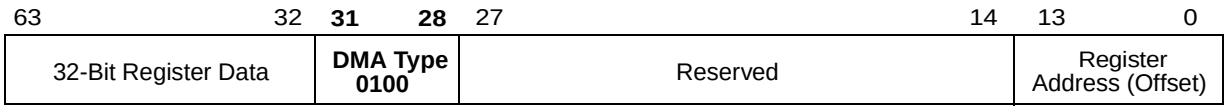
(Memory Map System Control register xxxx for slave mode)

DMA FIFO Not Empty	"1" if DMA Queue FIFO is not empty.
DMA Busy	"1" if DMA Queue is active.
3D Engine FIFO Not Empty	"1" if 3D Engine FIFO is not empty.
3D Setup Engine Busy	"1" if 3D Setup Engine is busy.
MIU FIFO Not Empty	"1" if 2D Engine FIFO is not empty.
2D Engine Busy	"1" if 2D Engine is busy.

Whenever parsing logic works on Status Test Command, it will stay in hardware test loop if any of the test bit is1 and the corresponding hardware status also true. This is a hardware status waiting for synchronization control.

- Miu Fifo Not Empty: All 2D, and 3D Local memory interface through this fifo.
- Parser Out Pipe Not Empty: True whenever valid register data or valid direct 64 bit data is true.
- DMA SRAM FIFO Empty: This Fifo share for slave and master mode. And the Parser is execute at output of this FIFO. So this bit should not be checked at DMA fifo. It was design for slave mode status polling.

Loading Of Single Register (Type=0100)

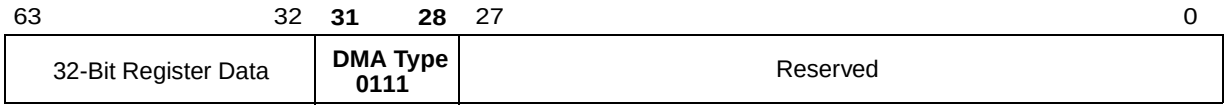


For both 2D & 3D registers.

Only support load 32-bit (2 16-bit 2D registers pair). No single 16-bit register loading.

Register Address (Offset) at Dword address unit.

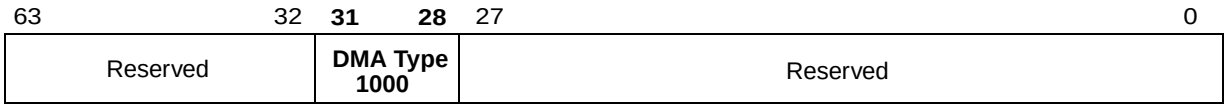
2D HbltW Data (Type=0111)



Tie with 2D Engine

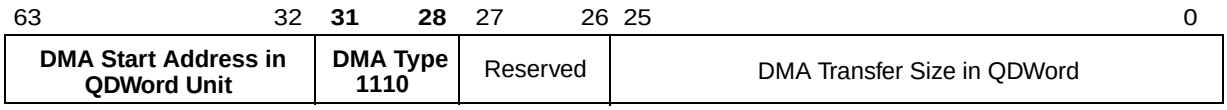
Follow the header is hbltw data. Before execute this header, 2D Hbltw registers should be setup - insert the 2D command before this header.

Write Back Header (Type=1000)



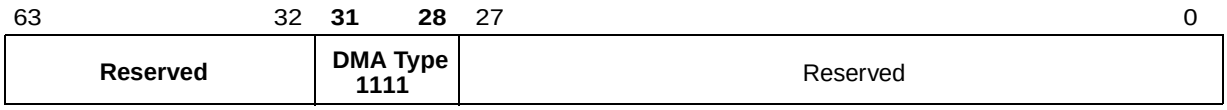
When the DMA Parser executes this header, it will generate a write back master request to the AGP address (specified at Register 3004) with a 128-bit data (specified at registers 3020 - 302C).

Loop DMA Activated with Sleep Counter (Type=1110)



When Hardware Parser detects this header, it will trash all the data in the DMA fifo and reset the DMA to Timed Sleep mode

Dummy Header (Type=1111)



Use this 64-bit Dummy Header to make the total DMA file size to become an integer number of 128-bits (Quad Double World).

Chapter 29: Electrical Specifications

Absolute Maximum Ratings

Table 34: Absolute Maximum Ratings

Specification	Maximum rating
Ambient temperature (TA)	0° C to 75° C
Storage temperature	-40° C to 125° C
Voltage on I/O pins with respect to VSS	- 0.5V to VDD + 5%
Operating power dissipation	TBD
Core DC Power supply voltage	2.5V ± 5%

DC Specifications

Table 35: Digital DC Specification

Name	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-	0.8	V	
V_{IH}	Input High Voltage	2.0	-	V	
V_{OL}	Output Low Voltage	-	0.4	V	
V_{OH}	Output High Voltage	2.4	VDD+0.5	V	
I_{OZL}	Output Tri-state Current	-	10	µA	
I_{OZH}	Output Tri-state Current	-	10	µA	
I_{OZL} (Pull up pins)	Output Tri-state Current	-130	-10	µA	
I_{OZH} (Pull up pins)	Output Tri-state Current	-	10	µA	
I_{OZL} (Pull down pins)	Output Tri-state Current	-	10	µA	
I_{OZH} (Pull down pins)	Output Tri-state Current	10	130	µA	
C_{IN}	Input Capacitance		TBD	pF	
C_{OUT}	Output Capacitance		TBD	pF	
I_{CC}	Power Supply Current		TBD	mA	

Table 36: RAMDAC Characteristics

Parameter	Min	Typical	Max	Unit
Resolution Each DAC	-	8		Bits
LSB Size	-	54.7		µA
Output Full Scale Current	-	14.0		mA
Integral Linearity Error	0	-	1	LSB
Differential Linearity Error	0	-	1	LSB
DAC to DAC Mismatch	0	-	5%	
Power Supply Rejection Ratio	0	-	0.5	% /% AVDD
Output Compliance	0	-	1.2	V
Output Capacitance	-	-	10	pF
Glitch Energy	-	30	-	pV-Sec

Table 37: RAMDAC/Clock Synthesizer DC Specifications

Symbol	Parameter	Min	Typical	Max	Unit
AVDD	DAC Supply Voltage	3.17	3.3	3.47	V
CVDD	PLL Supply Voltage	3.17	3.3	3.47	V
VREF	Internal DAC voltage reference	1.1	1.235	1.35	V

AC Specifications

Table 38: RAMDAC AC Specifications

Parameter	Typical	Max	Unit	Notes
DAC Output Delay	3		ns	1
DAC Output Rise/Fall Time	3		ns	2
DAC Output Setting Time	15		ns	
DAC-to-DAC Output Skew	2	15	ns	3

Notes:
1. Measured from the 50% of VCLK to the 50% point of full scale transaction
2. Measured from 10% to 90% full scale
3. With DAC outputs equally loaded

Parameter	I_{OUT} (mA)	V_{OUT} (V)	BLANK	Input Data
White	**14.0**	**0.7**	**1**	**FFh**
Data	**Data**	**Data**	**1**	**Data**
Black	**0**	**0**	**1**	**00h**
~BLANK	**0**	**0**	**0**	**Don't Care**

Notes:
- Condition for V_{OUT} is a 50 Ohm terminated load, use of the internal VREF and RFSC = 1.2 K Ohms.

AC Timing Specifications

Power On Reset

Table 39: Power-on Reset and Configuration Reset Timing

Symbol	Parameter	Min	Max	Unit
t1	Reset active from VCC stable	5	-	ms
t2	Reset active from external oscillator stable	0	-	
t3	Reset active from ~PWRDN signal stable	2	-	ms
t4	Internal Power On ~RESET from VCC stable	-	200	ns
t5	External ~RESET to internal Power On ~RESET inactive	-	20	ms
t6	External ~RESET Pulse Width		-	ns
t7	Configuration cycle setup time	20	-	ns
t8	Configuration cycle hold time	5		

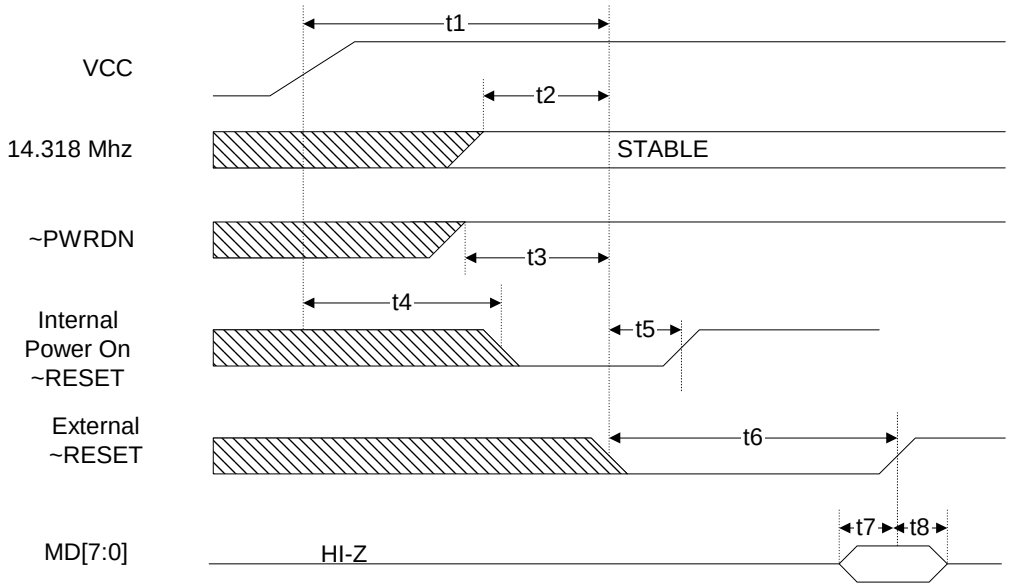


Figure 26: Power-on Reset and Reset Configuration Timing

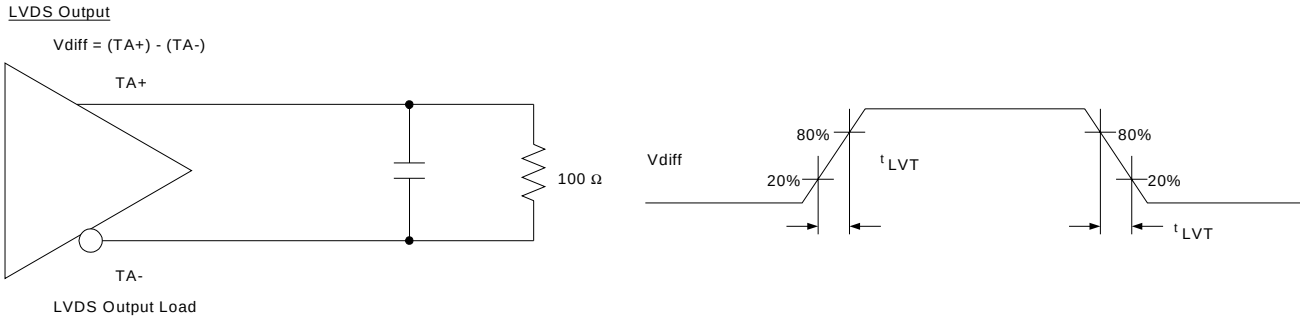


Figure 27: LVDS Transmitter Device Transition Times

Table 40: Switching Characteristics

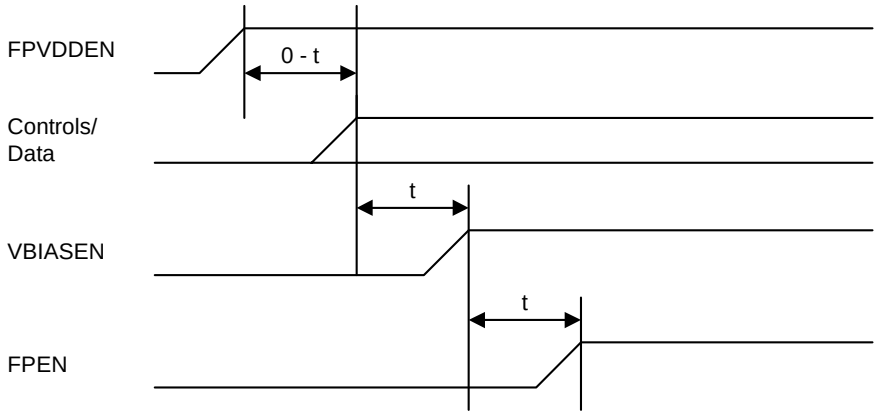
Symbol	Parameter	Min	Typ	Max	Units
t_{LVT}	LVDS Transition Time		0.6	1.5	ns

Table 41: LVDS Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS (CMOS/TTL) DC Specifications						
V_{IH}	High Level Input Voltage		2.0		Vcc	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IN}	Input Current	$OV \leq V_{IN} \leq Vcc$			±10	μA
LVDS Driver DC Specifications						
V_{OD}	Differential Output Voltage	RL = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in VOD between Complimentary Output States				35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in VOC between Complimentary Output States				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = OV, RL = 100 Ω			-24	mA
I_{OZ}	Output TRI-STATE Current	/PDWN = 0V, V_{OUT} = 0V to Vcc				

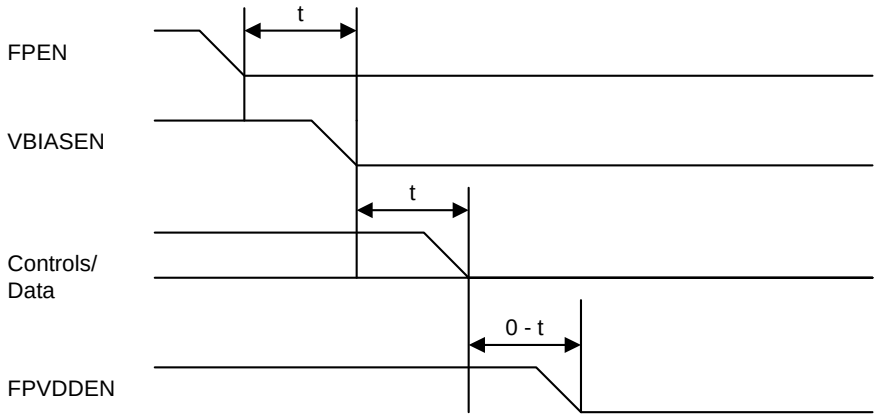
Note: LVDS transmitter licensed from Thine Electronics, Inc.

Panel On/Off Sequence



t is programmed via FPR33 [3:2]

Figure 28: Panel Power On



t is programmed via FPR33 [3:2]

Figure 29: Panel Power Off

PCI Bus Cycles

Table 42: PCI Bus Timing (33 MHz)

Symbol	Parameter	Min	Max	Unit
t1	~FRAME setup to CLK	7	-	ns
t2	AD[31:0] (address) setup to CLK	7	-	ns
t3	AD[31:0] (address) hold from CLK	0	-	ns
t4	AD[31:0] (Read Data) valid from CLK	2	11	ns
t5	AD[31:0] (Read Data) hold from CLK	0	-	ns
t6	AD[31:0] (Write Data) setup to CLK	7	-	ns
t7	AD[31:0] (Write Data) hold from CLK	0	-	ns
t8	C/~BE[3:0] (Command) setup to CLK	7	-	ns
t9	C/~BE[3:0] (Command) hold from CLK	0	-	ns
t10	C/~BE[3:0] (Byte Enable) hold from CLK	0	-	ns
t11	~TRDY High-Z to High from CLK	2	-	ns
t12	~TRDY active from CLK	2	11	ns
t13	~TRDY inactive from CLK	2	11	ns
t14	~TRDY High before High-Z	1T	-	CLK
t15	~IRDY setup to CLK	7	-	ns
t16	~IRDY hold from CLK	0	-	ns
t17	~DEVSEL active from CLK	2	11	ns
t18	~DEVSEL inactive from CLK	2	11	ns
t19	~DEVSEL High before High-Z	1T	-	CLK

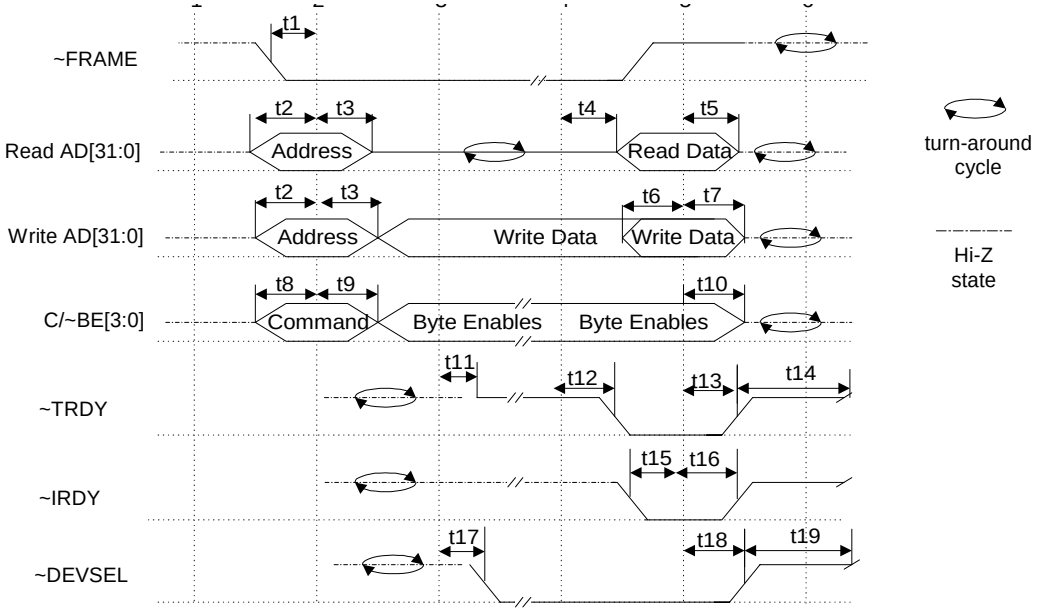


Figure 30: PCI Bus Timing Diagram

AGP BUS Cycles

Table 43: AGP 1X mode BUS Timing

Symbol	PARAMETER	Min Spec	Max Spec	units
t cyc	CLK Cycle Time	15.0	30.0	ns
t valc	CLK to control signal (Output) valid delay	1.0	5.5	ns
t vald	CLK to data (Output) valid delay	1.0	6.0	ns
t on	Float to Active (Output) Delay	1.0	6.0	ns
t off	Active to Float (Output) Delay	1.0	14.0	ns
t suc	Control signals (Input) setup time to CLK	6.0	-	ns
t sud	Data (Input) setup time to CLK	5.5	-	ns
t h	Control signals (Input) hold time to CLK	0.0	-	ns

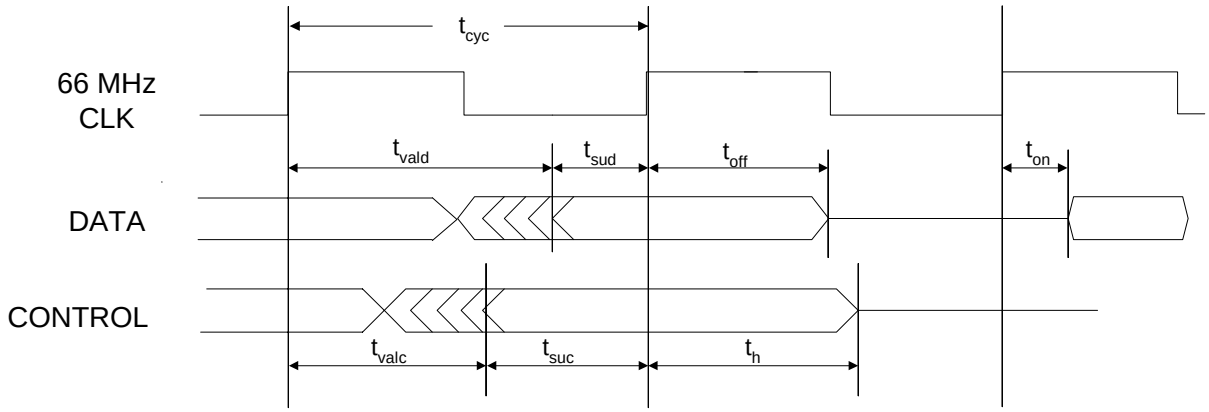


Figure 31: AGP Bus Timing Diagram

Table 44: AGP 2X Timing Parameters

Symbol	Description	Min (ns)	Max (ns)
tCLK	Clock	-	15
TDVB	Data valid before strobe	1.7	
tDVA	Data valid after strobe	1.9	
TVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

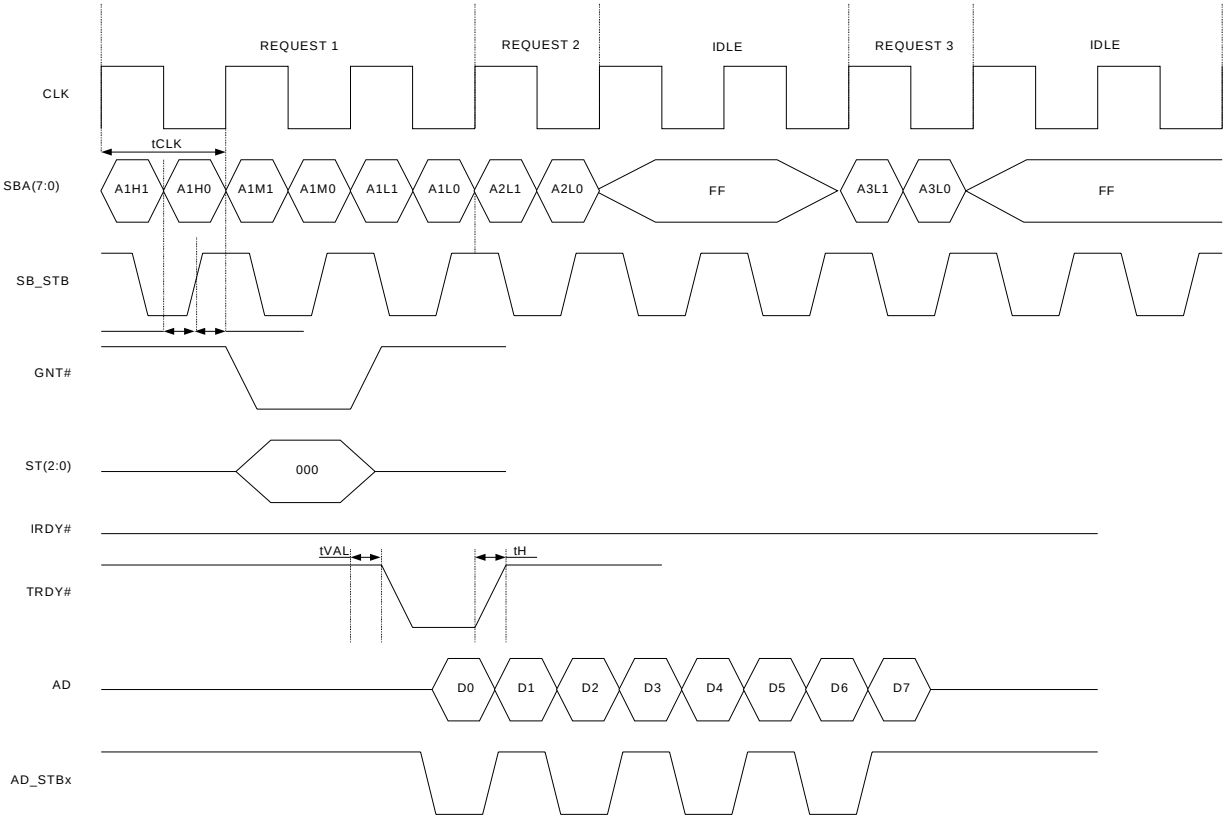


Figure 32: AGP 2X Read Request with Return Data (4Qw)

Table 45: AGP4X Timing Parameters

Symbol	Description	Min (ns)	Max (ns)
tCLK	Clock	-	15
TDVB	Data valid before strobe	TBD	
tDVA	Data valid after strobe	TBD	
TVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

Synchronous DRAM (SDRAM) and SGRAM Cycles

Table 46: SDRAM/SGRAM Memory Read Timing

Symbol	Parameter	Min	Max	Unit
t1	SDCK Cycle Time	12		ns
t2	SDCK High Time	4		ns
t3	SDCK Low Time	4		ns
t4	SDCKEN hold time	3.5		ns
t5	SDCKEN setup time	3.5		ns
t6	Command (˜CS, ˜RAS, ˜CAS, ˜WE, DSF, DQM) setup time	3.5		ns
t7	Command (˜CS, ˜RAS, ˜CAS, ˜WE, DSF, DQM) hold time	3.5		ns
t8	Address/BA setup time	3.5		ns
t9	Address/BA hold time	2.5		ns
t10	Access time from SDCK		T-2	ns
t11	Data Out hold time from SDCK	4		ns
t12	Data In setup time from SDCK	3.5		ns
t13	Data In hold time from SDCK	3.5		ns
t14	Active to READ, WRITE delay	3T		
t15	Read Latency	3T		
t16	Write recovery time	2T		

Note: T = SDCK clock period

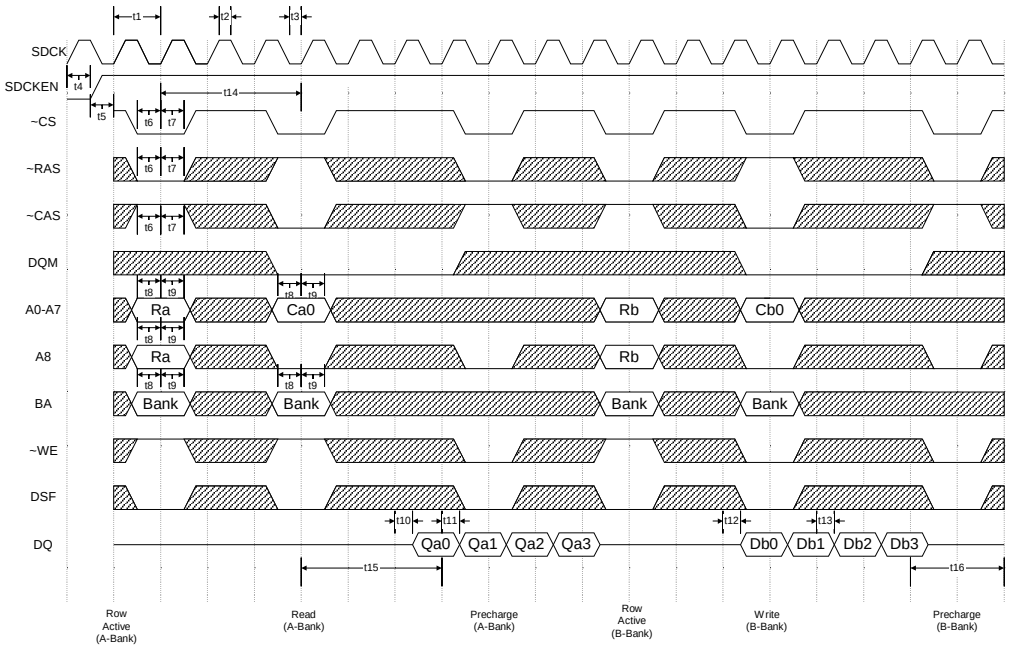


Figure 33: SDRAM/SGRAM Read and Write Cycles

Flat Panel Interface Cycle Timing

Table 47: Color TFT Interface Timing

Symbol	Parameter	Min	Max	Unit
t1	TFT FPSCLK Cycle Time	12		ns
t2f	FDATA setup to FPSCLK falling edge	0.5T-2		ns
t3f	FDATA hold from FPSCLK falling edge	0.5T-2		ns
t4f	DE setup to FPSCLK falling edge	0.5T-4		ns
t5f	DE hold from FPSCLK falling edge	0.5T-4		ns
t2r	FDATA setup to FPSCLK rising edge	0.5T-2		ns
t3r	FDATA hold from FPSCLK rising edge	0.5T-2		ns
t4r	DE VSYNC setup to FPSCLK rising edge	0.5T-4		ns
t5r	DE VSYNC hold from FPSCLK rising edge	0.5T-4		ns
t6	FHSYNC Pulse Width	8	16	T
t7	FVSYNC Pulse Width	1		FHSYNC

Note: T = pixel clock rate on LCD

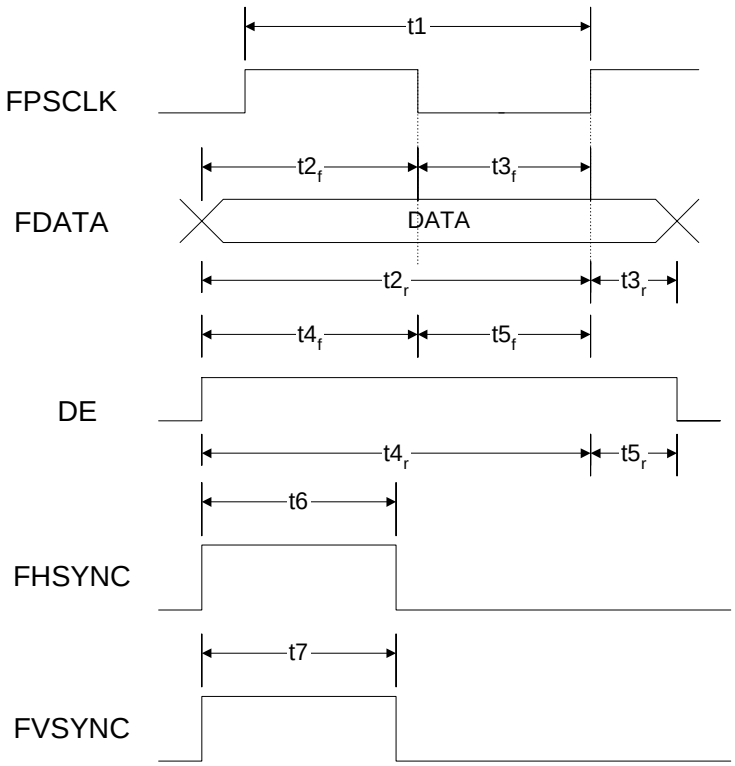
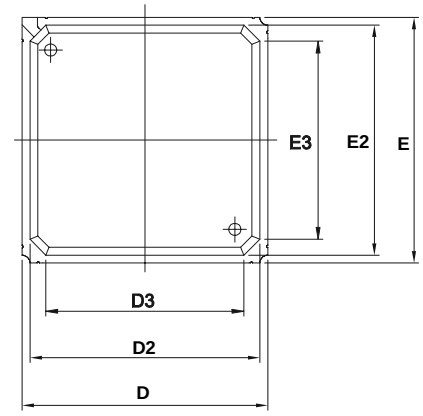
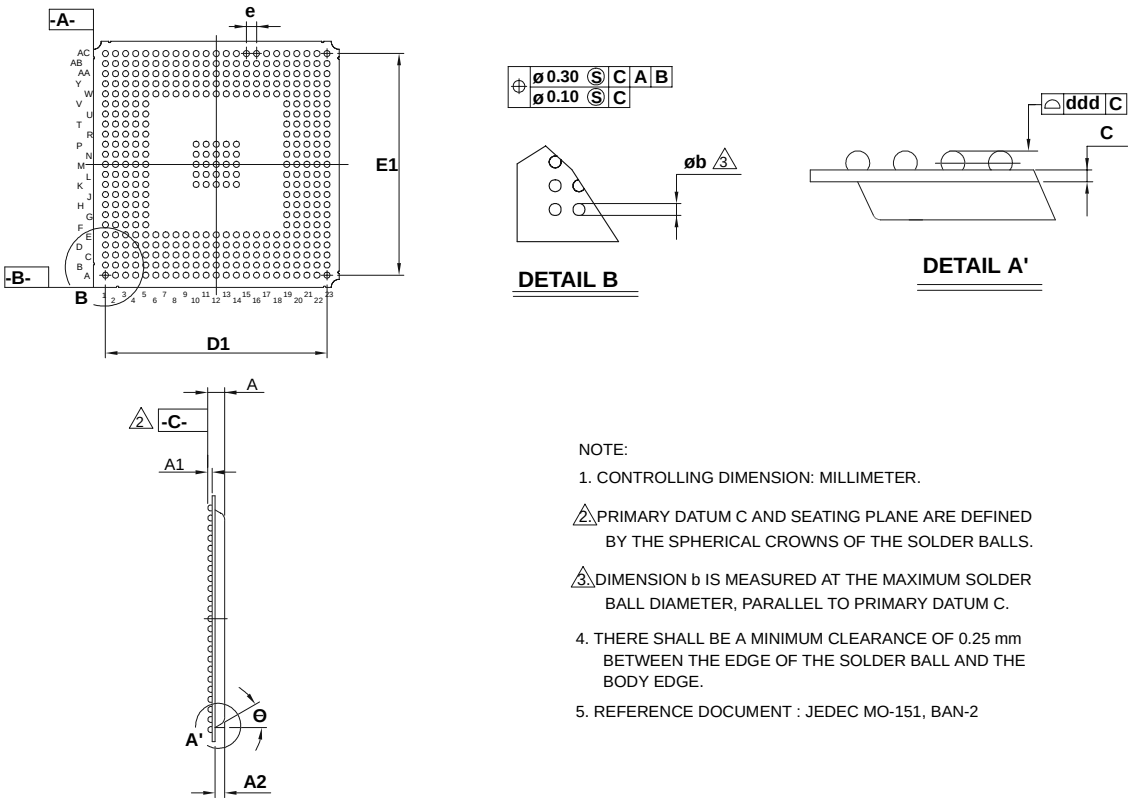


Figure 34: TFT Interface Timing

Chapter 30: Mechanical Dimensions



Symbol	dimension in mm			dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.13	2.33	2.53	0.084	0.092	0.100
A1	0.50	0.60	0.70	0.020	0.024	0.028
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	0.60	0.75	0.90	0.024	0.030	0.035
C	0.51	0.56	0.61	0.020	0.022	0.024
D	30.80	31.00	31.20	1.213	1.220	1.228
D1	27.94 BSC			1.100 BSC		
D2	28.80	29.00	29.20	1.134	1.142	1.150
D3	—	25.00	—	—	0.984	—
E	30.80	31.00	31.20	1.213	1.220	1.228
E1	27.94 BSC			1.100 BSC		
E2	28.80	29.00	29.20	1.134	1.142	1.150
E3	—	25.00	—	—	0.984	—
e	1.27 BASIC			0.050 BASIC		
ddd	—	—	0.20	—	—	0.008
Θ	30° TYP			30° TYP		



NOTE:

1. CONTROLLING DIMENSION: MILLIMETER.

2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25 mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.

5. REFERENCE DOCUMENT : JEDEC MO-151, BAN-2

Figure 35: 385 BGA Mechanical Dimensions

Appendix A: Video Modes

This appendix lists the various tables of video modes supported under various configurations of SM731: CRT only, LCD only, or simultaneous. The parameters listed in the following tables define the standard capabilities of the SM731 when it is used with the Silicon Motion's Video BIOS.

Abbreviations used:
Txt: text mode
Gr: graphics mode

Standard IBM Compatible VGA Modes

The table details the standard VGA modes supported in CRT only.

Table 48: Standard IBM Compatible VGA Modes

Mode # (Hex)	Type	Colors	Alpha	Resolution	Font	Clock MHz	Hsync KHz	Vsync Hz	Memory Min	Buffer Start
0,1	Txt	16	40x25	320x200	8x8	25.175	31.55	70.3	256K	B8000
0,1*	Txt	16	40x25	320x350	8x14	25.175	31.55	70.3	256K	B8000
0,1+	Txt	16	40x25	360x400	9x16	28.322	31.34	69.8	256K	B8000
2,3	Txt	16	80x25	640x200	8x8	25.175	31.55	70.3	256K	B8000
2,3*	Txt	16	80x25	640x350	8x14	25.175	31.55	70.3	256K	B8000
2,3+	Txt	16	80x25	720x400	9x16	28.322	31.34	69.8	256K	B8000
4,5	Gr	4	40x25	320x200	8x8	25.175	31.55	70.3	256K	B8000
6	Gr	2	80x25	640x200	8x8	25.175	31.55	70.3	256K	B8000
7	Txt	Mono	80x25	720x350	9x14	28.322	31.34	69.8	256K	B8000
7+	Txt	Mono	80x25	720x400	9x16	28.322	31.34	69.8	256K	B8000
D	Gr	16	40x25	320x200	8x8	25.175	31.55	70.3	256K	A0000
E	Gr	16	80x25	640x200	8x8	25.175	31.55	70.3	256K	A0000
F	Gr	Mono	80x25	640x350	8x14	25.175	31.55	70.3	256K	A0000
10	Gr	16	80x25	640x350	8x14	25.175	31.55	70.3	256K	A0000
11	Gr	2	80x30	640x480	8x16	25.175	31.55	60.1	256K	A0000
12	Gr	16	80x30	640x480	8x16	25.175	31.55	60.1	256K	A0000
13	Gr	256	40x25	320x200	8x8	25.175	31.55	70.3	256K	A0000

NOTE: For Modes 3 and 7, 8-dot Fonts are used on the LCD.

VESA Super VGA Modes

VESA extended video modes are supported by the LYNX family BIOS (subject to the constraints of the video subsystem hardware) as follows:

Table 49: VESA Super VGA Modes

VESA Mode # (Hex)	Extended Mode	Type	Colors	Alpha	Resolution	Font	Memory Min	Buffer Start
(Min.)	Buffer Start							
101	50	Gr	256	80x30	640x480	8x16	512K	A0000
102	6A	Gr	16	100x75	800x600	8x8	256K	A0000
103	55	Gr	256	100x75	800x600	8x8	512K	A0000
104	6B	Gr	16	128x48	1024x768	8x16	512K	A0000
105	60	Gr	256	128x48	1024x768	8x16	1M	A0000
107	65	Gr	256	160x64	1280x1024	8x16	2M	A0000
111	52	Gr	64K	80x30	640x480	8x16	1M	A0000
112	53	Gr	16M	80x30	640x480	8x16	1M	A0000
114	57	Gr	64K	100x75	800x600	8x8	1M	A0000
115	58	Gr	16M	100x75	800x600	8x8	2M	A0000
117	62	Gr	64K	128x100	1024x768	8x8	2M	A0000
118	63	Gr	16M	128x100	1024x768	8x8	4M	A0000
11A	67	Gr	64K	160x128	1280x1024	8x8	4M	A0000
11B	68	Gr	16M	160x128	1280x1024	8x8	4M	A0000

Low Resolution Modes

The BIOS supports low-resolution modes from 320x200 to 640x400 in 8/16-bit colors for DirectDraw. The low resolution modes are defined as follows:

Table 50: Low Resolution Modes

Mode # (Hex)	Type	Colors	Resolutions	Vsync (Hz)	Video Memory	Buffer Start
40	Gr	256	320x200	70	1MB	A0000
41	Gr	64K	320x200	70	1MB	A0000
42	Gr	256	320x240	75, 60	1MB	A0000
43	Gr	64K	320x240	75, 60	1MB	A0000
44	Gr	256	400x300	75, 60	1MB	A0000
45	Gr	64K	400x300	75, 60	1MB	A0000
46	Gr	256	512x384	75	1MB	A0000
47	Gr	64K	512x384	75	1MB	A0000
48	Gr	256	640x400	70	1MB	A0000
49	Gr	64K	640x400	70	1MB	A0000

NOTE: For modes 320x240 and 400x300, default refresh rate is set to 60Hz and optimal is set to 75Hz.

640 by 480 Resolution Modes

Table 51: 640 x 480 Extended Modes

Mode # (Hex)	VESA Mode # (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
50	101	Gr	256	80x30	8x16	25.175	31.5	60.0	512 KB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		
52	111	Gr	64K	80x30	8x16	25.0	31.5	60.0	1MB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		
53	112	Gr	16M (24-bit)	80x30	8x16	25.0	31.5	60.0	1MB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		
54		Gr	16M (32-bit)	80x30	8x16	25.0	31.5	60.0	2MB	A0000
						31.5	37.5-	75.0-		
						36	43.3	85.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz.

800 by 600 Resolution Modes

Table 52: 800x600 Extended Modes

Mode # (Hex)	Vesa Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
6A	6A	Gr	16	100x75	8x8	40.0	37.9+	60.3+	256KB	A0000
55	103	Gr	256	100x75	8x8	40.0	37.9+	60.3+	512KB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		
57	114	Gr	64K	100X75	8X8	40.0	37.9+	60.3+	1MB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		
58	115	Gr	16M (24-bit)	100X75	8X8	40.0	37.9+	60.3+	2MB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		
59		Gr	16M (32-bit)	100X75	8X8	40.0	37.9+	60.3+	2MB	A0000
						49.5	46.9+	75.0+		
						56.25	53.7	85.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz.

1024 by 768 Resolution Modes

Table 53: 1024x768 Extended Modes

Mode # (Hex)	VESA Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
6B	104	Gr	16	128x48	8x16	65.0	48.4 -	60.0 -	512KB	A0000
60	105	Gr	256	128x48	8x16	65.0	48.4 -	60.0 -	1MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		
62	117	Gr	64K	128x48	8x16	65.0	48.4 -	60.0 -	2MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		
63	118	Gr	16M (24-bit)	128x48	8x16	65.0	48.4 -	60.0 -	4MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		
64		Gr	16M (32-bit)	128x48	8x16	65.0	48.4 -	60.0 -	4MB	A0000
						78.8	60.0+	75.0+		
						94.5	68.7	85.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz

1280 by 1024 Resolution Modes

Table 54: 1280x1024 Extended Modes

Mode # (Hex)	VESA Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
65	107	Gr	256	160x64	8x16	78.8	46.4	86.8i+	2 MB	A0000
						108	64	60.0		
						135	79.98	75.0		
67	11A	Gr	64K	160x64	8x16	78.8	46.4	86.8i+	4 MB	A0000
						108	64	60.0		
						135	79.98	75.0		
68		Gr	16M (24-bit)	160x64	8x16	78.8	46.4	86.8i+	4 MB	A0000
						108	64	60.0		
						135	79.98	75.0		

NOTE: For the above resolutions, the default refresh rate for LCD and Simul mode is 60Hz

1600 by 1200 Resolution Modes

Table 55: 1600x1200 Extended Modes

Mode # (Hex)	VESA Mode# (Hex)	Type	Colors	Alpha Format	Font	VCLK (MHz)	Hsync +/- (KHz)	Vsync +/- (Hz)	Video Memory	Buffer Start
70		Gr	256	200x75	8x16	162	74.5	60	2 MB	A0000
						202	84	75		
						229	91.8	85		
72		Gr	64K	200x75	8x16	112	74.5	60	4 MB	A0000
						202	84	75		
						229	91.8	85		

Appendix B: Popup Icon Consideration

Introduction

The silicon supports both the hardware cursor and popup icon. System BIOS uses the popup icon to display system information, such as: Battery Status, LCD Brightness and more. The display driver for GUI operating system uses the hardware Cursor to increase performance. Since both popup icon and hardware cursor image locations are closely coupled both will be described. This appendix details popup icon support and how to implement the support in system BIOS.

Popup Icon

The popup icons are driven by the LCD and CRT backends. The popup icon size is 64x64, and can be zoomed up by 2 to become 128x128 popup icon. The popup icon can be programmed to anywhere on the screen display.

For example, in simultaneous mode or extended mode (CRT only), a display image is processed through the LCD pipe and the popup icon can be processed though the LCD backend. However, in Dual Monitor mode (Windows 98), the popup icons will be enabled in order to display on the CRT and LCD screens.

Icon Pattern Memory Location

The icon pattern memory locations are specified in the following registers: PHR80 and PHR81 for CRT, and FPRT160 for LCD. Each of these two icon registers allocates 2KB offscreen video memory within the maximum physical memory. Silicon Motion assigns the highest 2KB addresses for the physical memory to be installed. The lower 1KB is used to store the popup icon image, and the upper 1KB is used to store the hardware cursor image.

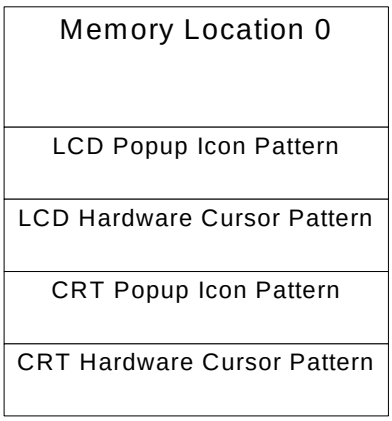


Figure 36: Hardware Cursor and Popup Icon Memory Location

Icon Pattern

Each pixel of the Icon pattern uses 2-bit to select the different color formats. The table below lists the various color selects: transparent, Icon Color1 is defined in POP84 register for CRT and FPRT164 for LCD.

Icon Pattern [1:0]	Color Source
00	Transparent
01	Icon Color1
10	Icon Color 2
11	Icon Color 3

Furthermore, pixel data is stored in sequential order. For example, Bit[7:6] of a byte in the video memory is the first pixel of the Icon pattern. Bit[5:4] is the second pixel of the Icon pattern.

Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0
1st pixel	2nd pixel	3rd pixel	4th pixel

Each of the popup icon color registers is defined in the same way described below:

The 8-bit color register is defined to be 3:3:2 for R:G:B respectively as shown on the table below:

7	6	5	4	3	2	1	0
Red			Green			Blue	
2	1	0	2	1	0	1	0

The silicon will take the 8-bit Icon color and convert it into 24-bit Icon color internally. For example, R2R1R0G2G1G0B1B0 will be expanded to R2R1R0R0R0R0R0R0G2G1G0G0G0G0G0G0B1B0B0B0B0B0B0B0.

Icon Control on CRT Backend

Register POP82 controls the popup icon enable and size.

POP82[7] controls the Popup Icon Enable
0 = Disable
1 = Enable

POP82[6] controls the Popup Icon Size
0 = 64x64
1 = 128x128

Icon Control on LCD backend

Register FPRT160 controls the popup icon enable and size.

FPRT160[13] controls the Popup Icon Enable
0 = Disable
1 = Enable

FPRT160[12] controls the Popup Icon Size
0 = 64x64
1 = 128x128

Video BIOS Function Call

Video BIOS has call services for the popup icon. The table below lists the available video BIOS function calls.

Popup Icon Control (AX = 5F01, BL = 00 - 05)

Enable/Disable Popup Icon

Description: This function changes the current status of the popup icon

Input: AX = 5F01h
BL = 00h
BH = [0] = 0 - No Change
= 1 - Change CRT to Icon state
[1] = 0 - No Change
= 1 - Change Panel Icon state
[2] = 0 - Set to Off state
= 1 - Set to On state

Output: AX = Return status

Select the Size of Popup Icon

Description: This function changes the current status of the popup icon

Input: AX = 5F01h
BL = 01h
BH = [0] = 0 - No Change
= 1 - Change CRT to Icon state
[1] = 0 - No Change
= 1 - Change Panel Icon state
[2] = 0 - 64x64x2
= 1 - 128x128x2

Output: AX = Return status

Set Popup Icon Location

Description: This function sets the location of the popup icon

Input: AX = 5F01h
BL = 02h
BH = [0] = 0 - No Change

=
= 1 - Change CRT to Icon state
[1] = 0 - No Change
= 1 - Change Panel Icon state
CX X position of the Icon
=
DX Y position of the icon
=

Output: AX Return status
=

Set Popup Icon Foreground Color

Description: This function sets the foreground color of the popup icon

Input: AX 5F01h
=
BL 03h
=
BH [0] = 0 - No Change
=
= 1 - Change CRT to Icon state
[1] = 0 - No Change
= 1 - Change Panel Icon state
CH 1 Color Index 1
=
2 Color Index 2
3 Color Index 3
CL Color value for popup icon
=

Output: AX Return status
=

Set Popup Icon Background Color

Description: This function loads the background color for the popup icon

Input: AX 5F01h
=
BL 04h
=
BH [0] = 0 - No Change
=
= 1 - Change CRT to Icon state
[1] = 0 - No Change
= 1 - Change Panel Icon state
CL Background Color
=
DX Y position of the icon
=

Output: AX Return status
=

Set Popup Icon Bitmap

Description: This function loads the background bitmap for the popup icon

Input: AX 5F01h
=
BL 05h
=
BH [0] = 0 - No Change
=
= 1 - Change CRT to Icon state
[1] = 0 - No Change
= 1 - Change Panel Icon state
ES Segment of popup icons bitmap
=
DI Offset of popup icons bitmap
=

Output: AX Return status
=

Appendix C: SMI Handler Programming Consideration

Introduction

The silicon is designed for notebook systems. Notebook systems require support of SMM (system management mode) for handling system-wide functions, such as: power management, system hardware control, and proprietary OEM-design code. This application note describes consideration for system BIOS when implementing SMI (System management interrupt) handler for the silicon.

Background

SMM is a special-purpose operating mode provided for handling system-wide functions. The main benefit of SMM is that it offers an easily isolated processor environment that operates transparently to the operating system or software applications.

When SMM is invoked through SMI, the processor saves the current state of the processor, then switches to a separate operating environment contained in the system management RAM. While in SMM, the processor executes a SMI handler code to perform operations such as power down HD when it is idle or displaying an OEM-design message on the screen. When the SMI handler has completed its operations, it executes a resume instruction. This instruction causes the processor to reload the saved context of the processor, switch back to protected or real mode, and resume executing the interrupted operating-system program or interrupted application programs.

System BIOS Consideration

The video BIOS provides an alternate INT 10h entry to allow SMI handlers to execute VGA BIOS function calls. This entry point bypasses the STI (Set Interrupt Flag) instruction at the beginning of the standard interrupt handler.

Int10 Vector Entry

The standard interrupt handler INT10 vector is located in 0000:0040h. This INT10 handler will issue STI instruction.

Alternate INT10 Entry

The alternate INT10 entry is specified within the content of location C000:0034h. This alternate INT10 handler entry does not issue STI.

Note: For system BIOS from Phoenix, there is a function named: PmModifyInt10Vector that can be used to modify the INT10 vector.

Video BIOS service calls read/modify the I/O and memory-mapped registers. The memory-mapped registers are accessed through A000-B000 range in real mode or SMM; they are video processor registers, drawing engine registers and capture port registers. Due to the fact that A000-B000 range is reserved for power management under SMM mode, special consideration is necessary:

There are two methods as listed below:

1. **Exit SMM**
   Exit SMM when calling video BIOS services or accessing memory-mapped registers. Upon completion, it is ok to resume back to SMM.

2. **Map Power Management Data to another location**
   The default area for storing the power management data is A000-B000. In order to allow video BIOS services to access A000-B000 area, system BIOS can map the A000-B000 data to another location, such as D000-E000.

Appendix D: Programming USR [3:0] Pins

Application Notes for control of USR [3:0] Pins

*GPR 72 is General Purpose Register 72 with address 3C5h and index 72h
GPR 73 is General Purpose Register 73 with address 3C5h and index 73h

USR0

GPR72 [4]	GPR72 [0]	USR0 Pad	Remark
0	0	Input	*
0	1	Input	
1	0	Output 0	
1	1	Input	

* When USR0 is in input state, the input status can be read from GRP72[2].

USR1

GPR72 [5]	GPR72 [1]	USR1 Pad	Remark
0	0	Input	*
0	1	Input	
1	0	Output 0	
1	1	Input	

* When USR1 is in input state, the input status can be read from GRP72[3].

USR2

GPR73 [5]	GPR73 [1]	USR1 Pad	Remark
0	0	Input	*
0	1	Input	
1	0	Output 0	
1	1	Input	

* When USR2 is in input state, the input status can be read from GRP73[2]. When toggling USR2 as an input pin, it will generate a hardware interrupt. The status of the interrupt can be read at bit 2 of SCR1C register.

USR3

GPR73 [5]	GPR73 [1]	USR1 Pad	Remark
0	0	Input	*
0	1	Input	
1	0	Output 0	
1	1	Input	

* When USR3 is in input state, the input status can be read from GRP73[3]. When toggling USR3 as an input pin, it will generate a hardware interrupt. The status of the interrupt can be read at bit 3 of SCR1C register.

Appendix E: Monitor and TV Detect

CRT Monitor Detect

To simplify the monitor detect procedure SM731 implemented four new registers (ccr7a, ccr7b, ccr7c, ccr7d) and detect circuitry. As for R, G, B corresponds to ccr7a, ccr7b, ccr7c data and ccr7d_[7] as enable. When all these registers are programmed properly, and without waiting for sync period the users can read back the register 3c2_[4] to determine if the monitor is connected.

3c2_[4] = 0; No monitor detect
3c2_[4] = 1; Color monitor detect

TV Detect

To simplify the TV monitor detect procedure SM731 also uses registers (ccr7a, ccr7b, ccr7c, ccr7d), and TV monitor detect circuitry.

For Y = {ccr7a,00} as 10 bit data
For C = {ccr7b,00} as 10 bit data
For CVBS = {ccr7c,00} as 10 bit data

With ccr7d_[7] as enable and all these registers are programmed properly the users can read back the register ccr7d_[6] to determine SVHS monitor's status.

Ccr7d_[6] = 0; No TV monitor detect
Ccr7d_[6] = 1; TV monitor detect

With ccr7d_[7] as enable and all these registers are programmed properly the users can read back the register ccr7d_[5] to determine CVBS monitor's status.

Ccr7d_[5] = 0; No TV monitor detect
Ccr7d_[5] = 1; TV monitor detect

Appendix F: CRT and LCD Timing Register Summary

CRT Timing Register Summary

Table 56: CRT Timing Register Summary

Parameter	CRT Register Bits						
	[10]	[9]	[8]	[7]	[6]	[5]	[4:0]
H Total				CRT00[7]	CRT00[6]	CRT00[5]	CRT00[4:0]
H Total Shadow				SVR40[7]	SVR40[6]	SVR40[5]	SVR40[4:0]
H Display End				CRT01[7]	CRT01[6]	CRT01[5]	CRT01[4:0]
H Blank Start				CRT02[7]	CRT02[6]	CRT02[5]	CRT02[4:0]
H Blank Start Shadow				SVR41[7]	SVR41[6]	SVR41[5]	SVR41[4:0]
H Blank End				CRT33[6]	CRT33[5]	CRT05[7]	CRT03[4:0]
H Blank End Shadow						SVR44[7]	SVR42[4:0]
H Sync Start				CRT04[7]	CRT04[6]	CRT04[5]	CRT04[4:0]
H Sync Start Shadow				SVR43[7]	SVR43[6]	SVR43[5]	SVR43[4:0]
H Sync End							CRT05[4:0]
H Sync End Shadow							SVR44[4:0]
V Total	CRT30[3]	CRT07[5]	CRT07[0]	CRT06[7]	CRT06[6]	CRT06[5]	CRT06[4:0]
V Total Shadow		SVR4A[5]	SVR4A[0]	SVR45[7]	SVR45[6]	SVR45[5]	SVR45[4:0]
V Sync Start	CRT30[0]	CRT07[7]	CRT07[2]	CRT10[7]	CRT10[6]	CRT10[5]	CRT010[4:0]
V Sync Start Shadow		SVR4A[7]	SVR4A[2]	SVR48[7]	SVR48[6]	SVR48[5]	SVR48[4:0]
V Sync End							CRT011[3:0]
V Sync End Shadow							SVR49[3:0]
V Display End	CRT30[2]	CRT07[6]	CRT07[1]	CRT12[7]	CRT12[6]	CRT12[5]	CRT012[4:0]
V Blank Start	CRT30[1]	CRT09[5]	CRT07[3]	CRT15[7]	CRT15[6]	CRT15[5]	CRT015[4:0]
V Blank Start Shadow		SVR4B[5]	SVR4A[3]	SVR46[7]	SVR46[6]	SVR46[5]	SVR46[4:0]
V Blank End		CRT33[4]	CRT33[3]	CRT16[7]	CRT16[6]	CRT16[5]	CRT016[4:0]
V Blank End Shadow				SVR47[7]	SVR47[6]	SVR47[5]	SVR47[4:0]
Line Compare				CRT18[7]	CRT18[6]	CRT18[5]	CRT018[4:0]
Offset				CRT13[7]	CRT13[6]	CRT13[5]	CRT013[4:0]

Note: Bits shown in bold text are SMI extended registers

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