6.0 Electrical Specifications

This section describes the specifications of the TGUI9680. The following topics are discussed:

6.1 Absolute Maximum Ratings

6.2 DC Specifications

6.3 AC Specifications

6.1 Absolute Maximum Ratings

Table 6-1. Absolute Maximum Ratings

Ambient Temperature	0° to 70° Celsius
Storage Temperature	-40° to 125° Celsius
DC Supply Voltage	-0.5 to 7.0 Volts
I/O Pin Voltage with Respect to VSS	-0.5 to VDD+0.5 Volts

6.2 DC Specifications

Table 6-2. DC Specifications

Symbol	Parameter	Min	Max	Units	Conditions
VIL	Input Low Voltage.		0.8	V	VCC = 5 V±5%
VIH	Input High Voltage.	2.0		V	VCC = 5 V±5%
VOL	Output Low Voltage.		VSS + 0.4	V	
VOH	Output High Voltage.	2.4	VCC – 0.4	V	
IIL	Input Low Current.		±10	µA	VIN = 0.0 V
IIH	Input High Current.		±10	µA	VIN = VCC
IOZ	Output Tri-state Leakage Current.		±10	µA	
CIN	Input Capacitance.		10	pF	FC = 1 MHz
COUT	Output Capacitance.		10	pF	FC = 1 MHz
CI/O	I/O Pin Capacitance.		10	pF	FC = 1 MHz
ICC	Power Supply Current.		400	mA	VCC = 5 V±5%

6.3 AC Specifications

6.3.1 Clock and Reset Timing

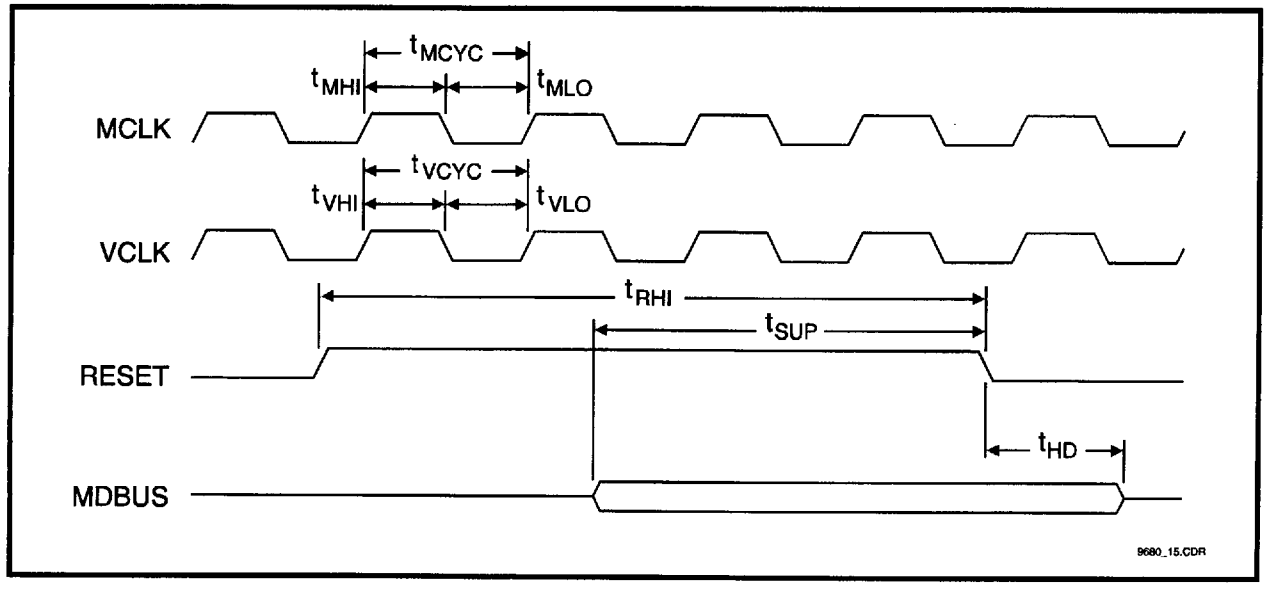

Figure 6-1. Clock and Reset Timing Diagram

Table 6-3. Clock and Reset Timing

Symbol	Min (ns)	Max (ns)	Comment
t_{MCYC}	12.5		MCLK period.
t_{MHI}	6		MCLK high time.
t_{MLO}	6		MCLK low time.
t_{VCYC}	12.5		VCLK period.
t_{VHI}	6		VCLK high time.
t_{VLO}	6		VCLK low time.
t_{RHI}	200		RESET high time.
t_{SUP}	30		Configuration setup time.
t_{HD}	10		Configuration hold time.

6.3.2 EEPROM Timing

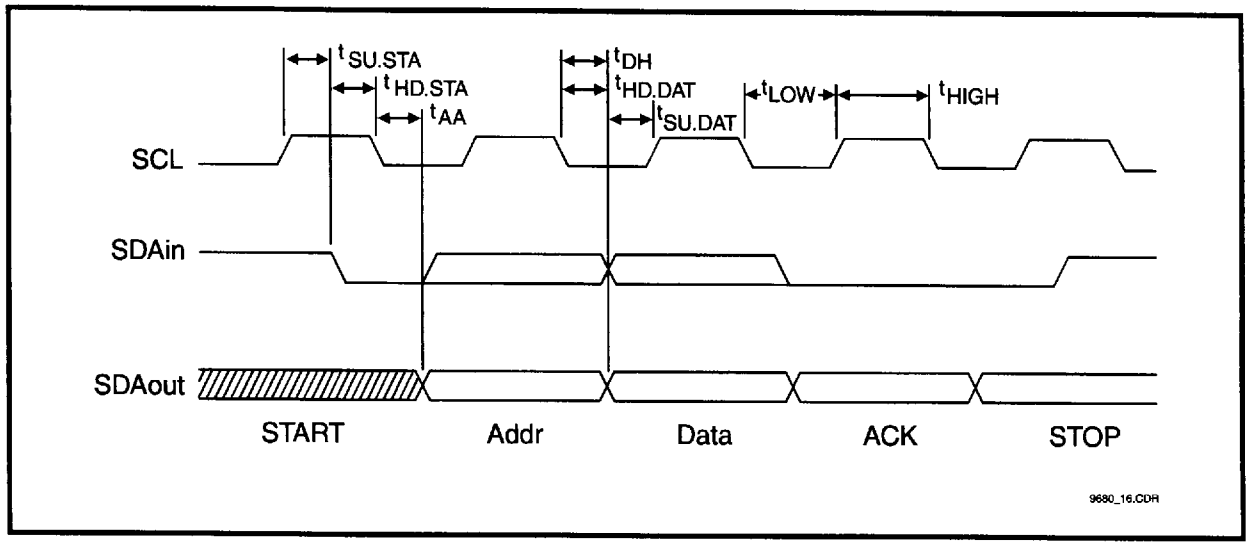

Figure 6-2. EEPROM Timing Diagram

Table 6-4. EEPROM Timing

Symbol	Min (µs)	Max (µs)	Comment
$t_{SU.STA}$	4.7		Start set-up time.
$t_{HD.STA}$	4.0		Start hold time.
t_{AA}	0.1	3.5	Clock low to data out valid.
t_{DH}	0.1		Data out hold time.
$t_{HD.DAT}$	0		Data in hold time.
$t_{SU.DAT}$	0.05		Data in set-up time.
t_{LOW}	4.7		Clock pulse width low.
t_{HIGH}	4.0		Clock pulse width high.

6.3.3 Multiplexed and Non-Multiplexed VL Interface Timing

The multiplexed VL interface timing is shown in Figure 6-3, which illustrates two zero-wait state memory write instructions and one memory or I/O read instruction. For the non-multiplexed VL timing, it is similar to that shown in Figure 6-4 except that the ADEN# and DTEN# signals are not used and the address signals are directly fed into the controller. The timing parameters are listed in Table 6-5.

Table 6-5. VL Interface Timing

Definition	Symbol	Min	Max
Clock rising edge to address/control delay (VL)	t_{A1}	3ns	18ns
Clock rising edge to data valid delay (VL)	t_{A2}		12ns
Clock rising edge to ADEN#, DTEN# and LRDY# delay (VL)	t_{A3}		10ns
Clock rising edge to ADEN#, DTEN# and LRDY# hold (VL)	t_{A4}		10ns
LDEV# to ADS# falling edge delay (VL)	t_{A5}		20ns
Clock rising edge to address/control delay (PCI)	t_{B1}		23ns
Clock rising edge to address/control hold (PCI)	t_{B2}	0ns	
Clock rising edge to ADEN#, DTEN# and TRDY# delay (PCI)	t_{B3}		10ns

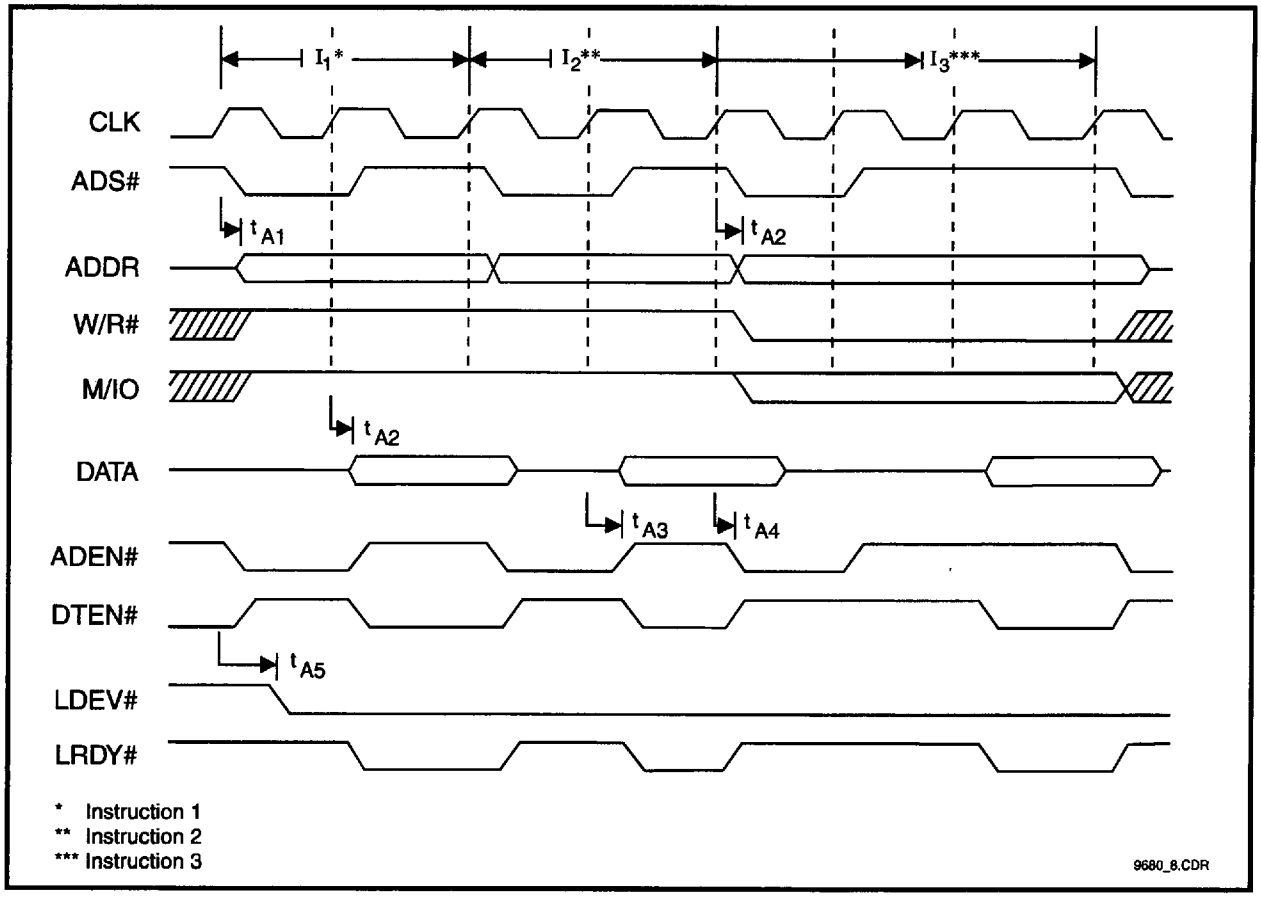

Figure 6-3. VL Interface Timing

6.3.4 PCI Interface Timing

The PCI interface timing is shown in Figure 6-4, which illustrates a burst memory read cycle and a memory write cycle without bursting.

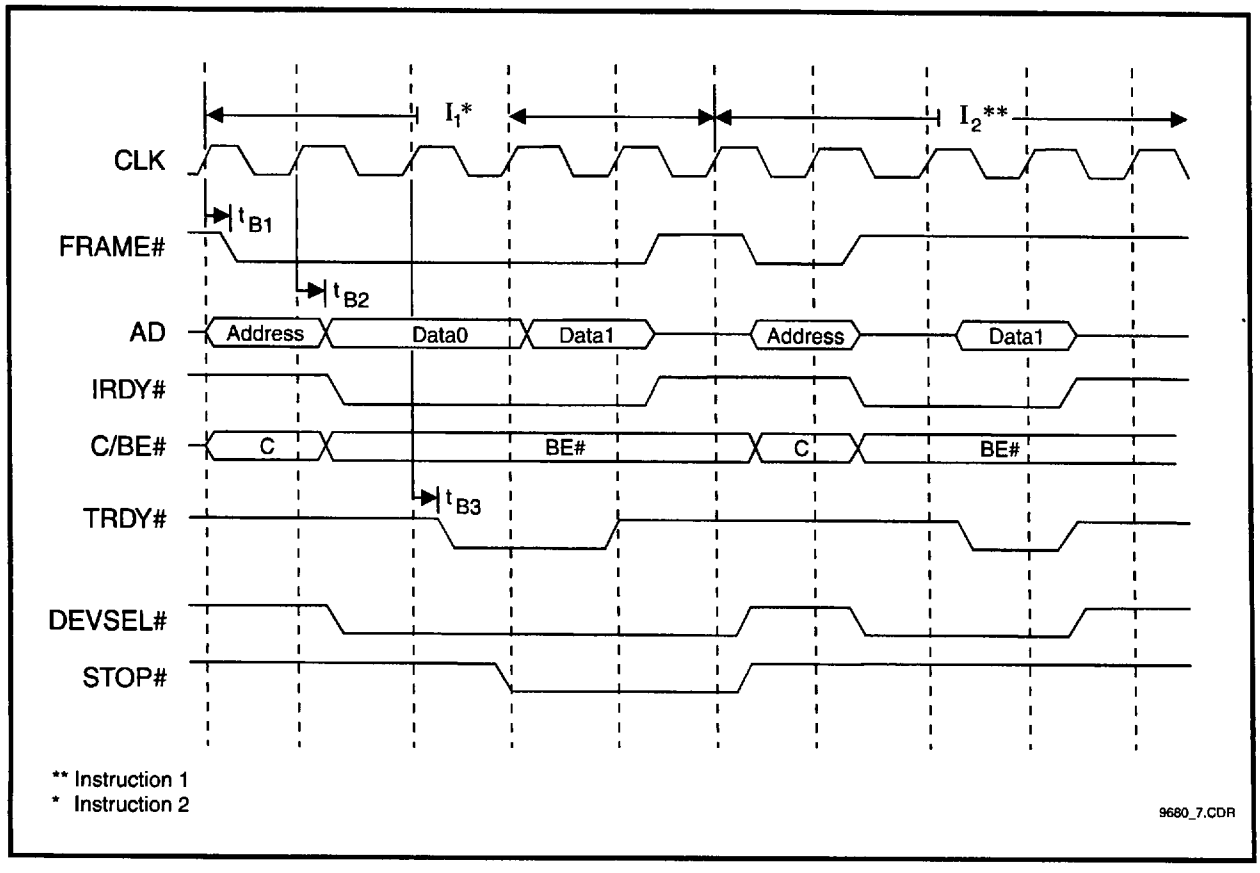

Figure 6-4. PCI Interface Timing

Table 6-6. PCI Interface Timing

Definition	Symbol	Min	Max
Clock rising edge to address/control delay (PCI)	t_{B1}		23ns
Clock rising edge to address/control hold (PCI)	t_{B2}	0ns	
Clock rising edge to ADEN#, DTEN# and TRDY# delay (PCI)	t_{B3}		10ns

6.3.5 DRAM Read Timing

The TGUI9680 controller supports regular fast page mode DRAM with page cycle time as short as 25ns because the MCLK can be as high as 80 MHz. For the nominal 40ns page cycle DRAM (70ns access time), the memory bandwidth is much less and the MCLK can only be 50 MHz. Regardless of the MCLK frequency, the timing for the regular DRAM is shown in Figure 6-5 when operating as graphic mode, using MCLK as reference. Note that the RAS precharge time, RAS access time, and the duty cycle of the page cycle can all be adjusted by software.

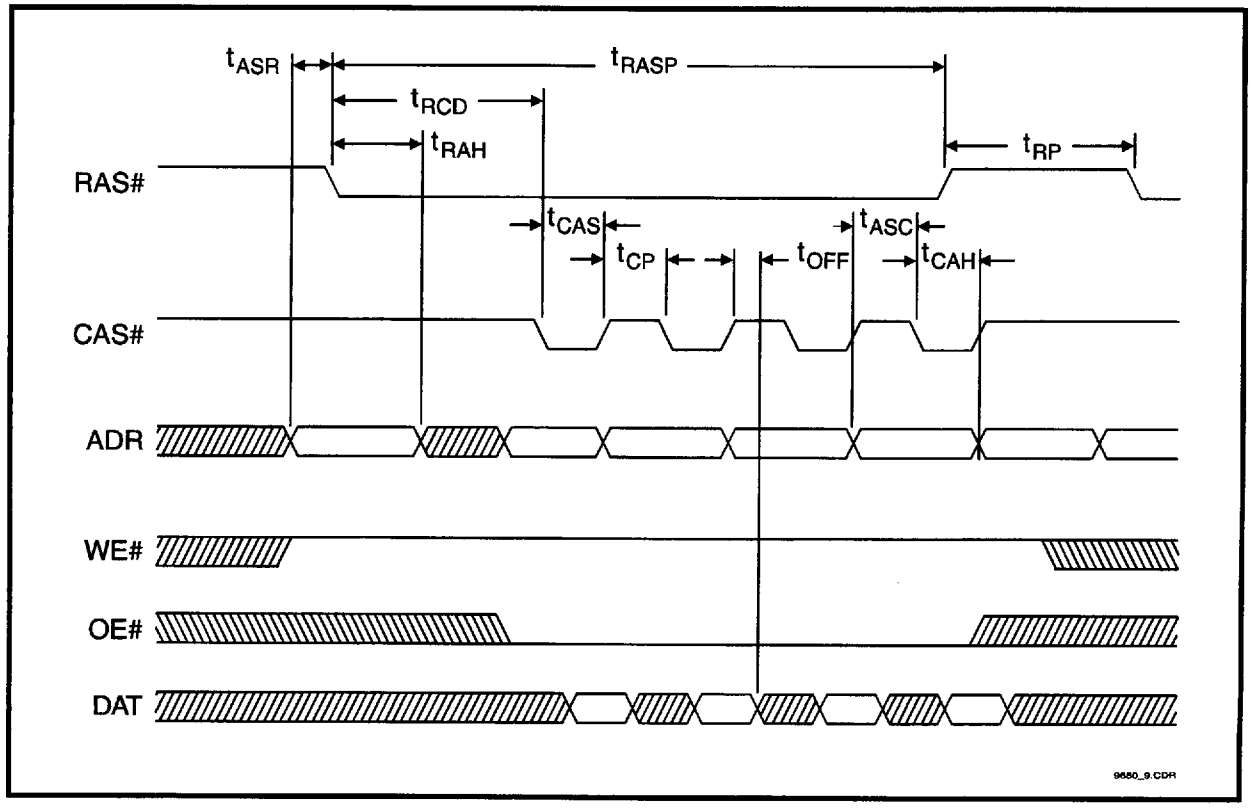

Figure 6-5. DRAM Read Timing

Table 6-7. DRAM Read Timing Cycle

	DRAM Speed (Memory Clock)	80ns (50.35 MHz)			70ns (57.27 MHz)			60ns (67.20 MHz)			45ns (77.00 MHz)		
	Temperature	0°C	50°C	70°C	0°C	50°C	70°C	0°C	50°C	70°C	0°C	50°C	70°C
Symbol	Voltage	4.75V	5V	5.25V	4.75V	5V	5.25V	4.75V	5V	5.25V	5V	5V	5V
t_{RASP}	RAS# Pulse Width	76	76	75	68	66	66	58	54	54	45	46	47
t_{RP}	RAS# Precharge Time	83	83	85	74	73	73	62	63	63	55	55	55
t_{RCD}	RAS# to CAS# Delay	56	56	56	48	48	48	43	41	42	34	34	34
t_{CAS}	CAS# Pulse Width	16	18	18	14	14	12	11	11	10	10	10	10
t_{CP}	CAS# Pulse Width	20	22	22	18	16	15	17	18	17	13	14	14
t_{ASR}	Row Address Setup Time	82	85	82	56	53	53	43	43	48	33	33	34
t_{RAH}	Row Address Hold Time	34	32	33	28	28	28	26	24	24	14	14	14
t_{ASC}	Column Address Setup Time	20	21	21	16	19	19	18	16	18	12	12	12
t_{CAH}	Column Address Hold Time	17	16	16	14	13	13	10	10	10	10	10	10

6.3.6 DRAM Write Timing

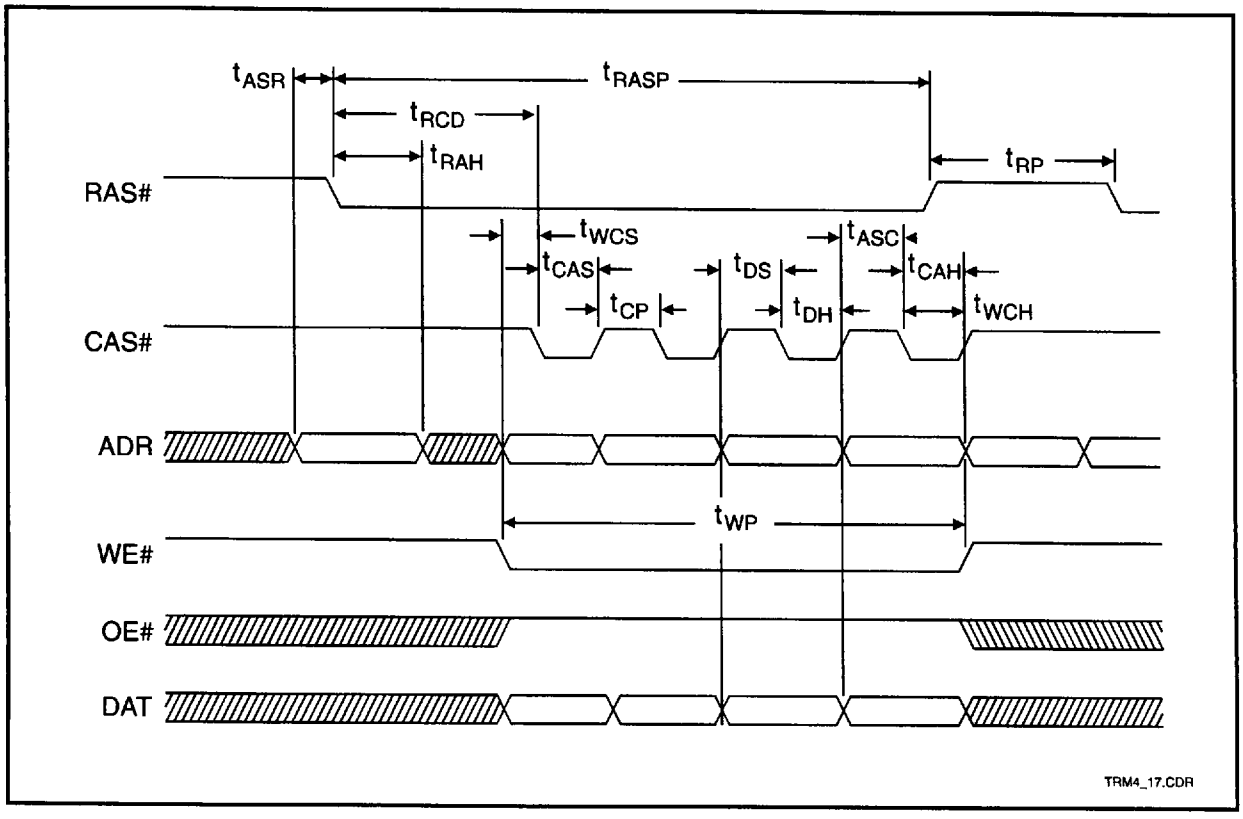

Figure 6-6. DRAM Write Timing

Table 6-8. DRAM Write Timing Cycle

	DRAM Speed (Memory Clock)	80ns (50.35 MHz)			70ns (57.27 MHz)			60ns (67.20 MHz)			45ns (77.00 MHz)		
	Temperature	0°C	50°C	70°C	0°C	50°C	70°C	0°C	50°C	70°C	0°C	50°C	70°C
Symbol	Voltage	4.75V	5V	5.25V	4.75V	5V	5.25V	4.75V	5V	5.25V	5V	5V	5V
t_{RASP}	RAS# Pulse Width	75	75	75	66	66	66	56	56	54	45	45	45
t_{RP}	RAS# Precharge Time	83	83	84	72	72	73	64	63	64	54	54	55
t_{RCD}	RAS# to CAS# Delay	57	58	56	48	50	49	42	44	41	33	34	33
t_{CAS}	CAS# Pulse Width	16	16	16	16	14	14	10	10	12	10	10	11
t_{CP}	CAS# Pulse Width	23	24	21	16	20	19	18	19	18	14	14	14
t_{ASR}	Row Address Setup Time	60	61	60	56	52	52	44	43	45	34	34	33
t_{RAH}	Row Address Hold Time	34	34	33	30	30	30	25	25	25	19	19	18
t_{ASC}	Column Address Setup Time	20	22	20	18	18	18	16	18	17	8	10	10
t_{CAH}	Column Address Hold Time	15	14	14	14	13	12	10	12	10	10	10	10
t_{WCS}	Write Command Setup Time	37	21	20	16	13	14	15	14	15	8	8	8
t_{WCH}	Write Command Hold Time	19	16	19	20	12	12	15	15	14	13	13	13
t_{WP}	Write Command Pulse Time	40	39	39	36	35	35	30	29	29	23	24	24
t_{DS}	Data In Setup Time	23	21	23	14	18	18	14	17	18	10	9	10
t_{DH}	Data In Hold Time	15	17	16	16	11	11	10	8	9	8	8	9

6.3.7 Vertical Timing

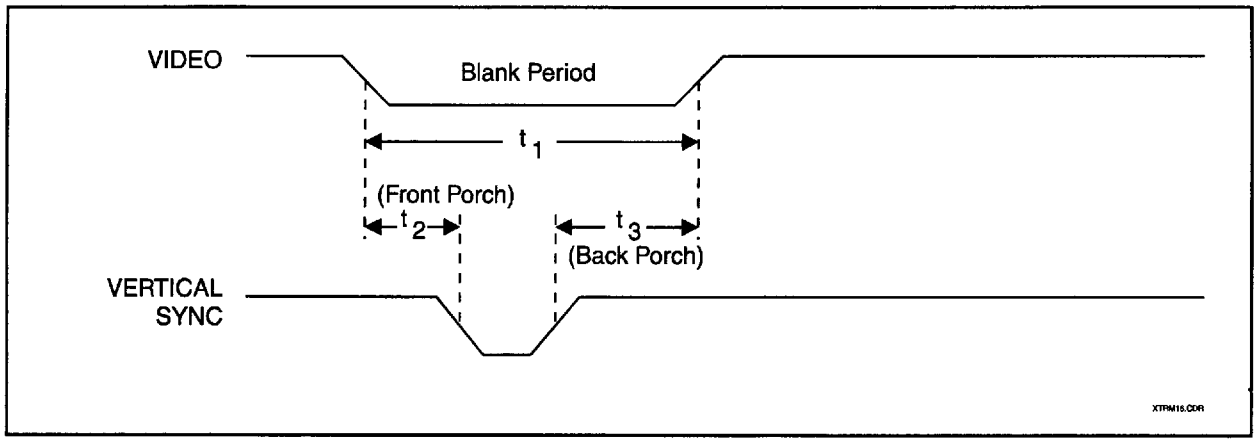

Figure 6-7. Vertical Timing Diagram

Table 6-9. Vertical Timing (μ sec)

Display	Refresh Rate (Hz)	t_1 (ms)	t_2 (ms)	t_3 (ms)	VESA Std.
640 x 480	72	1.057	0.238	0.740	Y
640 x 480	75	0.533	0.027	0.427	Y
640 x 480	85	1.000	0.244	0.711	N
800x600	60	0.739	0.026	0.607	Y
800x600	75	0.533	0.021	0.448	Y
1024x768	60	0.786	0.062	0.600	Y
1024x768	70	0.673	0.053	0.513	Y
1024x768	87i	0.696	0.014	0.563	N
1028x1024	87i	0.900	0.238	0.559	N
1028x1024	60	0.715	0.093	0.529	N
1600x1200	96i				N

6.3.8 Horizontal Timing

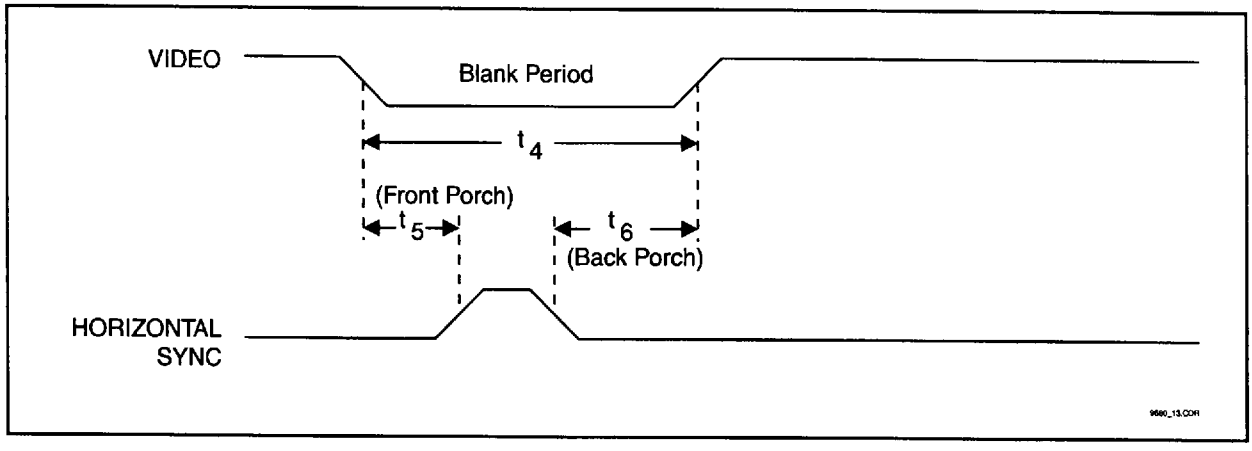

Figure 6-8. Horizontal Timing Diagram

Table 6-10. Horizontal Timing (μ sec)

Display	Refresh Rate (Hz)	t_4 (ms)	t_5 (ms)	t_6 (ms)	VESA Std.
640 x 480	72	5.095	0.762	4.063	Y
640 x 480	75	6.349	0.508	3.810	Y
640 x 480	85	4.444	0.444	1.333	N
800x600	60	6.400	1.000	2.200	Y
800x600	75	5.172	0.323	3.232	Y
1024x768	60	4.923	0.369	2.462	Y
1024x768	70	4.053	0.320	1.920	Y
1024x768	87i	5.350	0.180	1.250	N
1028x1024	87i	3.626	0.213	1.173	N
1028x1024	60	3.927	0.582	2.327	N
1600x1200	96i				N

6.3.9 BIOS Access Over VL Bus Timing

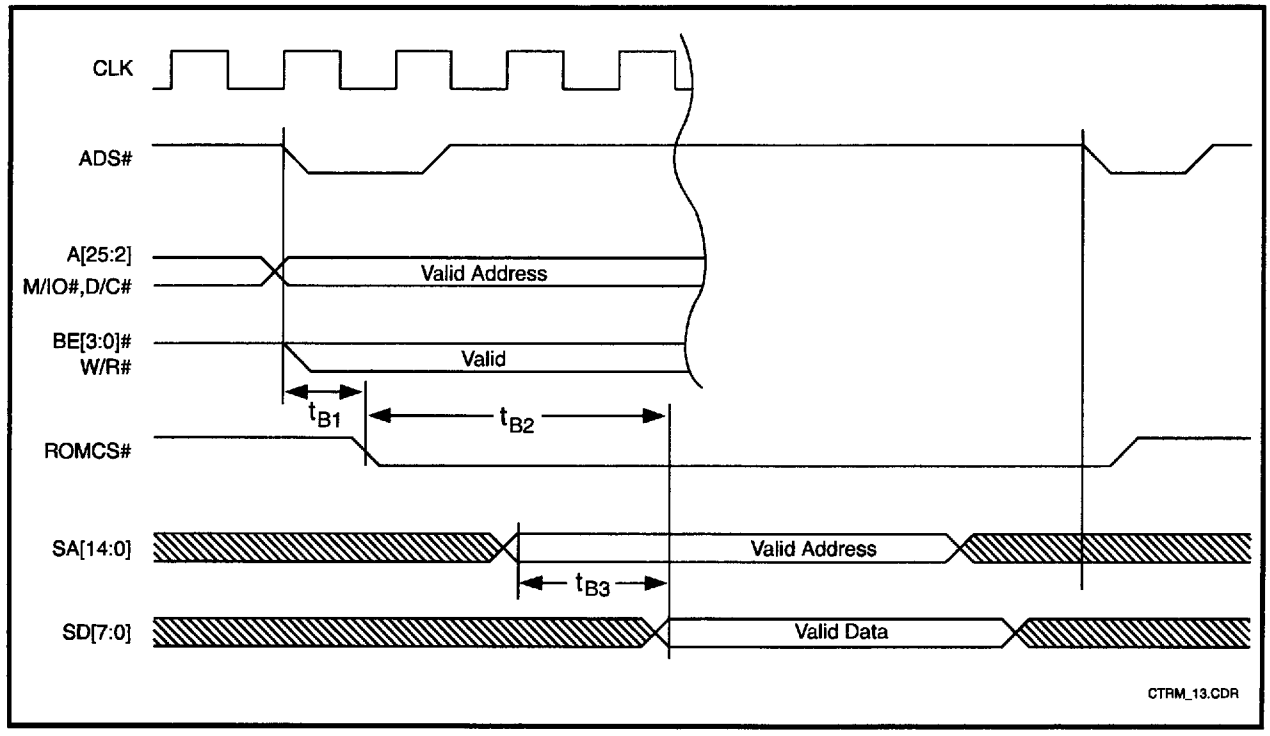

Figure 6-9. BIOS Access Over VL Bus Timing

Table 6-11. BIOS Access Over VL Bus Timing

Symbol	Description	Min (ns)	Max (ns)
t_{B1}	ROMCS# to VL Bus Address.		8
t_{B2}	ROMCS# to Data Valid.	68	
t_{B3}	ISA Address to Data Valid.	50	

6.3.10 PCI ROM BIOS Access Timing

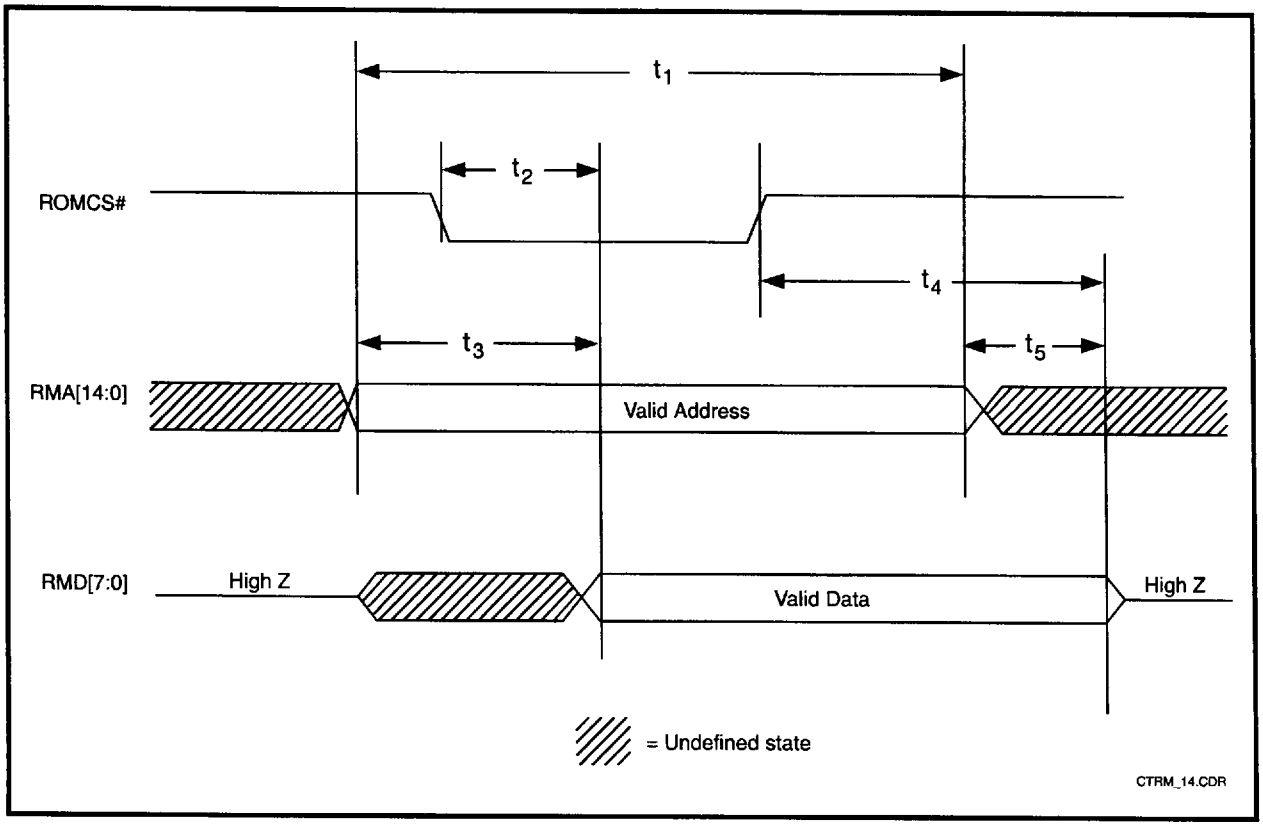

Figure 6-10. PCI ROM BIOS Access Timing Diagram

Table 6-12. PCI ROM BIOS Access Timing

Symbol	Description	Min (ns)	Typ (ns)	Max (ns)
t_1	Cycle time.		32 DMCLKs	
t_2	Chip enable access time.			150
t_3	Address access time.			150
t_4	Data to high Z delay time.			85
t_5	Valid data from invalid address hold time.	10		

6.3.11 EDO DRAM Timing

The TGUI9680 controller supports hyperpage or extended data out (EDO) DRAM. The EDO DRAM behaves the same as the regular DRAM, except that during memory read operation, memory data will hold until next CAS# falling edge, extended memory output data hold time. This will allow MCLK to run at high frequency without worrying about the memory access setup and hold time. Figure 6-11 shows the timing for the EDO memory operation.

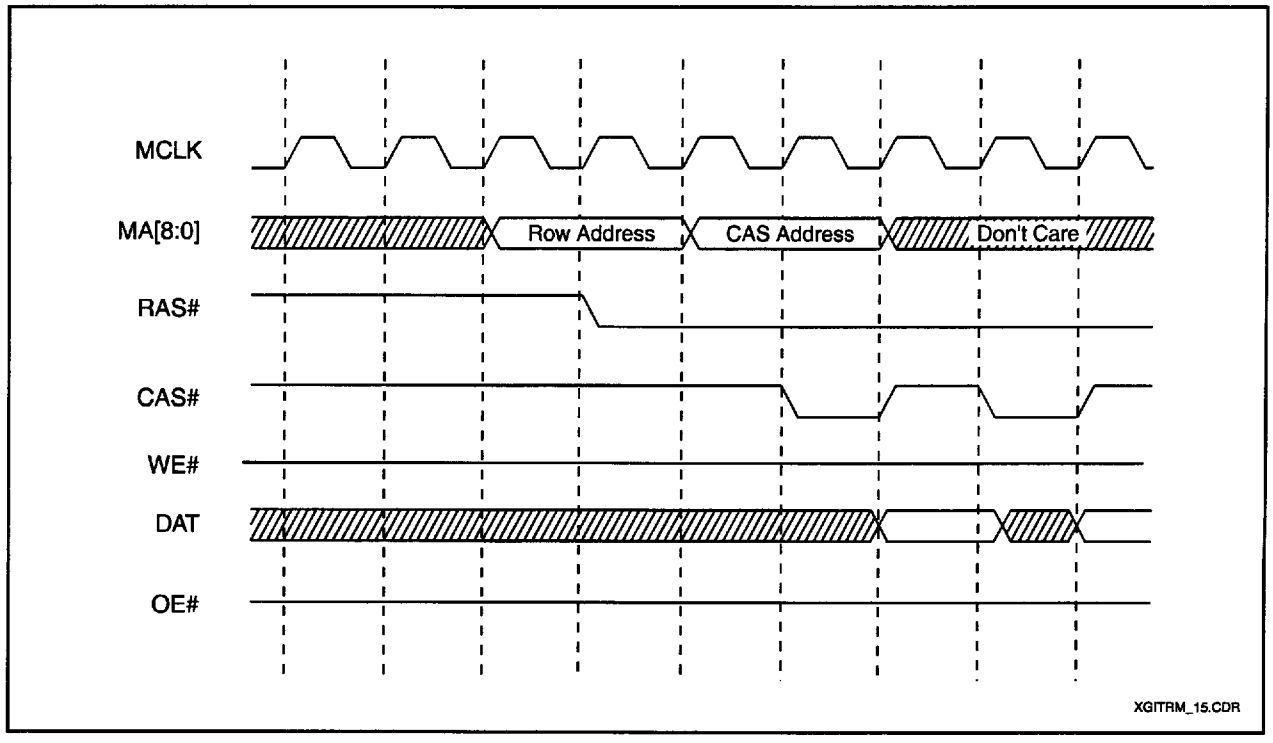

Figure 6-11. EDO DRAM Read Timing

6.3.12 WRAM Timing

The TGUI9680 controllers can support a new type of memory, DRAM–WRAM. As with VRAM, WRAM has a random port and a serial port. To support WRAM, the original 64-bit memory data is split into two sections: 32-bit interleaved random port and 32-bit serial port. The serial port can only be applied to the packed pixel modes; the text modes and planar modes are still operated from the random port. When operating as packed pixel modes, the pattern for the hardware cursor for the packed pixel modes are still accessed from the random port for ease of implementation. Because the TGUI9680 controller can support WRAM page cycle time as short as 25ns, the peak interleaved random port memory write bandwidth can be as high as 160 MB/sec, independent of the color resolution modes. Figure 6-2 shows the timing for the interleaved random port for memory write operation. Detailed memory and interface timing will be published separately. Table 6-1 shows the bandwidth of different types of memory that can be supported by the TGUI9680 controller.

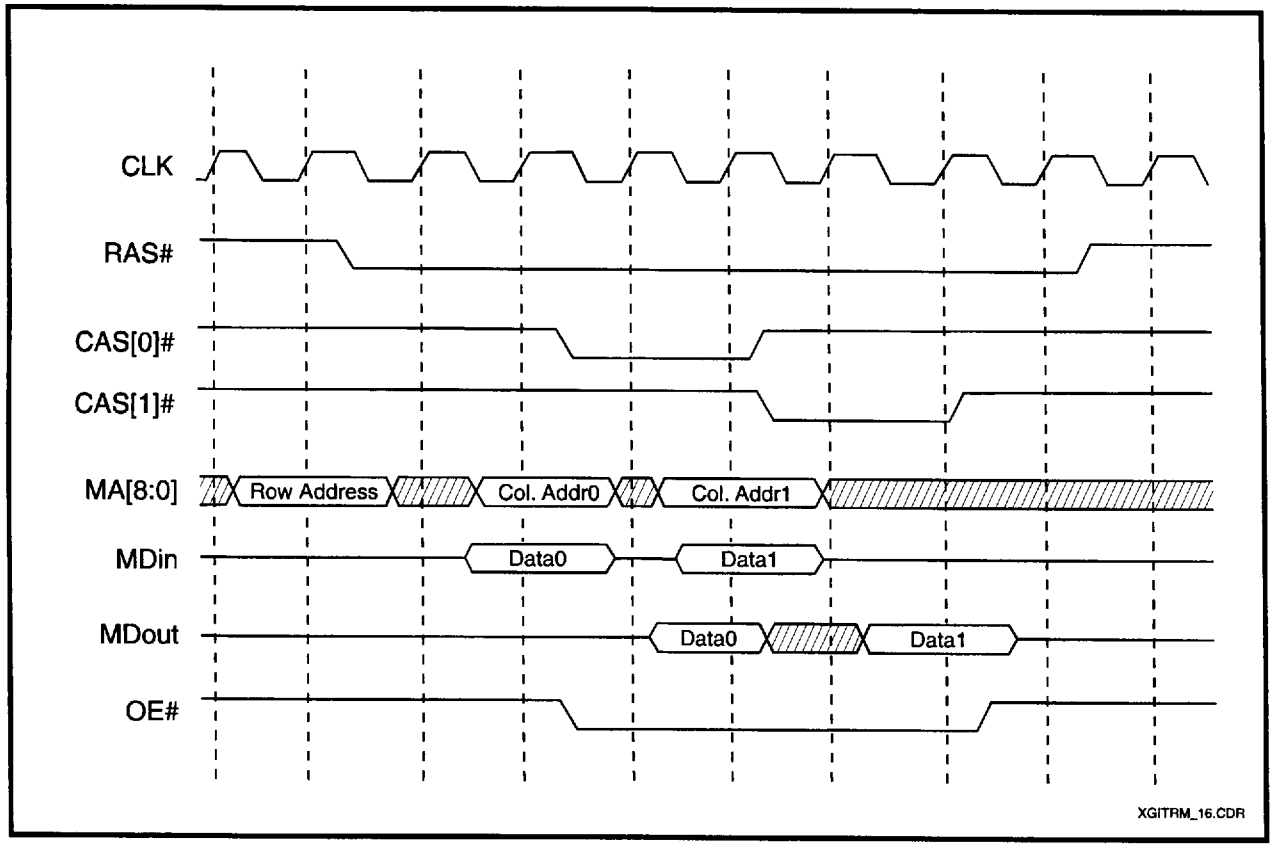

Figure 6-12. WRAM Random Port Write Timing