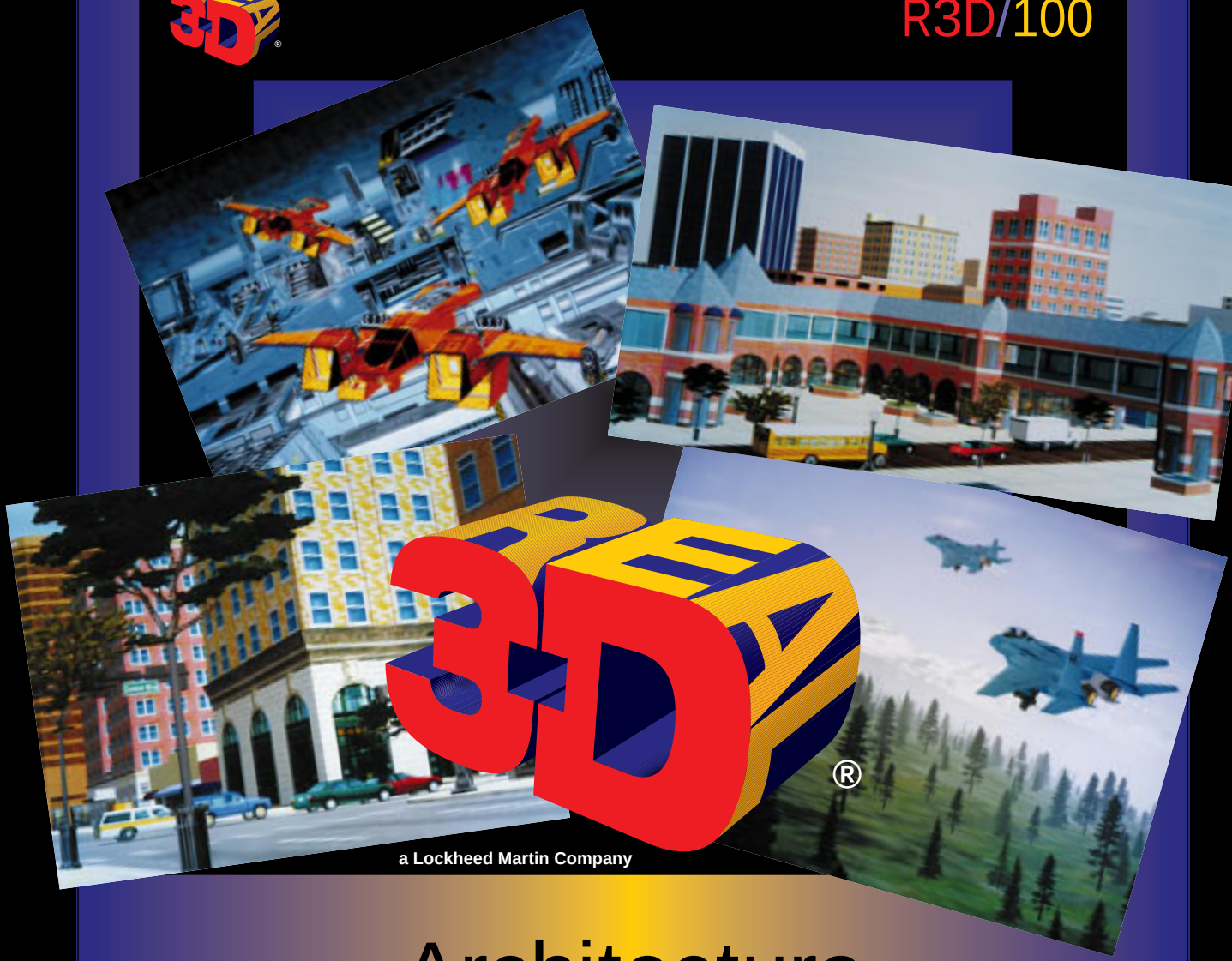
R3D/100



Architecture Overview

Ultimate Graphic Performance for the PC

Real 3D R3D/100

Architecture Overview

November 1996

Version 2.2

a Lockheed Martin Company

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Introduction

Built on a vast foundation of graphics experience traceable to 1962, the R3D/100 chip set is **Real 3D**'s new real-time graphics engine for the personal computer market. Years before the current explosion in personal computer 3-D graphics, special operations aircrews, tank personnel, ship bridge officers, and astronauts trained on the predecessors to the **Real 3D** graphics engines. These high-fidelity simulators furnished three-dimensional, photo-realistic virtual environments with no restrictions on how fast, how far, or where they traveled. This is the realm of real-time graphics – realistic detail combined with real-world dynamic response. This is the heritage of the **Real 3D** product line.

The R3D/100 chip set is the first PC product in this series, and the first 3-D graphics accelerator to bring true real-time performance to this platform. This architecture overview for engineering managers and system architects describes the **Real 3D** R3D/100 3-D graphics accelerator and suggests a range of applications this product can serve. Detailed information on the R3D/100 product is provided in the *R3D/100 Data Manual* and the *R3D/100 Programmer's Guide*.

Features

The R3D/100 product consists of a tightly integrated two-chip solution providing high throughput, high realism, and sustained real-time response that software solutions and other hardware solutions cannot achieve. To accomplish this, the R3D/100 chip set incorporates the following features:

- 32-bit PCI local bus interface running at up to 33.33 MHz
- Rasterization of drawing primitives in hardware for higher throughput
- Perspective divide of texture coefficients for correct transformation of texturing in hardware
- Direct addressing of on-board texture storage for superior throughput of mipmapped textured polygons
- Robust algorithms for texture filtering to remove aliasing effects
- On-chip setup and computation of Gouraud shading, depth, and fog for enhanced realism

- Advanced rendering features such as alpha testing, stenciling, and color blending
- Full depth buffering allowing freedom of movement of eyepoint and all objects and simpler/faster database design
- Rendering into multiple 3-D windows which can overlay/underlay 2-D windows
- Easy interface to external components such as phase-locked loop and digital to analog converter
- Software driver package based on the OpenGL® installable client driver and mini-client driver for Microsoft's Windows NT™ operating system

Applications

The only limit to the application of **Real 3D** technology is your imagination. The R3D/100 chip set can enhance any computer graphics application and complement a wide array of system configurations. Major applications include, but are not limited to:

- 3-D Animation
- Virtual Reality
- Telepresence
- Gameware
- Modeling
- CAD
- Medical Applications
- Part-task Training
- 3-D Reconstruction
- Simulation/Training
- Stereo Helmet-Mounted Displays
- Architectural Walk-throughs
- Object/Engineering Design
- Scientific Visualization
- Workstation-class Graphics
- Distributed Interactive Entertainment

Figure 1 shows a 3-D rendering window within a 2-D screen, a typical application for the R3D/100 chip set.

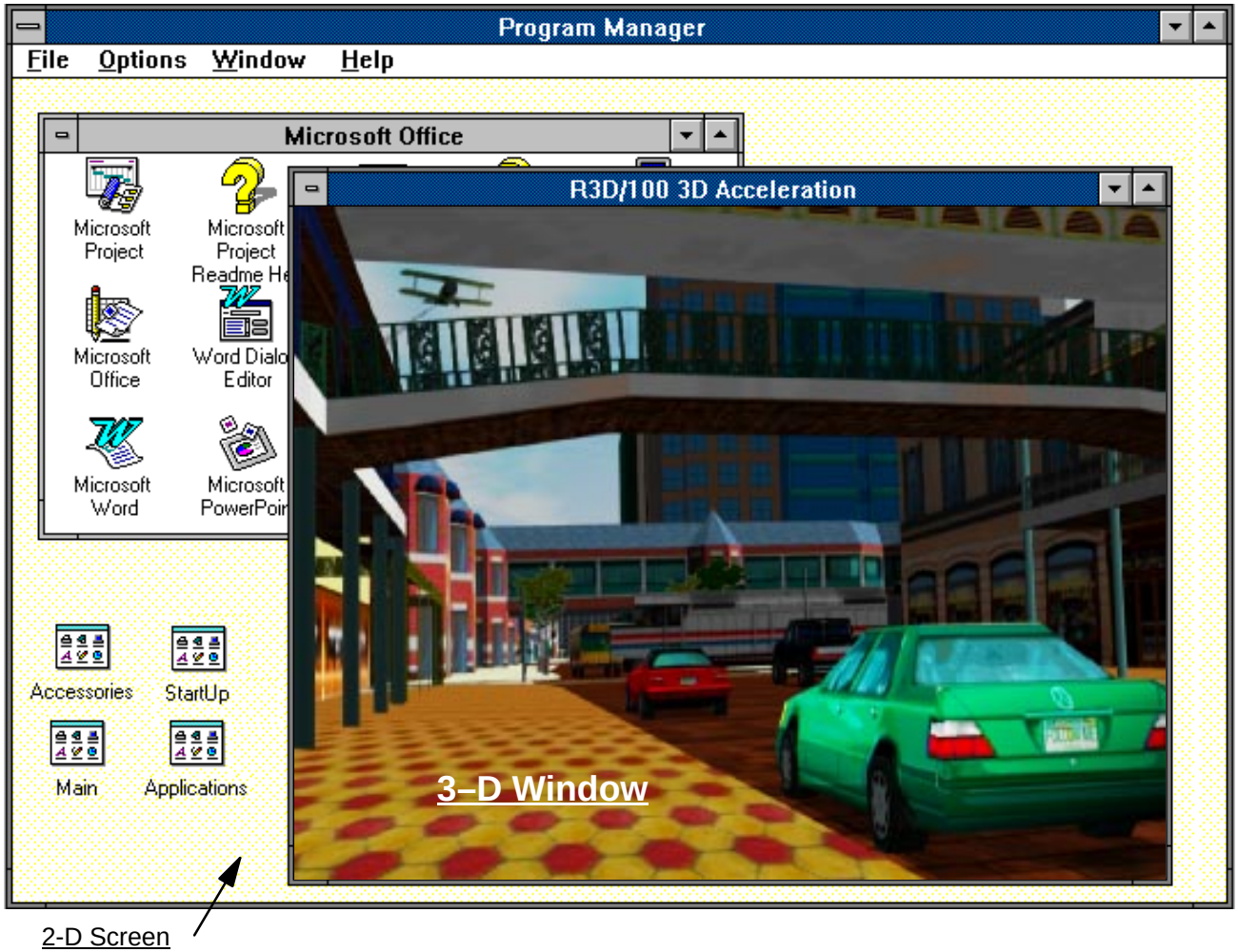

Figure 1. 3-D Rendering Window within 2-D Screen

Rendering Performance

The R3D/100 chip set has the following peak rendering performance:

- 750K 3-D triangles per second (25 pixel polygons, 32-bit RGBA with Gouraud shading, depth buffering, fogging, stenciling, color blending, and non-mipmapped texturing)
- 1.5M 3-D line strips per second (10 pixel lines, 32-bit RGBA with depth buffering, fogging, color blending, and stenciling)
- 33M pixel writes per second (Gouraud shaded, Z-buffered, fogged, color blended, with bi-linear filtered mipmapped texturing)
- 16M pixel writes per second (Gouraud shaded, Z-buffered, fogged, color blended, with tri-linear filtered mipmapped texturing)
- 133 MBytes per second rectangular fill, write, or read accesses to the depth and frame buffer
- 135M pixels/second (at 24 bits per pixel) video output rate (supports 1280 x 1024 non-interlaced resolution at 75 Hz refresh)

Architecture

R3D/100 Internal Components

The R3D/100 chip set consists of two devices. Figure 2 presents the interconnection of the internal processors/controllers.

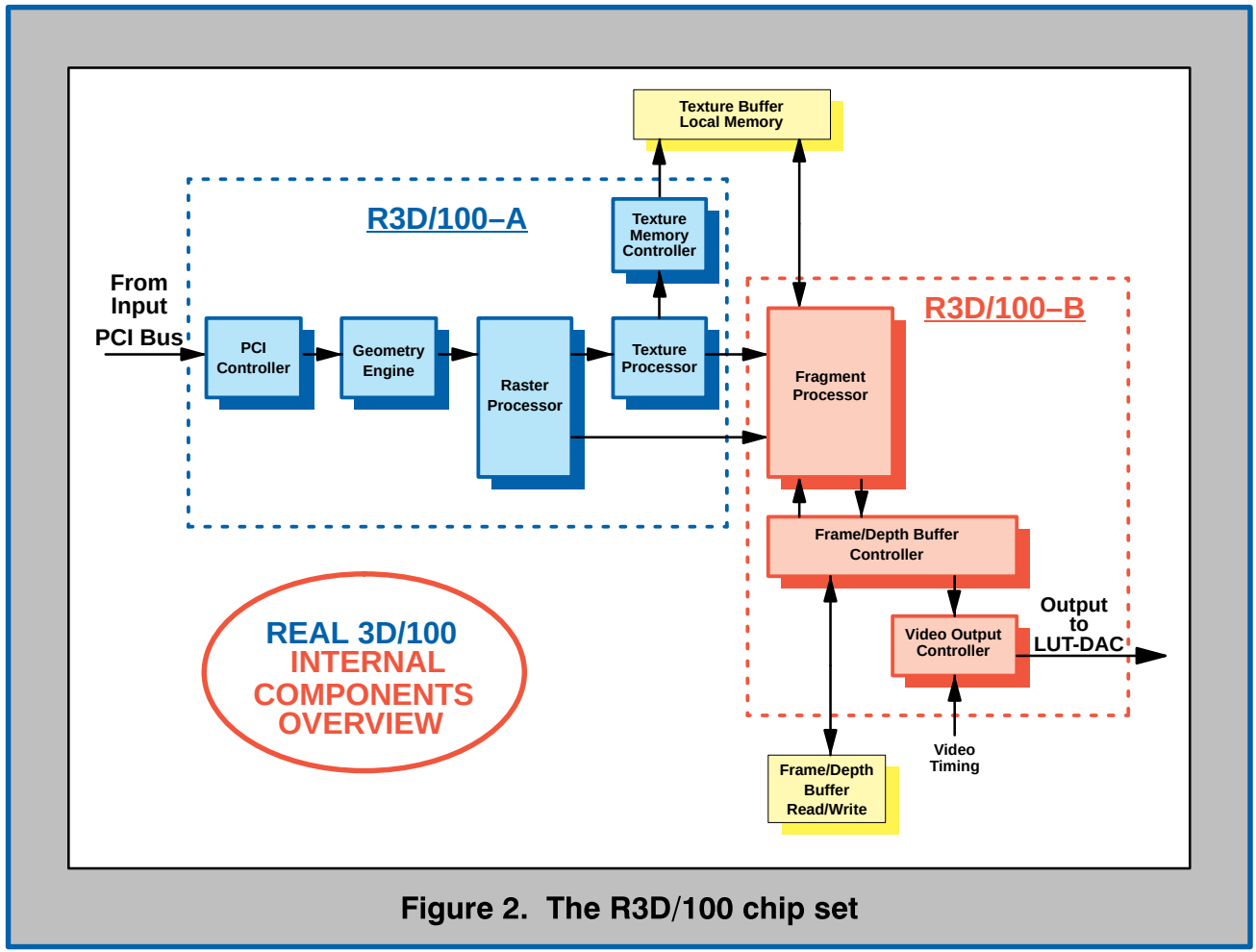

Figure 2. The R3D/100 chip set

PCI CONTROLLER

The PCI controller provides a fully compliant 32-bit PCI (Peripheral Component Interconnect) local bus interface operating at up to a 33.33 MHz clock rate. It is capable of providing single-cycle transfers in target and master modes of operation. In addition, burst direct memory access (DMA) mastering capability is provided to optimize data transfers. The DMA supports scatter/gather capability. A set of three FIFOs has been included on the chip set to provide highly efficient data buffering between the R3D/100 graphics core and the host CPU. The R3D/100 chip set supports both little- and big-endian processors by supplying hardware byte swapping of those formats to/from the chip set's internal format.

The PCI controller provides a set of configuration space registers that initialize to a default condition at power-up, making the R3D/100 chip set fully Plug and Play compliant. These registers may be reconfigured by the device driver, and contain the configuration values required by the Microsoft Windows NT™ 3.51 operating system.

The PCI controller provides an individual interrupt enable capability, providing applications with critical timing information such as display frame synchronization and read/write frame buffer primitive status.

GEOMETRY ENGINE

The geometry engine provides a RAM and ROM-based microcode sequencer which processes the following drawing primitives:

- Linestrips
- Linelists
- Tristrips
- Trilists
- Quadstrips
- Quadlists

The geometry engine consists of a numerical processor with scratchpad memory, fixed/floating point multiplier and adder, and $^1/_N$ functions providing100 MFLOP performance.

The ROM programming in the geometry engine performs various drawing primitive setup calculations, including texture level-of-detail (LOD) coefficients and data formatting.

A FIFO is provided at the output of the geometry engine to provide load balancing capability between it and the raster processor.

RASTER PROCESSOR

The raster processor is a true polygon/line rasterizer. It is designed to perform all gradient calculations for the rasterization process while requiring only vertex position, depth, color, and texture coordinate data from drawing primitives received from the geometry engine. This significantly reduces the load on the host CPU. This also has the added benefit of reducing the drawing primitive 'per vertex' bandwidth requirements between the host CPU and the R3D/100 chip set over the PCI Bus, allowing more usable bandwidth for additional rendering primitives.

The application of texture maps onto polygons in real-time has been one of the most significant advances in 3-D computer graphics in recent years. Texture mapping applied to a relatively few polygons can produce very realistic looking images. However, if texture mapping is not performed in true perspective, the resultant images will look distorted and have visually distracting artifacts. The R3D/100 raster processor provides true perspective-corrected texture coordinate calculations and texture LOD calculations for each fragment (pixel) created.

The raster processor can provide Gouraud shading for polygon and line drawing primitives. This is performed by interpolating between the RGBA color intensities specified per vertex. This allows lighting models to render multi-faceted prisms as if they were smooth cylinders, thus tremendously increasing scene realism.

The raster processor provides depth and fog factor values for each fragment produced by interpolating between depth and fog factor values specified per vertex. The depth value allows hidden-surface removal to be performed by the fragment processor. The fog value per pixel allows depth cueing and atmospheric effects.

TEXTURE PROCESSOR

The texture processor is at the heart of the realistic 3-D graphics that can be produced by the R3D/100 chip set.

While rendering drawing primitives, the texture processor receives the perspective-corrected texture coordinate values from the raster processor for each fragment created for a given drawing primitive. It also receives a texture LOD value for each fragment. These values, along with the texture filter mode selected (per-drawing primitive) for the texture map, allow the texture processor to calculate the addresses for the texture buffer controller. The texture LOD value allows the use of mipmapping and tri-linear interpolation, which gives far superior results to point sampled texturing.

In-between rendering drawing primitives, the texture processor can generate texel addresses for dynamic texture map loading for those applications that exceed the available texture buffer memory capacity. If so desired, an application can insert texture map 'load' primitives between drawing primitives and set up one of the chip set's PCI DMA controllers to automatically control the transfer of the texture map into the texture buffer. Texel addresses are generated automatically for each incoming texel based upon texture map attribute data received from the application.

TEXTURE BUFFER CONTROLLER

Because of the stringent storage and fast access requirements of texturing, the inherent differences between texel addressing versus pixel addressing in the frame buffer, and the performance requirements of the R3D/100 chip set, a completely separate and independent texture buffer memory interface and controller have been incorporated.

The texture buffer controller provides the read/write access with the on-board texture buffer using the address generated by the texture processor. Due to the unique topological nature of texture maps, the texture buffer controller uses a proprietary caching approach that minimizes cache misses, achieving more usable textured pixel write capability than other approaches.

The texture buffer controller is designed to support 0 to 8 MBytes of on-board CDRAM storage for the texture buffer, offering the system architect a variety of configurations options.

FRAGMENT PROCESSOR

The fragment processor performs all of the per-fragment (pixel) tests and color calculations that are required for high-quality 3-D rendering. These are implemented in a high-speed dedicated graphics pipeline for maximum throughput. These tests and calculations are discussed in the sections that follow.

Texture Antialiasing

The texture processor supports four modes of texture antialiasing, which can be selected on a per-drawing primitive basis for maximum flexibility. These are described in Table 1.

Table 1. Texture Antialiasing Modes

Texel Smoothing Mode	MIP LOD Smoothing Mode	System Clock Cycles (minimum)		Advantages
		16-bit	32- bit	
Nearest Neighbor	Nearest	1	1	Lowest memory requirements, highest performance
Nearest Neighbor	Linear Blending	2	2	Blends linearly between two closest LODs for reduced transitional aliasing
Bi-linear Interpolation	Nearest	1	2	Blends between four closest texel samples for reduced spatial aliasing
Bi-linear Interpolation	Linear Blending	2	4	(Tri-linear interpolation) Blends both between texel samples and closest LODs for highest quality

Number of memory cycles are shown for 16 bit/texel and 32 bit/texel operation. The rated peak performance of 33M pixels per second write/fill rate must be divided by the number of memory cycles shown above in the best case (for applications using texture mapping). In the worst case, accesses to the texture buffer result in Row Address Strobe (RAS) cycles that require up to four memory cycles per texel accessed.

Texture Modulation and Blending

Texture modulation and blending provides the ability to use the texels from a texture map directly as colors to be painted on the surface being rendered, modulate the non-textured color

of the surface, or blend the texel color with the non-textured color of the surface. It may be applied using a texture map with RGB components or with RGBA components and is selectable on a per-drawing primitive basis.

Fog

Fogging is an effect used to provide a more realistic appearance to 3D-rendered images. It can be used to simulate atmospheric effects such as smoke, haze, or fog, making objects fade into the distance, and providing visibility cues.

Drawing primitives sent to the R3D/100 chip set can include a fog factor intensity value at the vertex level. The fog factor is interpolated by the raster processor for each fragment to be output to the fragment processor. The fragment processor provides a fog blend equation that uses the fog factor to blend between the fragment color and the fog color.

Fog color can be specified by a state variable on a per-drawing primitive basis. The fog calculation may also be enabled/disabled on a per-drawing primitive basis.

Alpha Test

The alpha test provides the ability to test fragment alpha values against a user-specified alpha reference value. Typically, the alpha test can provide a simple way of providing drawing primitive translucency.

The alpha test compares the fragment's calculated alpha value to a reference value and, based on the compare, accepts or rejects the fragment. The compare can be *never, always, less than, less than or equal, equal, not equal, greater than or equal,* or *greater than.* Based on the result of the test, the fragment's RGBA color data will be written into the frame buffer or discarded. This test can be enabled or disabled on a per-drawing primitive basis.

Stencil Test

The stencil test is useful in overlay applications such as masking out an irregularly shaped area of the frame buffer or creating concave polygons.

The stencil test compares values in the stencil buffer, corresponding to the pixel location of the fragment being tested, with a reference value. Based on the result of the test, the fragment's

RGBA color data can be written into the frame buffer or discarded. The compare can be *never, always, less than, less than or equal, equal, not equal, greater than or equal,* or *greater than.* The stencil buffer contents can be modified on the basis of one of three possible conditions: stencil test fail, stencil test pass and depth test fail, or stencil test pass and depth test pass. Each of these three conditions can be set up independently to *keep, zero out, replace, increment, decrement,* or *invert* the current value in the stencil buffer at the fragment location. Also a bit mask is provided that is 'ANDed' with the value in the stencil buffer before the stencil test is performed. The R3D/100 chip set supports 0-, 5-, or 8-bit stencil configurations. This test can be enabled or disabled on a per-drawing primitive basis.

Depth Test

The depth test provides a very powerful 3-D graphics rendering capability. It provides the capability for hidden-surface removal (three-dimensional occulting). It also provides simpler database generation by allowing inter-penetration of surfaces, thus providing the ability to create more complex and realistic objects with fewer polygons.

The depth test compares the incoming fragment's Z value with the Z value residing in the depth buffer at the same pixel location. Based on the compare, the fragment's RGBA color value can be written into the frame buffer or discarded. Additionally, the fragment's Z value can be written into the depth buffer at the corresponding pixel location if the depth buffer is enabled for modification. The compare can be *never, always, less than, less than or equal, equal, not equal, greater than or equal,* or *greater than.* The R3D/100 chip set supports 0-, 16-, or 24-bit Z configurations. This test can be enabled or disabled on a per-drawing primitive basis.

Color Blending

Color blending (a.k.a. alpha blending, or just blending) provides an advanced 3-D rendering capability that allows the RGBA color value of the fragment being processed to be combined with that of the fragment(s) previously processed and stored in the frame buffer. This color blending is the mainstay in techniques such as painting, digital composition, and transparency.

The color blend function combines (blends) the incoming fragment's RGBA values with the corresponding values in the frame buffer based upon per-drawing primitive-selected blend

factors. The blend factors can be selected independently for the incoming (source) fragment and the current (destination) fragment stored in the frame buffer. Each color component of the source fragment is multiplied by the corresponding source blend factor component. The same types of calculations are performed on the destination fragment using the selected destination blend factors. The resultant source and blend color values are then added together to form the final RGBA color value to be written into the frame buffer. The color blend operation can be enabled/disabled on a per-drawing primitive basis.

FRAME/DEPTH BUFFER CONTROLLER

The frame/depth buffer controller performs all read and write operations with the frame/depth buffer. The controller is designed to provide the following performance and capabilities:

- Memory read/write access at a peak bandwidth of 1.1 GBytes/second
- Display refresh accesses at a maximum rate of 135M pixels per second
- Programmable frame and depth buffer storage for up to 1280 x 1024 pixels
- Double-buffered frame buffer support
- Stereo frame/depth buffer support
- Programmable frame and depth buffer pixel widths (bits/pixel)

The frame/depth buffer controller is designed to support up to 10 MBytes of MDRAM for frame buffer and up to 5 MBytes of MDRAM for depth buffer storage. The frame and depth buffers are physically stored in the same set of MDRAMs. They are provided in a flexible organization to allow the system architect several configuration options to meet storage/capability requirements.

VIDEO OUTPUT CONTROLLER

The video output controller (VOC) provides the display interface between the frame/depth buffer and the external digital-to-analog converter (DAC). The VOC is software programmable and supports a wide variety of display resolutions, refresh rates, and RGB pixel widths. RGB pixel widths of 5/5/5, 5/6/5, and 8/8/8 are supported. The VOC uses a reference clock from an external phase-locked loop (PLL) to provide the video clock. The VOC can align to an exter-

nal set of video sync signals or can generate video sync signals internally. A composite blanking signal is also provided as an output. The polarity of all video control signals can be programmed. The VOC outputs pixels at up to a 135M pixel/second rate, using a single 24-bit RGB pixel output or a dual 24-bit parallel pixel output path to minimize actual pixel transfer rates to the DAC. The VOC provides 3-D pixel data valid controls to allow pixel multiplexing of the R3D/100 3-D pixel outputs with a separate 2-D accelerator's pixel outputs to provide for 2-D/3-D pixel merging.

External Interfaces

PCI BUS

Since the R3D/100 chip set provides a fully compliant 32-bit PCI local bus (Rev. 2.1) running at up to 33.33 MHz, there are no requirements for any external logic in hooking up to a 3.3/5V PCI bus from the host. The PCI bus clock is not used as the system clock. Thus, 3-D graphics acceleration is not impacted by operating the PCI bus at speeds less than 33.33 MHz.

TEXTURE BUFFER

The R3D/100 chip set provides direct texture map addressing capability for up to 8 MBytes of texture map storage on board, providing abundant storage for most applications without requiring dynamic texture map paging. Those applications requiring more storage can take advantage of the dynamic texture map update capability that is built into the R3D/100 chip set.

The amount of on-board texture storage is determined by the number and size of Cached DRAM (CDRAM) storage devices provided. The various texture buffer storage options of CDRAMs are shown in Table 2.

Table 2. Texture Buffer Storage Options

Qty of CDRAMs		Amount of	Number of 128 x 128
4M	16M	Texture Storage	16-bit Maps
1	0	0.5 MBytes	16
2	0	1.0 MByte	32
4	0	2.0 MBytes	64
0	1	2.0 MBytes	64
0	2	4.0 MBytes	128
0	4	8.0 MBytes	256

As an example, a single 256 x 256 map requires 64k texture elements (texels), where each texel is represented by one to four bytes (8, 16, or 32 bits/texel). Map sizes can range up to 2048 x 2048 texels for non-mipmapped formats, or up to 512 x 512 texels for mipmapped formats. Rectangular formats are also supported. Note that mipmapped texture requires another $33^1/_3$ percent additional map storage space for all of the coarser LOD maps. Texture maps with borders are supported for applications requiring smooth boundaries between abutting texture maps on a surface. Sixteen-bit map formats include 4/4/4/4 RGBA, 4/6/5 RGB, and 5/5/5/1 RGBA. Thirty-two bit map formats include the above, plus 8/8/8/8 RGBA.

The R3D/100 chip set is designed to interface with industry standard Cached DRAMS (CDRAMs) such as Mitsubishi M5M4V4169 (4 Mbit) or M5M4V16169 (16 Mbit) for the texture buffer. No external bus transceivers are required.

FRAME/DEPTH BUFFER

The frame/depth buffer stores up to 10 MBytes of per-pixel color intensity and up to 5 MBytes of depth information. The frame buffer bit width may be either 16 or 32 bits per pixel. The depth buffer may be either 0, 16, or 32 bits per pixel.

The frame buffer can be configured as a single buffer or as a double buffer (front and back). In the double buffer configuration the frame buffer can operate in a full screen mode to allow page flipping by changing the video start address, or it can operate in a normal windowed GUI mode. Frame buffer width should be selected based on the color fidelity desired. A 16-bit wide frame buffer supports five bits (optionally six bits on green) of intensity resolution per color

component for a total of 32k (64k) colors, while a 32-bit wide frame buffer supports eight bits per color component (RGBA) for a total of 16.7M colors.

Depth buffer width should be selected based on the level of fidelity desired. Systems where the polygons are already sorted in front to back order can eliminate the requirement of depth (Z) values. Systems requiring a depth buffer can select from a 16-bit or 32-bit depth buffer configuration, providing a 16-bit or 24-bit Z value, respectively. In the 32-bit depth buffer configuration, additional storage is provided for parameters such as alpha and stenciling.

The R3D/100 frame/depth buffer architecture is designed to interface with MoSys™ Multibank DRAM (MDRAM). This is an extended performance synchronous DRAM, available in sizes from 0.5 to 2.3 MBytes per package. No external bus transceivers are required.

The R3D/100 chip set supports the resolutions shown in Table 3 when populated as shown. The “Pixel Resolution” describes the 3-D rendering portion of the total display, double buffered, and “Max Update Rate” indicates the image update rate of that region.

This table shows representative display resolutions and is not an exhaustive list of all possible display resolutions. Maximum update rates shown take into account display overhead for 72 Hz refresh, whereas display refresh rates from 30 to 75 Hz (interlaced or non-interlaced) are supported. Single-buffered memory systems can be configured with less total MDRAMs.

Depth complexity is an important measure of system capacity. Like a painter who must paint over portions of the canvas in certain areas, a 3-D renderer must have the capability to write and overwrite portions of the frame buffer. Certain portions of the screen may be written dozens – maybe even hundreds – of times due to the natural occultation of objects. An average depth complexity of three indicates the total number of pixels rendered is three times the number of pixels displayed. This accounts for very high overwrites in small areas, assuming they are balanced by larger areas of one or two writes.

Table 3. Frame/Depth Buffer Resolutions

Pixel Resolution	Number of Colors	Depth Buffer Bits/Pixel	MBytes of MDRAM	Max Update Rate (Hz)*
320 x 200	64k	0	0.25	72.0
320 x 200	64k	16	0.38	72.0
320 x 200	64k	32	0.50	72.0
320 x 200	16.7M	0	0.50	72.0
320 x 200	16.7M	16	0.64	72.0
320 x 200	16.7M	32	0.77	72.0
640 x 480	64k	0	1.28	24.0
640 x 480	64k	16	1.92	24.0
640 x 480	64k	32	2.56	24.0
640 x 480	16.7M	0	2.56	24.0
640 x 480	16.7M	16	3.33	24.0
640 x 480	16.7M	32	3.84	24.0
1024 x 768	64k	0	3.07	12.0
1024 x 768	64k	16	4.61	12.0
1024 x 768	64k	32	6.14	12.0
1024 x 768	16.7M	0	6.14	12.0
1024 x 768	16.7M	16	7.68	12.0
1024 x 768	16.7M	32	9.22	12.0
1280 x 1024	64k	0	5.12	8.0
1280 x 1024	64k	16	7.68	8.0
1280 x 1024	64k	32	10.24	8.0
1280 x 1024	16.7M	0	10.24	8.0
1280 x 1024	16.7M	16	12.80	8.0
1280 x 1024	16.7M	32	15.36	6.5

* Depth complexity = 3 (each pixel is written three times)

DIGITAL-TO-ANALOG CONVERTER

The R3D/100 chip set supports industry standard palette/lookup table LUT-DACs compatible with the Brooktree Bt485 register set. Choice of device depends on the output pixel rate and desired quality. The DAC is programmed through an 8-bit port provided on the R3D/100 chip set.

PHASE-LOCKED LOOP

A high-speed PLL must be provided to synthesize the reference frequencies to the video output controller in the R3D/100-B ASIC to ensure alignment between the 2-D video and the 3-D video. The R3D/100 supports the following PLL devices by providing a 3-bit programming port:

- Motorola MC145170
- Integrated Circuit Systems ICS1522

SYSTEM CLOCK CRYSTAL

The R3D/100 interfaces to an external clock crystal with a frequency of 33.33 MHz. On-chip PLL circuits are provided to generate the various system clock frequencies required by the R3D/100 chip set from the reference clock provided by the crystal.

SIGNAL MERGING (2-D/3-D)

An optional mapping bit in the frame/depth buffer (“3-D Pixel Data Valid”) can be used to define whether the R3D/100 chip set output has priority over the 2-D accelerator output on a per-pixel basis. This allows 2-D overlays and separate 3-D rendering contexts within the available frame/depth buffer screen space.

Both an analog and a digital merge solution are possible. The analog solution can utilize a fast color keying compare circuit and video-speed multiplexers. A specific color present in the 2-D output would key the multiplexer to select the 3-D output from the R3D/100. The digital solution would receive both the 2-D and the 3-D digital bitstreams, and based on selection logic, output multiplexed pixels to a high-speed DAC. DACs of this type are just now becoming available. Additional information on providing signal merging will be provided in the *R3D/100 Application Notes*.

Example Configurations

The R3D/100 graphics accelerator chip set allows the system architect the freedom to implement a wide variety of configurations.

Figure 3 shows an external 2-D graphics accelerator card connected to a dedicated 3-D accelerator card with a video cable. Figure 4 shows a single board with both 2-D and 3-D graphics accelerators driving an advanced LUT-DAC which merges the two (digital) signals. Figure 5 shows a stand-alone 3-D graphics accelerator board. These are representative of interface methods, and by no means demonstrate all possible configurations. More information will be provided in the *R3D/100 Application Notes*.

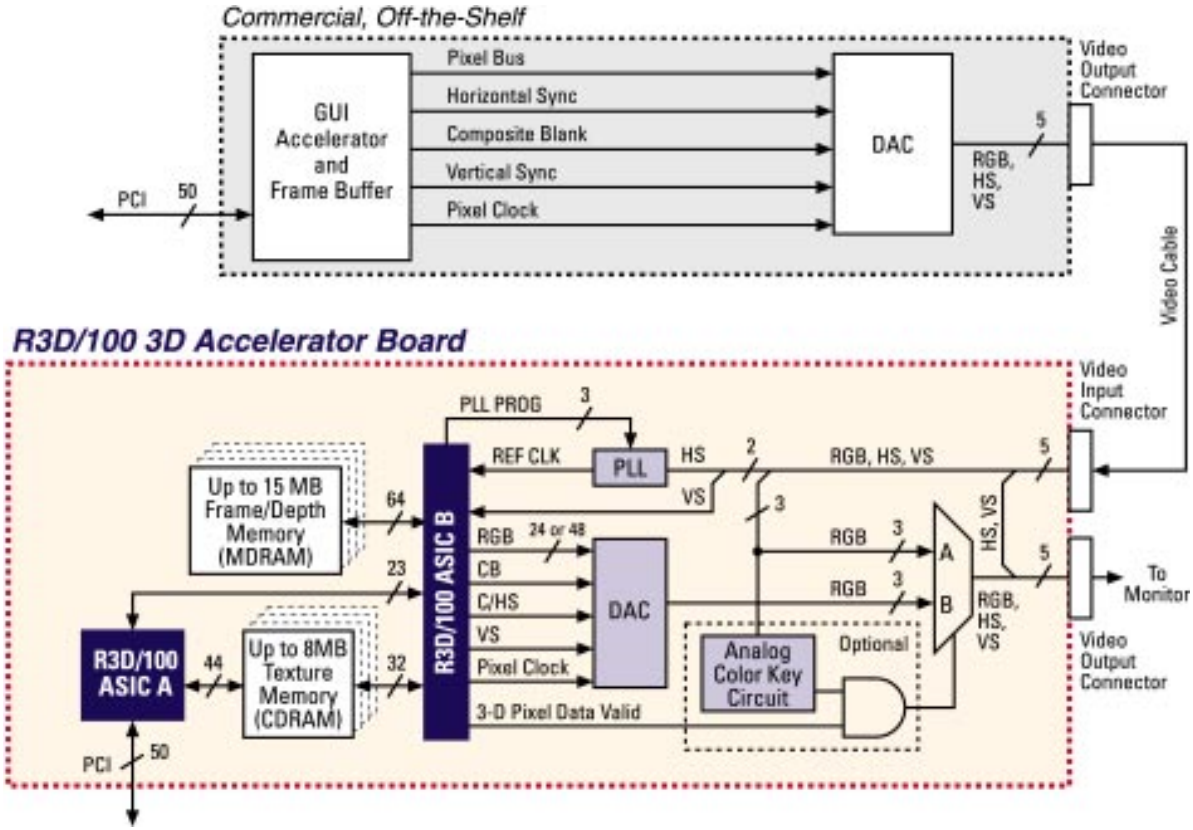

Figure 3. 2-D/3-D Analog Merge Separate Board Configuration

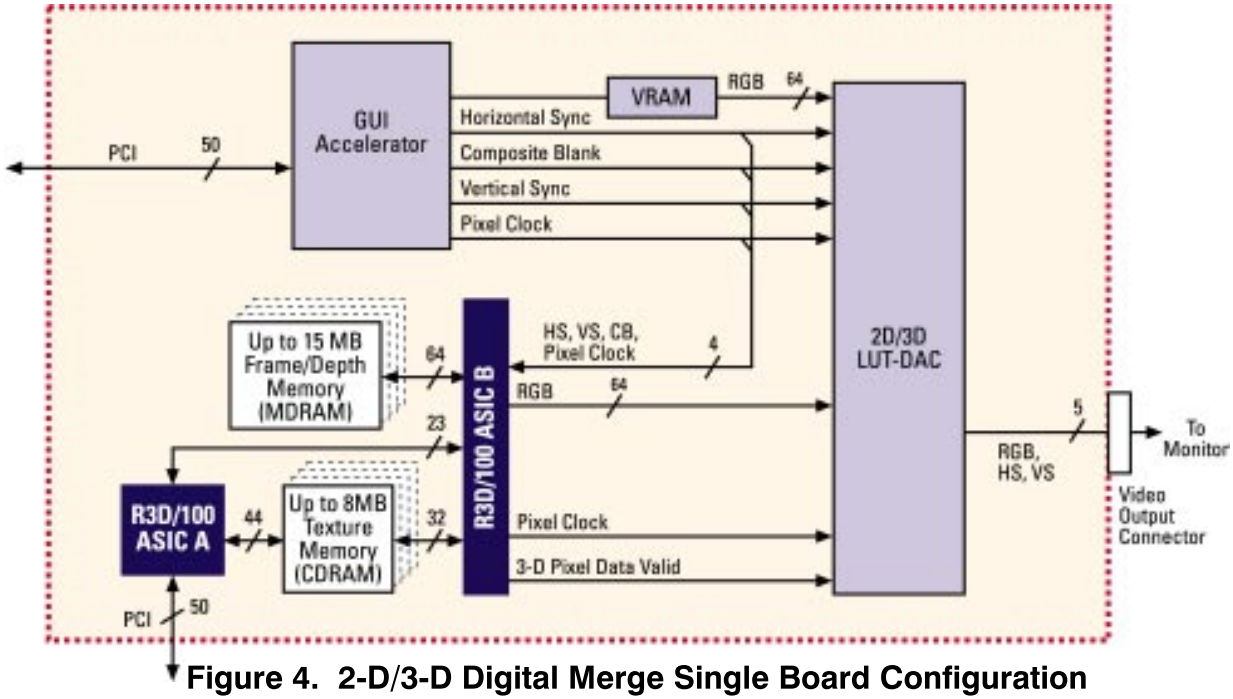

Figure 4. 2-D/3-D Digital Merge Single Board Configuration

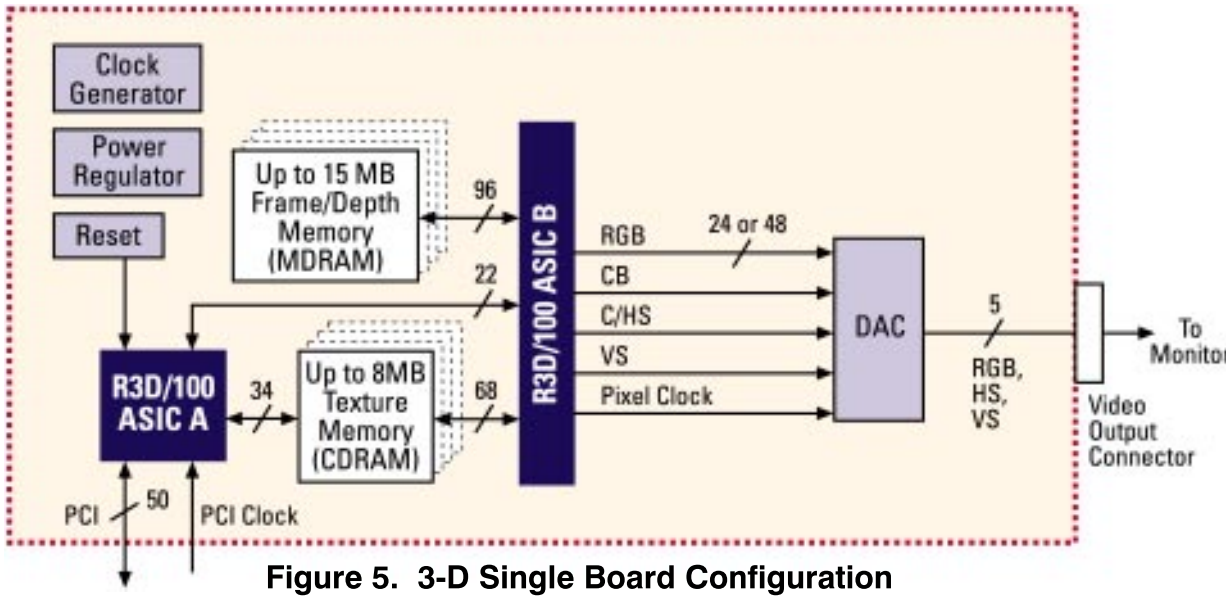

Figure 5. 3-D Single Board Configuration

Physical Characteristics

Common:

- Supply Voltage: 3.3V ±10 percent (5V tolerant I/O pins)
- Ambient temperature: 0° C to 70° C
- Storage temperature: -40° C to 125° C
- Junction temperature: 125° C

R3D/100-A:

- 352-pin SBGA Package
- Power Consumption: approximately 3W

R3D/100-B:

- 352-pin SBGA Package
- Power Consumption: approximately 3W

Software Support

The R3D/100 chip set comes with a 3-D device driver kit (DDK) and sample drivers for Windows NT™. DDKs and sample drivers for other operating systems are planned and will be forthcoming. There will be documentation and programming guides (including source code) to support development of drivers where DDKs and sample drivers do not exist.

The provided 3-D device driver has the following features:

- Supports OpenGL® Version 1.0 and 1.1 running in Windows NT™ 3.51
- Supports multiple 3-D contexts (windows)
- Is implemented in Microsoft Visual C++ without assembly language for easy porting to other platforms
- Maintains a synchronization mechanism to the R3D/100 display frame sync

The R3D/100 chip set is designed to be compliant with OpenGL® and other Microsoft Windows 3-D Application Programming Interfaces (APIs). Future support for Microsoft's Direct3D™ and DirectDraw™ APIs will be provided.

Reference Board Design Kit

The reference board design kit will allow hardware and software original equipment manufacturers to facilitate rapid development of products based on the R3D/100 chip set. It will provide:

- Full performance PC-based R3D/100 3-D graphics accelerator board (see Figure 3)
- Full set of R3D/100 hardware and software documentation
- Reference board schematic diagrams
- Gerber files for the reference board
- R3D/100 board design guidelines
- Device driver software kit

Additional Documentation

The following manuals make up the complete set of documentation for the R3D/100 chip set:

- *R3D/100 Architecture Overview*
- *R3D/100 Data Manual*
- *R3D/100 Programmer's Guide*
- *R3D/100 Application Notes*

For further reading about OpenGL®, the following are suggested:

- *OpenGL Programming Guide*, OpenGL Architecture Review Board, Neider, et al. Addison Wesley. ISBN 0-201-63274-8
- *OpenGL Reference Manual*, OpenGL Architecture Review Board, Neider, et al. Addison Wesley. ISBN 0-201-63276-4
- *The OpenGL Graphics System: A Specification* (World Wide Web document) http://www.sgi.com/Technology/openGL/glspec/glspec.html

For other related topics, the following are suggested:

- *PCI Local Bus Specification, Revision 2.1*, PCI Special Interest Group, 01 June 1995
- *Microsoft Windows NT 3.51 Operating System*
- *Video Electronics Standards Association (VESA) Monitor Timing Standards Version 1.0 Release 0.3*

Points of Contact

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