Programmable Media Processor

TriMedia TM-1300

Continuing a tradition of high-performance, low-cost media processors, the TriMedia™ TM-1300 delivers up to 66% more processing power[1] to multimedia applications at a lower unit cost. By combining a 166-MHz CPU and a full complement of enhanced on-chip I/O and coprocessing units, TM-1300 achieves up to 6.5 billion operations per second—ideal for applications requiring real-time processing of video, audio, graphics, and communications datastreams.

TM-1300 boosts performance through a faster clock speed and a faster main memory interface than previous TriMedia processors. Datastream I/O is enhanced with a new on-chip unit for handling audio output in Sony/Philips digital format (SPDIF). Lower power consumption and a smaller footprint contribute to making the TM-1300 a more efficient and compact processing solution for new multimedia designs.

TM-1300 is an ideal building block for applications requiring simultaneous processing of several types of multimedia datastreams. With ample computational power available to capture, compress and decompress many video and audio data formats in real time, TM-1300 is well suited for a broad range of video-centric applications such as videoconferencing, video editing, video-based security, surveillance, or industrial inspection systems, and multifunctional devices such as digital TV sets and set-top boxes. It also supports applications in a Java™ virtual machine environment.

With its comprehensive software development environment, the TriMedia SDE, TM-1300 is comparable in ease of programmability to general-purpose processors. The SDE enables multimedia application development entirely in the C and C++ languages improving time-to-market and lowering product development and maintenance costs.
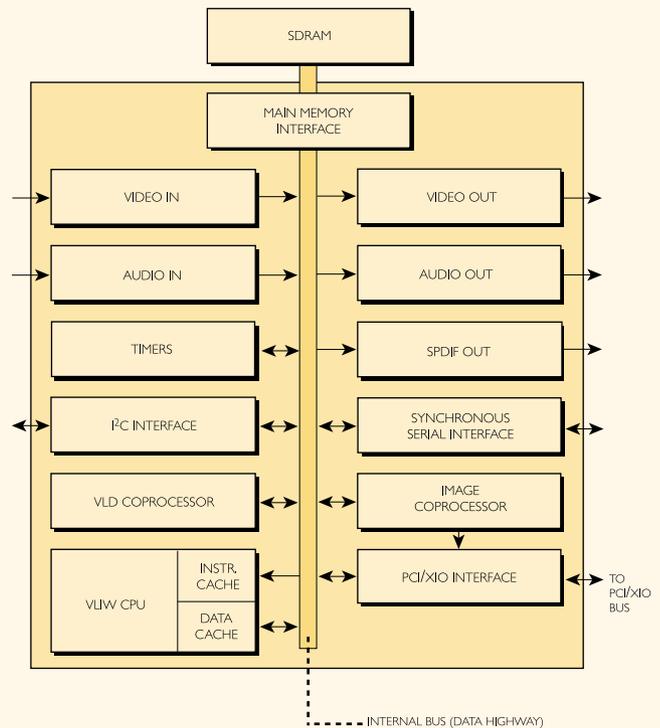
[1] compared to TM-1000 processors

FEATURES

+ Processes audio, video, graphics and communications datastreams on a single chip

+ Ideal for video-centric multimedia applications

+ Powerful, fine-grain parallel, 143- or 166-MHz VLIW CPU achieving up to 6.5 BOPS

+ Versatile instruction set includes traditional microprocessor, special multimedia SIMD, and IEEE floating-point operations

+ Comprehensive software development tools enable multimedia application development entirely in the C/C++ programming languages

+ On-chip, independent, DMA-driven multimedia I/O and coprocessing units offload the CPU

+ PCI/XIO host bus interface supports glueless interface to PCI and eight-bit microcomputer peripherals, including ROM/Flash, EEPROM, 68K, and x86 devices

+ 16- and 64-Mbit SDRAM support up to 143 MHz

+ On-chip DVD playback authentication/descrambling

+ TriMedia application libraries available from Philips and third-party suppliers provide solutions for MPEG-2 decode, Dolby Digital (AC-3)® decode, and more

PHILIPS

TriMedia TM-1300

System-on-a-chip multimedia engine

TRIMEDIA TM-1300 ARCHITECTURE
On a single chip, the TM-1300 incorporates a powerful CPU and peripherals to accelerate processing of audio, video, graphics, control, and communications datastreams.

The TriMedia TM-1300 strikes a perfect balance between cost and performance. A powerful C/C++-programmable VLIW CPU coordinates on-chip activities. To reap the full benefit of the CPU, independent, on-chip, bus-mastering DMA peripheral units manage and format datastream I/O and accelerate processing of multimedia algorithms. A sophisticated memory hierarchy manages internal I/O and streamlines access to external memory. The result—a single, low-cost, programmable system-on-a-chip uniquely suited for both standalone and hosted multimedia products.

PROGRAMMABLE VLIW CPU

A powerful DSP-like CPU delivers top performance through an elegant implementation of a fine-grain parallel, very-long instruction word (VLIW) architecture. Its five issue-slot instruction length enables up to five simultaneous operations to be scheduled into a single VLIW instruction. These operations can simultaneously target any five of the CPU's 27 pipelined functional units within one clock cycle. Most common operations have their results available in one clock cycle; more complex operations may have multicycle latencies.

Unique to the TriMedia VLIW implementation, parallelism is optimized at compile time by an innovative compilation system. No specialized scheduling hardware is required to parallelize code during execution. Hardware saved by eliminating complex scheduling logic

reduces cost and allows the integration of multimedia-specific features that enhance the power of the CPU.

The TM-1300 CPU implements a 32-bit linear address space and 128 fully general-purpose 32-bit registers. Registers are not separated into banks enabling any operation to use any register for any operand.

High-powered, DSP-like, C/C++-callable special operations—In addition to traditional microprocessor operations and a full complement of 32-bit, IEEE-compliant, floating point operations, the TM-1300 instruction set includes special multimedia and DSP operations (ops) to accelerate the performance of SIMD (single instruction, multiple data) computations common in multimedia applications. These special ops combine multiple simple operations into a single VLIW instruction that can implement up to 12 traditional microprocessor operations in a single clock cycle. When incorporated into application source code, special ops dramatically improve performance and increase the efficiency of the TM-1300 parallel architecture.

Special multimedia ops are invoked with familiar function-call syntax consistent with the C/C++ programming languages. They are automatically scheduled to take full advantage of the TriMedia processor's highly parallel VLIW implementation. As with all other operations generated by the TriMedia VLIW compilation system, the scheduler takes care of register allocation, operation packing, and flow analysis.
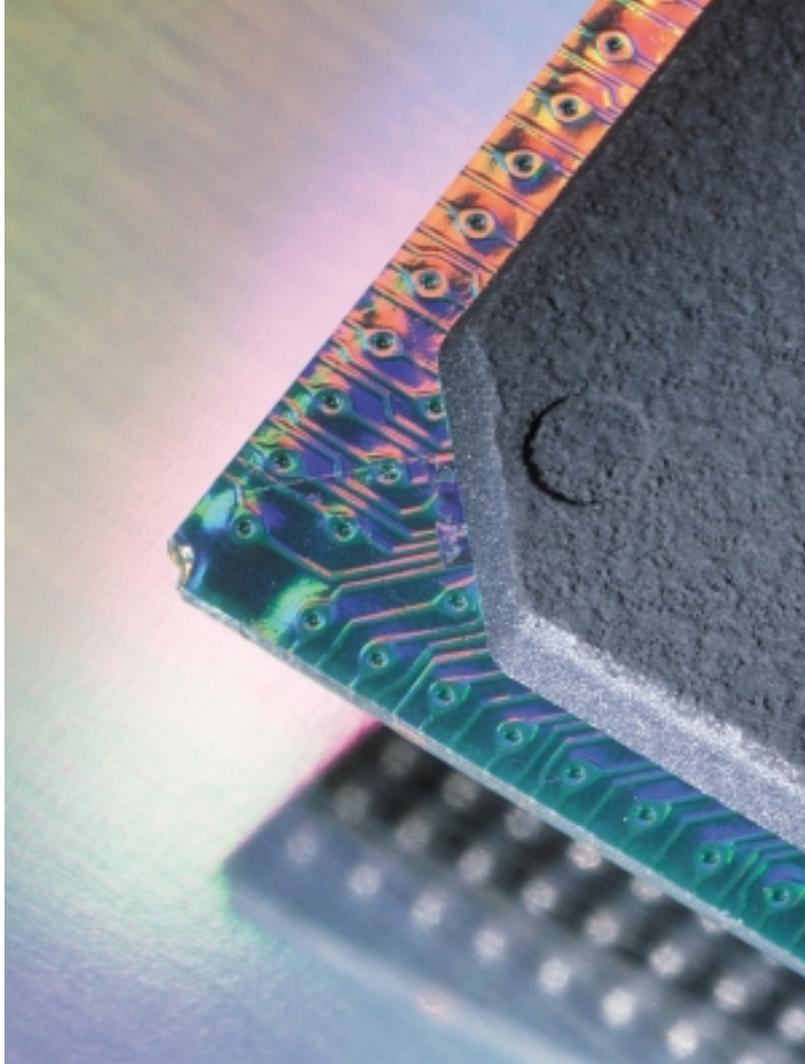
ON-CHIP I/O AND COPROCESSING UNITS

Video input—The video input (VI) unit reads digital video datastreams from an off-chip source into main memory. It accepts signals from any CCIR656-compliant device that outputs eight-bit parallel, 4:2:2 YUV time-multiplexed video data, such as a digital video camera, digital video decoder, or devices connected through ECL-level converters to the standard D1 parallel interface. After input, YUV data is demultiplexed, subsampled as needed, and written to SDRAM.

The VI unit can also be programmed to perform on-the-fly 2X horizontal resolution subsampling enabling high-resolution images (720 pixels/line) to be converted to 360 pixels/line without loading the CPU. When low resolution video is desirable, subsampling during data capture reduces initial storage and bus bandwidth requirements. The VI unit can also receive raw data and unidirectional messages from another TM-1300 video out port.

Video output—The video out (VO) unit outputs a digital YUV datastream to off-chip video subsystems such as a digital video encoder chip, digital video recorder, or other CCIR656-compatible device. The output signal is generated by gathering bytes from the separate Y, U, and V planes stored in SDRAM.

While generating the multiplexed stream, the VO unit can perform programmed processing tasks, including horizontal 2X upscaling to convert from CIF/SIF to CCIR 601 resolution. For simultaneous display of graphics and live video, the VO unit can perform 129-level

alpha blending to generate sophisticated graphics overlays of arbitrary size and position within the output image. Chroma keying, genlock frame synchronization, programmable YUV output clipping are also supported. The VO unit can also be used to pass raw data and unidirectional messages between TriMedia processors.

The VO unit can either supply or receive video clock and/or synchronizing signals from the external interface. Clock and timing registers can be precisely controlled through programmable registers. Programmable interrupts and dual buffers facilitate continuous data streaming by allowing the CPU to set up a buffer while another is being emptied by the VO unit.

Audio input and output—The audio input (AI) and audio output (AO) units provide all signals needed to read and write digital audio datastreams to/from most high-quality, low-cost serial audio oversampling A/D and D/A converters and codecs. Both units connect to off-chip stereo converters through flexible bit-serial interfaces.

The AI and AO units are highly programmable providing tremendous flexibility in handling custom datastreams, adapting to custom protocols, and upgrading to future audio standards. Driven by TM-1300, the programmable audio sampling clock system supports a variety of sample rates with fine-grain resolution enabling audio and video synchronization in even the most complex multimedia applications.

UME8UU: SUM OF ABSOLUTE VALUES OF UNSIGNED 8-BIT DIFFERENCES

SOURCE REGISTER 1

31			0
A	B	C	D

SOURCE REGISTER 2

31			0
E	F	G	H

|A-E| + |B-F| + |C-G| + |D-H|	DSPALU FUNCTIONAL UNIT

31   0

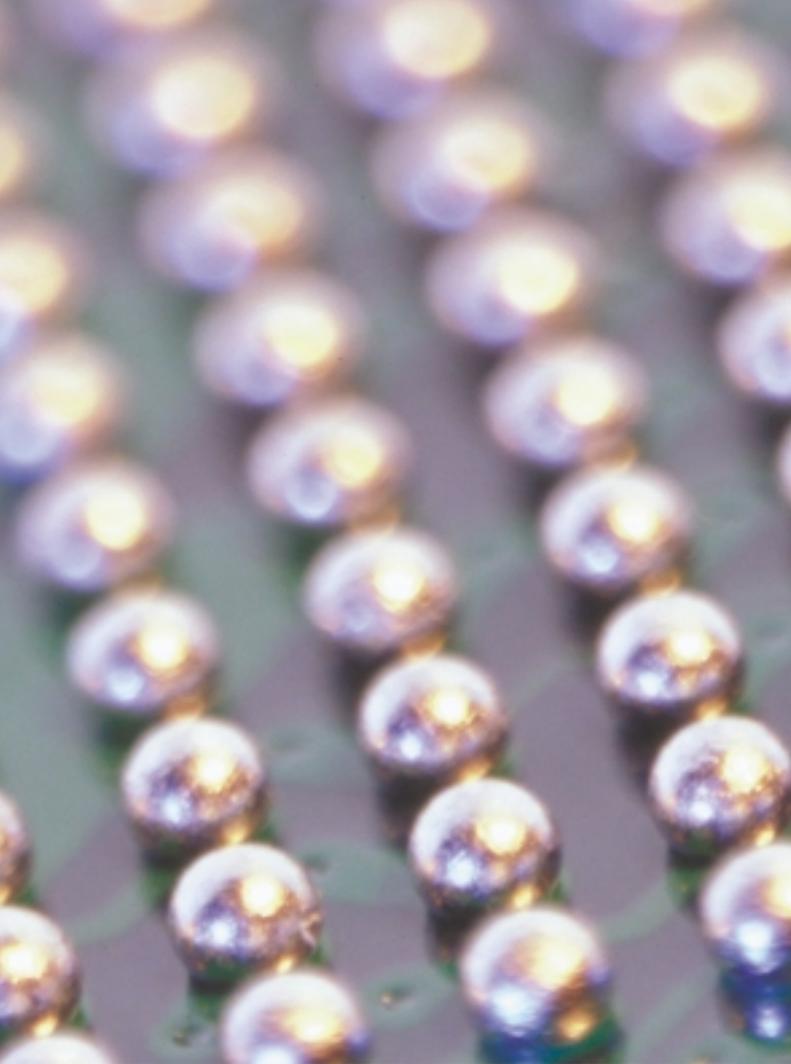| RESULT	DESTINATION REGISTER

SPECIAL MULTIMEDIA OPERATIONS
The ume8uu operation, commonly used for motion estimation in video compression, implements 11 simple operations in one TriMedia special op.

The AI unit supports up to two channels of audio input. Mono and 16-bit stereo formats are supported. The AO unit delivers up to eight channels of output using one external pin per channel. Output of 16-bit and 32-bit stereo and mono formats are supported. The AO unit can also be used to control highly integrated PC codecs. Software support for decode and output of Dolby ProLogic® and Dolby Digital (AC-3)® multichannel audio is provided through optional TriMedia application library modules.

SPDIF output—The SPDIF out unit allows output of a one-bit high-speed serial datastream. The primary application is output of digital audio data in SPDIF format to external audio equipment. Since datastream content is entirely software controlled, the SPDIF out unit can also be used as a general purpose high-speed datastream output device such as a UART.

The SPDIF out unit supports two-channel linear PCM audio, one or more Dolby Digital six-channel datastreams (embedded per Project 1937), or one or more MPEG-1 or MPEG-2 audio streams (embedded per Project 1937). It supports arbitrary, programmable sample rates independent of and asynchronous to the AO unit sample rate.

Image coprocessor—The image coprocessor (ICP) unit off-loads the CPU of cycle-consuming image processing tasks such as copying an image from SDRAM to a host video frame buffer. The ICP unit can operate as either a memory-to-memory or memory-to-PCI coprocessor device. In both modes, it can perform horizontal or vertical image

filtering and scaling and can optionally perform YUV to RGB color-space conversion for screen display (in memory-to-PCI mode).

The ICP also provides display support for live video in occluded windows. The number and sizes of windows processed are limited only by available bandwidth. The final resampled and converted images are transmitted over the PCI bus to an optional off-chip graphics card/frame buffer.

Variable length decoder—A variable length decoder (VLD) unit operates as a memory-to-memory coprocessor to decode Huffman-encoded MPEG-1 and MPEG-2 video datastreams. After processing, the VLD unit outputs a decoded stream optimized for MPEG-2 decompression software. This minimizes communications with the CPU where other steps of MPEG processing are performed.

DVD descrambler—The on-chip digital versatile disc (DVD) descrambler unit provides DVD authentication and descrambling. This enables developers to add low-cost, flexible DVD video playback functions into multimedia products with minimal effort.

I²C interface—An I²C interface provides an external I²C (or compatible interface) for use in hardware or software operation modes. In hardware mode, it can connect to and control a variety of different I²C multimedia devices allowing configuration and status inspection of off-chip peripheral video devices such as digital encoders and decoders, digital cameras, parallel I/O expanders, and more. I²C software mode enables full software control of the I²C interface. The interface can also be used to read the boot program from an off-chip EEPROM.

Synchronous serial interface—A synchronous serial interface (SSI) unit provides serial access for a variety of multimedia and data communications applications. It contains the buffers and logic necessary to interface with simple analog modem front ends. When used with a TriMedia V.34 application, the SSI unit can provide fully V.34-compliant modem capability. Alternatively, it can be connected to an ISDN interface chip to provide advanced digital modem capabilities.

Timers—TM-1300 provides four general purpose timers useful in counting/timing events such as CPU clock cycles, data/instruction breakpoints, cache tracing, audio/video clocks, and more. Three timers are available to programmers, the fourth is reserved for use by system software.

PCI/XIO bus interface—A PCI/XIO interface connects the CPU and on-chip peripheral units to a PCI/XIO bus. In embedded applications where TM-1300 is the main processor, this interface enables TM-1300 to access off-chip devices implementing functions not provided on-chip. In host-based applications, the interface connects TM-1300 to a standard PCI bus, allowing placement directly on the host mainboard or a plug-in card. For low-cost standalone systems, XIO support allows glueless connection of eight-bit x86 or 68K devices such as ROM, Flash, EEPROM, UARTs, and more.

MEMORY SYSTEM OVERVIEW

To meet the performance requirements of its target applications while maintaining low cost, the TM-1300 memory subsystem couples substantial on-chip caches with a glueless memory interface through a unique internal bus or data highway.

Dedicated instruction and data cache—The TM-1300 CPU is supported by separate, dedicated on-chip data and instruction caches that employ a variety of techniques to improve cache hit ratios and thus CPU performance.

The dual-ported data cache allows two simultaneous accesses. It is non-blocking thus cache misses and CPU cache accesses can be handled simultaneously. Early restart techniques reduce read-miss latency. Background copyback reduces CPU stalls.

To reduce internal bus bandwidth requirements, instructions in main memory and cache use a compressed format. Instructions are decompressed in the instruction cache decompression unit before being processed by the CPU.

To improve cache behavior and thus performance, both caches have a locking mechanism. Cache coherency is maintained by software.

Glueless memory system interface—The TM-1300 couples main memory to substantial on-chip caches through a glueless main memory interface (MMI). The MMI acts as the main memory controller and programmable central arbiter that allocates memory bandwidth for on-chip peripheral unit activities.

Support for a variety of memory configurations enables a wide variety of TM-1300-based systems to be built. The MMI supports 16-Mbit and 64-Mbit SDRAMs and provides sufficient drive capacity for an up to 143-MHz memory system comprising 8-MB (one 2Mx32), 16-MB (two 4Mx16 or two 2Mx32), or 32-MB (four 4Mx16 or four 2Mx32) memories. Larger memories (up to 64 MB) can be implemented using lower memory system clock frequencies or external buffers. Higher bandwidth SDRAM permits TM-1300 to use a narrower and simpler interface than is required to achieve similar performance with standard DRAM. Programmable speed ratios allow SDRAM to have a different clock speed than the TM-1300 CPU.

HIGH-SPEED INTERNAL BUS (DATA HIGHWAY)

The TM-1300 CPU and processing units access external SDRAM through the on-chip internal bus or data highway comprising separate 32-bit address and data buses. Handled by the MMI, programmable bus arbitration enables the data highway to maintain real-time responsiveness in a variety of applications.

ROBUST SOFTWARE DEVELOPMENT ENVIRONMENT

The TriMedia SDE includes a full suite of system software tools to compile and debug code, analyze and optimize performance, and simulate execution for the TM-1300 processor. The SDE dramatically lowers development costs, reduces time-to-market, and ensures code portability to next generation architecture by enabling development of multimedia applications entirely in the C and C++ programming languages.

The TriMedia SDE Version 2.0 also supports Metrowerks® CodeWarrior® plug-ins. These plug-ins enable programmers to develop C code for TriMedia processors using the popular CodeWarrior Integrated Professional Development Environment (IDE).

TRIMEDIA APPLICATION LIBRARIES

Many TriMedia application libraries are available to accelerate product development of common standard-compliant software algorithms used in processing multimedia datastreams. These C-callable routines are optimized for top performance on the TriMedia architecture.

Application libraries are available from Philips and third-party suppliers and include functions such as MPEG-1 encode or decode, MPEG-2 MP@ML decode, MPEG-2 1/2D1 MP@ML encode, H.320, H.324, Dolby ProLogic or Dolby Digital (AC-3) decode, communications protocols, and many more. The TM-1300 can also support Java applications with third-party Java virtual machine environments.

HOST-ASSISTED COPROCESSOR
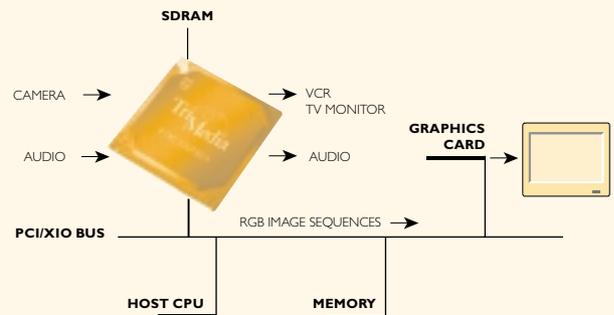
STANDALONE
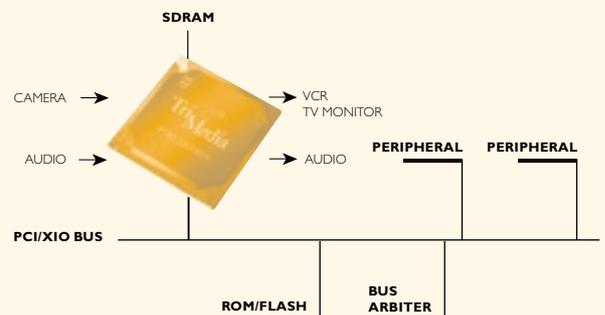
TM-1300 is designed for use as the sole CPU in standalone systems and as a coprocessor in a hosted or multiprocessor environment.

REAL-TIME OPERATION SYSTEM SUPPORT

For multimedia applications requiring system resource and task management, the TM-1300 media processor supports the pSOS+™ embedded real-time operating system kernels. Developed by Integrated Systems, Inc., the pSOS+ kernels are based on open system standards and are optimized for deterministic response essential for multimedia applications.

UPWARD COMPATIBILITY

TriMedia processors preserve investments in software development through software compatibility between family members at the source code level. Powerful, optimizing compilers ensure that programmers never need to resort to non-portable assembler programming.
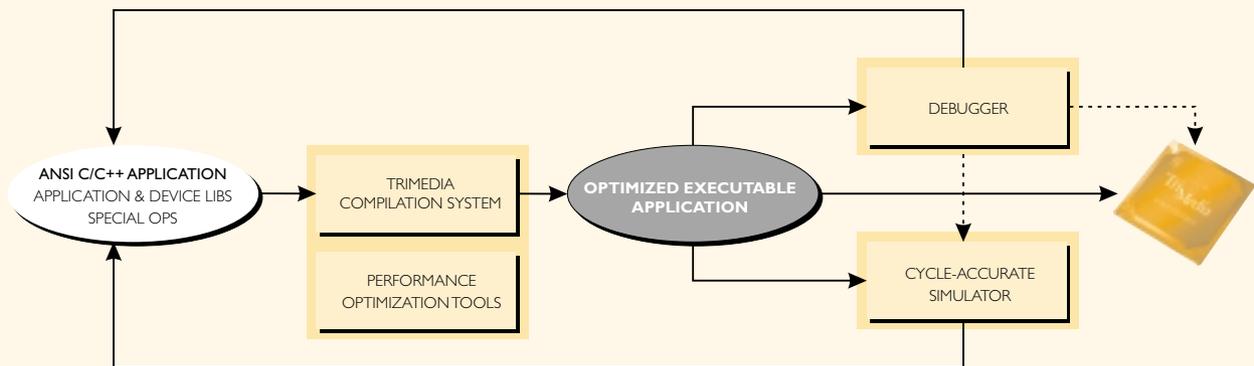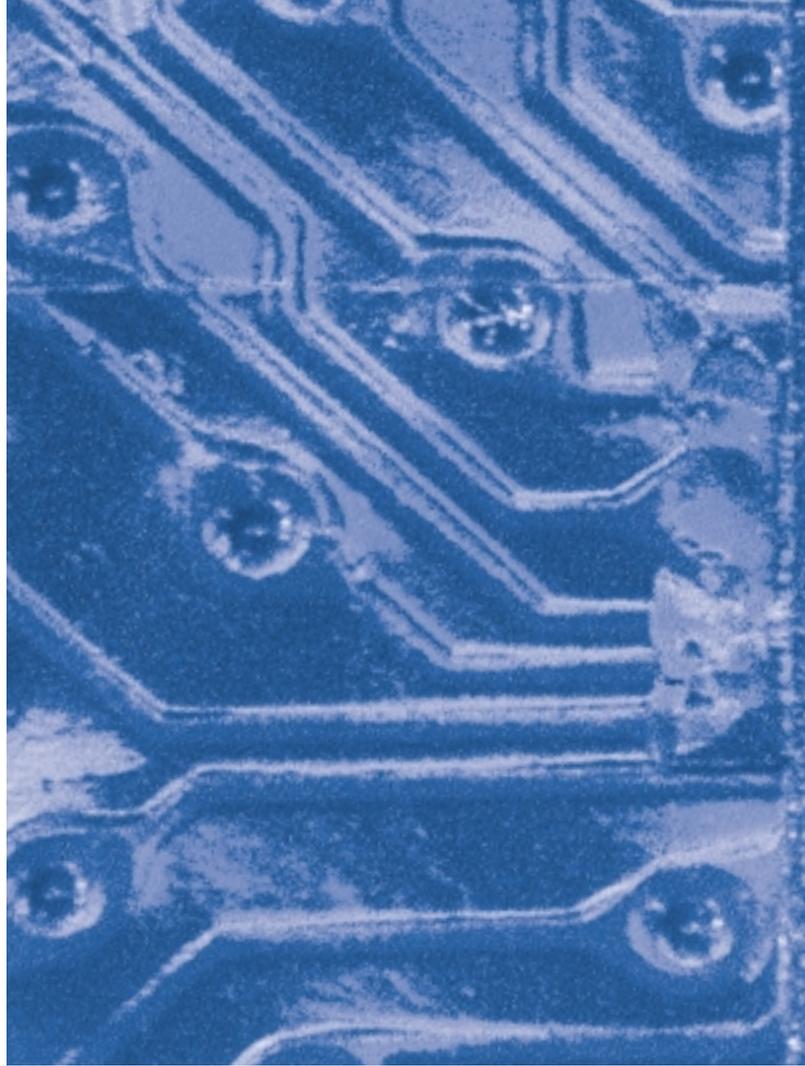
The TriMedia Software Development Environment includes a full suite of system software tools to compile and debug code, analyze and optimize performance, and simulate execution on TriMedia processors.

TM-1300 Specifications

PHYSICAL

Process	0.25-micron CMOS
Packaging	292 T^{2}BGA (169 functional)
Power	**supply** core: 2.5 V; I/O: 3.3 V (5 V tol.) **consumption** 1300 mA; 3.5 W **powerdown** 300 mA
Case Temperature	0 to 85 °C

CENTRAL PROCESSING UNIT

Clock Speed	143 or 166 MHz
Instruction Length	variable (2 to 23 bytes); compressed
Instruction Set	arithmetic and logical ops, load/store ops., special multimedia and DSP ops., IEEE-compliant floating point ops.
Issue Slots	5
Functional Units	27, pipelined integer and floating-point arithmetic units, data-parallel DSP-like units

name	qty	latency	recovery
constant	5	1	1
integer ALU	5	1	1
memory load/store	2	3	1
shift	2	1	1
DSPALU	2	2	1
DSP multiply	2	3	1
branch	3	3	1
float ALU	2	3	1
integer/float mul	2	3	1
float compare	1	1	1
float sqrt./divide	1	17	16

Registers	128 (32-bit width)
Special/SIMD Ops	32

MEMORY SYSTEM

Speed	143 MHz
CPU/Memory Speed Ratios	programmable; 1:1, 5:4, 4:3, 3:2, and 2:1
Memory Size	512 KB to 64 MB (up to four ranks)
Supported Types	SDRAM (x4, x8, x16); SGRAM (x32); 64-Mbit SDRAM (x8, x16, x32) 128-Mbit SDRAM (x16)
Recommended Configurations	8 MB: 1 2Mx32 16 MB: 2 4Mx16 or 2 2Mx32 32 MB: 4 2Mx32 or 4 4Mx16
Width	32-bit bus
Max. Bandwidth	572 MB/sec (at 143 MHz)
Interface	glueless up to 4 chips (at 143 MHz); more chips will require slower clock
Signal Levels	3.3 V LVTTL

CACHES

Access	**data** 8-, 16-, 32-bit word **instruction** 64 bytes
Associativity	8-way set-associative with hierarchical LRU replacement
Block Size	64 bytes
Size	**data** 16 KB **instruction** 32 KB

INTERNAL DATA HIGHWAY

Protocol	64-byte block-transfer separate 32-bit data and 32-bit address buses

VIDEO IN

Supported Signals	CCIR 601/656: 8-bit video (up to 40 Mpix/sec; raw 8-10-bit data up to 80 MB/sec
Image Sizes	all sizes, subject to sample rate
Functions	programmable on-the-fly 2X horizontal resolution subsampling

VIDEO OUT

Image Sizes	flexible, including CCIR601; max. 4K x 4K pixels (subject to 80 MB/sec data rate)
Input Formats	YUV 4:2:2, YUV 4:2:0
Output Format	CCIR601/656 8-bit video, PAL or NTSC
Clock Rates	programmable (4-80 MHz), typ. 27 MB/sec (13.5 Mpixels/sec for NTSC, PAL)
Transfer Speeds	up to 80 MB/sec in data-streaming and message passing modes; 40 Mpix/sec in YUV 4:2:2 mode
Functions	full 129-level alpha blending, genlock mode, frame synchronization, chroma key, programmable YUV color clipping

AUDIO IN

No. of Channels	2
Sample Size	8- or 16-bit samples per channel
Sample Rates	programmable with 0.001 Hz resolution; maximum is application dependent
Data Formats	8-bit or 16-bit mono and stereo; PC standard memory data format
External Interface	4 pins; 1 programmable clock; 3 flexible serial input
Clock Source	internal or external
Native Protocol	I^{2}S and other serial 3-wire protocols

AUDIO OUT

No. of Channels	8
Sample Size	16- or 32-bit samples per channel
Sample Rates	programmable with 0.001 Hz resolution; maximum is application dependent
Data Formats	16-bit (mono and stereo); 32-bit (mono and stereo; PC standard memory data format
External Interface	4 pins each; 1 programmable clock; 3 flexible serial output
Clock Source	internal or external
Native Protocol	I^{2}S and other serial 3-wire protocols

SPDIF OUT

No. of Channels	up to 6
Sample Size	16 or 24 bits per channel
Bit Rate	up to 40 Mbits/sec
External Interface	1 pin, self clocking interface per IEC-958
Clock Source	internal
Native Protocol	IEC-958, 1 wire

IMAGE COPROCESSOR

Functions	horizontal or vertical scaling and filtering of individual Y, U, or V
	horizontal scaling and filtering with color conversion and overlay: YUV to RGB, RGB overlay and alpha blending, bit mask blanking
Scaling	programmable scale factor (0.2X to 10X)
Filtering	32-polyphase, each instance 5-tap, fully programmable filter coefficients
Performance	horizontal scaling and filtering: 110 MB/sec vertical scaling and filtering: 40 MB/sec

VLD

Function	parses MPEG-1 and MPEG-2 elementary bitstreams generating run-level pairs and filling macroblock headers
External Interface	none

DVD DESCRAMBLER

Functions	authentication; descrambling
External Interface	none

I²C INTERFACE

Supported Modes	single master only
Addressing	7-bit
Rates	up to 400 kbps
External Interface	2 pins: 1 serial data, 1 clock

SYNCHRONOUS SERIAL INTERFACE

Data Formats	variable slots/frame
Frame Sync	external or internal
Clock Source	separate transmit, receive, frame sync; transmit/receive clocks external source; automatic frame sync error detection; settable edge polarity for transmit, receive, and frame sync
External Interface	6 pins (2 usable for tip and ring for phone connections); compatible with most telecom devices; can be configured with multiple chips

PCI/XIO INTERFACE

Speed	33 MHz
Bus Width	32 bits
Address Space	32 bits (4 GB)
Voltage	drive and receive at 3.3 V or 5 V
Standard Compliance	PCI Local Bus Specification 2.1

TIMERS

Number	4
Width	32-bits
Sources	external clock, (prescaled) CPU clock, data or instruction breakpoints, cache events, video in/out clocks, audio in/out word strobe, SSI receive/transmit frame sync

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