TM-1300 Power Consumption Study

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Summary

The purpose of this application note is to provide information on power consumption for systems powered by TM-1300. The presented results are from measurements conducted by Philips on applications currently owned by Philips.

This study is based on engineering data and is provided on an indicative basis. Results of measurements may vary. Under no circumstances can Philips accept any responsibility for failures in product design due to error in this document.

References

1. “TriMedia TM-1300 Media Processor Data Book”, 2000 Sep 30, Philips.
2. “TEA1211TT High Efficiency Up/Down DC/DC Converter”, To Be Published, Philips.
3. “I2C Bus Specification, version 2.1”, 2000 Jan, Philips.
4. “TM-1310 Power Consumption Study”, to be published, Philips.
5. “Voltage Supervisory Circuit With Watchdog Timer”, 2000, Summit Electronics, Inc.

Overview

The power consumption described in [1] is based on a “dummy” application that exercises all the capabilities of TM-1300 device and runs a program with a CPI (Clocks Per Instruction) of 1.4. This has been proven so far to be a worst case for typical applications that run on TM-1300, e.g. video encoding/decoding and/or audio processing.

Current consumption contains two components. The current used by the core (DSPCPU and Peripherals), Idd and the current used by the I/Os, Icc. Idd includes the current used by all transistors of TM-1300 that are powered by the Vdd power supply, i.e. 2.5V. Icc includes the current used by all transistors of TM-1300 that are powered by the Vcc power supply, i.e. 3.3V. All numbers are given for typical power supplies, meaning the total power of an application is Idd*Vdd + Icc*Vcc. All power numbers are rounded up to the next **0.1W** which compensates for process variation as well as measurement inaccuracy. Speeds are given for a CPU/SDRAM MHz ratio.

Power consumption on TM-1300 depends on many factors and can be itemized as follows:

- The internal clock distribution system inside the chip is the main power drain on the Vdd supply. Slowing down the clock frequency will considerably reduce the power consumption. Finding the optimal combination of CPU frequency and SDRAM frequency requires the final application and some effort.
- The activity of the CPU is also a key factor. The activity includes the amount of issue slots issued (i.e. non NOP operations), the amount of stall cycles (related to the CPI), the data transiting on the internal busses (a register access costs more than a cache hit ld/st operation). This means the optimization level of the application will change the total power consumption.

- The amount of peripherals required by the application, their operating mode and the frequency at which they run (higher frequency rate also increases the data transfer on the main memory interface).

The following sections describe the known power saving optimizations that can be applied to TM-1300. Each example will be illustrated by some measured numbers on TM-1300 silicon. H263 video conferencing, MPEG-2 video plus AC3 decoding (i.e. DVD playback) and AC3 decoding are used to illustrate these power saving features. Power numbers are summarized in Table 1. For details on column meaning refer to the next sections.

Table 1. Power Consumption Summary

Application	Optimized (Lowest Power)	Non Optimized (Out of the box)	Optimizations				
			With unused peripherals turned off	Plus Adjusted speed	Plus IDLE task with MMIO read	Plus Global Powerdown	Plus Lower voltage (Estimated)[a]
H.263 VConf.	1.7W	2.9W	2.7W	1.9W	1.7W	N/A	1.3W
DVD Playback	2.2W	3.0W	2.6W	2.6W	2.3W	2.2W	N/A
AC3 Playback	0.6W	2.5W	2.0W	0.7W	0.7W	0.6W	0.5W

a. With Vdd at 2.0V and Vcc at 3.2V

Application details:

- The H263 video conferencing application includes the following steps. It captures a CCIR656 video stream at 30 frames/second using the VI peripheral. The incoming video stream is downscaled, on the fly, to SIF resolution by VI. The captured frames are then downscaled to a QSIF resolution using the ICP co-processor. The resulting QSIF image is sent over the PCI bus via the ICP co-processor to a SVGA card (PC monitor display) and encoded by the DSPCPU. The resulting bitstream is then decoded by the DSPCPU and displayed as a SIF image on the same PC monitor (also using the ICP co-processor). All the encoding/decoding part is done in the YUV color space. The display is in the RGB16 color space. Level of code optimization is low.
- The DVD playback includes video display using the VO peripheral and audio streaming using AO peripheral. The bitstream is brought into the TM-1300 system over the PCI peripheral. The VLD co-processor is used to perform the bitstream parsing. The bitstream is not scrambled therefore the DVDD co-processor is not used and it is turned off. Level of code optimization is very high.
- AC3 decoding application is the audio subset of the DVD playback application. Level of code optimization is very high.

Run the processor at lower frequency.

This is the main factor of the power consumption. TM-1300 does not require to run the DSPCPU at the speed grade of the device. For example TM-1300 devices can be ran as low as 45 MHz for the DSPCPU frequency and the SDRAM frequency (MM_CLK[1:0] pins) should always be higher or equal to 36 MHz. Input frequency on TRI_CLKIN pin should not be lower than 18 MHz. Many application can actually be ran at low frequency speeds and therefore significant power consumption gain can be achieved.

TM-1300 does not provide dynamic clock rate change. However if TM-1300 is supposed to run different applications with different MHz requirement, it is possible to control the input frequency at board level by the host or other dedicated hardware. The recommended procedure is to put under reset TM-1300 by asserting to low the TRI_RESET# pin. Then change the input clock frequency, meet the Trst-clk-PCI timing parameter (100 ms) and release the TM-1300 reset pin. TM-1300 will then go over the boot process. Another possible solution is to gradually change the input clock frequency (i.e. small frequency step changes of less than 1 Hz without glitches). This procedure has not been extensively tested.

Similarly the PLL ratios (SDRAM 2:1 or 3:1, DSPCPU 1:1, 5:4, ... 2:1) can be changed in the EEPROM. Note that TM-1300 has to go through the same reset procedure described above to take into account these new PLL settings.

- H263 Video Conference application running at
  - 166/133 MHz requires 0.734*2.5 + 0.074*3.3 = **2.1W**.

  - 111/111 MHz (minimum frequency to keep up with a 30 frames/second rate for this non optimized application) the power consumption drops to 0.586*2.5 + 0.07*3.3 = **1.7W**.
- AC3 decoding application running at
  - 180/143 MHz requires 0.621*2.5 + 0.054*3.3 = **1.8W**.
  - 45/36 MHz (note that AC3 decoding does not need that many MHz, the setting is limited by the TM-1300 device) the power consumption drops to 0.203*2.5 + 0.026*3.3 = **0.6W**.

Note: these numbers include the other power saving features presented in the present document and therefore reflect the savings for clock reduction only.

Note: The REFRESH counter, page 12-3 of [1], for the SDRAM refresh commands, must be changed in the boot EEPROM accordingly with the new system clock frequencies.

Note: Changing the CPU and/or SDRAM ratios in the EEPROM can be done by TM-1300 via the I2C bus.

Simple setup with no external host or hardware

The following solution has not yet been tried in a real system but it is believed to be feasible. It is proposed for a stand alone system and based on the use of a power on reset device that contains a timer watchdog like the SMS2902 device [5].

For such devices the RESET# pin is asserted to low during the power up sequence (it actually acts as a Vcc power monitor) and when the timer watchdog is reached, i.e. not cleared. Therefore TM-1300 can write into the EEPROM new PLL/REFRESH settings and then wait for the watchdog to kick in (or use a board level solution to force the reset using TM-1300 software programmable pins), in order to reset TM-1300 system and take into account the new settings. By applying this technique it is possible to have several DSPCPU/SDRAM clock frequencies with only one input oscillator as shown in Table 2.

Table 2. Available System Clock Frequencies Based On An Input Clock of 44 MHz

SDRAM PLL	DSPCPU PLL				
	1:1	**5:4**	**4:3**	**3:2**	**2:1**
Bypass	44	55	58.666	66	88
2:1	88	110	117.333	132	N/A
3:1	132	165	N/A	N/A	N/A

Some tests need to be conducted on the behavior of the EEPROM programming in the case where the power supply has some glitches or when it is turned off during the writing of the EEPROM.

The IDLE time of the CPU

An operating system always contains an IDLE task. This task is called each time the operating system has nothing else to do. This condition happens very often in applications like video decoding or any application where the processing power required to run the application is not constant. For example the amount of processing cycles required to encode a still image is lower than when there is a lot of motion. In TM-1300, rather than looping forever waiting for something to process, it is possible to send the system into sleep mode using the MMIO(GLOBAL_POWERDOWN) register defined in Chapter 21 of [1], or it is possible to actually stall the DSPCPU within the IDLE task. The latest can be achieved by performing a load operation to an non existing MMIO register like GPI_BASE, defined in <tm1/mmio.h> file. The use of the GLOBAL_POWERDOWN register provides the best power saving. It has however the drawback to increase the latency for interrupts service routines and to increase the latency for the traffic on the internal bus because the SDRAM is also sent to power down mode. This mode also requires the SLEEPLESS bits of the used peripherals to be set and cannot be activated if the ICP or the VLD co-processor are running, due to customer visible bug #24851.

DVD playback is a perfect example of the use of this feature:

- DVD playback requires a 180/144 MHz configuration in order to handle the peaks in computation. If the IDLE task is set as a simple forever loop then the power consumption is 0.888*2.5 + 0.09*3.3 = **2.6W**.
- When the IDLE task contains a forever loop with a MMIO read operation to a non existent MMIO register the power consumption drops to 0.811*2.5 + 0.09*3.3 = **2.3W**.

- Using the GLOBAL_POWERDOWN MMIO register (note that despite the VLD is used for DVD playback, it is possible to use this feature because the VLD is always idle when the IDLE task is called) the power consumption drops to 0.74*2.5 + 0.09*3.3 = **2.2W**.

Peripheral Stand-by

Peripheral stand-by can be controlled in software on TM-1300. Power saving is up to **0.5W** when the system runs at 166/133 MHz. The peripheral blocks can be restarted by the software as well, it does not need a specific reset or reboot procedure. This feature is further documented in [1] Chapter 21, power saving numbers are available in Chapter 1.

This feature was used in all previously detailed measurements.

Lowering the Voltage

As of today TM-1300 has not been characterized out of the voltage ranges specified in [1]. However programmable board level voltage regulators could be used to reduce the voltage applied to TM-1300 in order to reduce the power consumption. TEA1211TT [2] is an example of such device. It can be programmed via the I2C bus [3]. It is expected that TM-1300 can work with a Vdd power supply as low as **2.0V** and a Vcc power supply as low as **3.2V**. Upon request for large volume applications it is in the interest of Philips Trimedia Product Segment (TPS), to investigate that route. It is also under study for the future products.

Complete Processor Shut Down.

This can be achieved by switching off completely the power supplies of TM-1300 device. This is not possible if for example there are some devices connected to the TM-1300 PCI bus and they remain powered (there is a strict voltage relationship between Vcc and Vdd for TM-1300 that excludes a Vcc power supply greater than Vdd by more than 1.2V).

The second option is to shutoff the input clock. This will reduce drastically the power consumption down to less than **0.05W**. TM-1300 needs to go trough a complete reset/boot sequence as described previously for the input clock rate change.

Optimize the processing

Another possibility, however, not yet sufficiently investigated to provide numbers is to disable the speculative load option during the compilation. This will reduce the amount of operations to be executed, which consumes less power. The trade off might then be higher clock frequency needed. Speculative loads offer an average of 10% increase in performances.

Future Improvements

TM-1310 has a Vdd power supply of 1.8V resulting in a **2W** worst case power consumption. Estimated numbers for the applications mentioned in this document are displayed in Table 3. Measured numbers can be found in [4] upon silicon availability. Similarly TPS is looking into characterizing TM-1310 at 1.5V.

TM-1305 is planned to target lower voltages and is planned to have the DSPCPU frequency to be controlled dynamically by software allowing a significant power consumption reduction.

Table 3. TM-1310 Estimated Power Consumption

Application	Estimated at 1.8V	Estimated at 1.5V
H.263 VConf.	1.0W	0.9W
DVD Playback	1.3W	1.0W
AC3 Playback	0.4W	0.3W