SPC8108F$_{OC}$

LOW POWER LCD & CRT VGA CONTROLLER

■ DESCRIPTION

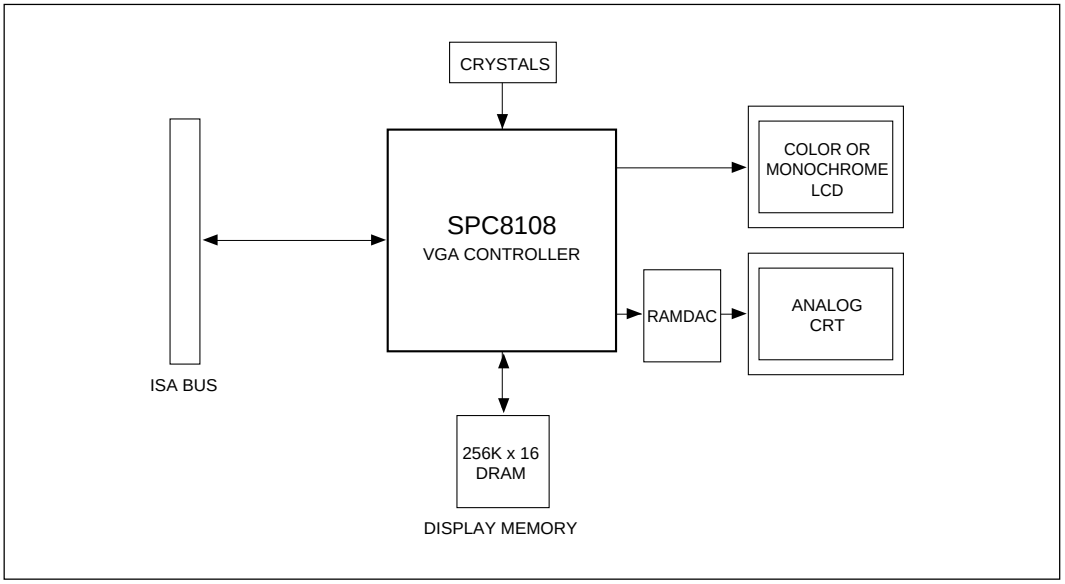
The SPC8108F$_{OC}$ is a versatile VGA graphics controller capable of driving liquid crystal displays and analog CRT monitors. The controller integrates all LCD interface, sequencing and gray shading logic into one small form factor 144 pin package. With the addition of an industry standard '477 type RAMDAC, the SPC8108F$_{OC}$ will also drive a VGA fixed frequency or multifrequency monitor.

The target products for this device are price and power sensitive 80x86 microprocessor based subnotebooks or other specialized LCD systems where a high quality 16 or 64 gray shade VGA image on a 320 x 200 to 640 x 480 LCD panel display are the major design criteria.

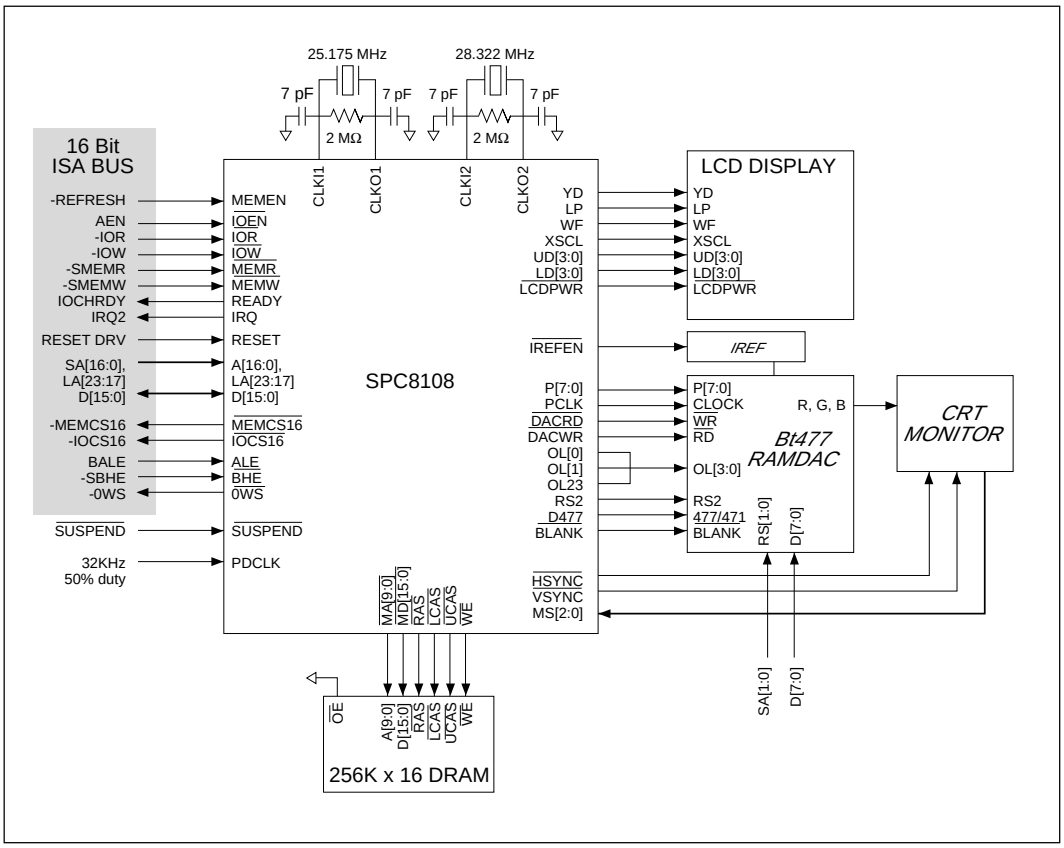
■ FEATURES

- Low-power CMOS technology
- Hardware VGA compatible
- High-performance 16-bit ISA support
- One 256K x 16 self-refresh DRAM
- Four-stage display pipeline
- 64 x 64 pixel hardware cursor
- Two-terminal crystals support
- Five power-down modes
- Video BIOS, software driver and utility support
- 5 volt operation
- QFP17-144 pin
- Monochrome LCD panel interface for sizes 320 x 200 to 640 x 480
- On-chip 256 x 6 grayscale look-up table
- 16 gray shades by frame rate modulation
- 64 gray shades by frame rate modulation and dithering
- Two programmable grayscale weightings (RGB), NTSC (30,59,11), and text (0,100,0)
- Vertical centering and expansion for LCDs
- Full CRT support with '477 RAMDAC

■ BLOCK DIAGRAM



■ ISA BUS SYSTEM BLOCK DIAGRAM



■ SPC8108 VIDEO MODES

Mode Number (Hex)	Horizontal Pixels Addressable	Vertical Pixels Addressable	Horizontal Pixels Displayed	Vertical Pixels Displayed	Monochrome LCD Display Gray Shades	CRT Colors
0	320	200	320	200/480	16	16
0+	320	350	320	350	16	16
0++	360/320	400	320	400/480	16	16
1	320	200	320	200/480	16	16
1+	320	350	320	350	16	16
1++	360/320	400	320	400/480	16	16
2	640	200	640	200/480	16	16
2+	640	350	640	350	16	16
2++	720/640	400	640	400/480	16	16
3	640	200	640	200/480	16	16
3+	640	350	640	350	16	16
3++	720/640	400	640	400/480	16	16
4	320	200	320	200/480	4	4
5	320	200	320	200/480	4	4
6	640	200	640	200/480	2	2
7	720/640	350	640	350	2	2
7+	720/640	400	640	400/480	2	2
0D	320	200	320	200/480	16	16
0E	640	200	640	200/480	16	16
0F	640	350	640	350	2	2
10	640	350	640	350	16	16
11	640	480	640	480	2	2
12	640	480	640	480	16	16
13	320	200	640	400/480	64	256

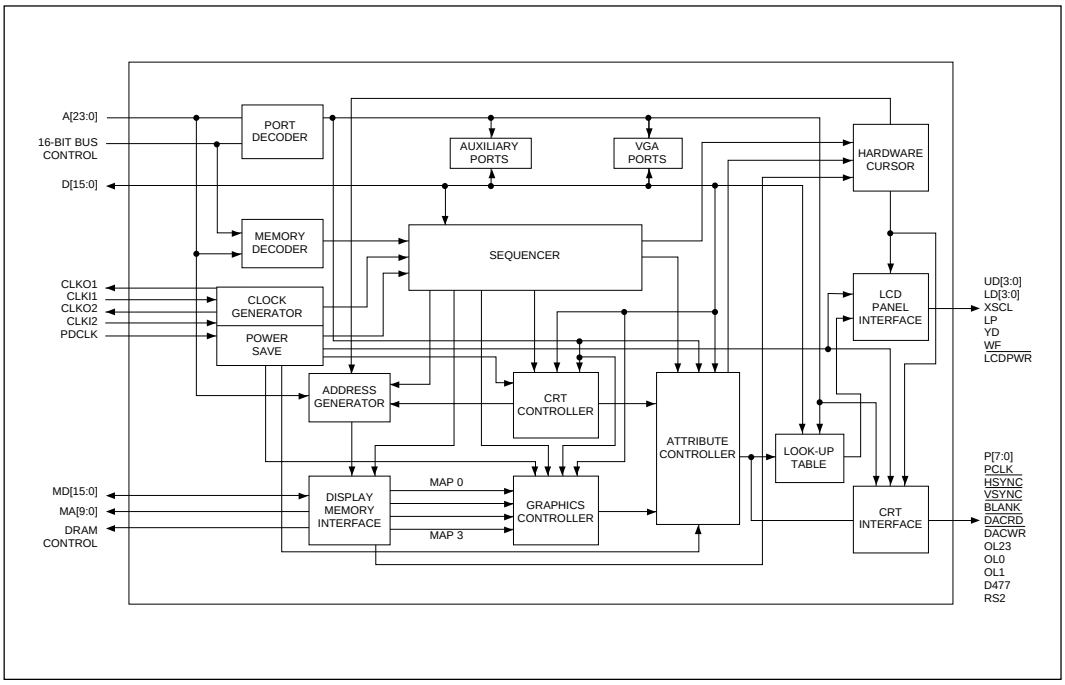
Notes: 400 line text and graphics modes can be stretched vertically to 480 lines as an option.

360 and 720 dot text modes are actually displayed as 320 and 640 dots on an LCD panel.

■ SUPPORTED STN LCD PANELS

8-bit Interface				4-bit Interface	
Dual Panel		Single Panel		Single Panel	
Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
640	400 480	640	400 480	320 480 640	200 240 320 400 480

■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

The Sequencer

The Sequencer generates internal signals to synchronize the operation of the chip as well as the signals to control the timing of the display DRAM. The Sequencer also arbitrates between CPU and video display accesses to the DRAM. It contains registers that allows selection of character font set, control the structure of the video memory and allow write masking of the individual plane of memory.

CRT Controller

The CRT Controller generates the horizontal and vertical synchronization signals for the CRT, single panel or dual panel LCD display and character and/or pixel addresses for display data from DRAM.

CRT Interface

The CRT interface aligns CRT signals to the Pixel Clock and generates the I/O Control signals for CPU access to the RAMDAC.

Address Generator

The Address Generator takes the display and refresh addresses from the CRT Controller and converts them into RAS and CAS addresses for the display DRAM, and multiplexes these display accesses with CPU memory accesses.

Attributes Controller

The Attributes Controller takes in pixel and attribute information from the Graphics Controller and display DRAM and formats the data into pixel information which then passes through the lookup table. It also controls display character attributes such as blink, underline and horizontal pixel panning.

Graphics Controller

The Graphics Controller supplies display memory data to the Attributes Controller during display time and provides data translation between the CPU bus and the display memory during CPU read or write access cycles.

Memory Decoder

The Memory Decoder monitors the CPU-bus activity and decodes cycles for the display DRAM. It supplies memory access control signals to the Sequencer.

Port Decoder

The Port Decoder decodes CPU-bus I/O cycles to provide enable and write strobes for the on-chip I/O registers.

Auxiliary Ports

The Auxiliary Ports are I/O registers used to control functions of the chip beyond the basic VGA register set. Registers are included for controlling the LCD interface circuits as well as the power save modes.

VGA Ports

The VGA Ports contain the Miscellaneous Output Status register and the Video Subsystem Enable register used in VGA mode.

Clock Generation

The Clock Generation contains oscillator support for external crystals.

Power Save

The Power Save block contains the logic to implement four software controlled and one hardware controlled power down modes.

Lookup Table

The Lookup Table consists of a memory array of 256 locations of 6 bits each and hardware to convert VGA palette writes to gray scale values.

LCD Interface

The LCD Interface block converts the display video data from the Lookup Table into LCD display data. It also generates control signals necessary to drive single or dual-panel LCD panels. The LCD interface block generates 16 levels of gray shades through frame rate modulation techniques and 64 levels of grey shades with additional dithering techniques.

Hardware Cursor

The Hardware Cursor block generates a 64 x 64 x 4 grey shade cursor or sprite that can be overlayed on the current displayed image.

■ DC SPECIFICATIONS

● Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS}–0.3 to +7.0	V
V_{IN}	Input Voltage	V_{SS}–0.3 to V_{DD}+0.3	V
V_{OUT}	Output Voltage	V_{SS} to V_{DD}	V
T_{OPR}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–65 to +150	°C
T_{SOL}	Soldering Temperature/Time	260 for 10 sec max at lead	°C

● Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage	V_{SS} = 0V	4.75	5.0	5.25	V
V_{IN}	Input Voltage		V_{SS}	—	V_{DD}	V
I_{OPR}	Average Power Consumption (estimated)		—	125	—	mA
IP_{D1}	Power Save Mode 1		—	75	—	mA
IP_{D2}	Power Save Mode 2		—	20	—	mA
$IP_{D3, 4}$	Power Save Modes 3, 4		—	1	—	mA
IP_{DSUS}	SUSPEND Mode		—	0.5	—	mA

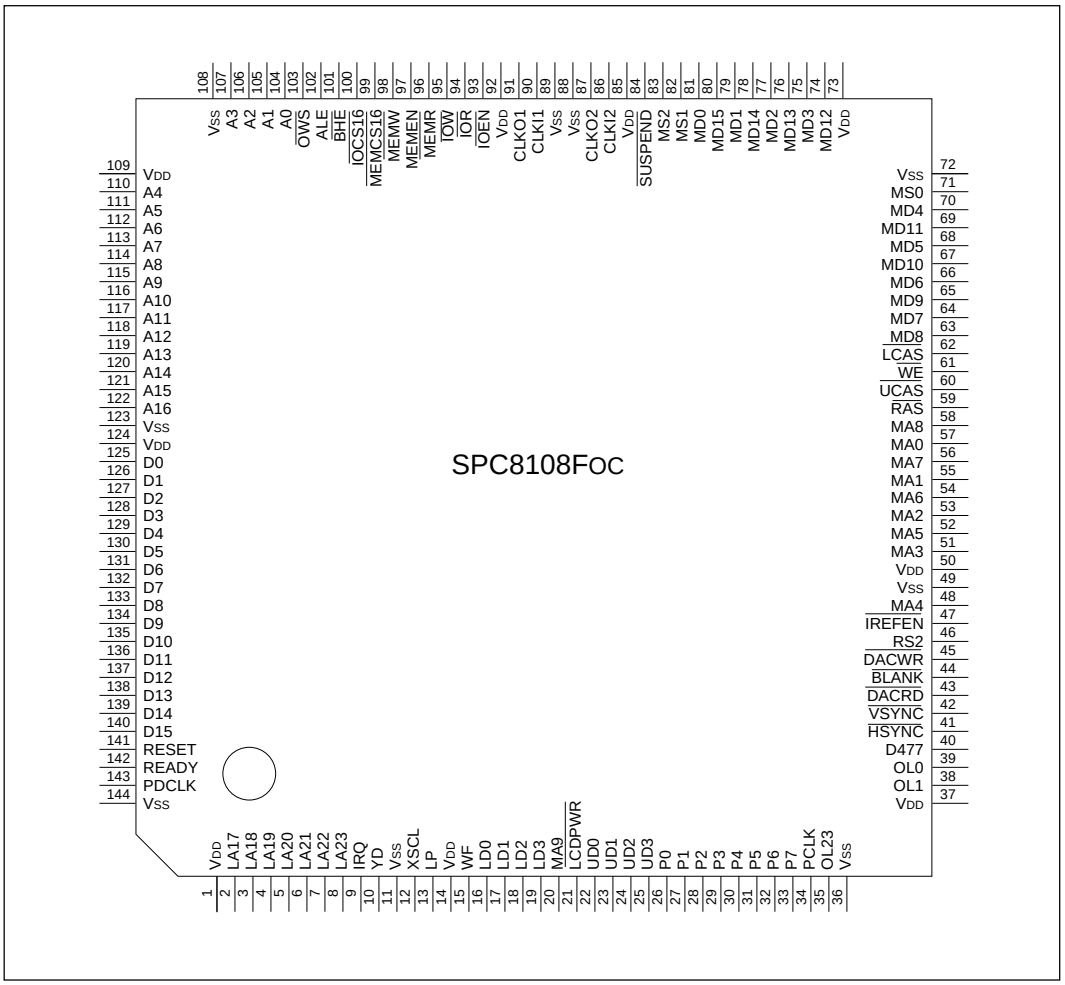
- **Input Specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (CMOS Inputs)	V_{DD} = MIN	—	—	1.0	V
V_{IL}	Low Level Input Voltage (TTL Inputs)	V_{DD} = MIN	—	—	0.8	V
V_{IH}	High Level Input Voltage (CMOS Inputs)	V_{DD} = MAX	3.5	—	—	V
V_{IH}	High Level Input Voltage (TTL Inputs)	V_{DD} = MAX	2.0	—	—	V
V_{T+}	Positive-going Threshold (TTL Schmitt inputs)	V_{DD} = 5.0	—	—	3.0	V
V_{T-}	Negative-going Threshold (TTL Schmitt inputs)	V_{DD} = 5.0	0.6	—	—	V
V_H	Hysteresis Voltage (TTL Schmitt inputs)	V_{DD} = 5.0	0.1	—	—	V
I_{IZ}	Input Leakage Current	V_{DD}= MAX $V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$	–1	—	1	µA
C_{IN}	Input Pin Capacitance		—	8	—	pF
R_{PU}	Pull Up Resistance	V_{DD} = 5.0 V	50	—	200	kW

- **Output Specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OL}	Low Level Output Current (TS2)	$V_{OL} = V_{SS}$+0.4V	6.0	—	—	mA
I_{OH}	High Level Output Current (TS2)	$V_{OH} = V_{DD}$–0.4V	–2.0	—	—	mA
I_O	Low Level Output Current (C03)	$V_{OL} = V_{SS}$+0.4V	12.0	—	—	mA
I_{OH}	High Level Output Current (C03)	$V_{OH} = V_{DD}$–0.4V	–4.0	—	—	mA
I_O	Low Level Output Current (TS4)	$V_{OL} = V_{SS}$+0.4V	24.0	—	—	mA
I_{OH}	High Level Output Current (TS4)	$V_{OH} = V_{DD}$-0.4V	–8.0	—	—	mA
I_{OZ}	Output Leakage Current	$V_{OH} = V_{DD}$ or $V_{OL} = V_{SS}$	–1	—	1	µA
C_{OUT}	Output Pin Capacitance		—	6	—	pF
C_{BID}	Bidirectional Pin Capacitance		—	10	—	pF

■ SPC8108 PIN OUTS



■ PIN DESCRIPTION

Key

Key

C = CMOS level input
CS = CMOS level input with hysteresis
COx = CMOS level output, x denotes cell type
TSx = Tri-state CMOS level driver, x denotes cell type
TSUx = Tri-state CMOS level driver with 100 kΩ pull up resistor, x denotes cell type

● Video Memory Interface

Pin Name	Type	Pin #	Drv	Description
MA[0:9]	O	20, 48, 51, 52, 54, 55, 56, 57, 58	TS2 (* C)	Multiplexed row/column address bits for video display memory.
MD[0:15]	I/O	63, 64, 66, 67, 68, 69, 70, 74, 75, 76, 77, 78, 79, 80, 81	TTL/ TS2U2	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET is high, or when the Sequencer is in a reset state. On the falling edge of RESET, the values on MD[3:0] and MD[12:9] are latched into a read-only Auxiliary Register and are available to be read as configuration inputs. Also, the value on MD[8:4] and MD[14:13] are used to configure various hardware options. See section on configuration options for details.
/RAS	O	59	TS3 (*C)	DRAM Row Address Strobe for single 256Kx16 DRAM.
/LCAS (/LWE)	O	62	TS3 (*C)	DRAM Column Address Strobe for low byte (/LCAS). For alternate function see *Multiple Function Pin Descriptions*.
/UCAS (/CAS)	O O	60 61	TS3 (*C)	DRAM Column Address Strobe for high byte (/UCAS). For alternate function see Multiple Function Pin Descriptions. DRAM Write Enable Strobe (/WE).
/WE (/UWE)			TS3 (*C)	For alternate function see *Multiple Function Pin Descriptions*.

- **Clock Inputs**

Pin Name	Type	Pin #	Drv	Description
CLKI1	I	90	C	This pin, along with CLKO1 is the 25.175 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO1	O	91	•	This pin, along with CLKI1 is the 25.175 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.
CLKI2	I	86	C	This pin, along with CLKO2 is the 28.322 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO2	O	87	•	This pin, along with CLKI2 is the 28.322 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.

- **CPU Interface**

Pin Name	Type	Pin #	Drv	Description
A[0:16], LA[17:23]	I	2..8, 104..107, 110..122	TTL	CPU bus address inputs. In Suspend Mode, the Address inputs are internally masked off. If the value on MD[5] at RESET = 1, then the ALE input is used to internally latch LA[23:20] and A[19:2], allowing these address bits to be driven by the processor address bus. If the value on MD[5] at RESET = 0, then standard ISA address timing is assumed.
D[0:15]	I/O	125..140	TTL TS2	16 bit ISA-Bus data bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times. In Suspend Mode, these inputs are internally masked off.
MEMEN	I	97	TTLS	ISA Bus Memory Enable. This signal should be connected to the /REFRESH signal on the ISA bus. When this signal is low (e.g. during a system memory refresh cycle), memory address decoding is disabled.
/IOR	I	94	TTL	ISA Bus I/O Read Strobe. In Suspend Mode the /IOR input is disabled.
/IOW	I	95	TTL	ISA Bus I/O Write Strobe. In Suspend Mode the /IOW input is disabled.
/MEMR	I	96	TTL	ISA Bus System Memory Read Strobe. In Suspend Mode the /MEMR input is disabled.
/MEMW	I	98	TTL	ISA Bus System Memory Write Strobe. In Suspend Mode the /MEMW input is disabled.
/IOEN	I	93	TTLS	ISA Bus I/O Enable. This input should be connected to the ISA bus AEN signal. When this signal is high, I/O address decoding is disabled. In Suspend Mode, the /IOEN input is disabled.

(continued)

- **CPU Interface (continued)**

Pin Name	Type	Pin #	Drv	Description
READY	O	142	TS2	ISA Bus READY signal. This output is driven low to force the CPU to insert wait states during memory cycles. READY is released to high-Z after a transfer is complete.
RESET	I	141	TTLS	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state. During Suspend Mode the RESET input is ignored.
IRQ	O	9	TS2	ISA Bus Vertical Interrupt. When enabled, a Vertical Retrace Interrupt will cause this signal to be driven from a logic 0 state to a logic 1 (rising-edge triggered interrupt). Once set, this interrupt must be cleared by a bit in the CRTC registers. A control bit in the Auxiliary Registers allows this output to be optionally disabled (tri-stated)
/MEMCS16	O	99	TS4 (*C)	ISA BusMemory Chip Select 16.
/IOCS16	O	100	TS4 (*C)	ISA Bus I/O Chip Select 16
/BHE	I	101	TTL	ISA Bus Byte High Enable. In Suspend Mode the /BHE input is disabled.
ALE	I	102	TTL	ISA Bus Address Latch Enable. In Suspend Mode the ALE input is disabled. If the value on MD[5] at RESET = 1, then the ALE input is used to internally latch LA[23:17] and A[16:2], allowing these address bits to be driven by the processor address bus. If the value on MD[5] at RESET = 0, then standard ISA address timing is assumed.
/0WS	O	103	TS2	ISA Bus 0 Wait State. This signal will be driven low during I/O accesses to indicate 0 wait state cycles may be performed. When inactive, this output will be in the high-impedance state.

- **External CRT/RAMDAC Interface**

Pin Name	Type	Pin #	Drv	Description
P[0:7]	O	26..33	TS2	Pixel Data outputs. These 8 bits are connected to the pixel select inputs of the external RAMDAC.
PCLK	O	34	TS2	Pixel Clock. Pixel data is clocked out of the chip on the falling edge of PCLK.
/BLANK	O	44	TS2	Blank output. This output is driven low during display blanking periods.
/HSYNC	O	41	TS4	Horizontal Sync. This output is driven to indicate the horizontal retrace period. The polarity of this signal is determined by a control bit in register 3C2H.
/VSYNC	O	42	TS4	Vertical Sync. This output is driven to indicate the vertical retrace period. The polarity of this signal is determined by a control bit in register 3C2H.
/DACRD	O	43	TS2	RAMDAC Read Strobe. This signal goes low when a valid read access to the VGA RAMDAC is decoded by the chip.
/DACWR	O	45	TS2	RAMDAC Write Strobe. This signal goes low when a valid write access to the VGA RAMDAC is decoded by the chip.
RS2	O	46	TS2	Register Select 2 output. This output should be connected to the RS2 input of the RAMDAC (Bt477 or equivalent). The logic level on this output may be set by setting Auxiliary Reigister [0B] bit 3. This signal is required to allow CPU access the control and overlay registers of the external RAMDAC.
OL[0:1]	O	38, 39	TS2	Multiple Function Pin Function is determined by the value on MD[13] at RESET. When MD[13]=0 at RESET, these pins are outputs used to provide sprite/HW cursor function on the CRT display. In this case, these outputs should be connected to the OL[0:1] inputs of the RAMDAC (Bt477 or equivalent). They are used by the sprite circuitry to access the overlay registers in the RAMDAC. When MD[13] = 1 at RESET, the sprite/HW cursor function is unavailable on the CRT display. Refer to functional specification for alternate function.
OL23	O	35	TS2	Overlay Select output 2/3. This output should be connected to both the OL2 and OL3 inputs of the RAMDAC (Bt477 or equivalent). This signal is used by the sprite circuitry to access the overlay registers in the RAMDAC.
D477	O	40	TS2	477 Control Signal. This output should be connected to the 477/471 input of the RAMDAC (Bt477 or equivalent). This signal is used to access the control register of the RAMDAC and to allow it to be powered down. The logic level on this output can be controlled by setting Auxiliary Regiser [0B] bit 4, and is also controlled by the power save logic.

(continued)

- **External CRT/RAMDAC Interface (continued)**

Pin Name	Type	Pin #	Drv	Description
/IREFEN	O	47	TS2U3 (*C)	IREF Control output. This signal is used to control the external current reference source required by the RAMDAC, allowing powering down the analog circuitry when not required. When this signal is driven low, the external current reference should be enabled. When this signal is high, the external current reference should be shut off.
MS[2:0]	I	71, 82, 83	TTL	Monitor Sense inputs. There are internal pullups on each of these inputs. These signals should be connected to the monitor sense lines from the CRT monitor cable. The status of these bits is readable in Auxiliary register [08] bits 2:0, and is used by BIOS software to determine the presence and type of monitor connected. Optionally, the SENSE output of the RAMDAC may be connected to one of these inputs to allow the BIOS to read the SENSE signal and detect the monitor.

- **Power Save Mode Control**

Pin Name	Type	Pin #	Drv	Description
/SUSPEND	I	84	CS	A low level on this pin puts the chip into a hardware power down mode. The /SUSPEND signal overrides any software initiated power down modes, and disables the ISA-Bus interface inputs. Address and Data inputs are also masked when this signal is low. When in Suspend Mode the UD(3:0), LD(3:0), XSCL, and WF signals are driven into a high impedance or low state (configurable) and the /LCDPWR signal is driven high.
PDCLK	I	143	TTL	Power Down Clock. This input may be used to provide a low frequency clock for generating refresh in Power Save Modes 4 and Suspend, as an optional alternative to using the pixel clock or MEMEN input as the refresh clock source. This clock input should be driven by either a 64 kHz or 32 kHz clock source. If using a 32 kHz clock source, MD[14] must be set to 0 at reset. Refer to the SPC8108 Functional Specification for PDCLK support details. If the use of Power Save modes while driving a CRT monitor is required, then this PDCLK input must be driven by a 32 kHz clock, since this input is used to generate sync signals to the CRT when a Power Save Mode is enabled.

- **Power Supply**

Pin Name	Type	Pin #	Description
VDD	P	14,37,85,92,109	VDD supply for core logic.
VDD	P	1, 50, 73, 124	VDD supply for I/O pins.
VSS	P	11,36,88,89,108	VSS supply for core logic.
VSS	P	49, 72, 123, 144	VSS supply for I/O pins.

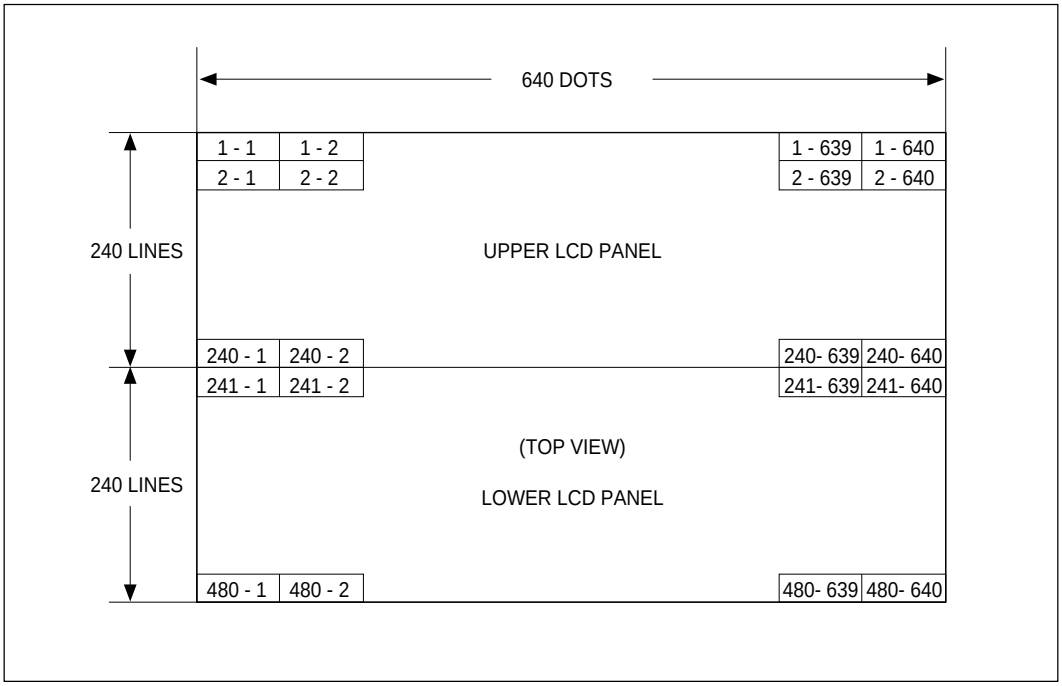
- **Configuration Options**

Pin Name	Value on this pin at falling edge of RESET is used to configure: (1/0)
MD[3:0]	Values latched into read-only Aux Reg[0C] bits 3:0 for software use
MD[4]	Reserved
MD[5]	A[19:2] latched internally by ALE (1) / standard ISA bus ALE - A[16:0] not latched (0) (this pin only has an effect if MD[4] = 1 at RESET)
MD[6]	2 CAS, 1 WE type DRAM (1) / 1 CAS, 2 WE type DRAM (0)
MD[7][8]	Reserved
MD[12:9]	Values latched into read-only bits 7:4 of Aux Reg[0C] for software use
MD[13]	Pins 38, 39 used for ext. RC for 32kHz PDCLK (1) / pins 38, 39 used for OL[1:0] (0)
MD[14]	Internal PDCLK disable (1) /enable (0)

- **LCD Panel Interface**

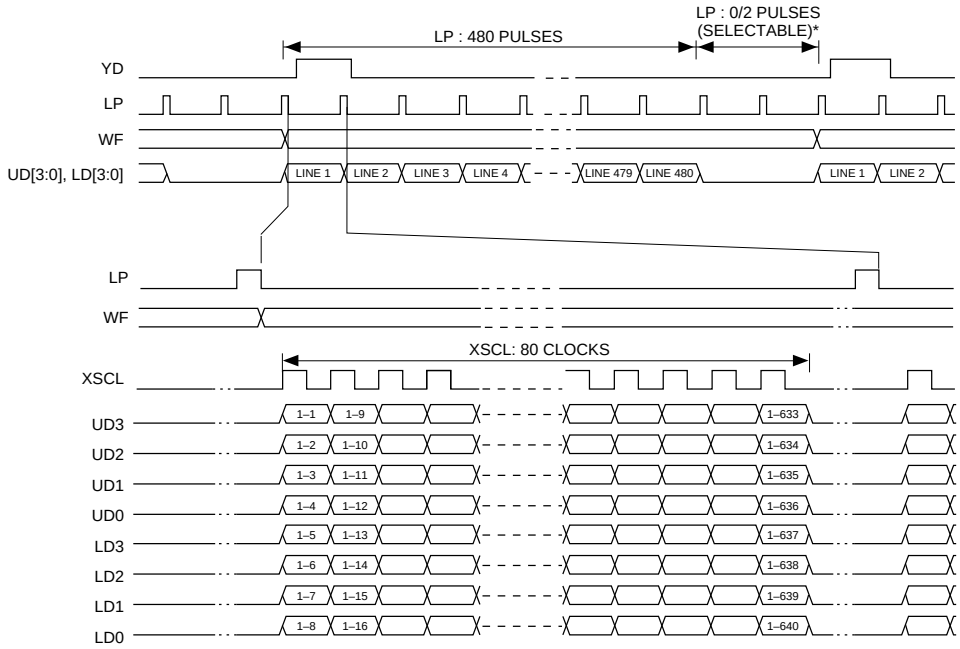
Pin Name	Type	Pin #	Drv	Description
YD	O	10	TS4	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of the vertical frame.
LP	O	13	TS4	Latch Pulse output. The falling edge of this signal is used to latch a row of display data in the LCD module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	O	12	TS4	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal, to be shifted into the LCD panel module column drivers (X drivers) on each falling edge.
UD[0:3]	O	22..25	TS4	Upper panel display data for dual panel - dual drive mode. For 8-bit single panel - single drive mode, these bits are the most significant 4 bits of the 8 bit output data to the panel (PD[4:7]). For 4 -bit single panel mode, these bits are the 4 bits of data output to the panel.
LD[0:3]	O	16..19	TS4	Lower panel display data for dual panel - dual drive mode. For 8-bit single panel - single drive mode, these bits are the least significant 4 bits of the 8 bit output data to the panel (PD[0:3]). For 4-bit single panel mode, these outputs are driven low.
/LCDPWR	O	21	TS2	LCD power control. In normal operation this signal is driven low to enable an external LCD power supply. This signal is driven high when the chip is put into any power save mode, or if the Sequencer is in a reset state. It can be used externally to turn off the panel supply voltage and backlight. After a RESET, this signal is held high until the CRTC is programmed and running.
WF	O	15	TS2	LCD Backplane Bias signal. This output can be programmed to toggle once per frame or once per 1-31 latch pulses (LP).

■ **LCD Panel Pixels**



■ LCD Panel Interface

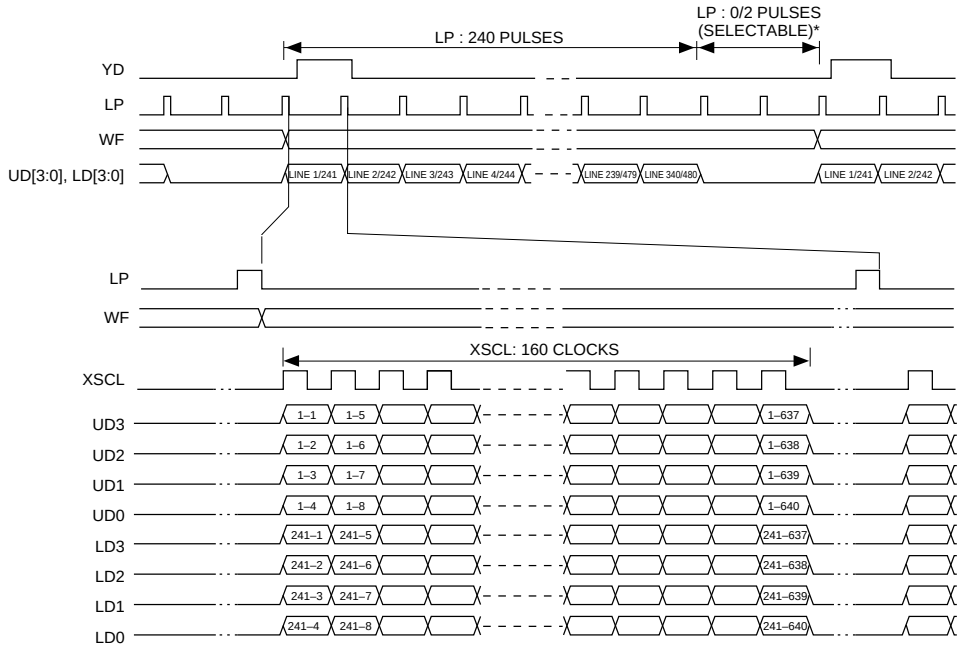
8-Bit Single Panel



* Diagram drawn with 2 LP vertical blank period

■ LCD Panel Interface

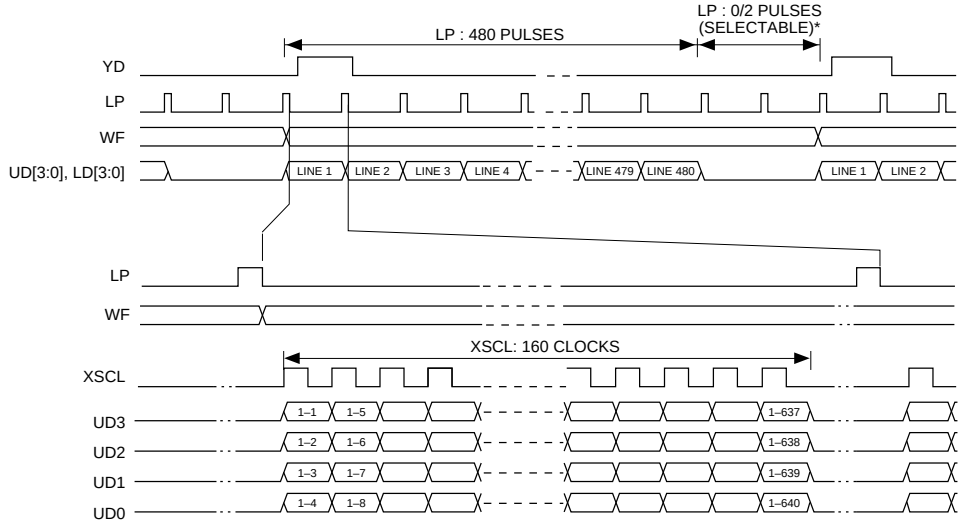
8-Bit Dual Panel



* Diagram drawn with 2 LP vertical blank period

■ LCD Panel Interface

4-bit Single Panel



* Diagram drawn with 2 LP vertical blank period

See Functional Specifications for variations in 4–bit timing.