TC8512G/YM

TENTATIVE

High Speed Shading Processor

1. GENERAL DESCRIPTION

The 3-D Graphics Processor (HSP) is an advanced high-performance VLSI chip for high-speed Smooth Shading and other 3-D, 2-D graphics functions. By controlling dual-port VRAM extensively, the HSP enables high-performance low-cost 3-D Graphics System, which has traditionally required many discrete components or software approach by host system, By using 4 chips in parallel, up to 24M Gouraud-shaded pixel/sec (@12MHz) performance can be achieved.

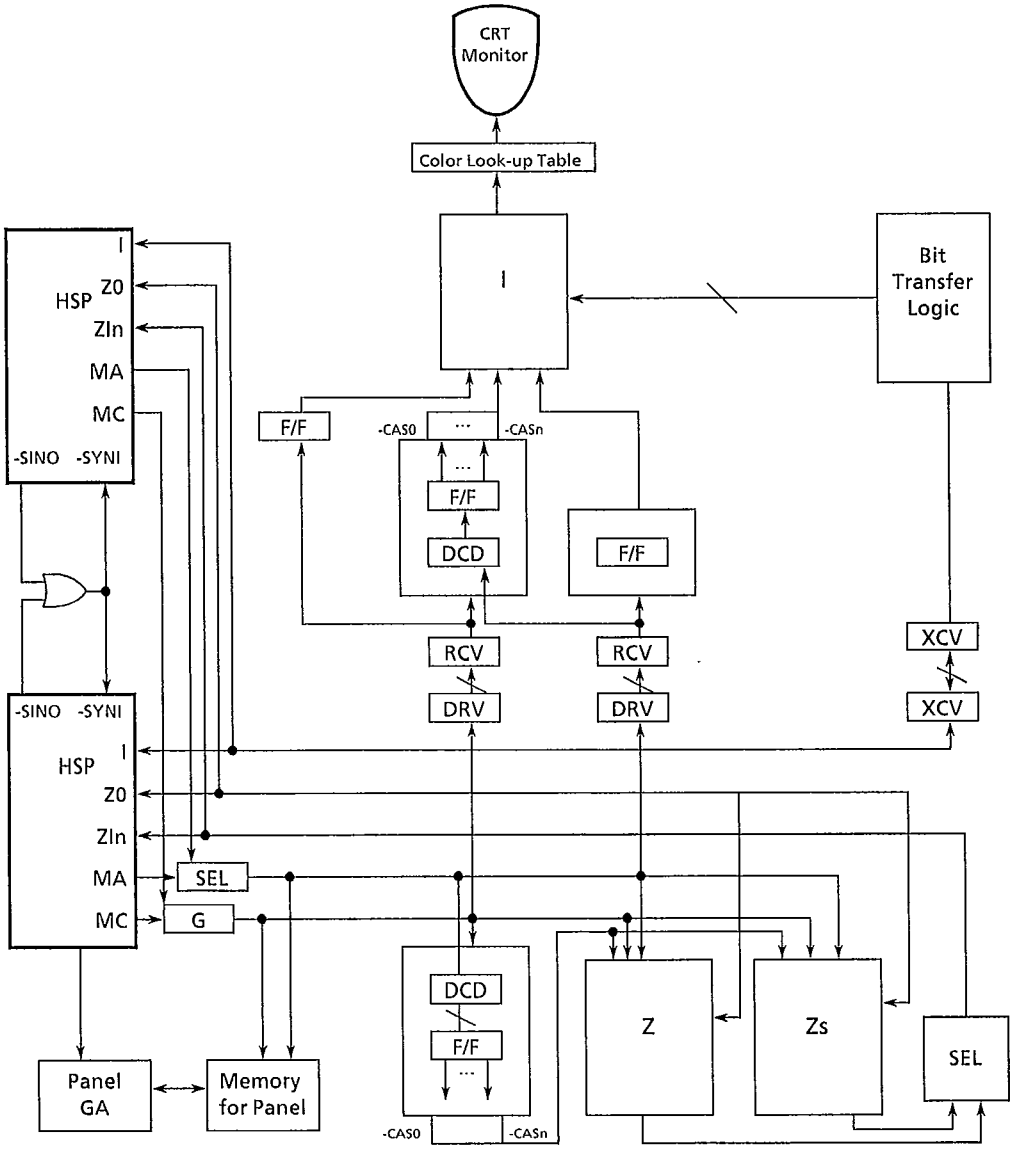
In one chip, the HSP architecture includes a 32-bit command processor, a pixel controller for shading, line drawing and other bit-map operation, dual-port video RAM control interface, and window logic. With advanced 1.2μm CMOS technology of TOSHIBA, over 130,000 transistors are integrated on the single VLSI chip.

2. FEATURES

- ☐ Si-gate CMOS technology
- ☐ +5V single power supply
- ☐ 144 pin Ceramic Flat or metal PGA package
- ☐ Dual-port VRAM control except for refreshing
- ☐ Variety of graphics functions on a single chip
- ☐ Multi-chip configuration support for faster Gouraud Shading, Address Generation and RGB support

3. HSP CONFIGURATION EXAMPLE

3.1 HSP CONFIGURATION EXAMPLE (2 CHIP CONFIGURATION)



4. PIN DESCRIPTIONS

4.1 PIN CONFIGURATION (Ceramic Flat Package)

PIN	I/O	SYMBOL	PIN	I/O	SYMBOL	PIN	I/O	SYMBOL
1	G	VSS	35	I	ZI8	69	O	-SRTP
2	I	WAIT	36	I	ZI7	70	I/O	B/P
3	O	-ADGD	37	G	VSS	71	O	XFR
4	O	-ADGS	38	I	ZI6	72	O	AM
5	O	FAST	39	I	ZI5	73	G	VSS
6	I/O	I15	40	I	ZI4	74	O	XREN
7	I/O	I14	41	I	ZI3	75	O	XLEN
8	I/O	I13	42	I	ZI2	76	O	YTEN
9	I/O	I12	43	I	ZI1	77	O	YBEN
10	I/O	I11	44	I	ZI0	78	I	-RESET
11	I/O	I10	45	I/O	ZO15	79	I	TEST
12	I/O	I9	46	I/O	ZO14	80	I	-RDX
13	I/O	I8	47	I/O	ZO13	81	V	VDD
14	I/O	I7	48	I/O	ZO12	82	I	-WDX
15	I/O	I6	49	I/O	ZO11	83	O	IBSY
16	I/O	I5	50	I/O	ZO10	84	O	NFLL
17	I/O	I4	51	I/O	ZO9	85	O	CBSY
18	V	VDD	52	I/O	ZO8	86	I/O	D0
19	G	VSS	53	I/O	ZO7	87	I/O	D1
20	I/O	I3	54	I/O	ZO6	88	I/O	D2
21	I/O	I2	55	I/O	ZO5	89	I/O	D3
22	I/O	I1	56	V	VDD	90	G	VSS
23	I/O	I0	57	G	VSS	91	V	VDD
24	O3	-WEZS	58	I/O	ZO4	92	I/O	D4
25	O3	-WEZ	59	I/O	ZO3	93	I/O	D5
26	O3	-WEI	60	I/O	ZO2	94	I/O	D6
27	I	ZI15	61	I/O	ZO1	95	I/O	D7
28	I	ZI14	62	I/O	ZO0	96	I/O	D8
29	I	ZI13	63	O	-REQ	97	I/O	D9
30	V	VDD	64	O	-SYNO	98	I/O	D10
31	I	ZI12	65	I	-SYNI	99	I/O	D11
32	I	ZI11	66	O	M/I	100	I/O	D12
33	I	ZI10	67	I/O	-PXEND	101	I/O	D13
34	I	ZI9	68	I/O	-PYEND	102	I/O	D14

DISPLAY CONTROLLER

PIN	I/O	SYMBOL	PIN	I/O	SYMBOL	PIN	I/O	SYMBOL
103	I/O	D15	117	O3	MA17	131	O3	MA6
104	I	A0	118	O3	MA16	132	I/O	MA5
105	I	A1	119	O3	MA15	133	I/O	MA4
106	I	A2	120	O3	MA14	134	I/O	MA3
107	I	A3	121	O3	MA13	135	I/O	MA2
108	O3	MA25	122	O3	MA12	136	I/O	MA1
109	G	VSS	123	O3	MA11	137	I/O	MA0
110	O3	MA24	124	G	VSS	138	O	OEACK
111	O3	MA23	125	V	VDD	139	O3	-RAS
112	O3	MA22	126	I	CLK	140	O3	-CAS
113	O3	MA21	127	O3	MA10	141	O3	-DTOEZ
114	O3	MA20	128	O3	MA9	142	O	SC
115	O3	MA19	129	O3	MA8	143	O	RD/WD
116	O3	MA18	130	O3	MA7	144	O3	-DTOEI

4.2 PIN CONFIGURATION (Metal PGA Package)

NO.	I/O	NAME	NO.	I/O	NAME	NO.	I/O	NAME	NO.	I/O	NAME
1(144)	O3	-DTEI	37 (92)	I/O	D4	73 (46)	I/O	ZO14	109 (13)	I/O	I8
2 (3)	O	-ADGD	38 (93)	I/O	D5	74 (48)	I/O	ZO12	110 (18)	V	VDD
3 (6)	I/O	I15	39 (97)	I/O	D9	75 (52)	I/O	ZO8	111 (19)	G	VSS
4 (8)	I/O	I13	40 (99)	I/O	D11	76 (58)	I/O	ZO4	112 (24)	O3	-WEZS
5 (11)	I/O	I10	41(100)	I/O	D12	77 (59)	I/O	ZO3	113 (30)	V	VDD
6 (14)	I/O	I7	42 (104)	I	A0	78 (62)	I/O	ZO0	114 (33)	I	ZI10
7 (15)	I/O	I6	43 (108)	O3	MA25	79 (65)	I	-SYNI	115 (34)	I	ZI9
8 (17)	I/O	I4	44 (111)	O3	MA23	80 (67)	I/O	-PXEND	116 (37)	G	VSS
9 (20)	I/O	I3	45 (114)	O3	MA20	81 (71)	O	XFR	117 (41)	I	ZI3
10 (21)	I/O	I2	46 (116)	O3	MA18	82 (74)	O	XREN	118 (45)	I/O	ZO15
11 (25)	O3	-WEZ	47 (119)	O3	MA15	83 (76)	O	YTEN	119 (49)	I/O	ZO11
12 (27)	I	ZI15	48 (122)	O3	MA12	84 (79)	I	TEST	120 (54)	I/O	ZO6
13 (28)	I	ZI14	49 (123)	O3	MA11	85 (82)	I	-WDX	121 (55)	I/O	ZO5
14 (32)	I	ZI11	50 (125)	V	VDD	86 (84)	O	NFLL	122 (60)	I/O	ZO2
15 (36)	I	ZI7	51 (128)	O3	MA9	87 (88)	I/O	D2	123 (66)	O	M/I
16 (39)	I	ZI5	52 (129)	O3	MA8	88 (94)	I/O	D6	124 (69)	O	-SRTP
17 (42)	I	ZI2	53 (133)	I/O	MA4	89 (95)	I/O	D7	125 (70)	I/O	B/P
18 (44)	I	ZI0	54 (135)	I/O	MA2	90 (98)	I/O	D10	126 (73)	G	VSS
19 (47)	I/O	ZO13	55 (136)	I/O	MA1	91(101)	I/O	D13	127 (77)	O	YBEN
20 (50)	I/O	ZO10	56 (140)	O3	-CAS	92(103)	I/O	D15	128 (81)	V	VDD
21 (51)	I/O	ZO9	57 (143)	O	RD/WD	93(107)	I	A3	129 (85)	O	CBSY
22 (53)	I/O	ZO7	58 (2)	I	WAIT	94(110)	O3	MA24	130 (90)	G	VSS
23 (56)	V	VDD	59 (4)	O	-ADGS	95(112)	O3	MA22	131 (91)	V	VDD
24 (57)	G	VSS	60 (7)	I/O	I14	96(115)	O3	MA19	132 (96)	I/O	D8
25 (61)	I/O	ZO1	61 (10)	I/O	I11	97(118)	O3	MA16	133(102)	I/O	D14
26 (63)	O	-REQ	62 (12)	I/O	I9	98(120)	O3	MA14	134(105)	I	A1
27 (64)	O	-SYNO	63 (16)	I/O	I5	99(124)	G	VSS	135(106)	I	A2
28 (67)	I/O	-PYEND	64 (22)	I/O	I1	100(130)	O3	MA7	136(125)	V	VDD
29 (72)	O	AM	65 (23)	I/O	I0	101(131)	O3	MA6	137(113)	O3	MA21
30 (75)	O	XLEN	66 (26)	O3	-WEI	102(134)	I/O	MA3	138(117)	O3	MA17
31 (78)	I	-RESET	67 (29)	I	ZI13	103(137)	I/O	MA0	139(121)	O3	MA13
32 (80)	I	-RDX	68 (31)	I	ZI12	104(139)	O3	-RAS	140(126)	I	CLK
33 (83)	O	IBSY	69 (35)	I	ZI8	105(142)	O	SC	141(127)	O3	MA10
34 (86)	I/O	D0	70 (38)	I	ZI6	106 (1)	G	VSS	142(132)	I/O	MA5
35 (87)	I/O	D1	71 (40)	I	ZI4	107 (5)	O	FAST	143(138)	O	OEACK
36 (89)	I/O	D3	72 (43)	I	ZI1	108 (9)	I/O	I12	144(141)	O3	-DTOEZ

* Pin number in parentheses are ceramic flat package (TC8512G).

4.3 PIN FUNCTION

The host interface pins are used for communication between the HSP and a host processor.

SYMBOL	I/O	DESCRIPTION
D15-D0	I/O	Data Bus : The host data pins, D15-D0, form a bidirectional 16-bit bus. The bus inputs Graphics Parameter or Image Data, and outputs Image Data from the Frame Buffer Memory (FBM).
A3-A0	I	Address Bus : The Address Bus inputs Graphics Commands together with Graphics Parameter from the Data Bus. At Image Data Input or Output operation, these pins are used as Acknowledgement of Data transfer.
-WDX	I	Write Data Strobe: The -WDX is Write Strobe of the Data through D15-D0 and A3-A0. The data is either the Graphics Commands sending to FIFO or Image Data not though FIFO but directly sending to FBM.
-RDX	I	Read Data Strobe: The -RDX is Read Strobe of Image Data from FBM. While active low, Data Bus is switched toward Output direction.
TEST	I	Test : The TEST is used by HSP test. Normally, it should be kept in "Low level".
CBSY	O	Channel Busy : The CBSY remains high during the HSP is in operation, as follows. a. Some unprocessed command or data still remain in FIFO. b. Command Processor is processing. c. Pixel processor is in operation.
NFLL	O	Not Full : The NFLL indicates whether FIFO is full or not. 1- FIFO is not full. Command data transfer is available. 0- FIFO is full. Command data transfer is not available.
IBSY	O	Image Data Transfer Busy : The IBSY is the synchronous signal at Image Input/Output operation. 1- The HSP is reading Image Data from FBM or writing to FBM. Host processor must wait during this high period. 0- The HSP has finished reading or writing Data and is ready to next Data transfer.
CLK	I	Clock : The One-Phase 50% duty cycle Clock provides the basic timing for the HSP.
-RESET	I	Reset : The -RESET causes the HSP to initialize internal state. This signal must be active lo and is enough only one clock cycle to initialize. -RESET is internally synchronized.

The HSP support dual-port VRAMs as the Frame Buffer Memory (FBM) and Z-buffer. The following signals are used to control dual-port VRAMs.

SYMBOL	TYPE	DESCRIPTION
-RAS	O, 3-state	Row Address Strobe : The -RAS output is used to drive the -RAS inputs of dual-port VRAMs.
-CAS	O, 3-state	Column Address Strobe : The -CAS output is either the timing for the -CAS inputs of dual-port VRAMs or the enable signal to generate the -CAS timing of dual-port VRAMs in external circuits. (1) Random access mode The -CAS is the timing signal for DRAMs. But the -CAS signal changes earlier than normal timing by one clock cycle, the external circuits need to delay this signal one clock cycle. (2) Page mode a. FAST = 0 The -CAS is the enable signal. In the external circuits, the generation of CAS timing is required. b. FAST = 1 b-1 FS = 0 The same as the random access mode b-2 FS = 1 The -CAS is the enable signal. In the external circuits, the generation of CAS timing is needed.
XFR	O	Data Transfer : The XFR indicates that HSP is in serial-read cycle of Z-buffer, and used to inhibit the access to the FBM.
-DTOEI	O, 3-state	Data Transfer/Output Enable to I memory : The -DTOEI output is used to drive the DT/OE (or TR/OE) inputs of dual-port VRAMs of I data. During dual-port VRAM shift-register-transfer cycle, DT/OE is driven active low during high-to-low transition of -RAS . During serial read of Z value for Z compare, this signal is kept high to be non-active and -WEI is also high level.
-DTOEZ	O, 3-state	Data Transfer/Output Enable to Z Buffer : The -DTOEZ output is used to drive the DT/OE (or TR/OE) inputs of dual-port VRAMs of Z Buffer. During dual-port VRAM shift-register-transfer cycle, DT/OE is driven active low during high-to-low transition of -RAM. During serial read of Z value for Z compare, this signal is used to enable serial read from the Z VRAM.
SC	O	Serial Clock : The SC output is used to drive the SC inputs of dual-port VRAMs. This pin is used only for Z-buffer.
RD/WD	O	Read/Write : RD/WD indicates whether HSP read or write dual-port VRAMs. 1- reading memory 0- writing memory

DISPLAY CONTROLLER

SYMBOL	TYPE	DESCRIPTION
-ADGD	O	Address Generator Destination : -ADGD is used to switch the memory pins of the two HSPs in the address generator mode. 0- During low period, memory timing and addrss pins of destination HSP should be used. 1- During high period, memory timing and address pins of source HSP should be used.
-ADGS	O	Address Generator Source : The -ADGS indicates whether HSP is set source LSI in the address generator mode or other operation mode. 0- The HSP is set as a source LSI in the address generator mode 1- The HSP is set in other operation mode
FAST	O	FAST : The FAST indicates whether 16pixel access mode (constant shading) or not. This signal is used to generate CAS timing described at the -CAS part.
-WEI	O, 3-state	Write Enable of the Index buffer : The -WEI is the write enable signal of FBM.
-WEZ	O, 3-state	Write Enable of the Z-buffer : The -WEZ is the write enable signal of the Z-buffer.
-WEZS	O, 3-state	Write Enable of the Z Sectioning buffer : The -WEZS is the write enable signal of the Z sectioning buffer.
M/I	O	Mask / Index : The M/I indicates which data output from I pins. 1- Color Index data from I pins. 0- Maskbit data for write-per-bit of DRAMs from I pins. For image data input operation, the M/I generates the select signal of the Z data input from the Z Buffer or from the Z Section Buffer. 1- Z data input from the external Z Section Buffer. 0- Z data input from the V Buffer
I15-I0	I/O,3-state	Color Intensity (or Index) Data Bus : The Color Intensity (or Index) data pins, I15-I0 form a bidirectional 16-bit bus. The bus outputs the Color Intensity (or Index) data written to FBM or Mask bits for Write-per-Bit control. Also used to input Image Data from FBM.
ZO15-ZO0	I/O, 3-state	Z Data Bus : The Z Data Bus oututs the Z data written to the Z-buffer or Color Index Data just same as the I/O pins, and inputs Image Data from FBM.
ZI15-ZI0	I	Z Input Bus : The bus inputs the Z data or Z-sectioning data. Incase of using external Z-sectioning buffer, the bus has to be multiplexd. In HSP, the Z data are latched at the low-to-high transition edge of SC and the Z-sectioning data are latched at the high-to-low transition edge of SC.

SYMBOL	TYPE	DESCRIPTION
MA25-MA0	O, 3-state	Memory Address Bus : The MA25-MA0 form the memory address of FBM or Z buffer. The MA Bus outputs either linear address or XY-address selectively. As the MA pins handle non-multiplexed row and column addresses, the MA must be multiplexed externally.
WAIT	I	Wait : The WAIT requests to inhibit generating memory timing and to float memory pins as listed below. MA25-MA0, -RAS, -CAS, -DTOEI, -DTOEZ, ZO15-ZO0, I15-I0, -WEI, -WEZ, -WEZS
OEACK	O	Output Enable Acknowledge : The OEACK indicates that the HSP accepts WAIT request and float memory pins listed in WAIT pin.

DISPLAY CONTROLLER

SYNCHRONOUS SIGNALS

These following signals are used as the synchronous signals in the multi-chip HSP applications, such as cascaded Gouraud shading, address generator or RGB Color system.

SYMBOL	TYPE	DESCRIPTION
-SYNO	O	Synchronous signal Out. The -SYNO differs its meaning in various applications. 1. Gouraud shading cascading 2 or 4 HSPs can be cascaded for Gouraud shading. In this case, it is not matter the time differences of sending commands to FIFO. But after finishing the calculation of polygon's parameters, each pixels of polygon must be written to the memory synchronously. The -SYNO is active low when HSP finishes the calculation of one polygon's parameter and is ready to write pixels to the memory. When all of the -SYNOs of HSPs are active, HSPs begins to write the value of pixels simultaneously. 2. RGB cascaded Fundamentally, the role of this signal is same as in Gouraud shading cascading. 3. Address generator In address generator mode, two HSPs are required. One is the source address generator which generates the read address and timing, the other is the destination address generator which generates the write address and timing. The source HSP makes the -SYNO active-low when it finishes to read the data of memory (assuming that some logic like BTL (bit- transfer logic) exists). The -SYNO of the source HSP makes the -SYNO which directly connects to the -SYNO of the source HSP's active-low after finishing to write the data
-SYNI	I	Synchronous signal In : In the image input operation, the external circuits (for example the memory system) indicates that the data is prepared to be read by using this SYNI0. In other operations using multiple HSP chips, the SYNI0 is connected directly or indirectly (through some gates) to the other HSP's -SYNO described in the -SYNO part.
-PXEND	I/O	X address END : In address generator operation, two HSPs (source or destination) need to be synchronized at the end of each horizontal scan. The -PXEND indicates the final point of one horizontal scan and is used to synchronize the end of one horizontal scan.
-PYEND	I/O	Y address END : In address generator operation, two HSPs needs to be synchronized at the end of one area to be transferred. The -PYEND indicates the final line of whole area and is used to synchronize.

SIGNALS OF MEMORY STRUCTURE

These signals are used to indicate the type of the memory system structure.

SYMBOL	TYPE	DESCRIPTION
B/P	O	Block / Pixel : The B/P indicates how many pixels are written at one memory access. 1- 16pixels in horizontal scan are written at one memory access. (in constant shading mode) 0- 1pixel in 16-bit is written at one memory access.
AM	O	Address Mode : The AM indicates the structure of memory system 1- 4 x 4 two dimensional memory array for pixel cache 0- 1 x 16 one dimensional horizontal memory array for pixel cache

FILLING SIGNALS

These signals are used for the external circuits which is prepared to fill the 2-dimensioned closed polygon. They have the same circuits to generate lines as the HSP has.

SYMBOL	TYPE	DESCRIPTION
-REQ	O	Memory Request : The -REQ is the request signal accessing to the DRAMs. This signal is active for two clock cycles in advance before DRAMs are accessed.
-SRT	O	Start point : The -SRT signal indicates the first point of each lines or each scan lines.
XLEN	O	X Left Enable : The XLEN indicates that the pixel is onto or on the left side of the right border of the window.
XREN	O	X Right Enable : The XREN indicates that the pixel is onto or on the right side of the left border of the window.
YTEN	O	Y Top Enable : The YTEN indicates that the pixel is onto or below the top border of the window.
YBEN	O	Y Bottom Enable : The YBEN indicates that the pixel is onto or above the bottom border of the window.

5. FUNCTIONAL DESCRIPTIONS

The HSP chip performs several 3-D, 2-D Graphics operations with minimum external circuits. The most remarkable functional feature of it is the fast Gouraud shading in minimum system configuration. Also it has the functions such as Depth Cuing for the wire-frame representation of 3 dimensional object, 2-D Line Drawing, Address Generation for bit-map operation, Image Data bi-directional Transfer between the host and the Frame Buffer Memory (FBM).

The chip itself controls the VRAM as the FBM and the Z Buffer, except for refresh control of the VRAM. For refreshing purposes the HSP can relinquish the VRAM control through WAIT pin request. The simple commands and the necessary parameters input from the host can reduce the system bottle-neck.

5.1 GOURAUD SHADING

This is a shading for obtaining the realistic 3-dimensional objects in solid model graphics. In advance the host processor such as geometric transformation processor describes the objects by a set of convex planar polygons that approximate the surfaces of the object. As the planar polygons, triangles or trapezoids are assumed for the HSP input. Then the x, y, z coordinates and the color intensity (I) of the polygon vertices are sent to the HSP as parameters together with command. The HSP internally calculates the coordinates and the color intensity and Z (depth) value of each pixel by interpolation. It draws the I into the FBM, and controls the Z buffer (hidden-surface removal), both in each pixel write control basis.

5.1.1 TRIANGLE as a POLYGON

The general case allows to use a triangle as a polygon. The (X, Y, Z) and the (X, Y, I) of 3 vertices of a triangle can generally make two kinds of planes. There are 2 kinds of triangle input mode.

Two modes can be selected by triangle drawing command for each polygon basis.

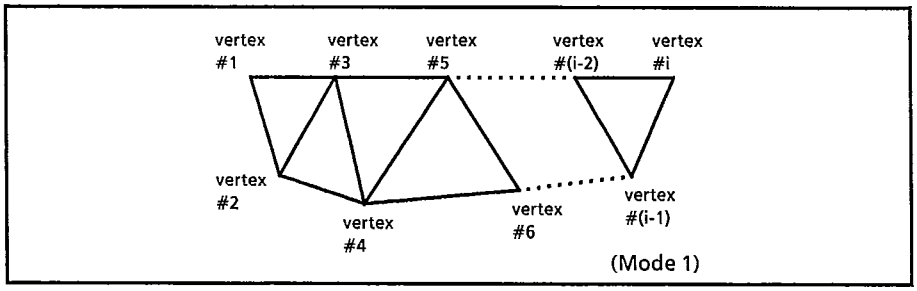


FIG.5.1.1a MODE 1

In this mode, two vertices are commonly contained in only two adjacent triangles.

STEP 1 : When the coordinates (X, Y, Z) and the color intensity information of 3 vertices P0, P1, P2 are transferred to the HSP, it starts Gouraud shading of Triangle P0, P1 ,P2.

STEP 2 : When the coordinates and the color intensity of vertex P3 are transferred to the HSP, by using the previous input values of vertices P1 and P2 it starts Gouraud shading of Triangle P1, P2, P3, and so on.

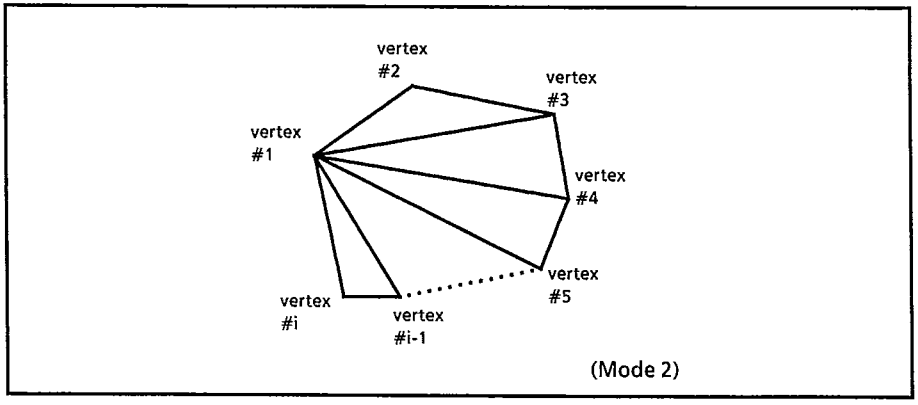


FIG.5.1.1b MODE 2

In this mode, one vertex is commonly contained in the triangle groups and other one vertex is commonly contained in two adjacent triangle.

STEP 1 : When the coordinates (X, Y, Z) and the color intensity information of 3 vertices P0, P1, P2 are transferred to the HSP, it starts Gouraud shading of Triangle P0, P1, P2.

STEP 2 : When the coordinates and the color intensity of vertex P3 are transferred to the HSP, by using the previous input values of vertices P0 and P2 it starts Gouraud shading of Triangle P0, P2, P3, and so on.

5.1.2 FASTER GOURAUD SHADING by MULTI-CHIP CONFIGURATION

For faster Gouraud shading, 2 or 4 HSP chips can be configured in parallel. In this mode the drawing performances become as follows.

- ☐ The HSP 1 chip 6M pixels/sec
- ☐ The HSP 2 chips 12M pixels/sec
- ☐ The HSP 4 chips 24M pixels/sec

For this operation, each HSP ID number should be designated by command. And each HSP should control the FBM and the Z Buffer in interleave mode. The number (i) HSP controls FBM and Z Buffer, the LSB 2 or 1 bit address of which a correspond to the 2 or 1 bit number (i).

5.2 DEPTH CUING

This is a function of representing 3-dimensional object in wire-frame shape with color intensity and hidden-point removal for wire models. The object are represented in 3-D wire-frame by transferring coordinates (X, Y, Z) and color intensities at each points sequentially.

The Z Buffer Algorithm can be applied to this function.

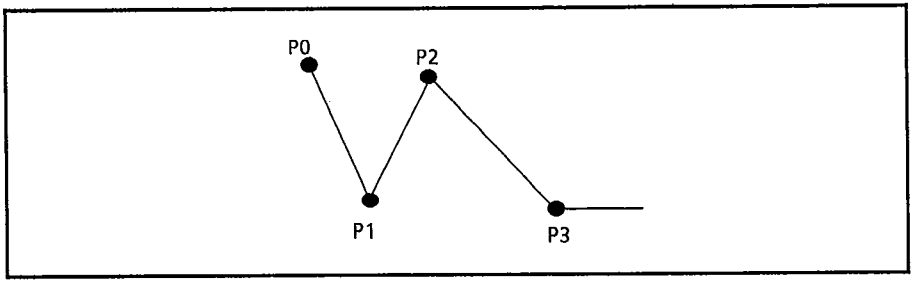


FIG.5.2

5.3 LINE DRAWING

This function enables 2-dimensional line drawing in Bresenham algorithm. It has two kinds of line generation mode.

In both modes, Opaque or Transparent options are available.

5.3.1 MODE 1 – PIXEL PATTERN GENERATION MODE

The HSP contains a 32-bit Line pattern register which is used in cyclic shift mode to enable line drawings of 2 kinds of color index for each pixel. Lines are drawn by selecting one of two color index contained in the HSP or each pixel according to 1 or 0 value of each bit of that register.

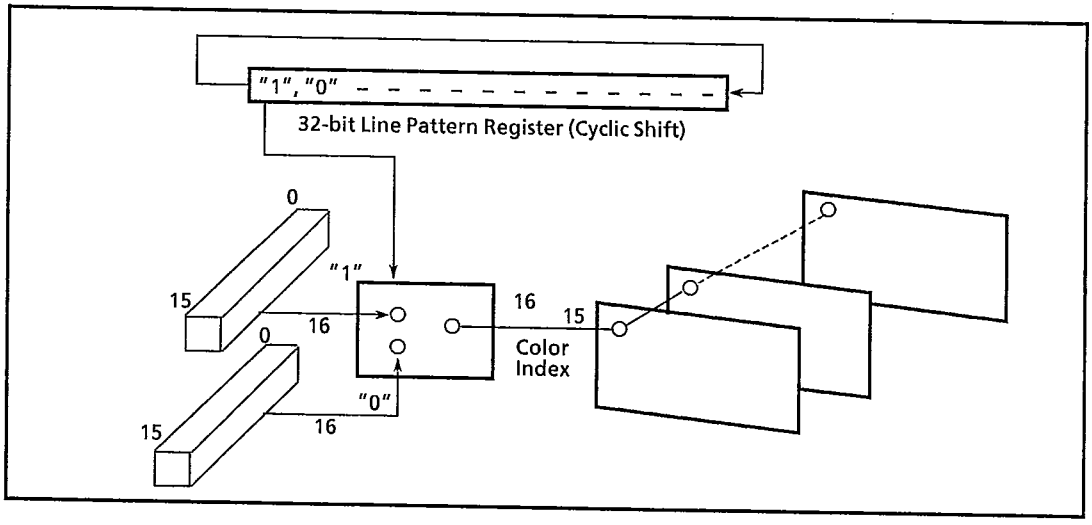


FIG.5.3.1

This line drawing is executed by each pixel (16-bit) write to the FBM. As this function does not require a external circuit, the compact hardware configuration is possible.

5.3.2 MODE 2 – LINE PATTERN GENERATION MODE

The function is described at section 5.10.2.

5.3.3 LINE MODES

There are 2 kinds of line mode.

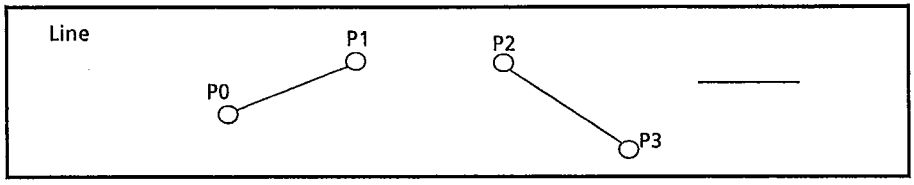


FIG. 5.3.3a

The beginning points (P0, P2, etc.) and end points (P1, P3, etc.) are designated for all lines.

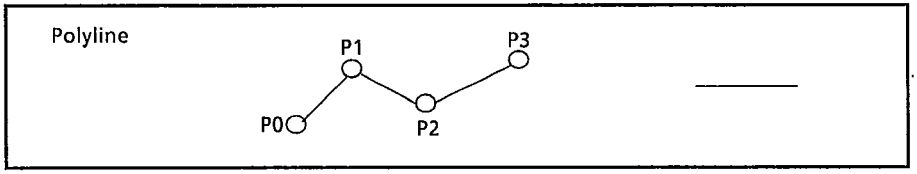


FIG. 5.3.3b

After designating the beginning point (P0), sequential points (P1, P2, etc.) are designated for connected polylines drawing.

5.4 IMAGE DATA OUTPUT TRANSFER

This function enables the data transfer (data write) from the host system to the square area of the FBM through the HSP. This data write operation has two pixel data modes of 1 pixel in 16-bit, and 16 pixels in horizontal scan line.

5.4.1 16-BIT ONE PIXEL MODE

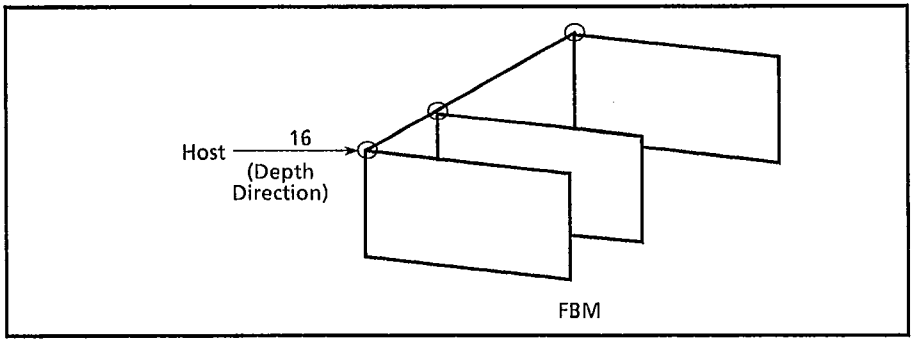


FIG. 5.4.1

5.4.2 HORIZONTAL 16 PIXELS MODE

This function is described at section 5.10.3.

5.5 IMAGE DATA INPUT TRANSFER

This function enables the data transfer (data read) to the host system from the square area of the FBM though the HSP. This data write operation has two pixel data modes of 1 pixel in 16-bit, and 16 pixels in horizontal scan line. To read the pixel data in the horizontal mode, external circuit is required to select the designated plane of the FBM.

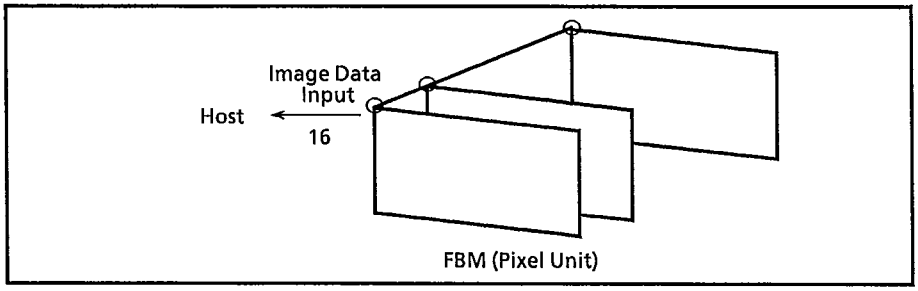


FIG.5.5a

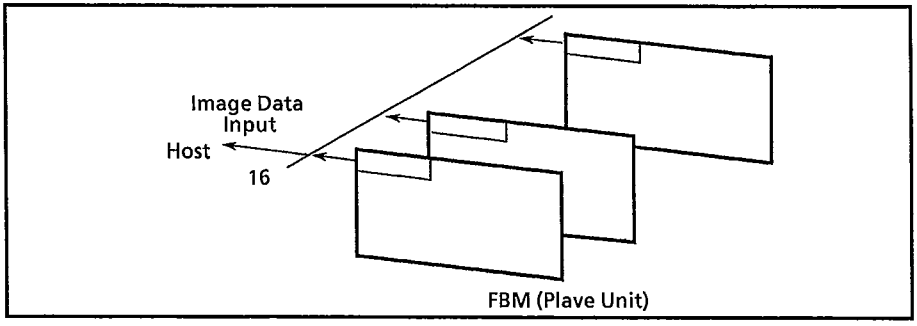


FIG. 5.5b

5.6 HIDDEN-SURFACE REMOVAL

To accomplish the hidden-surface removal based on the Z Buffer Algorithm on the HSP LSI, Z Buffer memory is required externally in the Graphic system. The Z Buffer Algorithm is implemented by the HSP chip as follows :

(a) Use the VRAM as Z Buffer Memory. (b) Write the depth value (Z coordinate) for each pixel of the 3-D object into the Z Buffer. (c) The Z Buffer always record the closest depth value of each pixel on the screen to the observer. (d) The HSP LSI reads the Z value of the current closest pixel in the scene from the serial port of the VRAM as the Z Buffer, and compares the newly computed Z value of the new object to be drawn. (e) If newly generated Z value is closer than that from the Z Buffer for each pixel location of the screen, set the new Z value to the Z Buffer and set color intensity. (f) If the opposite is the case, new Z value and color intensity writing are inhibited by controlling the WE (write enable) of the Z VRAM and the I VRAM.

This hidden-surface removal operation is available for the Gouraud shading and the Depth Cuing.

5.7 DEPTH SECTIONING

3-D objects are drawn by te HSP LSI in the form of depth sectioning. The closer parts to the observer may not be drawn or may be transparent pattern. There are two modes, one uses the constant depth value (Z coordinate) in the HSP LSI and the other uses the specific Z Sectioning Buffer which is externally required.

5.7.1 DEPTH SECTIONING with INTERNAL SECTIONING REGISTER

In this mode, the depth value is constant and is stored in the HSP chip. The control is simple because no external sectioning memory is required.

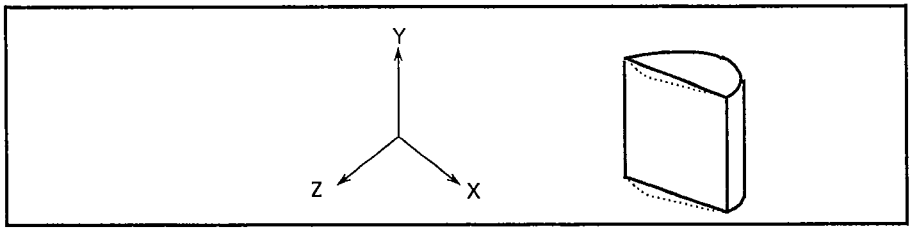


FIG.5.7.1

5.7.2 DEPTH SECTIONING with EXTERNAL SECTIONING MEMORY

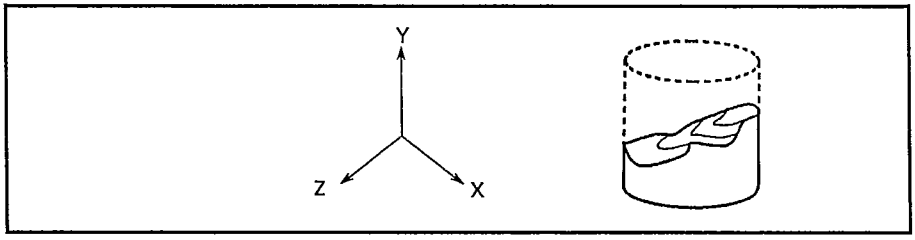


FIG.5.7.2

The Z Sectioning Buffer mode enables the flexible sectioning surface. The Z sectioning information is read with Z information to the HSP, through the same Z Input pins of the HSP LSI, each serially in time-sharing mode from the Z Sectioning VRAM and from the Z VRAM.

Note) We are developing this function now. Accordingly, our recommendation is not using of it.

5.8 TRANSPARENCY PATTERN

When several objects are displayed in overlapping mode, the transparency pattern approach is effective for the scene creation.

The HSP LSI includes 4 by 4, 2-D transparency pattern inside the chip. The FBM write control is done on the transparency pattern bit basis. The pattern bit "1" enables the corresponding pixel drawing, on the other hand the pattern bit "0" inhibits it from drawing.

This transparency pattern option is available for the 1 pixel Memory Access mode shown in 5.14.6.

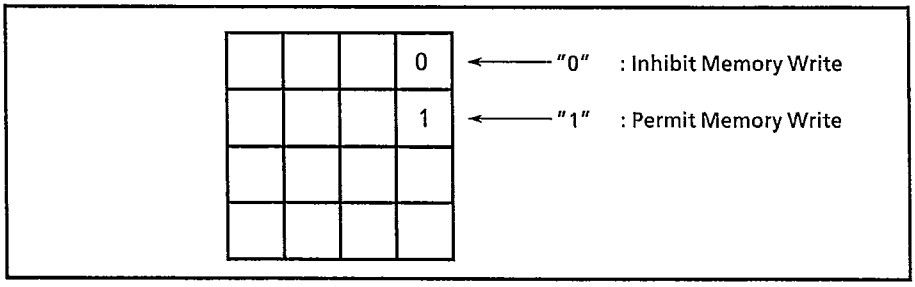


FIG.5.8

5.9 WINDOW

One kind of hardware rectangle window can be used in the HSP. The rectangle area lies in the 8K by 8K, X, Y Coordinate bitmap address space. This area works as a clipping rectangle against which all drawings are clipped, and drawing is updated for the pixels on or within the area.

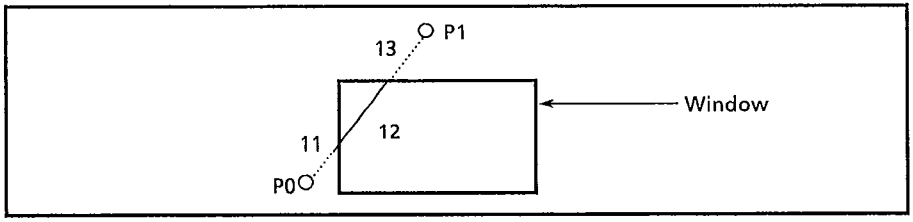


FIG.5.9

5.10 COMPLICATED MEMORY STRUCTURE

The memory structure is complicated.

5.10.1 CONSTANT SHADING

This is a fast flat shading for 3-dimensional objects in solid model graphics, especially effective for fast animation and fast FBM clear operation. Same as Gouraud shading, in advance the host processor such as geometric transformation processor describes the objects by a set of convex planar polygons that approximate the surfaces of the object. As the planar polygons, triangles or trapezoids are assumed for the HSP input.

In this shading, Z (depth) and I (Color Intensity) of each pixel inside one polygon have constant values (i.e. initial values). Hidden-surface removal function is not available in this mode. The FBM access in this shading are assumed to be in horizontal 16 pixels access mode for faster shading. First, the color intensity which is constant inside one polygon, is transferred from the HSP to the FBM and should be memorized externally. First, the HSP send mask information of the horizontal 16 pixels to the FBM through IO (Color Intensity) pins, each time the horizontal pixel numbers might be changed. (For example, for horizontal full 16 pixels - NO MASK pattern and for bit-mapped drawing less than 16 horizontal pixels - PARTIAL MASK pattern) Therefore, the horizontal write control-per-bit circuit (which uses MASK pattern and controls the Write Enable of the FBM), is required.

After each mask information transfer, the color intensity value (I) which is constant inside one polygon, is transferred through the IO pins from the HSP to the FBM. To distinguish the bit-mask pattern from the color intensity on the same IO pins, the M10 pin is used for mode indication. Thus pair informations of mask pattern and color intensity for horizontal 16 pixels unit are used for fast Constant shading.

The peak performance of the constant shading is 96M pixels/sec. As this shading mode enables display clear in 10 msec range, it is effective for the FBM clear.

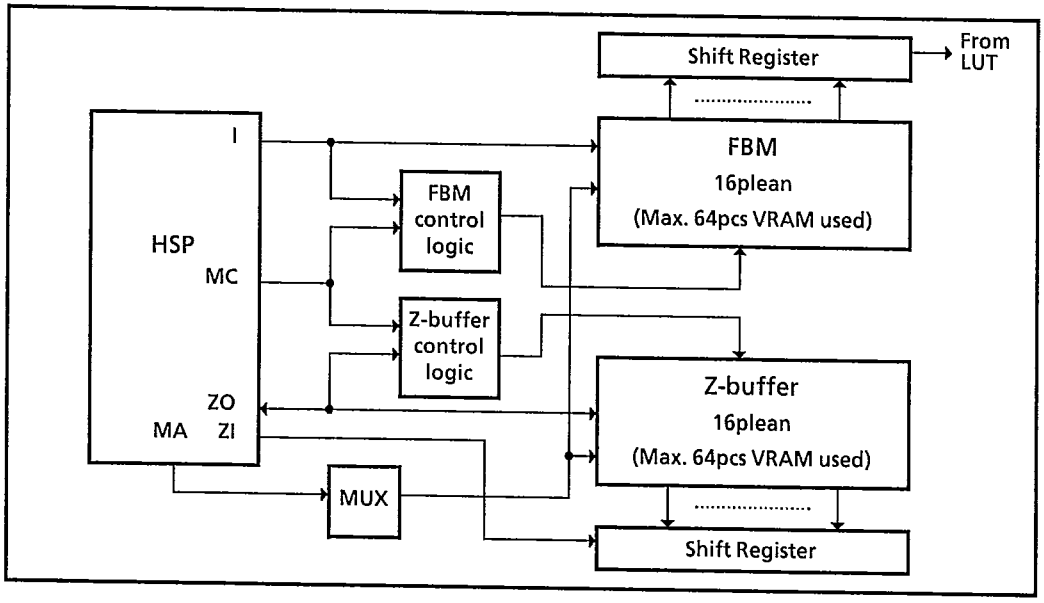


FIG. 5.10.1

5.10.2 LINE DRAWING (MODE2 – LINE PATTERN GENERATION MODE)

This is a fast line drawing function combined with the cache register inside the HSP. 1 or 0 pattern data inside the line pattern register are used to draw the line in opaque or transparent mode, and are stored in the cache register. When the cache register is filled up by these data, the register content is transferred to the FBM.

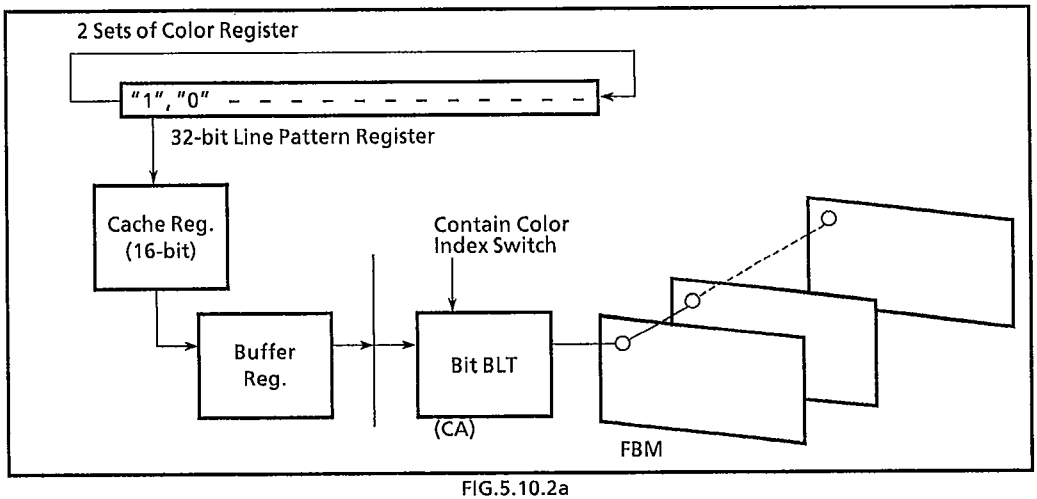


FIG.5.10.2a

There are 2 kinds of cache register. One is a 4 by 4, 16-bit cache register. And the other is horizontal 16 by 1, 16-bit register. These are selectable according to the system configuration. In 4 by 4 configuration, the FBM access logic circuit is necessary externally.

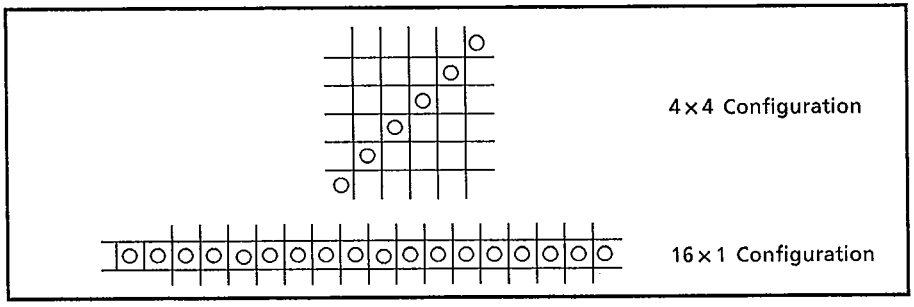


FIG. 5.10.2b

In the cache mode, for generating color index from the Line pattern register content, external transforming circuit is required. To support the opaque or transparent mode, the VRAM function is effectively utilized in the HSP. The bit-mask pattern is generated in the HSP for bit-write-control of 4 by 4 or 16 by 1 cache registers, and the combination of that pattern and the cache register content enables opaque or transparent line generation.

Note) We are developing this function now. Accordingly, our recommendation is not using of it.

5.10.3 IMAGE DATA OUTPUT TRANSFER (HORIZONTAL 16 PIXELS MODE)

The HSP includes the SHIFT and the MARGE circuit to make the bit-boundary transformation possible.

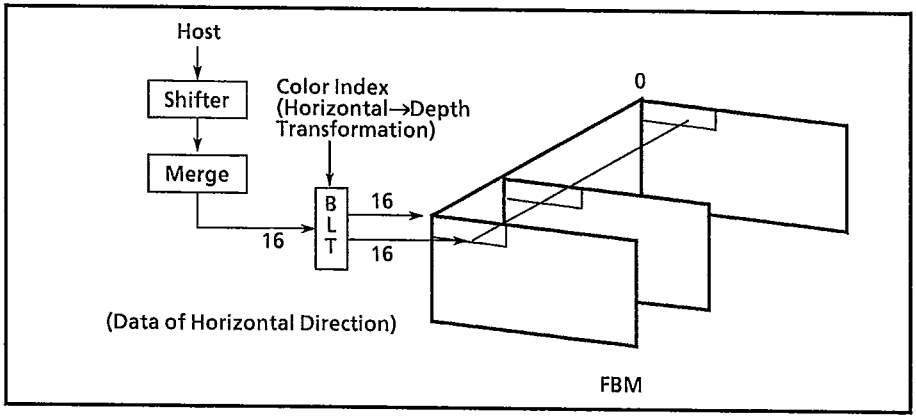


FIG. 5.10.3a

The opaque or the transparent selection is possible.

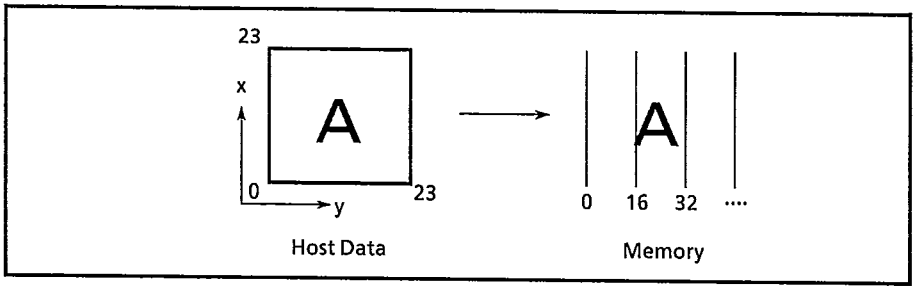


FIG.5.10.3b

5.10.4 ADDRESS GENERATOR

High speed address generation of a rectangler block of pixels is available by 2 HSP LSI chips. This operation is used for the rectangular block copy from the source area to the destination area. One HSP chip is used as the Source Address Generator (ADGS) and the other HSP is used as the Destination Address Generator (ADGD). The HSPs generate address of 16-bit width data each time. The ADGS chip generates the 16-bit horizontal mask pattern for the bit boundary block transfer. The ADGS and ADGD chips support the memory data transfer timing for the identical memory module. If the memory data transfer between the separated memory modules are required, the synchronization control of the ADGS and ADGD chips must be supported by external circuits.

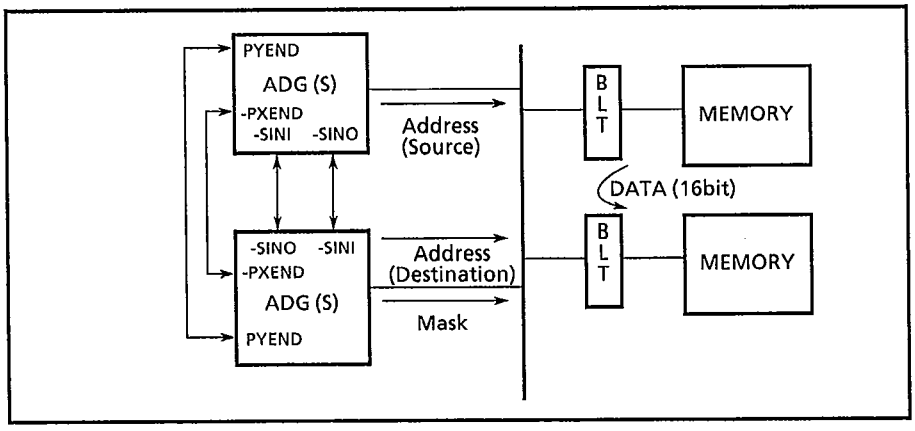


FIG.5.10.4

5.10.5 MAGNIFICATION/REDUCTION

The basic operation is same as the above-mentioned address generator operation. The bitmap data in the source rectangle are magnified or reduced according to the designated parameters, and are coped to the destination area. The HSP generates address of 1 bit width data each time. Magnification range is from 1 to 64, and reduction range is from 1 to 1/64.

5.11 MEMORY OPERATION

5.11.1 MEMORY OPERATION MODE vs. GRAPHICS FUNCTIONS

The HSP VLSI chip extensively controls the several function of dual-port VRAM to obtain the powerful Graphics system performance in low cost. The memory system configuration is one of the key issue for higher performance.

Basically, serial-port access of VRAM is assumed and fully supported by the HSP to realize the Hidden Surface Removal by Z Buffer Algorithm. VRAM control signals such as RAS, CAS etc. are generated by the HSP. Write-per-Bit function of VRAM for color plane selection in several functions (Gouraud shading, Depth Cuing, Line drawing and Image Data transfer etc.), for bit write control in Constant shading and Cache mode Line drawing, is fully supported. Following table summarizes several memory operation mode versus the HSP graphics functions.

TABLE 5.11.1 MEMORY OPERATION MODE vs. GRAPHICS FUNCTIONS

HSP FUNCTIONS	MEMORY OPERATION MODE					
	Page	Write	R/w	Read	Serial in	
Gouraud shading w/ Z check w/o Z check	○ ○	○ ○			○	Fast page Write Access
Const. shading	○	○				
Depth Cuing w/ Z check w/o Z check		○ ○			○	
Line Drawing		○	○			Write or Read Modify Write Select Possible
Address Gen.		○	○			
Scaling Mag./Reduc.		○	○			
Image Data Out		○	○			
Image Data In				○		

5.11.2 MEMORY ACCESS MODE

The HSP VLSI has two kinds of Memory Read/Write Access mode. The first mode allows 1 pixel (16-bit) handling at one memory access, and the other mode allows 16pixels handling.

TABLE 5.11.2 MEMORY ACCESS MODE vs. GRAPHICS FUNCTIONS

HSP FUNCTIONS	MEMORY ACCESS MODE	
	1 pixel (16-bit)	16 pixels
Gouraud up shading	○	
Const. shading		○
Depth Cuing	○	
Line Drawing color pixel pattern	○	○
Address Gen.		○
Scaling Mag./Reduc.	○	
Image Data Out color pixel pattern	○	○
Image Data In pixel horizontal	○	○

5.11.3 MEMORY WRITE CONTROL

The memory write control has several control mode when data overflow from the square window or when data are in the transparent mode operation.

a) 1pixel mode
The memory write logic controls the WE (write enable) signal to the FBM.

b) 16 pixels (for 1 plane) mode
The HSP generates 16-bit mask pattern data for pixel write control at the trailing edge of RAS control signal of the VRAM.

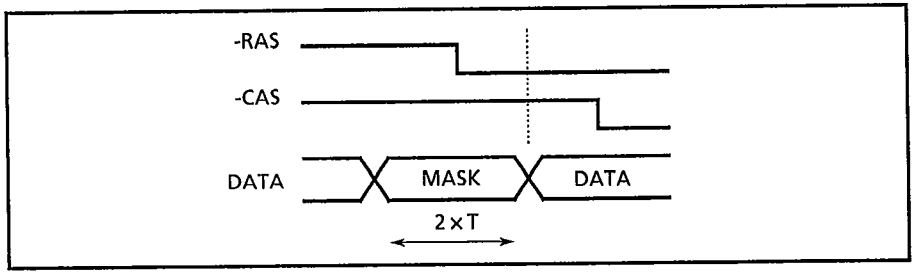


FIG.5.11.3

In this mode, the external control circuit is required to latch the above-mentioned 16-bit mask pattern, and to write-control the enable bit by using it.

In the two modes, there are several ways to write-control each enable bit :

(i) Use the Write Mask Operation of the VRAM as the FBM.
The HSP LSI can control the bit mask pattern generation timing.

(ii) Use the Read-Modify-Write operation of the FBM.

(iii) External circuit controls the WE (write enable) signal.

5.11.4 LINEAR ADDRESS GENERATION MODE

The (X, Y) coordinates of the screen are transferred to the linear address of the FBM inside the HSP LSI.

The flexible size of screen resolution is supported by the HSP LSI. The available screen width are as follows.

Available screen widths :

256, 320,384, 448, 512, 576, 640, 704, 768, 832, 1024, 1088, 1152, 1216, 1280, 1344, 1536, 1600, 2048, 2112, 2176, 2240, 2304, 2368, 2560, 2624, 4096, 4160, 4352, 4416, 4672, 8192, 8256, 8704, 8768

5.12 COMMAND DESCRIPTIONS

The 4-bit command input through ADRS (Address) pins together with 16-bit Graphic Parameter input through D (Data) pins, if necessary, both from Host System enable high level operation in the HSP. The following table summarizes the functional description of each Command and Parameter.

COMMAND (4-bit)	DATA (16-bit)

5.12.1 GENERAL COMMAND DESCRIPTION

TABLE 5.12.1 COMMAND DESCRIPTION

COMMAND (4-Bit)	CODE (Hex)	DATA (16-Bit)	DESCRIPTION
INT	F	System Configuration Information	LSI initialization and Default mode setting for the system configuration
AUX	E	Auxiliary or Sub Command	Several mode setting and other Sub Command are defined in Data part
I	1	Color Index (I) of current Point	I Value (16-bit) Definition of current Point
Z	2	Depth value (Z) of current Point	Z value (16-bit) Definition of current Point
Y	3	Y coordinate value (Y, 13-bit) of current Point	Y Address value (13-bit) Definition of current Point
X	4	X coordinate value (X,13-bit) of current Point	X Address value (13-bit) Definition of current Point definition.
T1X	5	X coordinate value (X, 13-bit) of the first Vertex of a Triangle	In mode 1, used at the end of first Vertex definition of a Triangle
T2X	6	X coordinate value (X,13-bit) of the first Vertex of a Triangle	In mode 2, used at the end of first Vertex definition of a Triangle
LX	8	X coordinate value (X, 13-bit) of the first Point of a Line	Used at the end of first Point definition of a Line
IMG	9	Image data Input (= 1)/ Output (= 0) to/from Host System	Image data (I or O) start
PTRN	0	Image output data from Host System or Image input data from FBM	Image pattern data (16-bit)
ADDR	A	Source (= 1)/Destination (= 0)	Source or Destination Address Generation
PX	B	X coordinate values (X,13-bit) from the second point to the final point of Polyline	Used for point definitions in Line drawing
PARM	D	Graphic Parameter	Parameter setting followed by AUX command with sub-command definition at Data part

5.12.2 AUXILIARY COMMAND LIST

The Auxiliary command (AUX) requires sub-command in the Data part. It is accompanied with the Parameter command (PARM), as the next command, together with the Parameter in the Data part.

TABLE : AUXILIARY COMMAND LIST

Command (4-bit)	Data/Sub-command (Description)
AUX	PMOD (= 0)
PARM	Shading mode (Gouraud/Constant)

AUX	LMOD (= 1)
PARM	Line Drawing mode (Depth Cuing / Opaque /Transparent)

AUX	IMOD (= 2)
PARM	Image (16bit-1pixel/16pixel of 1 plane)

AUX	ZCNT (= 3)
PARM	Z Buffer (Y/N) X Section (Y/N)

AUX	HCNT (= 4)
PARM	Hardware control mode *External Z sectioning *Bit mask enable control *RW or RMW select *Z pins data select (Z in & I out/I in & Z out)

AUX	HCNT (= 5)
PARM	Transparency Pattern (4 × 4 pixels)

AUX	WNDW (= 6)
PARM	Square Window Boundary set

AUX	SEC (= 7)
PARM	Z Sectioning value

AUX	COLR (= 8)
PARM	Color Pattern for Line Drawing or Image data transfer

AUX	MSK (= 9)
PARM	32-bit Line pattern used cyclically for line drawing, not used for Depth Cuing

AUX	SCL (= 11)
PARM	In Address Generation operation, Scaling of X, Y direction

AUX	LSTA (= 12)
PARM	Line status definition (Continuous Poly Line/Separate Line)

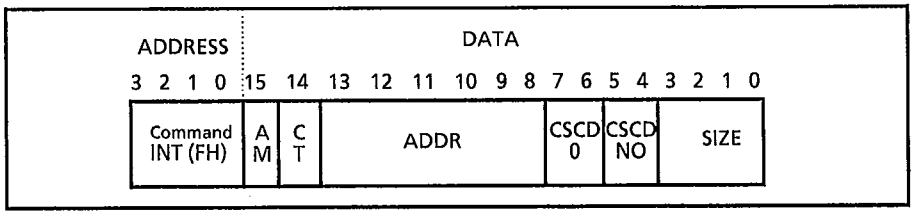
5.13 COMMAND DETAILS

The following subsections describe the HSP commands in detail. The topics related to each command are also described in each subsection. The commands are organized in the order of the commands list in section 5.12.1.

5.13.1 INIT – LSI INITIALIZATION and DEFAULT MODE SETTING

Command code (Hex) # F

Format



Description :

AM (bit 15)

Cache Mode selection :

0-16 by 1 cache size (Horizontal cache)

1-4 by 4 cache size (Square cache)

CT (bit 14)

Cache support selection :

0- No cache support

1- Cache support

ADDR (bit 13-8)

X, Y to Linear Address Conversion Mode :

From 256, through 1152, up to 8768 pixel size screen horizontal resolution is supported by automatic X, Y address to linear address conversion. 6-bit of ADDR field vs. horizontal resolution is summarized in the following table.

TABLE 5.13.1 ADDR field vs. SCREEN HORIZONTAL RESOLUTION

ADDR						HORIZON. RESOLU.	ADDR						HORIZON. RESOLU.
13	12	11	10	9	8		13	12	11	10	9	8	
0	0	0	0	0	0	256	0	1	1	0	0	0	2048
0	0	0	0	0	1	320	0	1	1	0	0	1	2112
0	0	0	0	1	0	384	0	1	1	0	1	0	2304
0	0	0	0	1	1	448	0	1	1	0	1	1	2368
0	0	0	1	0	0	512	0	1	1	1	0	0	4096
0	0	0	1	0	1	576	0	1	1	1	0	1	4160
0	0	0	1	1	0	640	0	1	1	1	1	0	4352
0	0	0	1	1	1	704	0	1	1	1	1	1	4416
0	0	1	0	0	0	1024	1	0	0	0	0	0	1024
0	0	1	0	0	1	1088	1	0	0	0	0	1	1088
0	0	1	0	1	0	1152	1	0	0	0	1	0	1536
0	0	1	0	1	1	1216	1	0	0	0	1	1	1600
0	0	1	1	0	0	2048	1	0	0	1	0	0	2048
0	0	1	1	0	1	2112	1	0	0	1	0	1	2112
0	0	1	1	1	0	2176	1	0	0	1	1	0	2560
0	0	1	1	1	1	2240	1	0	0	1	1	1	2624
0	1	0	0	0	0	512	1	0	1	0	0	0	4096
0	1	0	0	0	1	576	1	0	1	0	0	1	4160
0	1	0	0	1	0	768	1	0	1	0	1	0	4608
0	1	0	0	1	1	832	1	0	1	0	1	1	4672
0	1	0	1	0	0	1025	1	0	1	1	0	0	8192
0	1	0	1	0	1	1088	1	0	1	1	0	1	8256
0	1	0	1	1	0	1280	1	0	1	1	1	0	8704
0	1	0	1	1	1	1344	1	0	1	1	1	1	8768

ADDR						HORIZON. RESOLU.
13	12	11	10	9	8	
1	1	-	-	-	-	Not Available

CSCD0 (bit 7, 6)

Parallel chip (cascaded) configuration selection :

0- No cascaded configuration

1- Cascaded configuration of 2 chips

2- Cascaded configuration of 4 chips

CSCDNO (bit 5, 4)
Chip ID Number in cascaded configuration

0- Chip #0
1- Chip #1
2- Chip #2
3- Chip #3

SIZE (bit 3-0)
Memory Page Size (information for DRAM refresh)

SIZE (3-0)	PAGE SIZE
X000	256
X001	512
X010	1K
X011	2K
X100	4K
X101	8K
X110	16K
X111	32K

When the memory access occurs over this page size, the HSP can automatically detect the page fault and control the memory control signals (RAS, CAS, and so on) to meet the VRAM-control requirement.

Default Parameter Sets

When the HSP LSI receives the INIT Command, several parameters at the initial stage are defined as follow :

Polygon drawing mode	–	Gouraud shading	(=0)
Line drawing mode	–	Transparent line	(=1)
Image data input/output	–	1 pixel in 16-bit	(=0)
Z Control mode	–	No Z Buffer, No Z Section	(=0)
Transparency pattern	–	No Mask	(=FFFF(Hex))
Window boundary	–	Max range	((0, 8191) - (8191, 0)
Depth sectioning Z value	–	Be able to show objects in transparent mode	(=FFFF(Hex))
Color index value	–	1 for bit '1', 0 for bit '0'	
Line pattern	–	Solid line	(=FFFF(Hex))
Hardware control mode	–	All 0	(=0000(Hex))
Plane mask value	–	Write enable to all planes	(=FFFF(Hex))
Zoom scale at Address Generator	–	1 to 1	(=0000(Hex))
Line status	–	First point for Polyline/Separate line	(=0000(Hex))

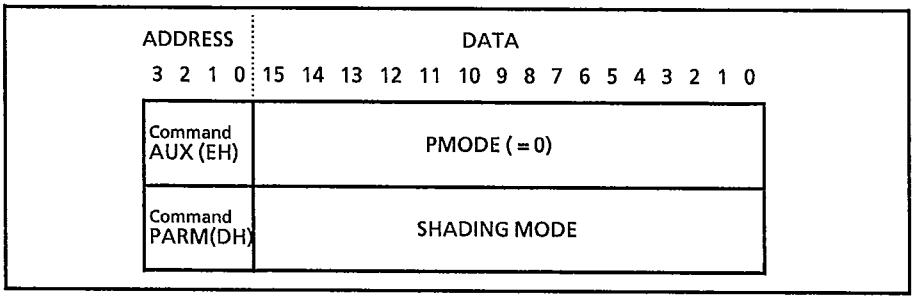
5.14 AUX - AUXILIARY COMMAND

A variety of sub-commands are available in this command Format : The 16-bit Data part of the AUX command determines the sub-command. Executing a set of AUX command and accompanying PARM command causes following described operations. The number of accompanying PARM commands depends on each AUX sub-command.

5.14.1 PMODE - POLYGON DRAWING MODE DEFINITION

Data code (Hex) #0

Format



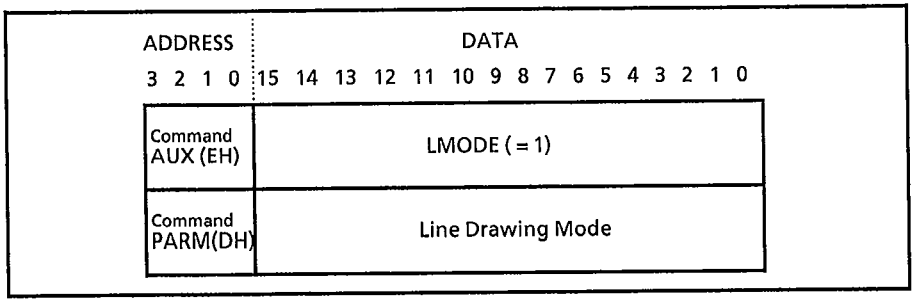
Description :

- Define the polygon shading mode. After this sub-command setting, polygons are shaded in Gouraud shading mode or constant shading mode.
- If Shading Mode = 0, Gouraud shading is selected, and if Shading Mode = 1, constant shading is selected for polygon shading.
- This polygon shading mode remains the same until changed by new INIT command, or by another PMODE sub-command.
- Initial value of Shading Mode is 0 (Gouraud shading).
- For Gouraud shading (Shading Mode = 0), coordinates X, Y and color intensity I of each vertex of the polygon should be defined. When Z Buffer algorithm or Z Sectioning is applied, coordinate Z of above vertex should also be defined.
- For Constant shading (Shading Mode = 1), coordinates X, Y of each vertex of the polygon should be defined. The coordinate Z and the color intensity I of the first vertex of the polygon should also be defined. This Z value is used for Z Buffer clear.

5.14.2 LMODE - LINE DRAWING MODE DEFINITION

Data code (Hex) #1

Format :



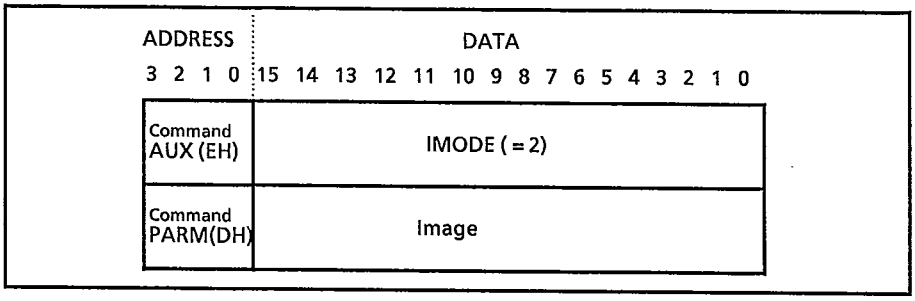
Description :

- ☐ Define the line drawing mode. After this sub-command setting, lines are drawn in Depth Cuing mode or transparent 2-D line drawing mode or opaque 2-D line drawing mode.
- ☐ If Line Drawing Mode = 0, Opaque 2-D line drawing is selected.
  If Line Drawing Mode = 1, Transparent 2-D line drawing selected.
  If Line Drawing Mode = 2, Depth Cuing is selected.
- ☐ This line drawing mode remains the same until changed by new INIT command, or by another LMODE sub-command.
- ☐ Initial value of Line Drawing Mode is 1 (Transparent 2-D line drawing).
- ☐ In Opaque line drawing (Line Drawing Mode = 0), the line pixel of the foreground color is drawn and the pixels between the line dots are filled in the background color. The color of each pixel is selected from 2 kinds of colors defined by COLOR sub-command, and is dependent on the 1 or 0 value of corresponding Line Pattern register bit which is defined in the sub-command LPATTERN.
- ☐ In Transparent line drawing (Line Drawing Mode = 1), only the line pixel of the foreground color is drawn and the pixels between the line dots are not overwritten. Only when the corresponding line pattern bit is 1, the pixel is drawn in foreground color.
- ☐ In Depth Cuing (Line Drawing Mode = 2), the content of the Line Pattern register is ignored. Also the each pixel color is interpolated from the color intensities at two pixels of the line edge. The hidden-surface removal (Z Buffer) option is available in this mode.

5.14.3 IMODE - DATA TRANSFER MODE DEFINITION of IMAGE DATA I/O

Data code (Hex) #2

Format:



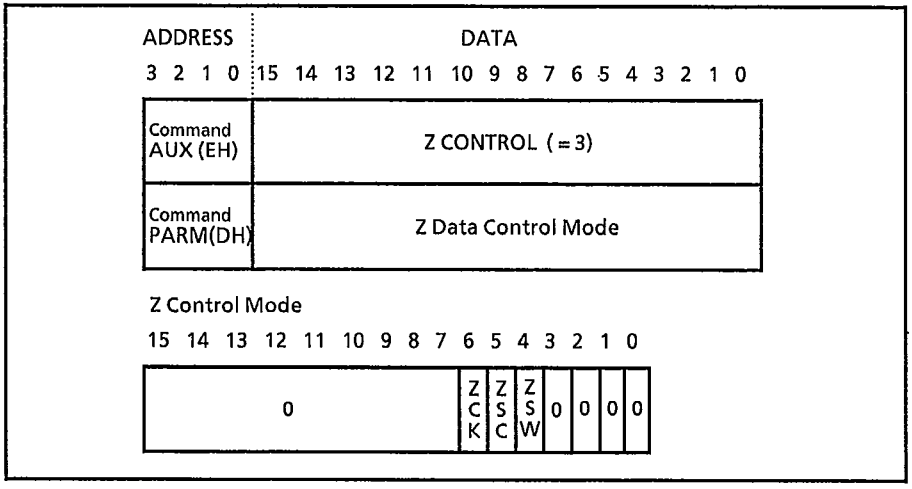
Description:

- Define the image data transfer mode. When the image input or output data are transferred, data are defined as 16 horizontal pixel of 1 plane, or as 16-bit (16 plane) one pixel. After this sub-command setting, transferred data mode of image data is fixed.
- If Image =0, image data are defined as 16-bit (16 plane) one pixel, and if Image =1, image data are defined as 16 horizontal pixels of 1 plane.
- This image data transfer mode is fixed until new INIT command is executed, or next IMODE sub-command is executed.
- Initial value of Image is 0 (16-bit one pixel).
- This data transfer mode is also used for Address Generation operation. In order to perform the scaling operation in the address generation, 16-bit one pixel mode (Image=0) setting is required.

5.14.4 ZCONTROL - Z Buffer USAGE SELECTION, Z SECTIONING MODE SELECTION

Data code (Hex) #3

Format :



Description :

☐ Define the Z value (depth value) mode. After this sub-command setting, hidden-surface removal (by Z-Buffer) mode, depth sectioning mode are selected in Gouraud shading operation of triangles or trapezoids and in Depth Cuing operation.

ZSW (bit 4)

When ZSC = 1, Depth value data selection :

0- Constant depth value defined by SECTION sub-command

1- Flexible depth value from external Z Sectioning VRAM

ZSC (bit 5)

Depth sectioning enable/disable selection :

0- Disable depth sectioning

1- Enable depth sectioning

ZCK (bit 6)

Hidden-surface removal mode selection :

0- Disable hidden-surface removal

1- Enable hidden-surface removal

☐ This Z value mode selection is fixed until new INIT command is executed, or next ZCONTROL sub-command is executed.

☐ Initial values of Z Data Control Mode (ZCK, ZSC, ZSW) are all 0. That is, disable hidden-surface removal, disable depth sectioning.

5.14.5 HCONTROL - HARDWARE CONTROL MODE DEFINITION

Data code (Hex) #4

Format :

ADDRESS 3 2 1 0	DATA 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Command AUX (EH)	H CONTROL (= 4)
Command PARM(DH)	H W Control Mode

HARDWARE CONTROL MODE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		CORR	0	EXSYN	RMW	0	FS	BMSK	0			ZI	IE	ZE	ZSCE

Description :

☐ Define the usage of several LSI pins.

CORR (bit 13)

Sub-pixel correction for Color intensity and Z values :

0- No correction. I and Z values at rounded X coordinate are rounded.

1- Sub-pixel correction. I and Z values are corrected by sub-pixel X coordinate.

EXSYN (bit 11)

Synchronization selection : Synchro. at Image data input. And multi-chip synchoro. in RGB system or in parallel Gouraud-shading system.

0- Operation by internal timing

1- Externally synchronized operation. In RGB system or parallel Gouraud shading system this bit must be 1 to enable externally synchronized operation of multi-chips.

RMW (bit 10)

Select the Read-Modify-Write mode or Read-Write mode in FBM operation.

0- Read-Write operation

1- Read-Modify-Write operation

FS (bit 8)

Select the CAS operation cycle timing in FBM operation. This selection bit is effective only for Constant shading of page mode memory operation.

0- CAS cycle is 333ns (@ 12MHz)

1- CAS cycle is 167ns (@ 12MHz)

BMSK (bit 7)

Control the Write pulse of Bit Mask data.

0- No write pulse control

1- Write pulse control

ZI (bit 3)

Define the output data to the ZO pins in output mode and select the input data to the host in Image data input command.

0- In output mode, Z data are output from ZO pins. In Image data input command, data through IO pins are transferred to the host.

1- In output mode, I data are output from ZO pins. In Image data input command, data through ZO pins are transferred to the host.

IE (bit 2)

Control the Write pulse of data of IO pins

0- Write pulse of data of IO pins inhibited.

1-Write pulse of data of IO pins permitted

ZE (bit 1)

Control the Write pulse of data of ZO pins

0- Write pulse of data of ZO pins inhibited.

1- Write pulse of data of ZO pins permitted.

ZSCE (bit 0)

Control Read or Write to external Depth Sectioning Buffer

0- Read or Write to external Depth Sectioning Buffer inhibited.

1- Read or Write to external Depth Sectioning Buffer permitted.

5.14.6 TPATTERN - 4 by 4 TRANSPARENCY PATTERN DEFINITION

Data code (Hex) #5

Format :

ADDRESS	DATA
3 2 1 0	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Command AUX (EH)	TPATTERN (= 5)
Command PARM(DH)	Transparency Pattern

LSB 2-bit of X / LSB 2-bit of Y	00	01	10	11
00	0	1	2	3
01	4	5	6	7
10	8	9	10	11
11	12	13	14	15

Description :

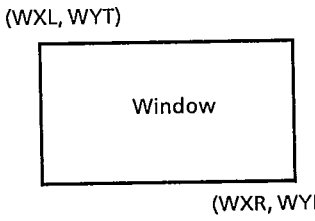
- ☐ Define the transparency pattern mode. After this sub-command setting, all objects are generated in masked transparency pattern according to this transparency pattern mode.
- ☐ However, for triangles or trapezoids of Gouraud shading (PMODE sub-command and 0 of the Shading Mode are selected), or Depth Cuing line (LMODE sub-command and 2 of the Line Drawing Mode are selected), the transparency mask pattern is ignored when these objects or their portions exist beyond the Depth Sectioning area (the area with lager depth value than that at the Depth Sectioning area).
- ☐ This transparency pattern mode is fixed until new INIT command is executed, or next TPATTERN sub-command is executed.
- ☐ The initial value of the transparency pattern mode is 0xFFFF, which is equivalent to non-masking.
- ☐ The transparency pattern is defined by the 16-bit mask data, as shown in the above table.
- ☐ The pixel at location (X, Y) of the display is determined to be written or not by transparency mask pattern. The LSB 2 bits of each X and Y select the transparency pattern bit 1 (write) or 0 (mask) depending on the content of the above table.
- ☐ The 0 to 15 figures in the transparency pattern table correspond to the bit location of the Transparency Pattern defined in PARM data field.

5.14.7 WINDOW - a CLIPPING RECTANGLE AREA DEFINITION

Data code (Hex) #6

Format :

ADDRESS 3 2 1 0	DATA 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Command AUX (EH)	WINDOW (= 6)
Command PARM(DH)	WXL (Upper Left X)
Command PARM(DH)	WYT (Upper Left Y)
Command PARM(DH)	WXR (Lower Right X)
Command PARM(DH)	WYB (Lower Right Y)
Command PARM(DH)	0



Description :

- ☐ Define the rectangle window size and the location,. After this sub-command setting, all portions of objects can be drawn when they exist inside the defined clipping rectangle window boundaries.
- ☐ The output region is defined by (x, y) where WXL≦x≦WXR and WYB≦y≦WYT. The pixel on the boundary is not clipped.
- ☐ This window boundary values are fixed until new INIT command is executed, or next WINDOW sub-command is executed.

☐ The initial value of the window boundaries are as follows.

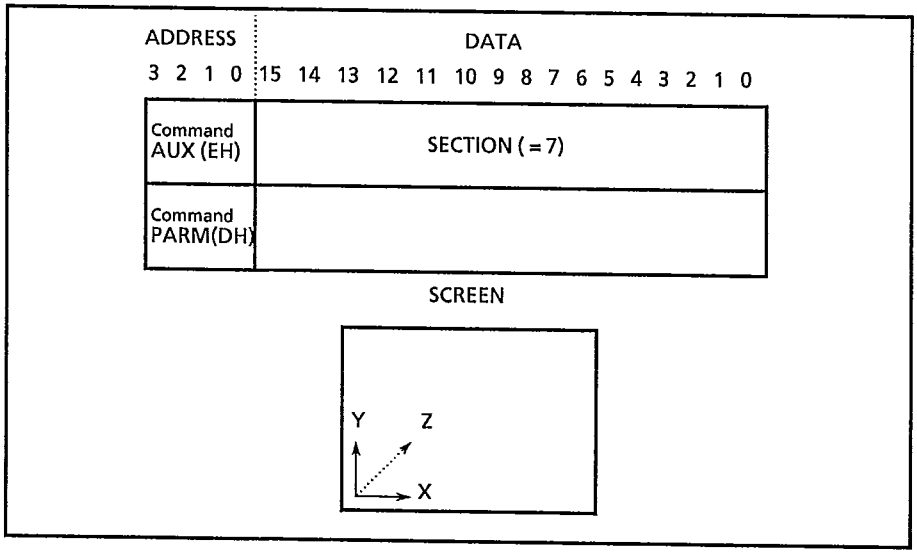
WXL=0
WYT=0
WXR=8191 (=1FFF (Hex))
WYB=8191 (=1FFF (Hex))

☐ This rectangular clipping is effective for all pixel drawing operation of the HSP.

5.14.8 SECTION - Z SECTIONING VALUE DEFINITION

Data code (Hex) #7

Format :



Description :

☐ Define the depth value (Z value) of the depth sectioning. After this sub-command setting, this Z value is used as the boundary value of transparency pattern region.

Condition :

In ZCONTROL sub-command setting, ZSC=1 and ZSW=0 conditions should be selected to enable the depth sectioning and the constant depth value usage.

In PMODE sub-command setting, Gouraud shading mode (=0) should be selected for triangle or trapezoid drawing to make the depth value useful.

In LMODE sub-command setting, Depth Cuing mode (=2) should be selected for line drawing to make the depth value useful.

☐ The depth sectioning value is effective until new INIT command is executed, or next SECTION sub-command is executed.

☐ The screen coordinates are defined as shown in the following figure.
Objects with larger Z value (i.e. depth value) are located farther in depth from the view point.
As above-mentioned, the initial depth sectioning value is the maximum Z value. The transparency masking are executed to the objects which are in front of the depth sectioning region. Therefore, in the initial state, all objects composed of triangles or trapezoids can be generated as the transparency masked pattern. However, since the initial transparency pattern is 0xFFFF, no transparency mask affects objects in the initial state.

5.14.9 COLOR - COLOR INDEX PATTERN DEFINITION for LINE DRAWING or IMAGE DATA

Data code (Hex) #8
Format:

ADDRESS 3 2 1 0	DATA 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Command AUX (EH)	COLOR (= 8)
Command PARM(DH)	Color Index for "1" pixel
Command PARM(DH)	Color Index for "0" pixel

Description:

☐ Define the active foreground and background colors of line for LMODE sub-command setting (Line Drawing Mode=0 or 1 for 2-D line), or define the image pattern data for IMODE sub-command setting (Image=1, which indicates that image data are defined as 16 horizontal pixels of 1 plane). After this sub-command setting, line colors or image patterns are fixed according to this color index pattern.

☐ These Color Index patterns remain the same until changed by new INIT command or by another COLOR sub-command.

☐ The first Color Index value defines the active foregournd color of the pixel the corresponding Line Pattern bit of which is a 1. The second Color Index value defines the background color of the pixel the corresponding Line Pattern bit of which is a 0.

☐ The initial value of the first color index is 0001 (Hex) and that of the second index is 0000 (Hex).

5.4.10 LPATTERN - CYCLICALLY USED LINE PATTERN DEFINITION (32-BIT)

Data code (Hex) #9

Format :

ADDRESS 3 2 1 0	DATA 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Command AUX (EH)	LPATTERN (= 9)
Command PARM(DH)	Line Pattern (Upper 16-bit)
Command PARM(DH)	Line Pattern (Lower 16-bit)

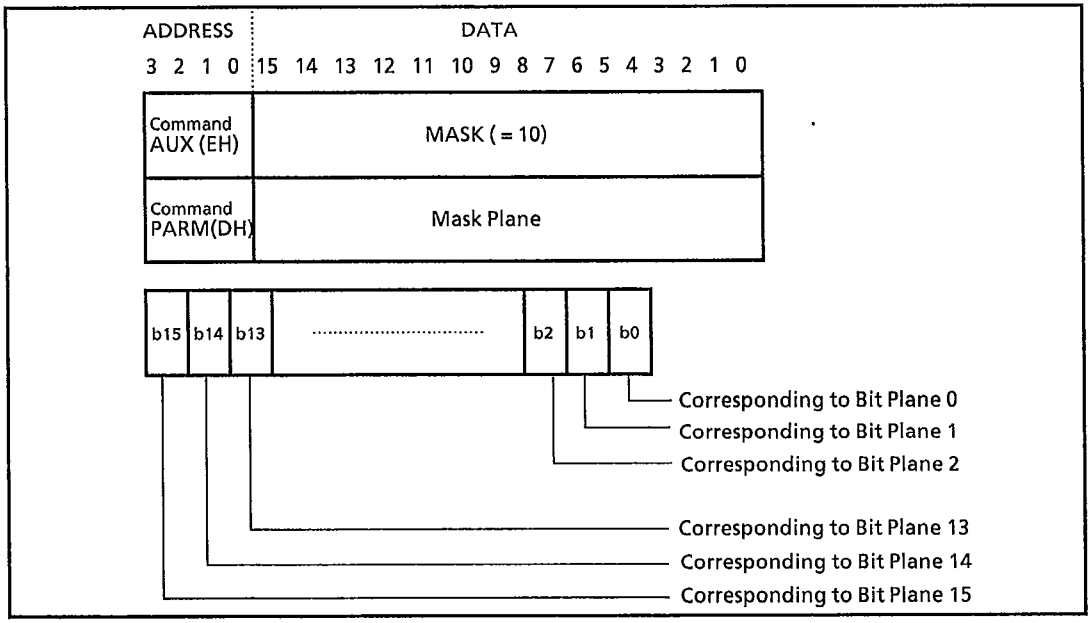
Description :

- Define the texture of line. After this sub-command setting, this 32-bit Line Pattern specifies the texture for the subsequent line drawing except depth cuing.
- The Line Pattern value remains the same until changed by new INIT command or by another LPATTERN sub-command.
- The initial value of the Line Pattern is FFFFFFFF (Hex), which indicates solid line.
- The 32-bit Line Pattern is defined as either Opaque or Transparent depending on the LMODE sub-command. In Opaque line mode, a value of 1 in the Line Pattern signifies that the corresponding pixel is to be drawn in the foreground color (the first Color Index) and a 0 signifies that the corresponding pixel is to be drawn in the background color (the second Color Index).
  In Transparent line mode, a value of 1 in the Line Pattern means that the corresponding pixel should be overwritten using foreground color ; a 0 means that corresponding pixel is not overwritten. (Refer to the LMODE sub-command and the COLOR sub-command.)
- The first pixel to be drawn corresponds to the MSB of the Line Pattern, and following pixels are drawn using the Line Pattern cyclically.
- In 2-D polyline drawing, except line drawing in cache mode, the first vertex of the first line segment of the polyline corresponds to the MSB of the Line Pattern and following pixels of the polyline are drawn using the Line Pattern cyclically to the end of the polyline.

5.14.11 MASK - BIT PLANE SELECTION

Data code (Hex) #A

Format :



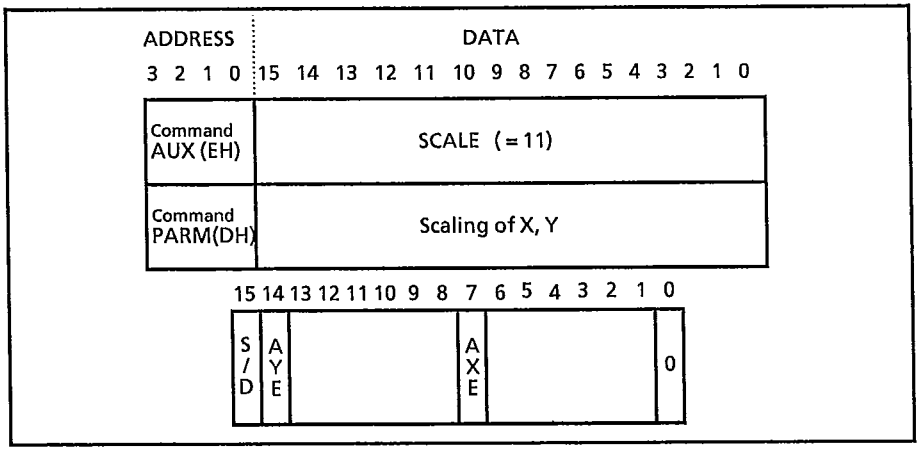
Description

- ☐ Select the bit planes for the drawing. A value of 1 in the Mask Plane indicates that the corresponding bit plane is write-permitted ; a 0 means that the corresponding bit plane is write-inhibited.
- ☐ This Mask Plane selection is destroyed after the data access mode of 16 horizontal pixels of 1 plane are executed.

5.14.12 SCALE - SCALING of X, Y in ADDRESS GENERATION OPERATION

Data code (Hex) #B

Format



Description :

☐ Define the X and Y scaling of the rectangular block for address generator operation. (AX, AY = 0~63)

S/D (bit 5)

Define the data source or destination :

0- Destination

1- Source

AYE (bit 4)

Compare the AY counter value of the source side with that of the destination side and set 1 or 0 to each side depending on the comparison result :

0- If the value is larger

1- If the value is smaller

If each AY value is same, set 0 to the AYE of the source side and set 1 to the other.

AY (bit 13-8)

Magnification or reduction counter value for Y direction :

AXE (bit 7)

Compare the AX counter value of the source side with that of the destination side and set 1 or 0 to each side depending on the comparison result :

0- If the value is larger

1- If the value is smaller

If each AX value is same, set 0 to the AXE of the source side and set 1 to the other.

AX (bit 6-1)

Magnification or reduction counter value for X direction :

☐ The following formula are used to obtain the X or Y scaling value from the AX or AY counter values of the source and the destination side.

$$\frac{\text{source AX value} + 1}{\text{destination AX value} + 1} = \text{Scaling of X}$$

$$\frac{\text{source AY value} + 1}{\text{destination AY value} + 1} = \text{Scaling of Y}$$

☐ The following case shows the parameters for 10 times magnification to X direction and 5 times reduction to Y direction in address generation operation.

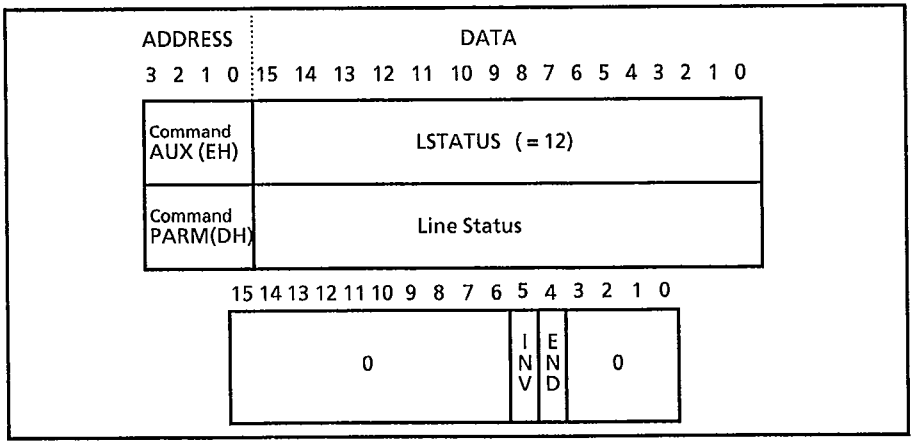
The source side : S/D=1, AYE=1, AY=0, AXE=0, AX=9

The destination side : S/D=0, AYE=0, AY=4, AXE=1, AX=0

5.14.13 LSTATUS - LINE STATUS DEFINITION

Data code (Hex) #C

Format :



Description :

☐ Set the line status. The Line Status contains 2 bits for the imaginary border line and the end line setting.

INV (bit 5)

Define the border line :

0- Real border line

1- Imaginary border line

END (bit 4)
1- End line of the border lines

☐ In the polyline drawing, this sub-command is set to change the status of a line if required when drawing it to the next vertex. Just before the coordinate setting of the next vertex, this sub-command must be used if necessary.

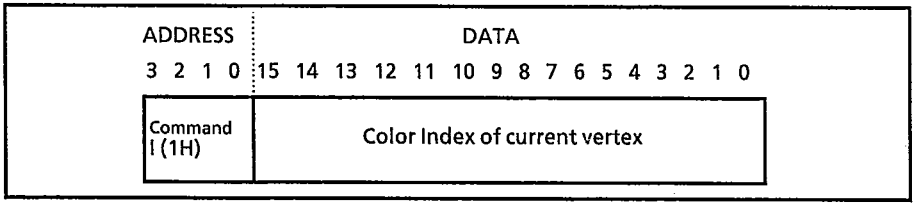
☐ This line status remains the same until changed by another LSTATUS sub-command.

The general rule for the line status setting along the shown example is as follows :

- After the first vertex setting, set both INV and END as 0.
- During the line drawing to the second vertex, the line status remains same and the LSTATUS sub-command is not required.
- To draw the line from the second vertex to the third, this LSTATUS sub-command must be set just before the line drawing command to make INV as 1.
- During the line drawing to the fourth vertex, the line status remains same and the LSTATUS sub-command is not required.
- To draw the line from the fourth vertex to the fifth, this LSTATUS sub-command must be set just before the line drawing command to make INV as 0 and END as 1.

5.15.1 I - COLOR INTENSITY or INDEX VALUE of the CURRENT VERTEX

Command code (Hex) #1
Format :



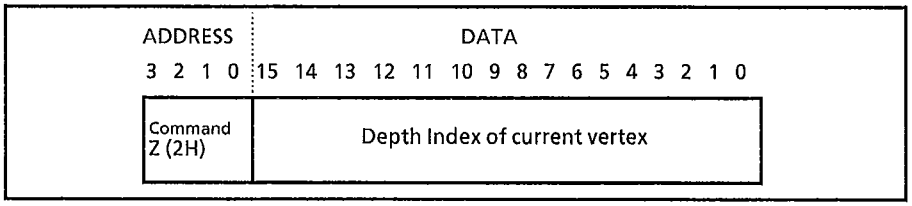
Description :

☐ Define a color intensity or a color index value of the current vertex in 16-bit unsigned integer.

5.15.2 Z - DEPTH VALUE (Z COORDINATE) of the CURRENT VERTEX

Command code (Hex) #2

Format :



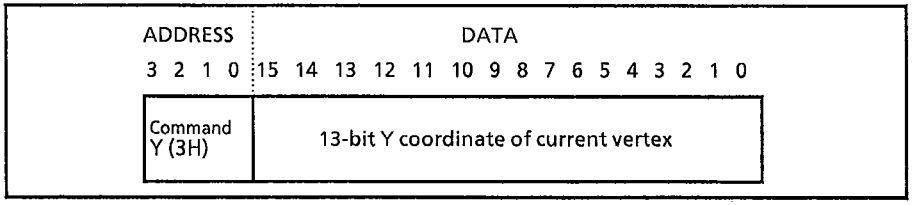
Description :

☐ Define a depth value of the current vertex in 16-bit unsigned integer. The Z axis extends from the viewpoint and increases from front to depth of the screen.

5.15.3 Y - Y COORDINATE of the CURRENT VERTEX

Command code (Hex) #3

Format



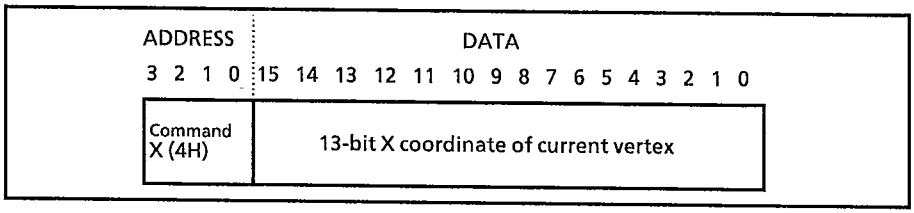
Description :

☐ Define a Y coordinate of the current vertex in 13-bit unsigned integer. Origin Point locates at the bottom left corner of the screen. The Y axis extends up the left side and increases from bottom to top.

5.15.4 X -X COORDINATE of the CURRENT VERTEX

Command code (Hex) #4

Format :



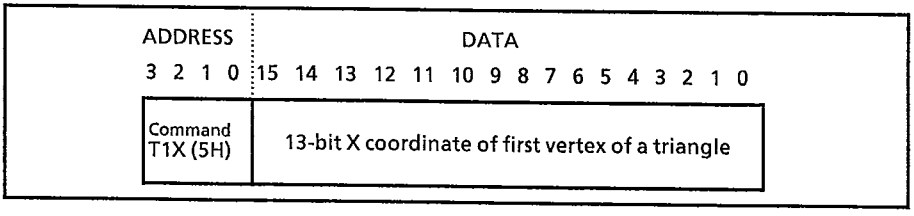
Description :

- Define a X coordinate of the current vertex in 13-bit unsigned integer.
- Origin Point locates at the bottom left corner of the screen. The X axis extends across the bottom and increases from left to right.
- This X command must be used each time in the last for each vertex of a triangle, a trapezoid or a line. The usage orders of the above-mentioned I, Z and Y commands can be arbitrary, however, this X command must be the final command for each vertex.

5.15.5 T1X -X COORDINATE of the FIRST VERTEX of a TRIANGLE (in MODE 1)

Command code (Hex) #5

Format :

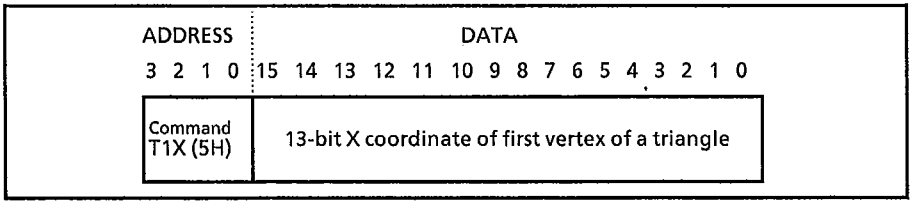


Description :

- Define a X coordinate of the first vertex of a triangle in 13-bit unsigned integer.
- This command must be used in the last for the first vertex definition of a triangle. The usage orders of the above-mentioned I, Z and Y commands can be arbitrary, however, this T1X command must be the final command for the first vertex of a triangle.
- In the sequential triangles input mode, this command is used to define triangles of mode 1. In this mode the last two vertices of a triangle are commonly used again as the first two vertices of the next adjacent triangle, and parameters setting of these two vertices are required only once.

5.15.6 T2X - X COORDINATE of the FIRST VERTEX of a TRIANGLE (in MODE 2)

Command code (Hex) #6
Format:

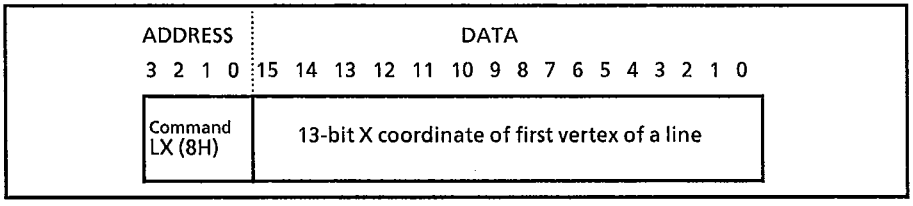


Description:

- ☐ Define a X coordinate of the first vertex of a triangle in 13-bit unsigned integer.
- ☐ This command must be used in the last for the first vertex definition of a triangle. The usage orders of the above-mentioned I, Z and Y commands can be arbitrary, however, this T2X command must be the final command for the first vertex of a triangle.
- ☐ In the sequential triangles input mode, this command is used to define triangles of mode 2. In this mode the first vertex of a triangle and the third vertex are commonly used again as the first two vertices of the next adjacent triangle. The first vertex of the first triangle is commonly used as the first vertices of following triangles, and parameters setting of these two vertices are required only once.

5.15.7 LX - X COORDINATE of the FIRST VERTEX of a LINE

Command code (Hex) #8
Format:



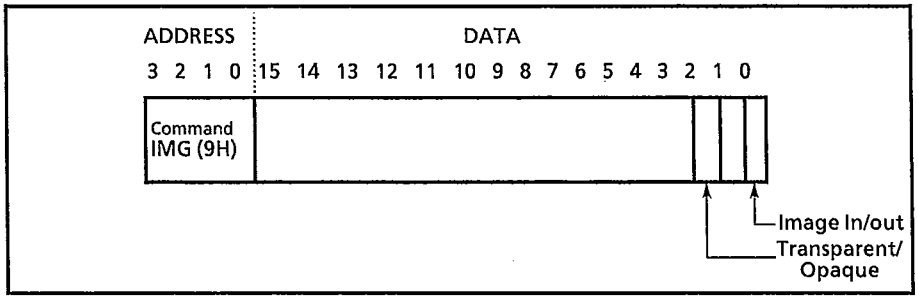
Description:

- ☐ Define a X coordinate of the first vertex of a line or a polyline in 13-bit unsigned integer.
- ☐ This command must be used in the last for the first vertex definition of a line. The usage orders of the above-mentioned I, Z and Y commands can be arbitrary, however, this RX command must be the final command for the first vertex of a line.

5.15.8 IMG - IMAGE DATA OUTPUT to the HOST SYSTEM or IMAGE DATA INPUT from the HOST SYSTEM

Command code (Hex) #9

Format :



Description :

☐ Issue image data input or output by accompanying 4 PARM sub-commands for transferring square data area.

☐ The 0 value of the bit 0 data code defines the image data output from the host system to the FBM through the HSP chip. The 1 value of the bit 0 data code defines the image data input to the host system from the FBM through the HSP chip.

☐ The 0 value of the bit 2 data code defines the image data output in Opaque mode. The 1 value of the bit 2 data code defines the image data output in Transparent mode.

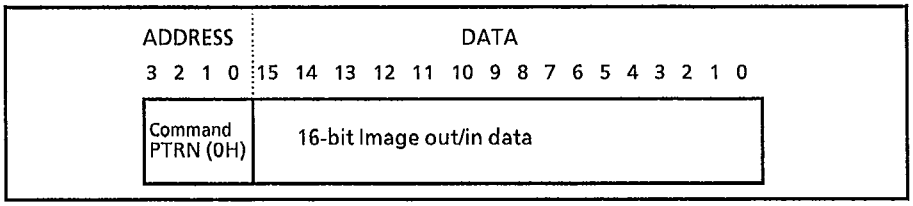
☐ IMODE sub-command defines the access data mode as 1 pixel in 16-bit or horizontal 16 pixels of 1 plane.

☐ For image input, the input order of accompanying 4 ARM sub-commands to IMG command determines the data transfer mode.

- The 2 vertices input order from top-left to bottom-right enables image data transfer from the FBM square region to the Host as same pattern to FBM pattern.
- The 2 vertices input order from bottom-right to top-left enables image data transfer from the FBM square region to the Host by transforming the FBM pattern into X and Y axis symmetry one.
- The 2 vertices input order from bottom-left to top-right enables image data transfer from the FBM square region to the Host by transforming the FBM pattern into X axis symmetry one.
- The 2 vertices input order form top-right to bottom-left enables image data transfer from the FBM square region to the Host by transforming the FBM pattern into Y axis symmetry one.

5.15.9 PTRN - IMAGE DATA PATTERN for IMAGE DATA OUTPUT or IMAGE DATA INPUT

Command code (Hex) #0
Format

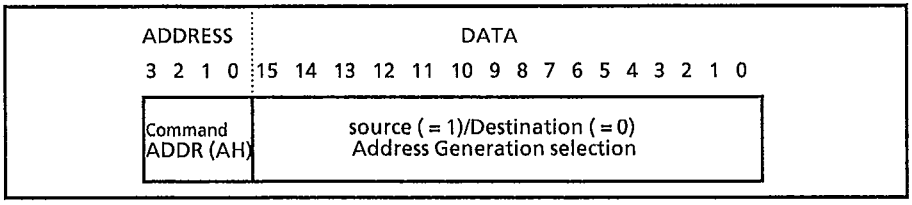


Description :

☐ Transfer image data from the Host system to the FBM for image data output operation. For image data input operation. For image data input operation, this command is used for the read data handshake from the FBM to the Host, and 16-bit image data is read from the D pins.

5.15.10 ADDR - SOURCE or DESTINATION ADDRESS GENERATION

Command code (Hex) #A
Format :



Description :

☐ Transfer data from the source square region to the destination square region. The accompanying PARM sub-commands define the source and the destination regions.

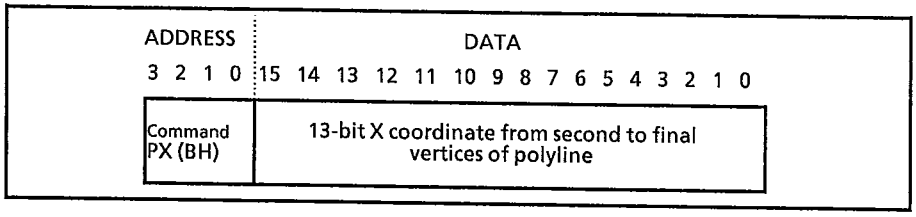
☐ The data can be transferred even if the source region and the destination region locate on the same memory.

☐ Scaling to both the source and the destination regions are available by using the SCALE sub-command to both the source and the destination HSPs.

5.15.11 PX - X COORDINATE from the SECOND VERTEX to the FINAL VERTEX of POLYLINE

Command code (Hex) #B

Format :



Description :

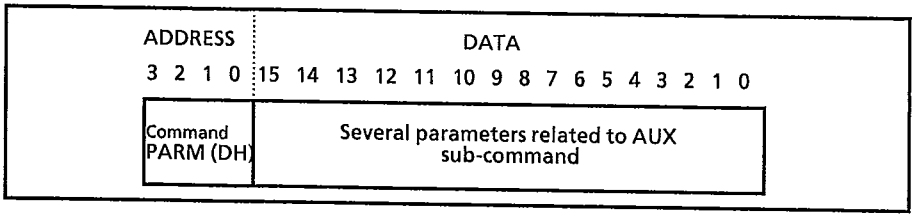
☐ Define a X coordinate from the second vertex to the final vertex of a polyline in 13-bit unsigned integer. This command is used for fast 2-D line drawing, and should not be used for depth cuing.

☐ This command must be used in the last for each vertex definition of a polyline. The above-mentioned Y commands must be used before RX command for the required vertex definition of a polyline.

5.15.12 PARM - PARAMETER SETTING FOLLOWED by AUX COMMAND with SUB-COMMAND DEFINITION at DATA PART

Command code (Hex) #D

Format :



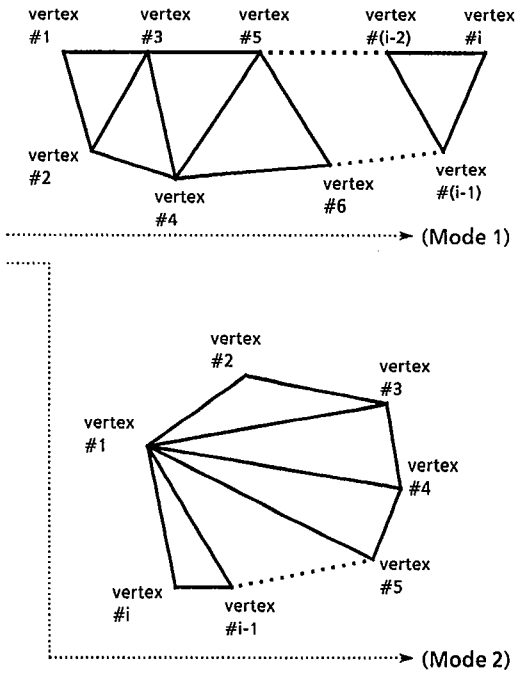
Description :

☐ Define a parameter in 16-bit data field after AUX sub-command setting. One or several set of this command accompanies AUX sub-command. The detail of PARM command related to each AUX sub-command is described in each sub-command section.

5.16 COMMAND SEQUENCE EXAMPLES

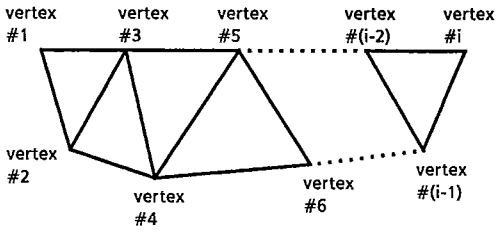
5.16.1 GOURAUD SHADING (TRIANGLE)

COMMAND	DATA CONTENTS
AUX	PMOD (polygon mode)
PARM	Gourand Shadign (= 0)
AUX	ZCNT
PARM	Z Buffer Y/N, Z Section Y/N
I	I value of Vertex #1
Z	Z value of Vertex #1
Y	Y value of Vertex #1
T1X T2X	X value of Vertex #1 for Triangle (Mode 1) X value of Vertex #1 for Triangle (Mode 2)
I	I value of Vertex #2
Z	Z value of Vertex #2
Y	Y value of Vertex #2
X	X value of Vertex #2
⋮	⋮
I	I value of Vertex #(i-1)
Z	Z value of Vertex #(i-1)
Y	Y value of Vertex #(i-1)
X	X value of Vertex #(i-1)
I	I value of Vertex #i
Z	Z value of Vertex #i
Y	Y value of Vertex #i
X	X value of Vertex #i

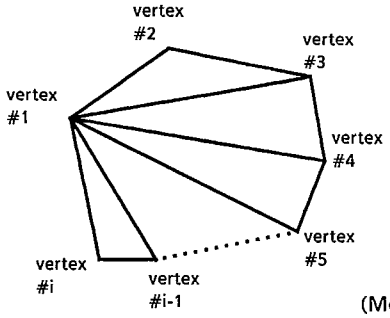


5.16.2 CONSTANT SHADING (TRIANGLE)

COMMAND	DATA CONTENTS
AUX	PMOD (polygon mode)
PARM	Constant Shading (= 1)
I	I value of Vertex #1
Z	Z value of Vertex #1
Y	Y value of Vertex #1
T1X T2X	X value of Vertex #1 for Triangle (Mode 1) X value of Vertex #1 for Triangle (Mode 2)
Y	Y value of Vertex #2
X	X value of Vertex #2
Y	Y value of Vertex #3
X	X value of Vertex #3
Y	
X	
Y	Y value of Vertex #(i-1)
X	X value of Vertex #(i-1)
Z	Z value of Vertex #i
Y	Y value of Vertex #i
X	X value of Vertex #i



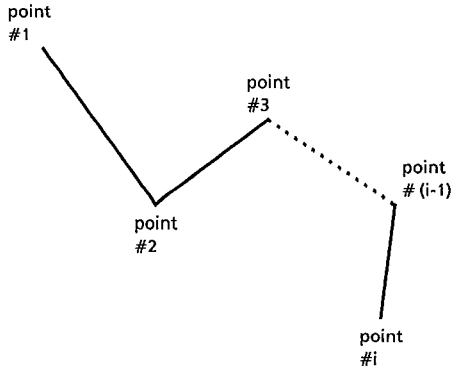
(Mode 1)



(Mode 2)

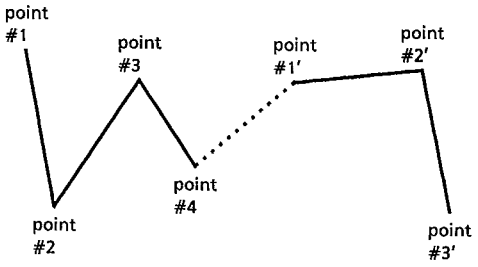
5.16.3 DEPTH CUING

COMMAND	DATA CONTENTS
AUX	LMOD (ling drawing mode)
PARM	Depth Cueing (= 2)
AUX	ZCNT
PARM	Z Buffer Y/N, Z Section Y/N
⋮	⋮
I	I value of Point #1
Z	Z value of Point #1
Y	Y value of Point #1
LX	X value of Point #1 for Line Drawing
I	I value of Point #2
Z	Z value of Point #2
Y	Y value of Point #2
X	X value of Point #2
AUX	LSTA (line status def.)
PARM	Polyline/Separate line def.
I	I value of Point #3
Z	Z value of Point #3
Y	Y value of Point #3
X	X value of Point #3
AUX	LSTA (line status def.)
PARM	Polyline/Separate line def.



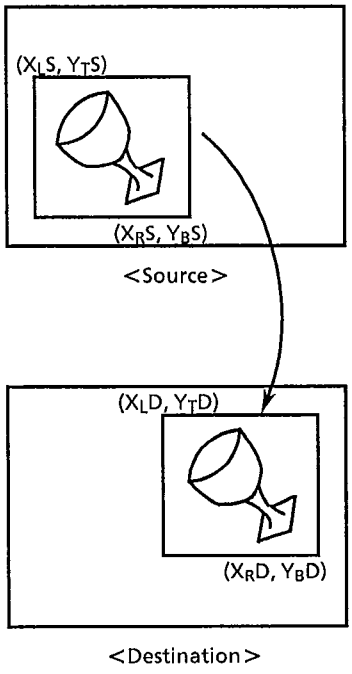
5.16.4 LINE DRAWING

COMMAND	DATA CONTENTS
INIT	System Configuration def. CT = 0/1
AUX	LMOD (ling drawing mode)
PARM	Line (Opaque = 0, Transparent = 1)
⋮	⋮
Y	Y value of Point #1
LX	X value of Point #1 for Line Drawing
AUX	LSTA (line status def.)
PARM	Polyline/Separate line def.
Y	Y value of Point #2
PX	X value of Point #2
Y	Y value of Point #3
PX	X value of Point #3
AUX	LSTA (line status def.)
PARM	Polyline/Separate line def.
Y	Y value of Point #4
PX	X value of Point #4
Y	Y value of Point #1'
LX	X value of Point #1' for Line Drawing
Y	Y value of Point #2'
PX	X value of Point #2'
Y	Y value of Point #3'
PX	X value of Point #3'



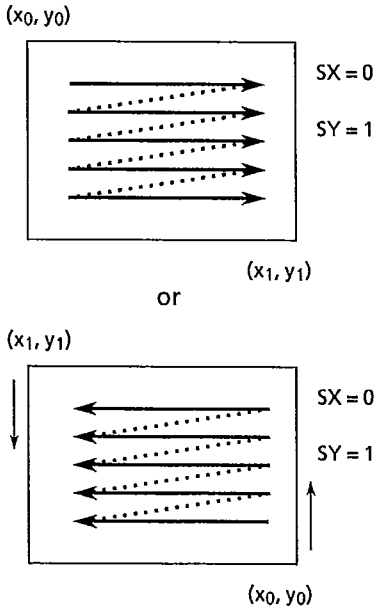
5.16.5 ADDRESS GENERATOR (SCALING)

COMMAND	DATA CONTENTS	
AUX	LMOD (ling drawing mode)	
PARM	16 pixel (= 0)/1 pixel of 16bit (= 1)	
AUX	SCL (scale)	Input to Source LSI
PARM	Magnification Scale of Source	
AUX	SCL (scale)	Input to Destination LSI
PARM	Magnification Scale of Destination	
ADDR	INPUT (= 1)	
PARM	Source Addr. Upper Left x (X_LS)	
PARM	Source Addr. Lower Right y (Y_TS)	
PARM	Source Addr. Upper Left x (X_RS)	
PARM	Source Addr. Lower Right y (Y_BS)	
ADDR	OUTPUT(= 0)	
PARM	Destination Addr. Upper Left x (X_LS)	
PARM	Destination Addr. Lower Right y (Y_TS)	
PARM	Destination Addr. Upper Left x (X_RS)	
PARM	Destination Addr. Lower Right y (Y_BS)	



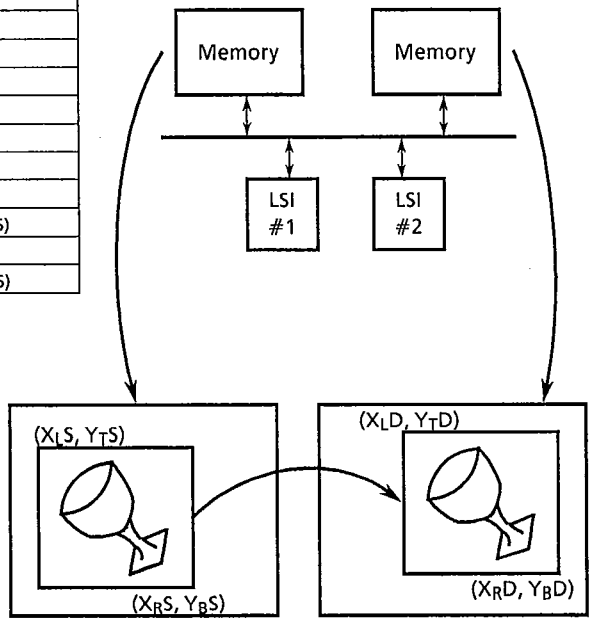
5.16.6 IMAGE DATA

COMMAND	DATA CONTENTS
AUX	LMOD (Image Data I/O)
PARM	16 pixel (= 0)/1 pixel of 16bit (= 1)
AUX	HCNT (Hardware Control Mode)
PARM	Read Modify Write (Y/N)
IMG	Image Data I/O, Opeque/Trasparent
PARM	Square for Image Out x (x_0)
PARM	Square for Image Out y (y_0)
PARM	Square for Image Out x (x_1)
PARM	Square for Image Out y (y_1)



5.16.7 ADDRESS GENERATION (SOURCE & DESTINATION)

NO.	COMMAND	DATA CONTENTS
1	ADDR	LMOD (Image Data I/O)
2	PARM	Source Addr. Upper Left x ($X_L S$)
3	PARM	Source Addr. Lower Right y ($Y_T S$)
4	PARM	Source Addr. Upper Left x ($X_R S$)
5	PARM	Source Addr. Lower Right y ($Y_B S$)
6	ADDR	OUTPUT (= 0)
7	PARM	Destination Addr. Upper Left x ($X_L S$)
8	PARM	Destination Addr. Lower Right y ($Y_T S$)
9	PARM	Destination Addr. Upper Left x ($X_R S$)
10	PARM	Destination Addr. Lower Right y ($Y_B S$)



5.17 GENERAL DESCRIPTION of OPERATIONS

5.17.1 GRAPHICS CONCEPTS

☐ SCREEN COORDINATES

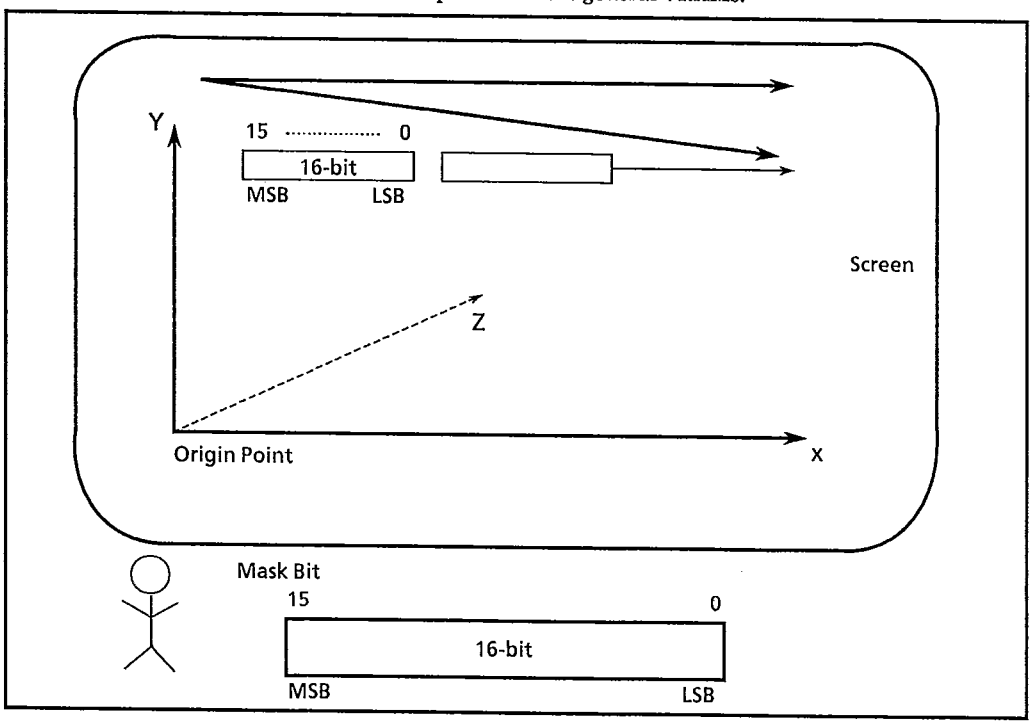
Any location in the 3-dimensional space can be referenced through a set of (x, y, z) coordinates. The HSP uses a set of 3-dimensional coordinates whose Origin Point begins at coordinates (0, 0, 0), which is located in the bottom-left corner. The X axis extends across the bottom and increases from left to right of the screen. The Y axis extends up the left side and increases from bottom to top of the screen. The Z axis extends from the viewpoint and increases from front to depth direction of the screen.

☐ PIXELS

The HSP can manipulate one pixel of 16-bit color intensity (or color index) or horizontal 16 pixels of one plane selectively.

In one pixel of 16-bit color mode, the write enables signals (-WEI, -WEZ, -WEZS) to the external memories are used to control each pixel drawing in the HSP. Also in this mode, the bit plane selection by MASK sub-command is available. This is supported in the HSP by generating a bit plane selection pattern and sending that on the I bus at write per bit operation of the general VRAMs.

In horizontal 16 pixels of one plane mode, the mask bit (16-bit unit) is generated and sent externally as a mask pattern on the I bus at bit-mask operation of the general VRAMs.



5.17.2 REMARKS to SEVERAL OPERAITONS

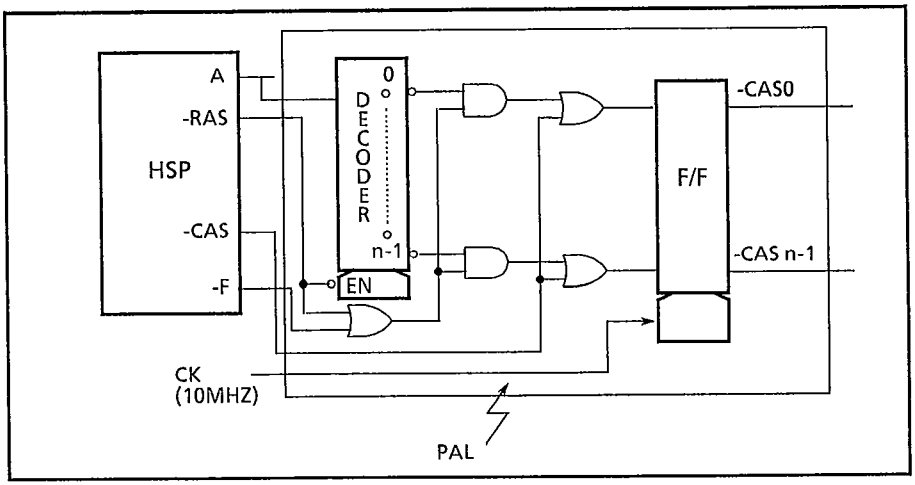
The HSP operations are classified briefly as Gouraud shading, Constant shading, Depth Cueing, Line drawing, Address Generator (source or destination), Image data output and Image data input.

☐ HOST INTERFACE

The control signals of the host interface such as RESET0, WDX0, RDX0 are synchronized internally.

☐ GOURAUD SHADING

The CAS signal is externally generated for Gouraud shading. The pixel display control usually requires VRAM's interleaved configuration for memory read operation to the CRT display. Therefore CAS signals are interleaved externally by using the CAS* signal from the HSP. The external CAS generation circuit example is shown in this figure.



☐ MULTI-CHIPS GOURAUD SHADING

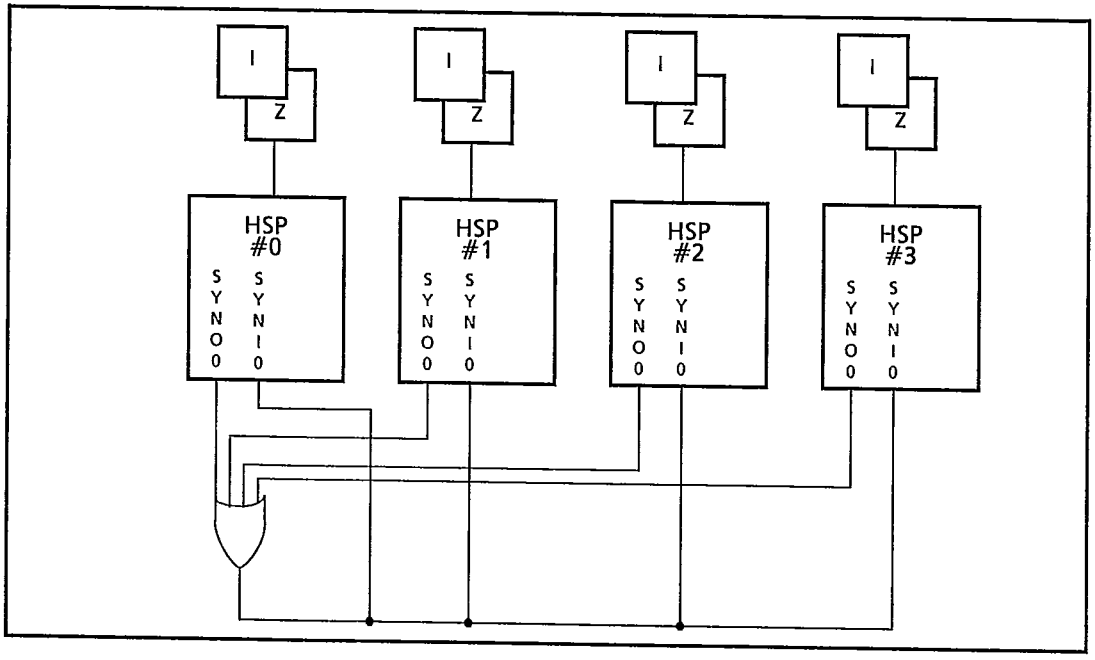
For Gouraud shading using multi HSP chips, following setups are required.

Give cascade operation information by INIT command.

Set EXSYN bit (bit 11) as value 1 in HCONTROL sub-command.

All -SYNO pins of all chips should be logical-ORed externally, and the results signal is commonly sent to -SYNI pin of each chip. This configuration assures the synchronized Gouraud shading by 2 or 4 HSP chips. Z Buffer and FBM (I memory) should be parallel structure to correspond to each HSP chip.

As for command setting, polygon commands such as color intensity and 3-D coordinates can be set simultaneously to all HSPs.



5.17.3 R.G.B GRAPHICS OPERATION by 2 HSP CHIPS

For operations except Address Generator and Image Input operations , R, G, B graphics system can be configured by 2 HSP chips. The following figure shows the configuration example. The write-enable and other control signals should be carefully connected. Especially the write enable control signals of the chip ② should be neglected.

- ☐ In INITIALIZATION command, CSCD0 bits should be selected as value 0. (No cascaded configuration selected.)
- ☐ In ZCONTROL sub-command, ZCK bit should be selected as value 1. Z control mode is selected.
- ☐ In HCONTROL sub-command, ZI bit should be selected as value 0, to transfer internally calculated Z value to ZO pins.
- ☐ Also in HCONTROL sub-command, EXTSYN bit should be selected as value 1 to enable externally synchronized operations between 2 HSP chips.
- ☐ For command settings, Z command should be used to set color value instead of Z value (depth value) to make color interpolation possible in the ① chip.
- ☐ Also for command settings, the X and Y commands can be used commonly to 2 HSP.

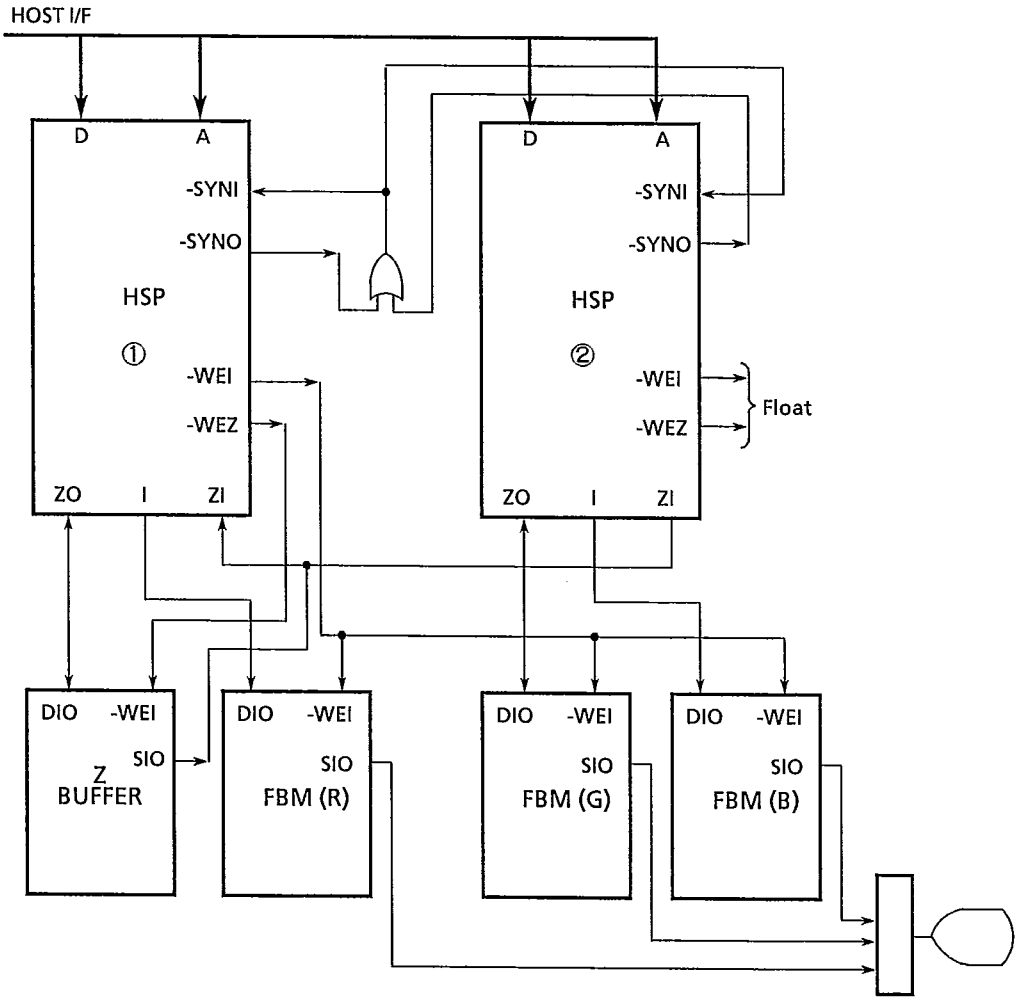


FIG. 5.17.3 EXAMPLE for R, G, B, GRAPHIC SYSTEM

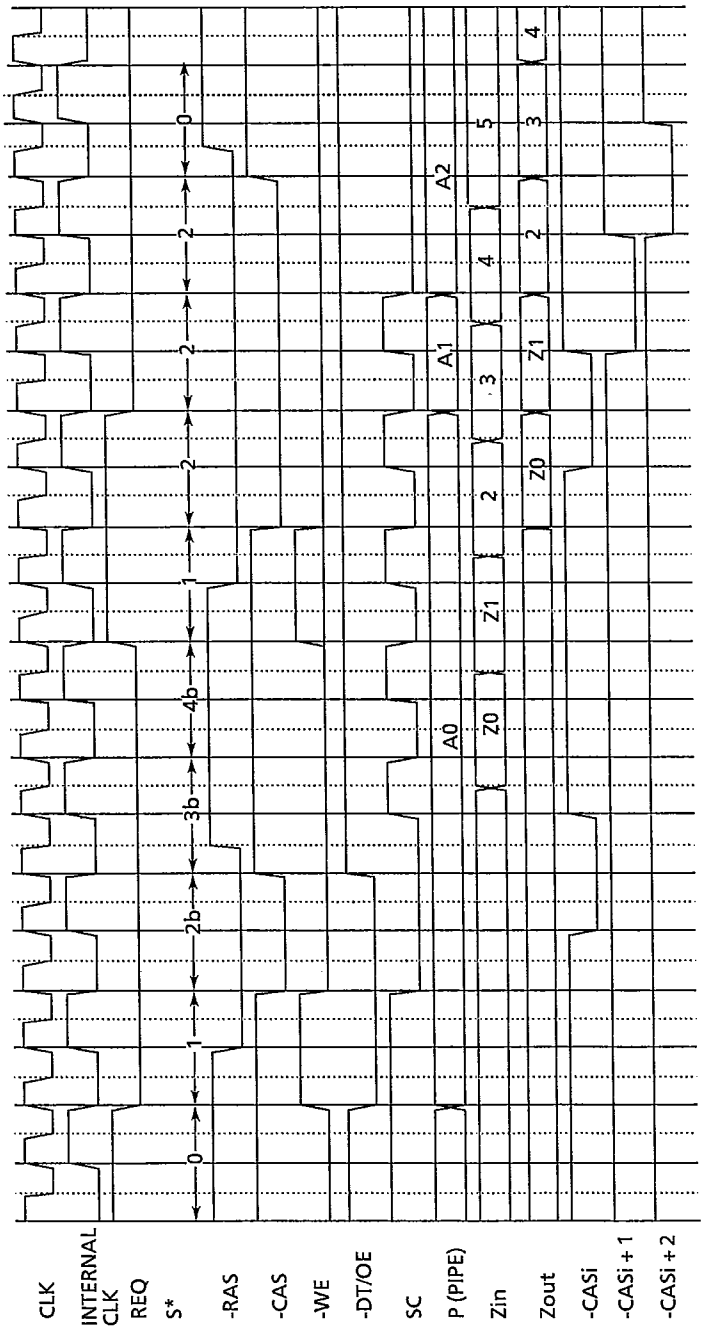
5.17.4 TIMING EXAMPLE of SEVERAL OPERATIONS

Following 11 figures show the typical timing example of HSP operations. S* indicates the internal memory state. For Gouraud shading, the external CASi, CASi + 1, and so on should be generated.

The constant shading has two mode which are selected by FS bit of HCONTROL sub-command. When FS bit is value 1, FCASi and GCASi should be generated externally. When FS bit is value 0, externally used CAS signals are CASi, CASi + 1, and so on.

For line drawing in cache mode, mask information and the write data pattern information are utilized to enable Opaque and Transparent operations. In Opaque mode the mask pattern at write-per-bit timing of VRAM is generated for all pixels of line, and the data pattern is selected as value 1 or 0 depending on the LPATTERN sub-command. 1 or 0 value of this data pattern should choose the color corresponding to its value. In Transparent mode, the mask pattern is generated for the write-permitted pixel and the data pattern has the same value as the mask pattern., thus enable line drawing.

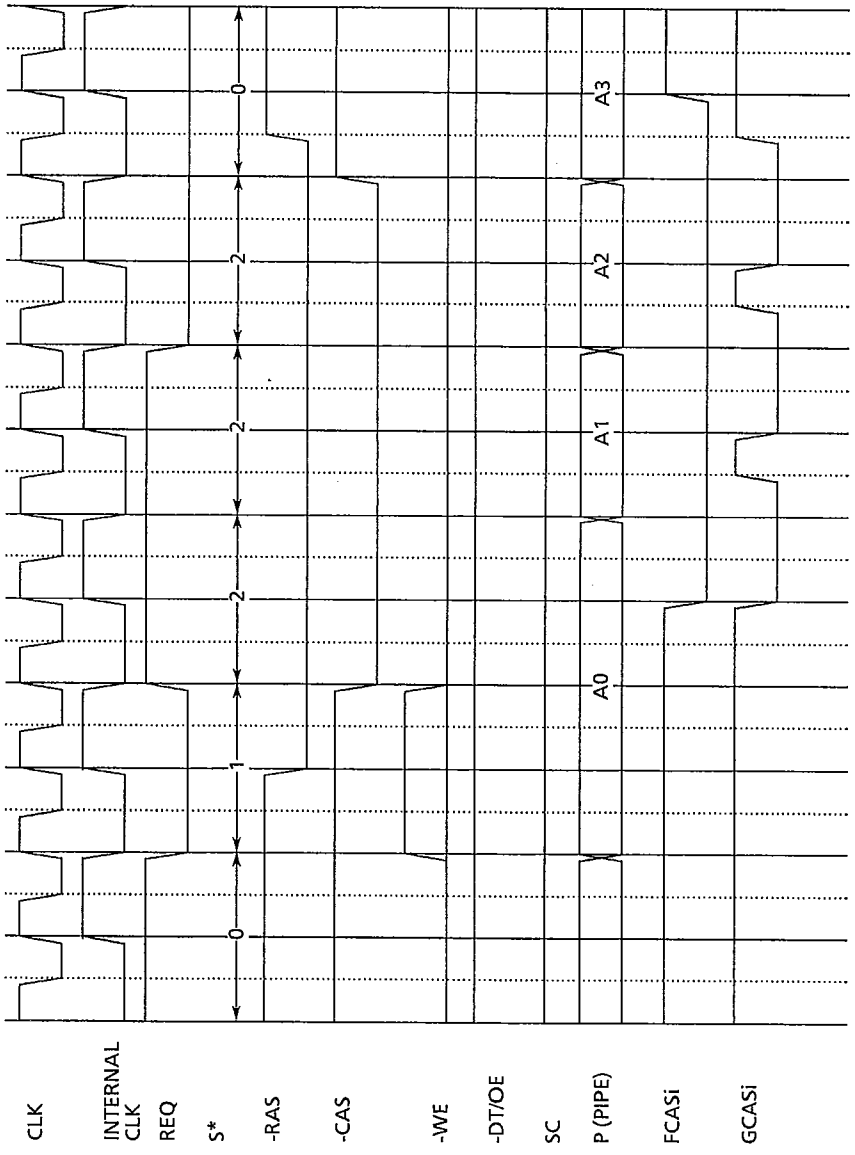
In image output, the horizontal 16 pixels of 1 plane access is possible same as the cache line drawing. The Opaque or Transparent mode selection mechanism is realized by the mask and pattern data combination mechanism as in cache line.



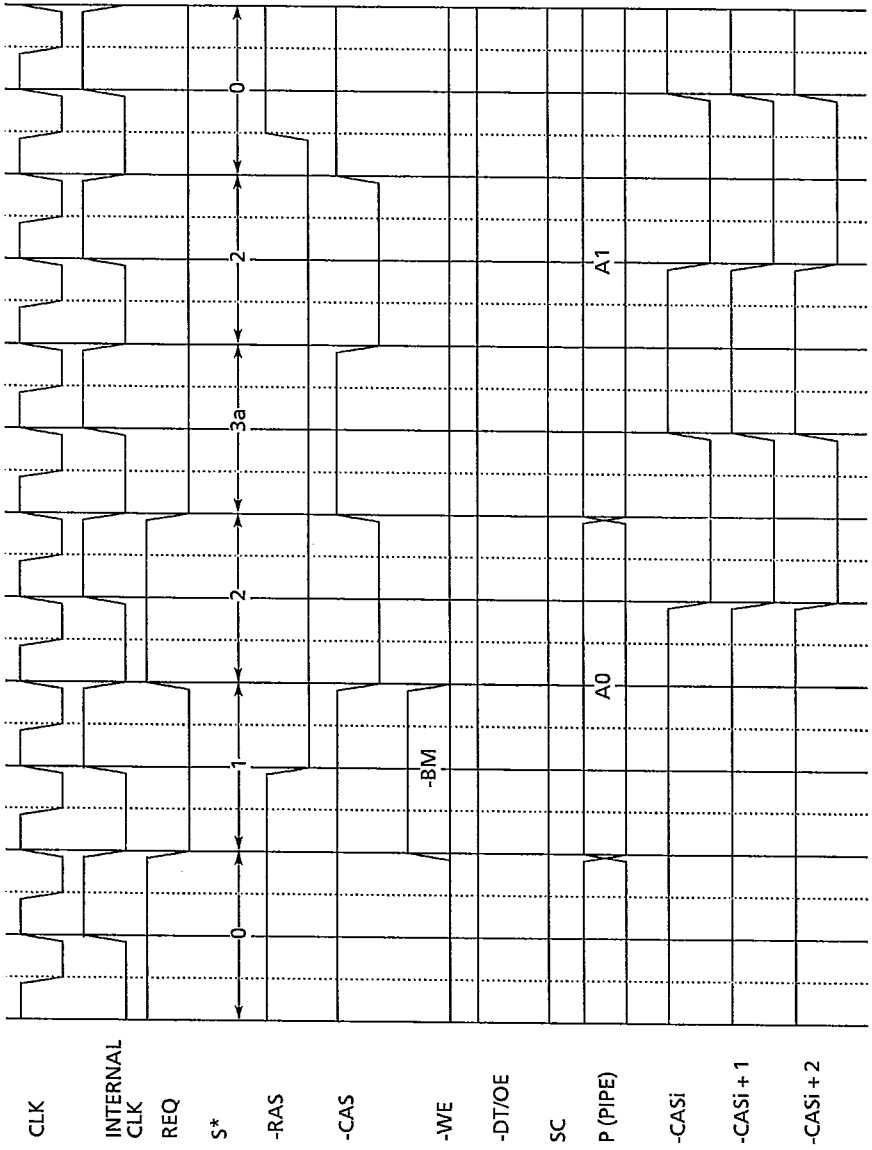
Gouraud Shading

DISPLAY CONTROLLER

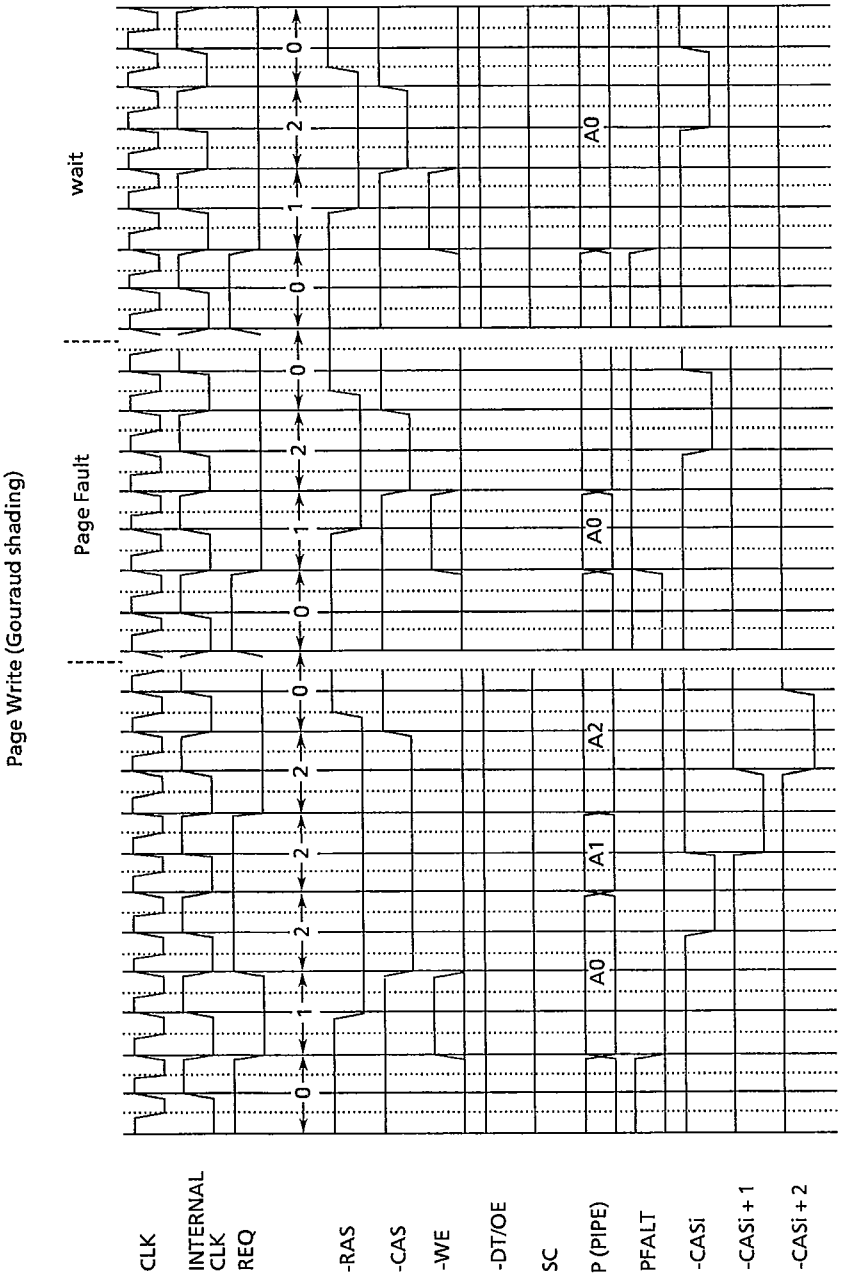
Page Write Constant Shading (FS mode)



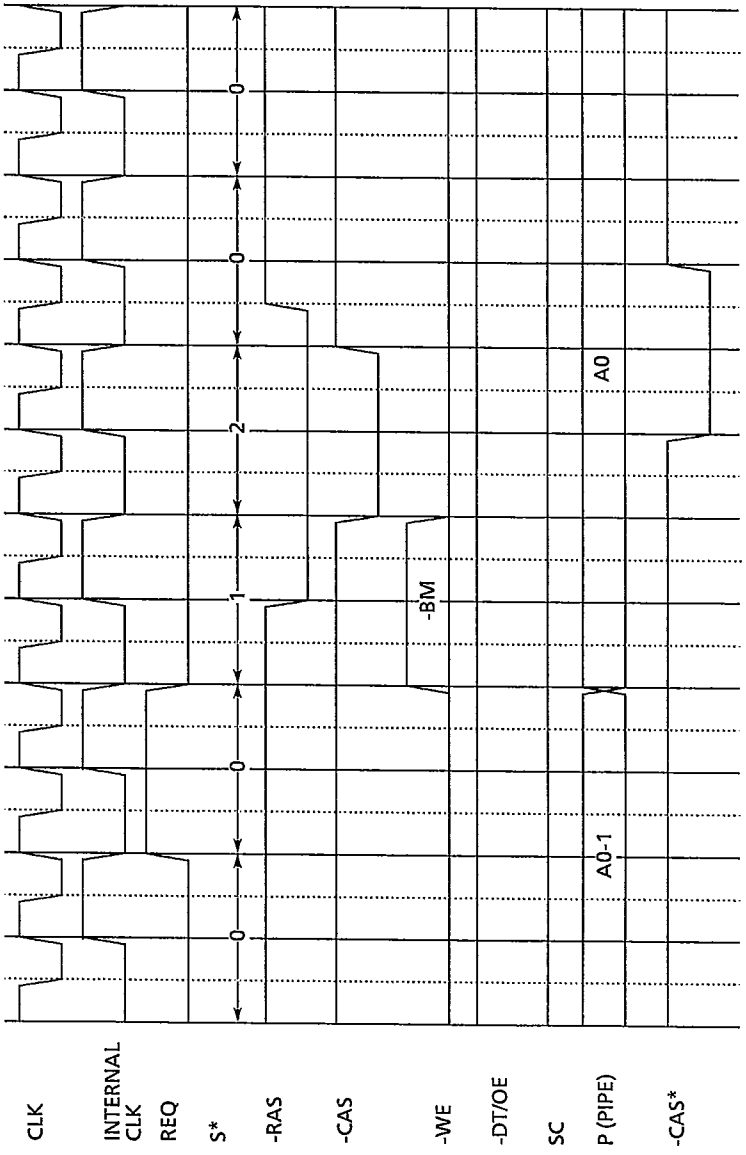
Page Write Constant Shading (-FS mode)



DISPLAY CONTROLLER

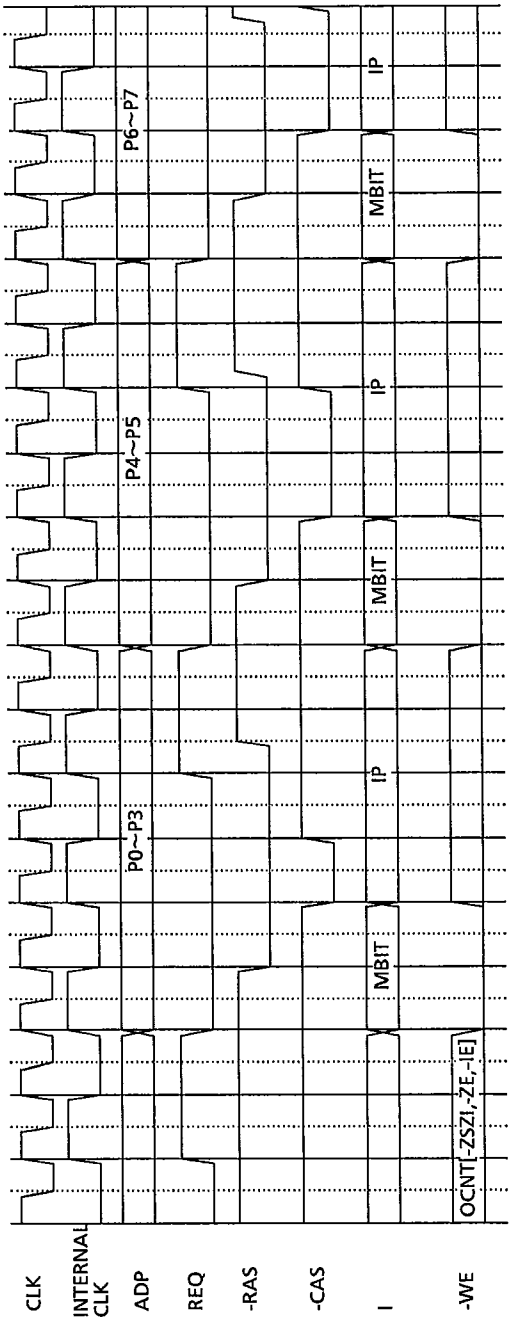


LINE DRAWING (PIXEL Write)



DISPLAY CONTROLLER

LINE DRAWING (CACHE)



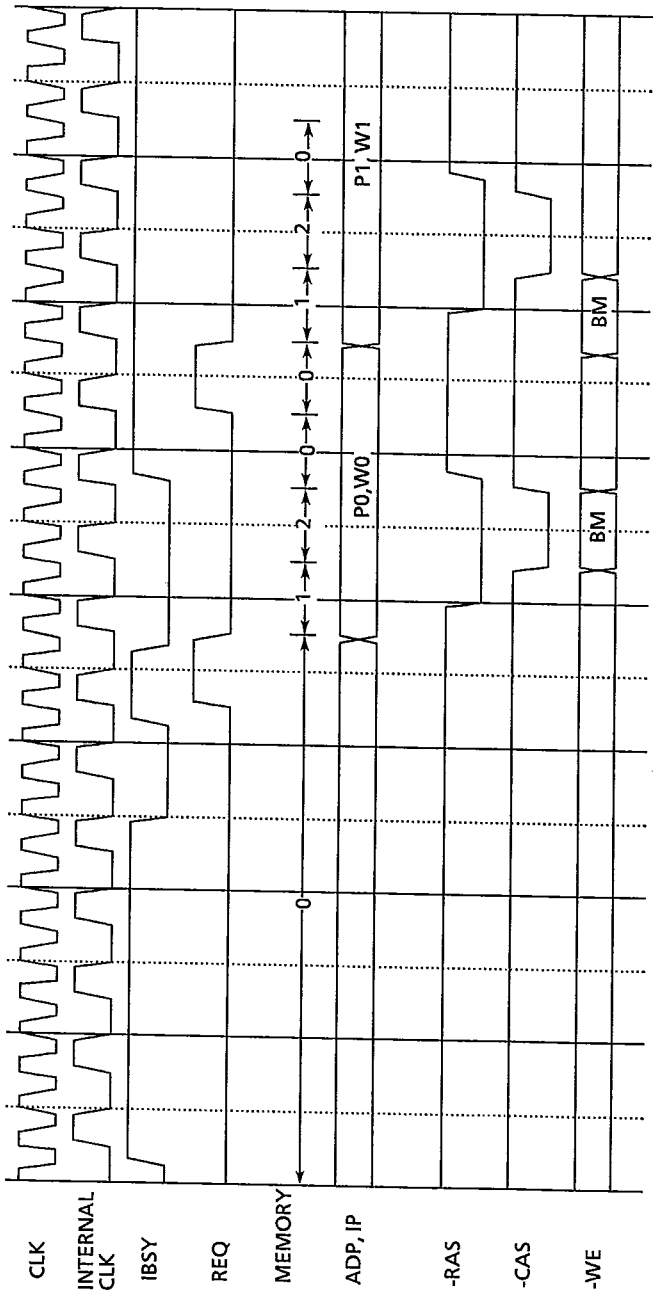
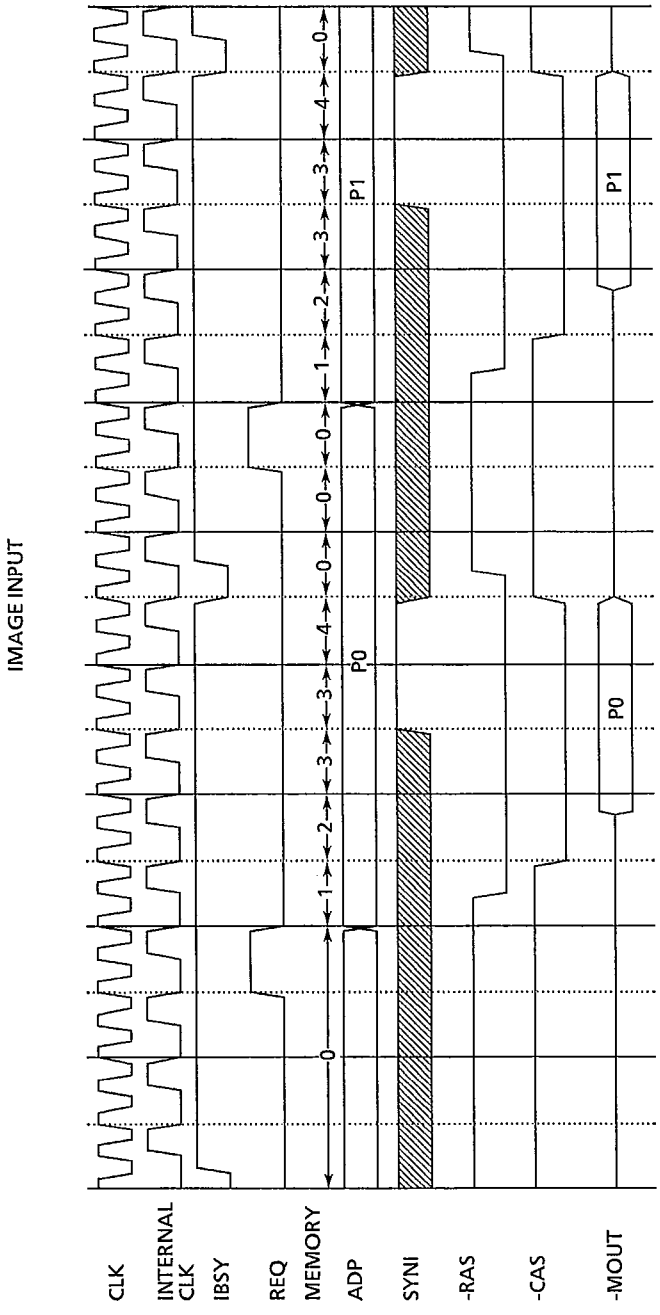
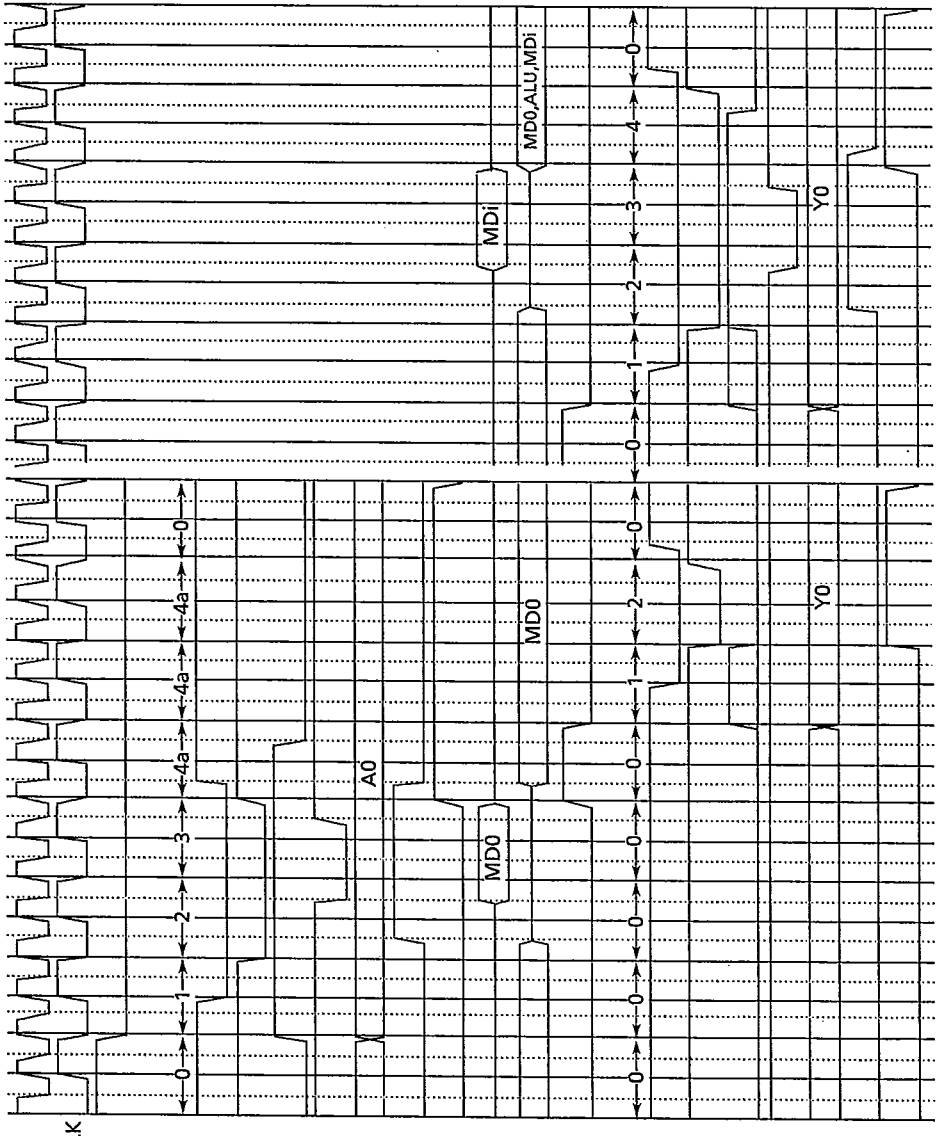


IMAGE OUT
CLK
INTERNAL CLK
IBSY
REQ
MEMORY
ADP, IP
-RAS
-CAS
-WE
0
1
2
0
0
1
0
2
P0,W0
P1,W1
BM
BM

DISPLAY CONTROLLER

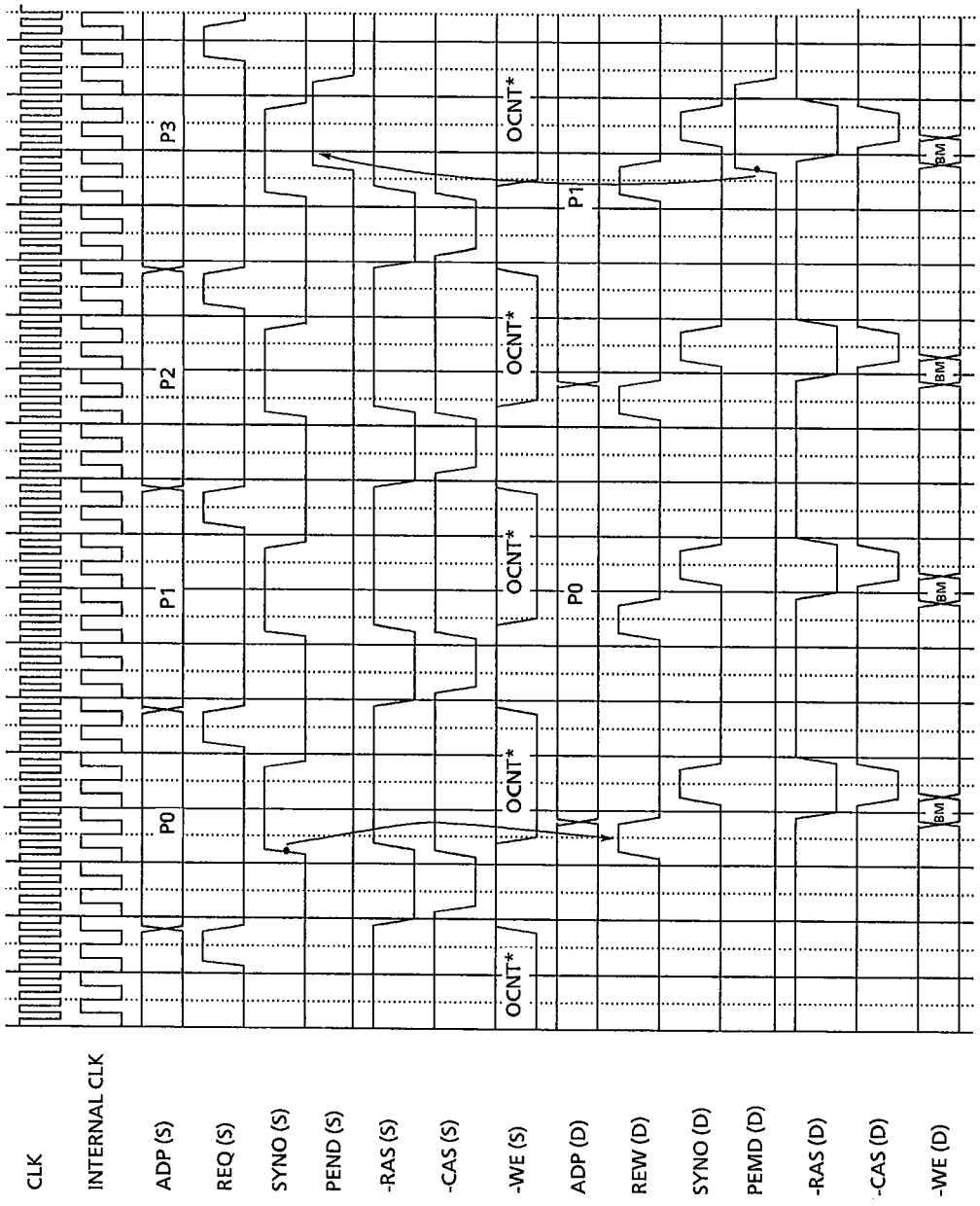


Address Generator (Source & Destination)

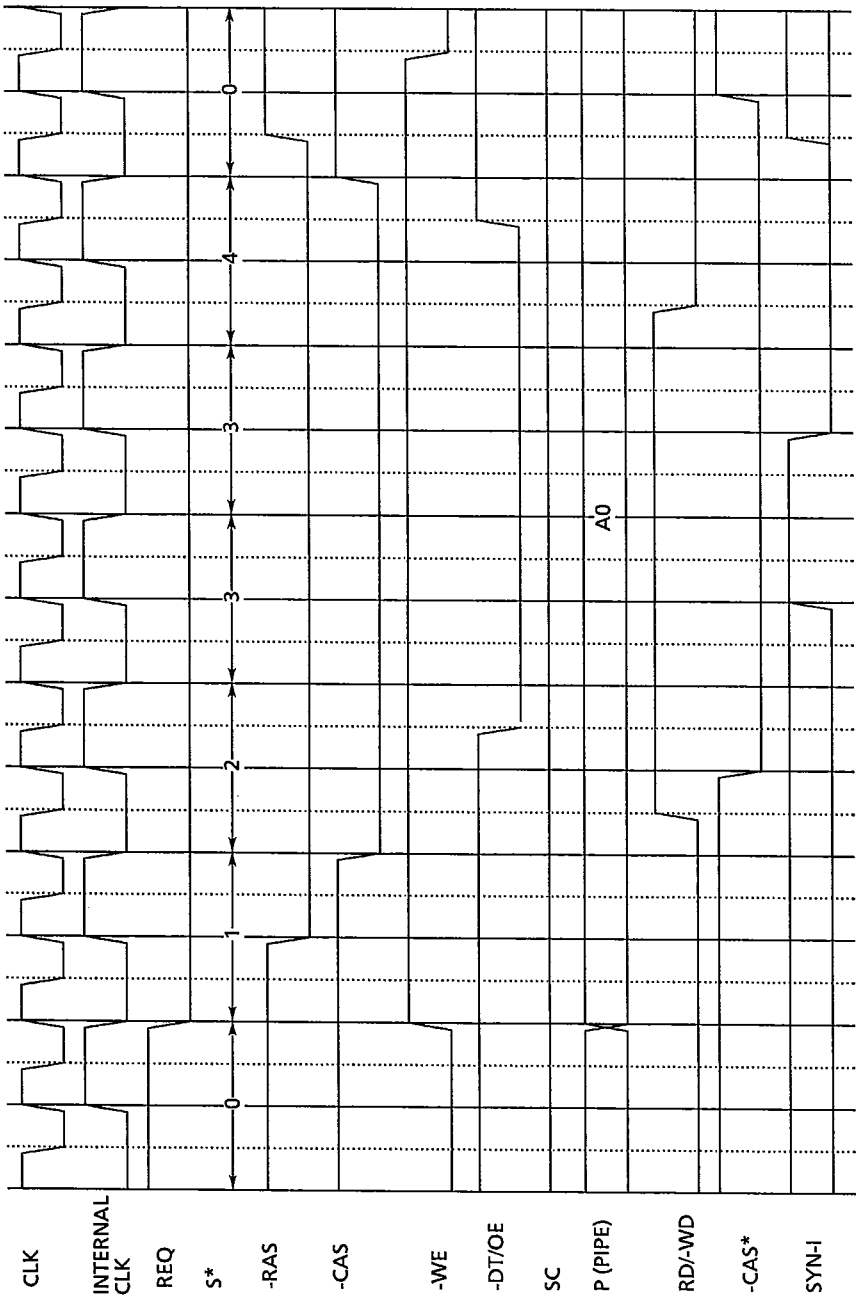


DISPLAY CONTROLLER

Address Generator (scaling)



Read Mode (CPU)



6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0V (GND)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	−0.5 ~ +7.0	V
Input Voltage	V_{IN}	−0.3 ~ +7.0	V
Operating Temperature	T_{OPR}	0 ~ +70	°C
Storage Temperature	T_{STG}	−65 ~ +125	°C

6.2 DC CHARACTERISTICS

Ta = 0°C~70°C, VSS = 0V, VDD = 5V ± 5%

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Input Low Voltage	V_{IL}		0	0.8	v
Input High Voltage	V_{IH}		2.2	VDD	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −0.4mA	2.4	–	V
Power Supply Current	I_{DD}		–	200	mA
Input Leakage Current	I_{LI}		–	±5	μA
Output Leadage Current	I_{LO}		–	±5	μA
Input Low Voltage	V_{IL} (CLK)		0	0.4	V
Input High Voltage	V_{IH} (CLK)		3.6	VDD	V
Capacitance of Input Buffer	C_{IN}		–	10	pF

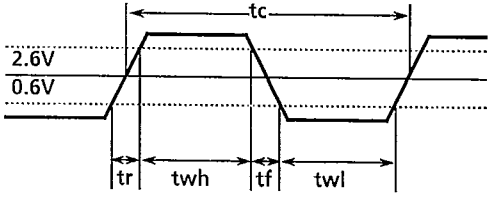
6.3 AC CHARACTERISTICS

6.3.1 HOST INTERFACE

Ta = 0°C~70°C, VSS = 0V, VDD = 5V ± 5%, C_L = 60pF

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Clock Cycle Period	tcyc		83	–	ns
-RESET Setup Time	tress		5	–	ns
-RESET Hold Time	tresh		20	–	ns
-RESET to -WDX Delay Time	trw		2tcyc	–	ns
-WDX Cycle Time	twc		2tcyc	–	ns
-WDX, -RDX Setup Time	tcmds		5	–	ns
-WDX, -RDX Hold Time	tcmdh		10	–	ns
Data, A Setup Time	tds		5	–	ns
Data, A Hold Time	tdh		20	–	ns
NFLL Active Delay	tndf		–	50	ns
NFLL Inactive Delay	tndr		–	50	ns
IBSY, CBSY Active Delay	ticr		–	50	ns
IBSY, CBSY Inactive Delay	ticf		–	50	ns

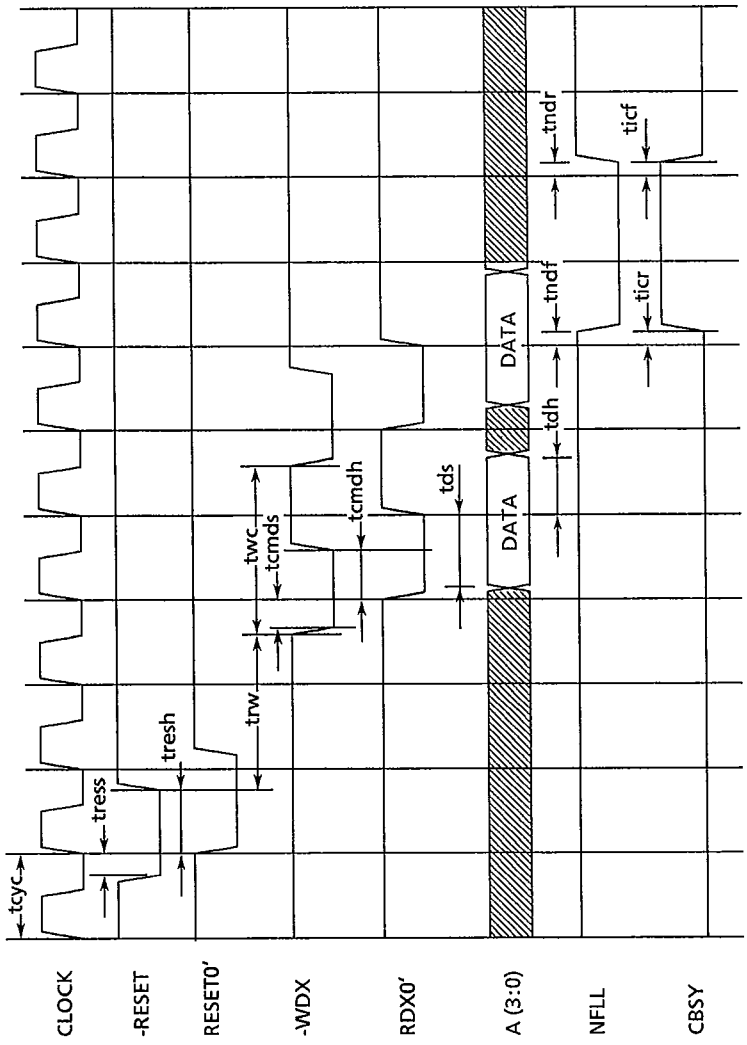
CLOCK TIMING



PARAMETER	SYMBOL	MIN.	MAX	UNIT
Cycle Time	tc	83	–	ns
Rise Time	tr	–	5	ns
Fall Time	tf	–	5	ns
H-level Pulse Width	twh	36	–	ns
L-level Pulse Width	twl	36	–	ns

DISPLAY CONTROLLER

HSP Host interface command input mode



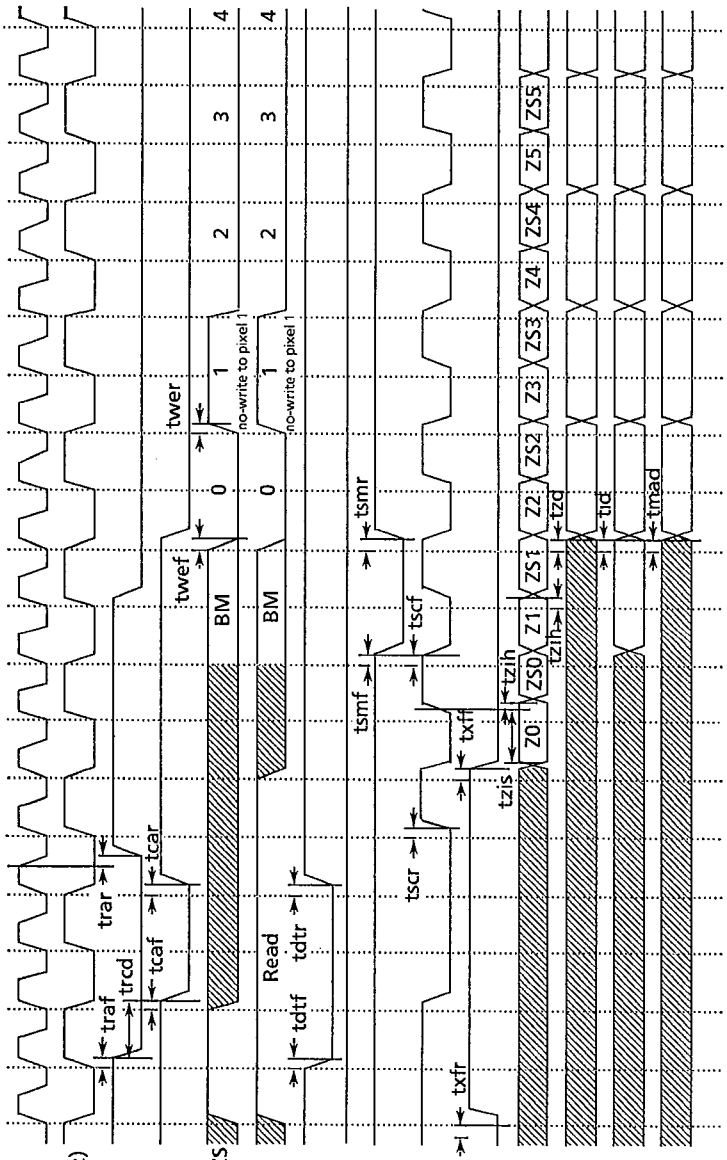
RESET0', WDX0' and RDX0' are internal synchronized signal in the HSP.

6.3.2 SERIAL READ and PAGE WRITE

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
-RAS Active Delay	traf		10	40	ns
-RAS Inactive Delay	trar		10	40	ns
-CAS Active Delay	tcaf		10	40	ns
-CAS Inactive Delay	tcar		10	40	ns
-WEI, -WEZ, -WEZS, Active Delay	twef		–	50	ns
-WEI, -WEZ, -WEZS, Inactive Delay	twer		–	50	ns
-DTOEI, -DTOEZ Active Delay	tdtf		–	50	ns
-DTOEI, -DTOEZ Inactive Delay	tdtr		–	50	ns
SC Active Delay	tscr		–	40	ns
SC Inactive Delay	tscf		–	40	ns
XFR Active Delay	txfr		–	50	ns
XFR Inactive Delay	txff		–	50	ns
ZO Delay Time	tzd		–	50	ns
I Delay Time	tid		–	50	ns
MA Delay Time	tmad		–	50	ns
ZI Setup Time	tzis		25	–	ns
ZI Hold Time	tzih		0	–	ns
M/I Active Delay	tsmf		–	45	ns
M/I Inactive Delay	tsmr		–	45	ns
-RAS to-CAS Delay	trcd		tcycl-20	tcycl + 20	ns

DISPLAY CONTROLLER

Serial read page write



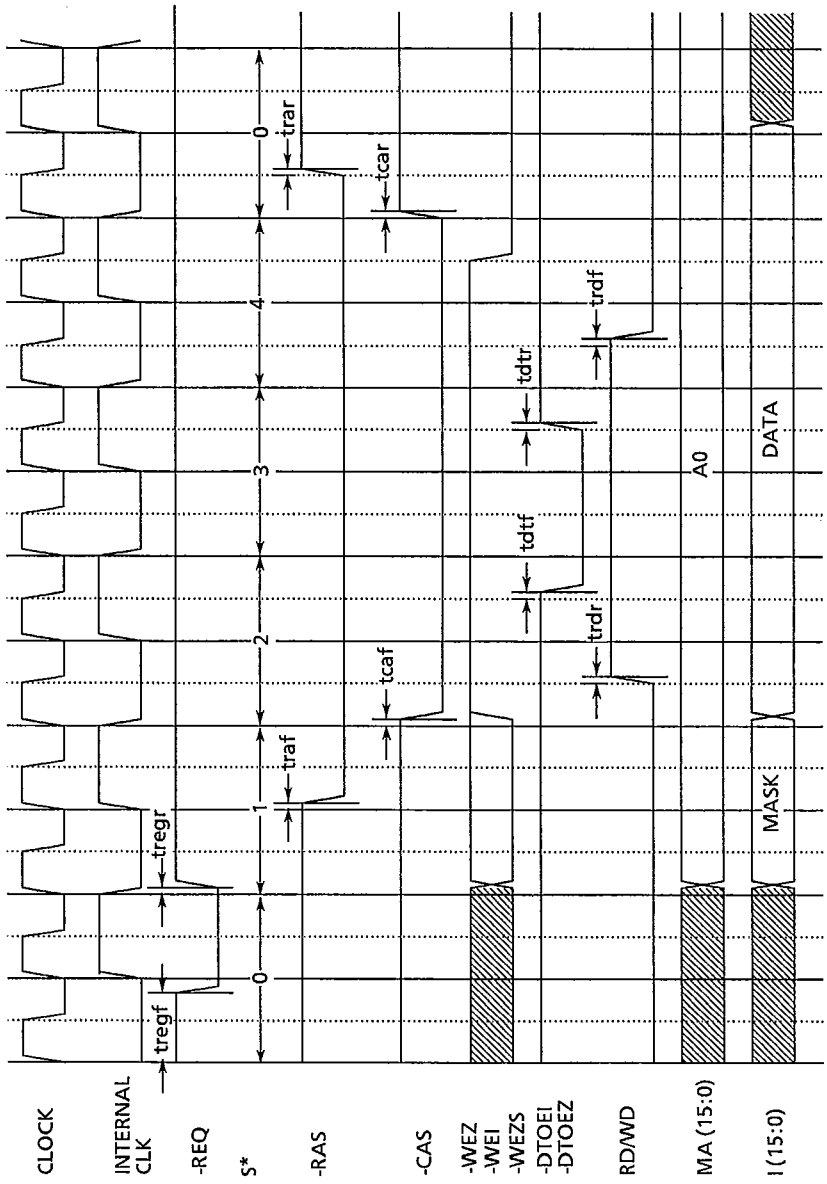
WE stands for -WEZS , -WEI and -WEZ.

6.3.3 READ MODIFY WRITE

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
-REQ Active Delay	treqf		–	60	ns
-REQ Inactive Delay	treqr		–	60	ns
-DTOEI, -DTOEZ Active Delay (from CLK down edge)	tdtf		–	50	ns
-DTOEI, -DTOEZ Inactive Delay (from CLK down edge)	tdtr		–	50	ns
RD/WD Active Delay	trdf		–	40	ns
RD/WD Inactive Delay	trdr		–	40	ns

DISPLAY CONTROLLER

Read/Write modify

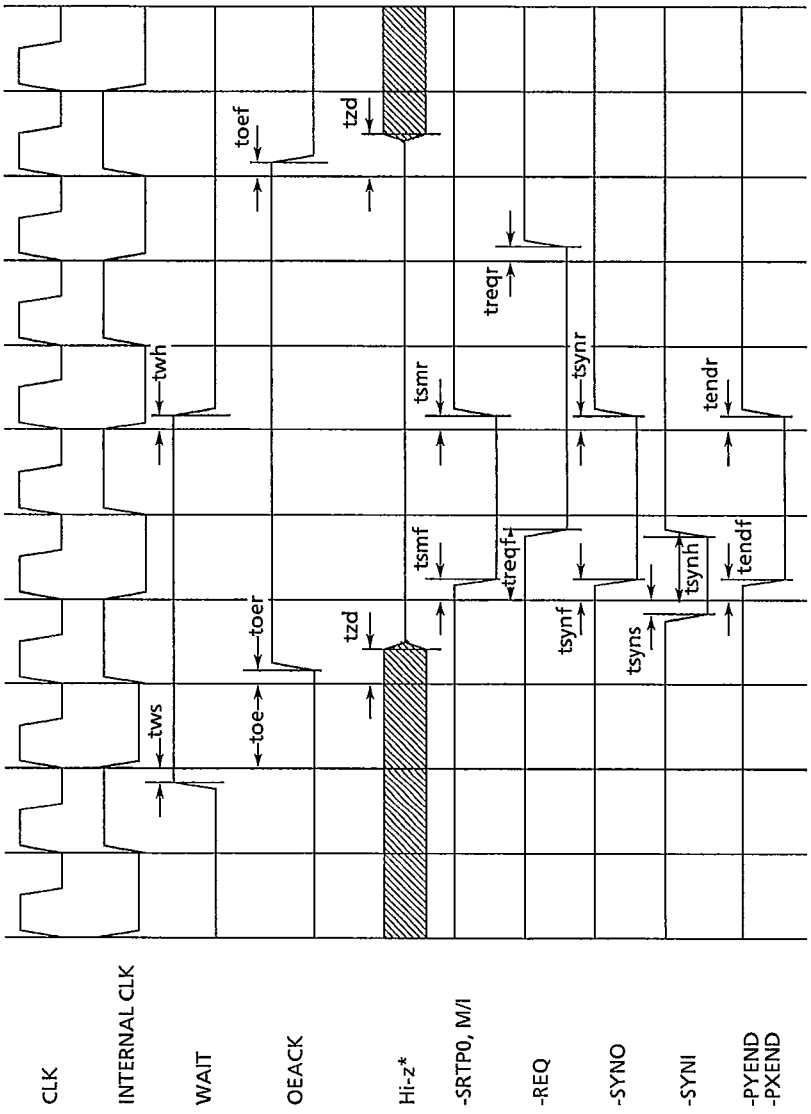


6.3.4 WAIT TIMING & SYNCHRONOUS TIMING

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
WAIT Setup Time	tws		–	5	ns
WAIT Hold Time	twh		–	20	ns
WAIT to OEACK Delay Time	toe		–	13tcyc	ns
OEACK Active Delay	toer		–	45	ns
OEACK Inactive Delay	toef		–	40	ns
PIN Float/Valid Delay	tzd		–	50	ns
-SRTP, M/I Active Delay	tsmf		–	50	ns
-SRTP, M/I Inactive Delay	tsmr		–	50	ns
-SYNO Active Delay	tsynf		–	40	ns
-SYNI Set-up Time	tsyns		30	–	ns
-SYNI Hold Time	tsynh		30	–	ns
-SYNO Inactive Delay	tsynr		–	40	ns
PY, PXEND Active Delay	tendf		–	50	ns
PY, PXEND Inactive Delay	tendr		–	50	ns

DISPLAY CONTROLLER

Wait and Synchronize timing



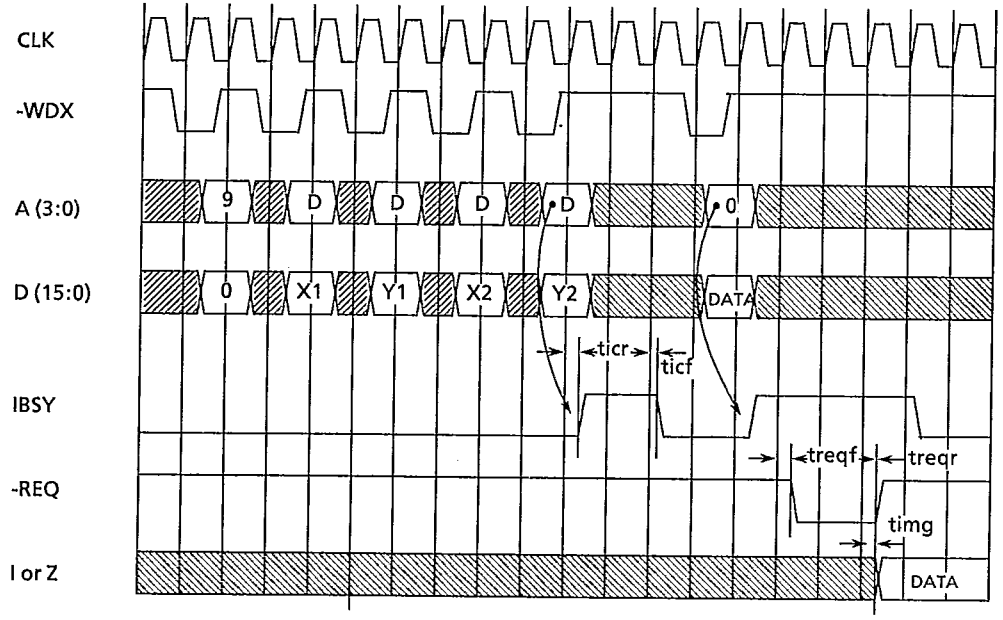
Hi-z pin : MA (25:0) I (15:0) Z (15:0) RAS0 CAS0 DTOE0 WEZS0 WEZ0 WEI0

6.3.5 IMAGE DATA INPUT and OUTPUT

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
IBSY Active Delay	ticr		–	50	ns
IBSY Inactive Delay	ticf		–	50	ns
Data Valid Delay	tdv		–	40	ns
Data Invalid Delay	tdiv		–	40	ns
Z.I. Delay	timg		–	40	ns

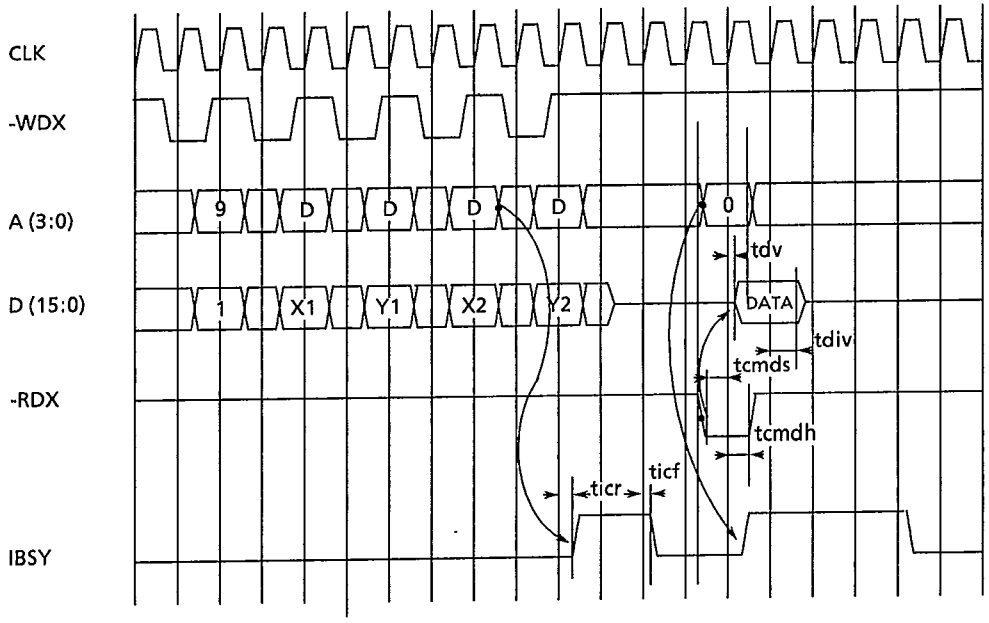
2

Image data output



DISPLAY CONTROLLER

Image data input

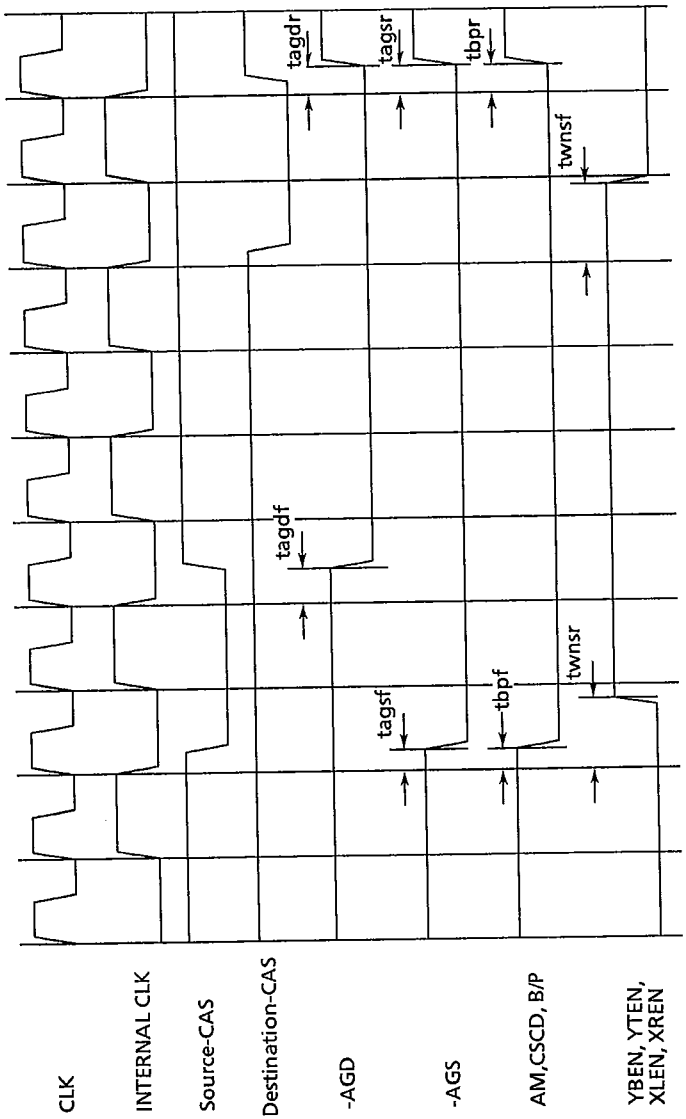


6.3.6 ADDRESS GENERATOR

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
-AGD Active Delay	tagdf		–	50	ns
-AGD Inactive Delay	tagdr		–	50	ns
-AGS Active Delay	tagsf		–	50	
-AGS Inactive Delay	tagsr		–	50	
AM, B/P Fall Time	tbpf		–	50	ns
AM, B/P Rise Time	tbpr		–	50	ns
YBEN, YTEN, XLEN,M XREN Inactive Delay	twnsr		–	50	ns
YBEN, YTEN, XLEN,M XREN Active Delay	twnsf		–	50	ns

DISPLAY CONTROLLER

Address Generator

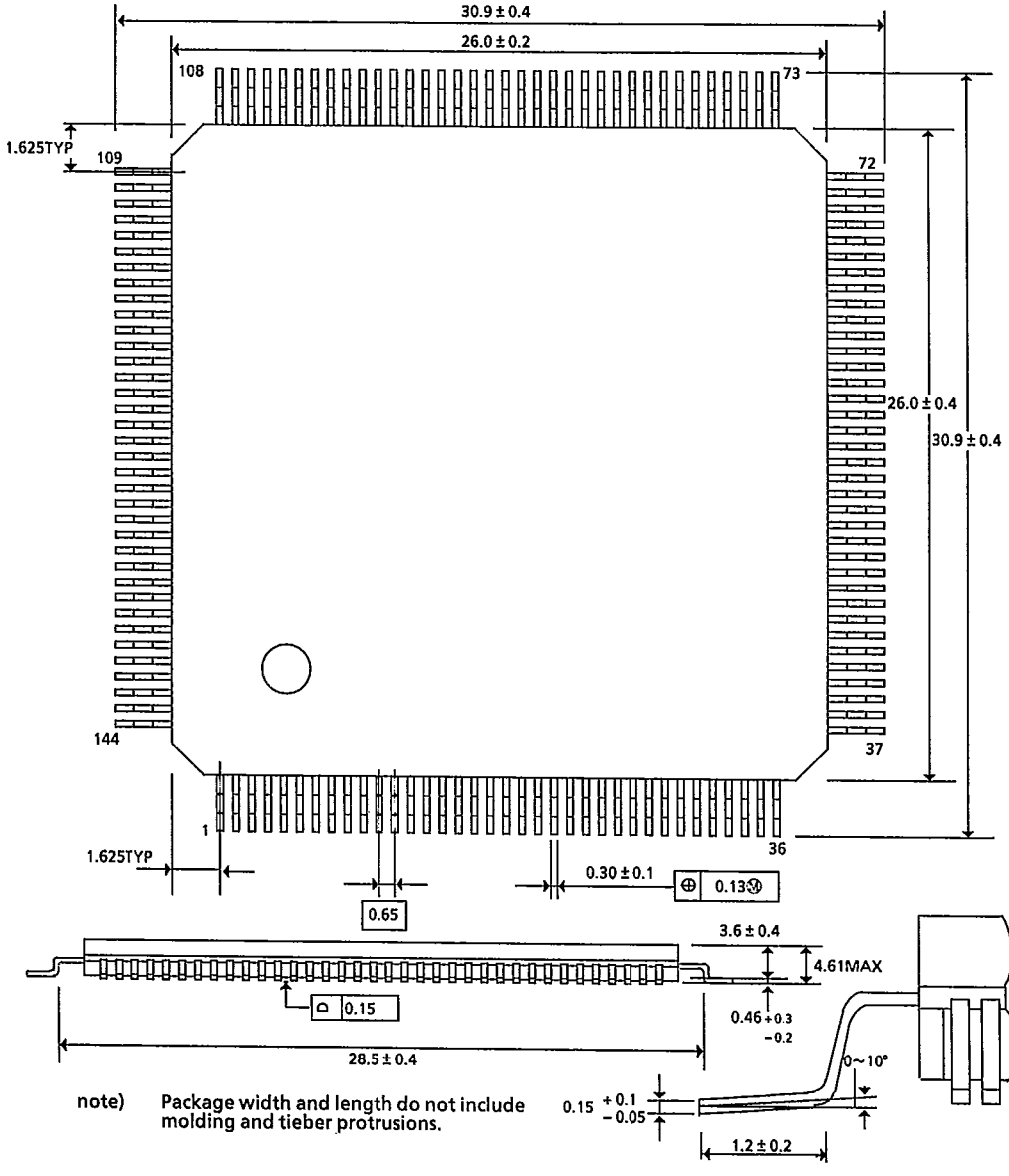


7. PACKAGE DIMENSION

7.1 144 PIN CERAMIC QUAD FLAT PACKAGE

QFP144-G-2626

unit : mm

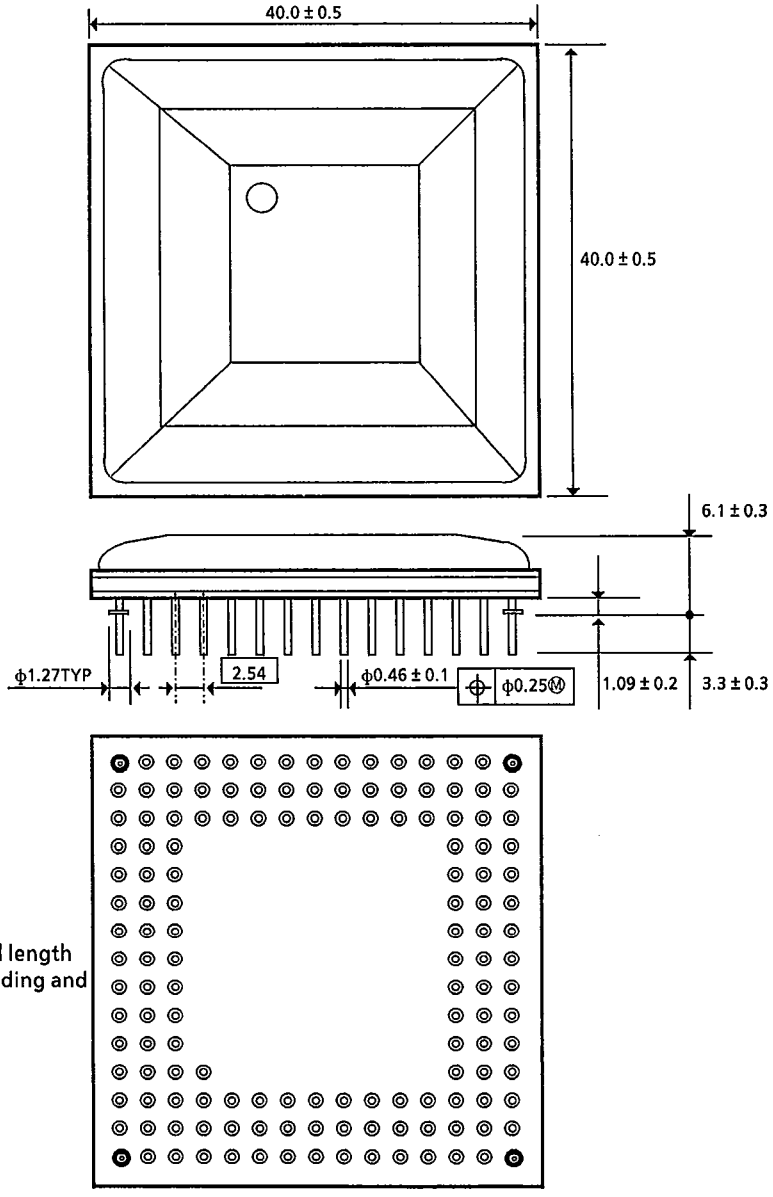


note) Package width and length do not include molding and tieber protrusions.

7.2 144 PIN METAL PGA PACKAGE

PGA144--M-S15U

Unit : mm



note) Package width and length do not include molding and tieber protrusions.