Open Graphics Programming Manual

Chrome9 HCM Graphics Processor

VX855 and VX875

Part I: Graphics Core / 2D

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1.0	7/29/09	Initial public release	LW

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INTRODUCTION

This document contains detailed graphics registers descriptions and other general information for the Chrome9 HCM graphic engine. The graphics registers for the Chrome9 HCM main features and its underlying subsystems are described explicitly in the following chapters.

About This Programming Guide

The programming manual is organized into 2 volumes (Part I & Part II). A brief description of each chapter is given below:

Part I:

Introduction.

An overview of the Chrome9 HCM design features is given in this chapter, along with block diagram and reference list.

Register Overview

Register specifications for register addressing and I/O space division are shown in this chapter.

PCI Interface Register Descriptions

PCI interface summary table and detailed register descriptions are presented in this chapter.

VGA I/O Register Descriptions

This chapter provides detailed VGA-related register summary and descriptions. The various video modes support by the Chrome9 HCM controller are also included in the configuration section.

2D Engine Register Descriptions

In this chapter provides detailed 2D Engine register summary and descriptions.

DMA Register Descriptions

This chapter provides detailed DMA register summary and descriptions.

CBU Rotation Register Descriptions

This chapter provides detailed CBU rotation register summary and descriptions.

LVDS Register Descriptions

This chapter provides detailed LVDS register summary and descriptions.

Part II:

Video Display Engine Register Descriptions

This chapter provides detailed video display engine register summary and descriptions.

Video Capture Engine Register Descriptions

This chapter provides detailed video capture engine register summary and descriptions.

HQV Register Descriptions

This chapter provides detailed HQV register summary and descriptions.

Command Regulator (CR) Register Descriptions

This chapter provides detailed CR register summary and descriptions.

3D Engine Register Descriptions

This chapter provides detailed 3D Engine register summary and descriptions.

Supporting Products and Features

This document includes all the GFX registers for VIA VX855 and VX875. Please refer to Table 1 for the specification differences of VX855 and VX875 products.

This chip integrates functional modules of the traditional North Bridge and South Bridge chips, plus 3D/2D and Video Processors, Video Decoding Accelerator and controller for external display interface. The register set is partitioned into three blocks: North Module, South Module and Graphics and Video Module; of which, North Module and South Module registers are described in this **System Programming Manual** while graphics and video registers are described in the **Graphics Programming Guide**.

Table 1. VX855 / VX875 Series Comparison Table

Product Model	VX855	VX875
FSB Speed (MHz)	400-800	400-533
Memory Type	DDR2-800 1.5V / 1.8V	DDR2-667 1.5V / 1.8V
Snapshot Memory	Yes	Yes
Core Voltage	1.2V	1.0V
Package Dimension	27x27mm FCBGA 906 balls	21x21mm FCBGA 945 balls

System Block Diagram

The block diagram for the Chrome9 HCM is shown Figure 1.

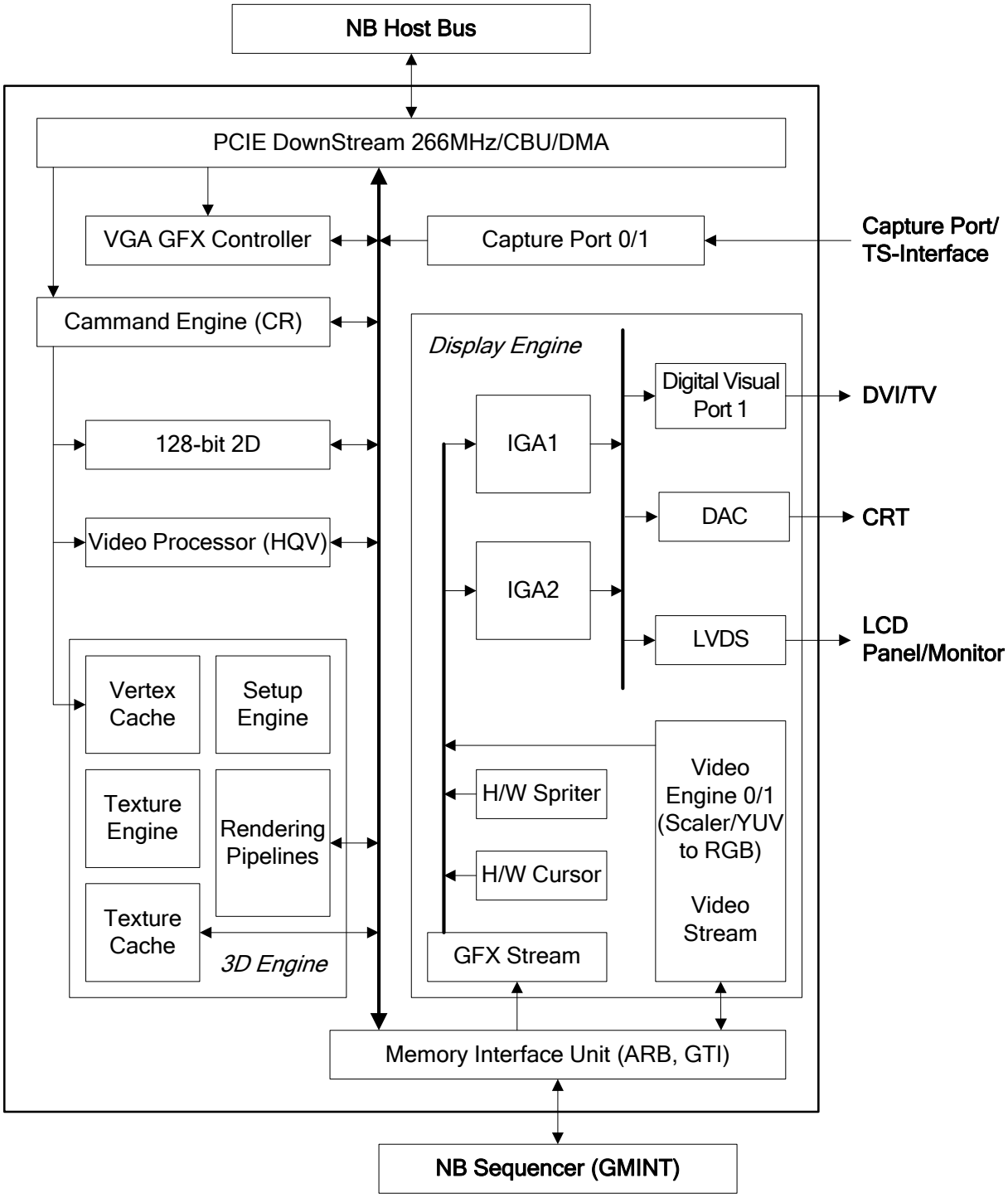


Figure 1. The Chrome9 HCM Block Diagram

REGISTER OVERVIEW

For the register tables used in following chapters, column “Default” indicates the default value of register bit, while column “Attribute” indicates access type of register bit(s).

Abbreviation

Attribute Definitions

Basic Attributes: *indicate common read-write operations.*

RO:	Read Only.
WO:	Write Only. (register value can not be read by the software)
RW:	Read / Write.
RW1:	Write Once then Read Only after that.
RW1C:	Read / Write of “1” clears bit to zero.

Sticky Attributes**:** adding an “S” in tail to indicate a sticky register, which means that register will not be set or altered by hot reset.

ROS:	Sticky-Read-Only.
WOS:	Sticky-Write-Only.
RWS:	Sticky-Read/Write.
RW1S:	Sticky-Write-Once.
RW1CS:	Sticky-Write-1-to-Clear.

Default Value Definitions

Dip: means the default value is set by dip switch or strapping.
HwInit: Hardware initialized; bit default value is set by hardware.
ROMSIP: The default will be overwritten by the value defined in ROMSIP after system reset.

I/O Address Space

The I/O space of the Chrome9 HCM processor is divided into the following subspaces for various functions of the processor:

- PCI Interface: PCI/AGP/Power Management configuration space
- VGA space
- Extended I/O space
- Secondary Display Engine / LCD Display
- 2D engine space
- 3D engine space
- Video Playback / Blending / Video Capture / HQV engines space
- DMA engine space
- CBU engine space

The table below lists the various I/O space categories and their corresponding I/O addresses for the Chrome9 HCM processor. Please note that in the monochrome mode, the "X" contained within the I/O addresses stands for **"B",** and in the color mode the "X" stands for **"D".**

Table 2. Chrome9 HCM Processor I/O Space

Categories	I/O Address
PCI Interface	PCI Configuration Space
VGA Space	Standard VGA Space
Extended I/O Space	3C5.10 ~ 3C5.FF / 3CF.20 ~ 3CF.2F / 3X5.30 ~ 3X5.4F
Secondary Display Engine / LCD Display	3X5.50 ~ 3X5.FC

Memory Address Space

There are two memory spaces implemented in the Chrome9 HCM graphics processor:

1. Starting from PCI Memory Base 0, **MB0**, there is a **512MB** memory space reserved as the graphics and video playback buffer.(Named as **S.L.** – System Local Frame Buffer)
2. Starting from PCI Memory Base 1**, MB1**, there is a **16MB** memory space reserved for **memory-mapped I/O**, 2D Host BitBLT space and burst **command area**.

MB0 is declared in the register with offset address 10h~13h in the PCI configuration space.

MB1 is declared in the register with offset address 14h~17h in the PCI configuration space.

Memory Mapped I/O Register Address Spaces

Table 3. Memory Mapped I/O Address Space Partition Table

Memory Range (Note)	Usage
0 ~ 2M-1:	
0x00000000 ~ 0x000001FF	2D Engine Register Space
0x00000200 ~ 0x000003FF	Video Related Engines Register Space 1
0x00000400 ~ 0x000007FF	3D Engine Register Space
0x00000800 ~ 0x00000BFF	Burst Command Area
0x00000C00 ~ 0x00000DFF	Reserved
0x00000E00 ~ 0x00000FFF	DMA(AGP) Register Space 1
0x00001200 ~ 0x000013FF	Video Related Engines Register Space 2
0x00001C00 ~ 0x00001DFF	Reserved
0x00001E00 ~ 0x00001FFF	CBU Rotate Related Register Space
0x00002200 ~ 0x000023FF	Extended Video Engines Register Space 1
0x00002E00 ~ 0x00002FFF	DMA(AGP) Register Space 2
0x00003200 ~ 0x000033FF	Extended Video Engines Register Space 2
0x000083CX ~ 0x000083DX	VGA memory mapped IO Space
0x0000C000 ~ 0x0000C1FF	Reserved
2M ~ 4M-1	**2D Host BitBLT Space**
4M ~ 8M-1	**Burst Command Area**
8M ~ 16M-1	**Reserved**

Notes These addresses are offset address from MB1.

PCI INTERFACE

This section provides a complete PCI register overview. All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism through I/O registers CF8 / CFC with bus number 0, device number 1 and function number 0.

PCI Commands

The Chrome9 HCM processor complies with the PCI bus interface protocol, Rev. 2.2. The design clock rate is 66 MHz and both of master and slave modes are supported. The table below shows the PCI command support of the Chrome9 HCM graphics processor.

Table 4. PCI Command

Command Code	Command
0000	**Interrupt Acknowledge**
0001	**Special**
0010	I/O Read
0011	I/O Write
0100	**Reserved**
0101	**Reserved**
0110	Memory Read
0111	Memory Write
1000	**Reserved**
1001	**Reserved**
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple; treated as 0110 memory read
1101	**Dual Address**
1110	Memory Read Line; treated as 0110 memory read
1111	Memory Write and Invalid; treated as 0111 memory write

Note: The command codes in **bold** are not supported in Chrome9 HCM.

PCI Configuration Register Summary Table

The following table summarizes PCI configuration registers of Chrome9 HCM processor. This table also documents the power-on default value ("Default") and attribute ("Attribute") for each register. Access type definitions used are RW (Read/Write), RO (Read-Only), WO (Write-Only) and RW1C (Read / Write of "1" clears bit to zero). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RW1C may have some read-only or read write bits (see individual register descriptions for details).

Table 5. PCI Configuration Registers

Offset Address (Hex)	Normal PCI Configuration Area	Default Value (Hex)	Attribute
01-00	VIA Technology ID	1106h	RO
03-02	Device ID	5122h	RO
05-04	PCI Command	0000h	RW
07-06	PCI Status	0010h	RW
08	Revision ID	00h	RO
0B-09	Class Code	03 0000h	RO
13-10	Memory Base 0 Address (S.L.)	0000 0008h	RW
17-14	Memory Base 1 Address (MMIO)	0000 0000h	RW
2D-2C	Subsystem Vendor ID	1106h	RO
2F-2E	Subsystem ID	5122h	RO
33-30	ROM Base Address	0000 0000h	RW
34	Capabilities Pointer	60h	RO
3C	Interrupt Line	00h	RW
3D	Interrupt Pin	01h	RO

Offset Address	Power Management Configuration Area	Default Value	Attribute
60	Capability ID (01h)	01h	RO
61	Next Item Pointer	90h	RO
63-62	Power Management Capability	0622h	RO
65-64	Power Management Control / Status	0000h	RO / RW

Offset Address	MSI Configuration Area	Default Value	Attribute
90	MSI Capability ID	05h	RO
91	Next Cap Pointer	00h	RO
93-92	Message Control	0000h	RW
9B~94	Message Address	0	RW
9D~9C	Message Data	0000h	RW

Offset Address	VIA GFX Configuration Area	Default Value	Attribute
B0	Memory Base Control	00h	RW
B2	Memory Base 0 Size (S.L.)	00h	RW

PCI REGISTER DESCRIPTIONS

PCI Configuration Registers (AGP GFX)

Normal PCI Configuration Area (00-3Dh)

Offset Address: 01-00h (GFX-PCI)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID**

Offset Address: 03-02h (GFX-PCI)

Device ID **Default Value: 5122h**

Bit	Attribute	Default	Description
15:0	RO	5122h	**Device ID**

Offset Address: 05-04h (GFX-PCI)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** 0: Enable interrupt 1: Disable interrupt
9	RW	0	**Fast Back-to-Back Enable** 0: Disable 1: Enable
8	RW	0	**SERR# Enable** 0: Disable 1: Enable
7	RW	0	**Wait Cycle Control** 0: Disable 1: Enable
6	RW	0	**Parity Error Response** 0: Disable 1: Enable
5	RW	0	**VGA Palette Snoop** 0: Disable 1: Enable
4	RW	0	**Memory Write and Invalidate Enable** 0: Disable 1: Enable
3	RW	0	**Special Cycle** 0: Disable 1: Enable
2	RW	0	**Bus Master** 0: Disable 1: Enable
1	RW	0	**Memory Space** 0: Disable 1: Enable
0	RW	0	**IO Space** 0: Disable 1: Enable

Offset Address: 07-06h (GFX-PCI)

PCI Status **Default Value: 0010h**

Bit	Attribut	Default	Description
15	RW1C	0	**Detected Parity Error** Assert 1 whenever a parity error is detected.
14	RO	0	**Signaled System Error**
13	RW1C	0	**Received Master Abort** Assert 0 when a master abort is detected.
12	RW1C	0	**Received Target Abort** Assert 0 when a target abort is detected.
11	RW	0	**Signaled Target Abort**
10:9	RO	00b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error**
7	RO	0	**Fast Back-to-back Capable**
6	RO	0	**Reserved**
5	RO	0	**66MHz Capable**
4	RO	1b	**Capabilities List** 1 indicates presence of the extended capability list.
3	RO	0	**Interrupt Status** 1: Assert an interrupt at the INTA#.
2:0	RO	0	**Reserved**

Offset Address: 08h (GFX-PCI)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-09h (GFX-PCI)

Class Code **Default Value: 03 0000h**

Bit	Attribute	Default	Description
23:0	RO	03 0000h	**Class Code**

Offset Address: 0C-0Fh – Reserved

Offset Address: 13-10h (GFX-PCI)

Memory Base 0 Address (S.L.) **Default Value: 0000 0008h**

Bit	Attribute	Default	Description
31:0	RW	0000 0008h	**Memory Base 0 Address (S.L.)**

Offset Address: 17-14h (GFX-PCI)

Memory Base 1 Address (MB1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0000 0000h	**Memory Base 1 Address (For MMIO Registers)**

Offset Address: 18-2Bh – Reserved

Offset Address: 2D-2Ch (GFX-PCI)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (GFX-PCI)
Subsystem ID **Default Value: 5122h**

Bit	Attribute	Default	Description
15:0	RO	5122h	**Subsystem ID**

Offset Address: 33-30h (GFX-PCI)
ROM Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**ROM Base Address**

Offset Address: 34h (GFX-PCI)
Capabilities Pointer **Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RO	60h	**Capabilities Pointer**

Offset Address: 35-3Bh – Reserved

Offset Address: 3Ch (GFX-PCI)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line**

Offset Address: 3Dh (GFX-PCI)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin**

Offset Address: 3E-5Fh – Reserved

Power Management Configuration Area (60-65h)

Offset Address: 60h (GFX-PCI)

Capability ID (01h) **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Capability ID**

Offset Address: 61h (GFX-PCI)

Next Item Pointer **Default Value: 90h**

Bit	Attribute	Default	Description
7:0	RO	90h	**Next Item Pointer** Points to MSI capability list.

Offset Address: 63-62h (GFX-PCI)

Power Management Capability **Default Value: 0622h**

Bit	Attribute	Default	Description
15:11	RO	0	**Power Management Event (PME) Support**
10	RO	1b	**D2 Support**
9	RO	1b	**D1 Support**
8:6	RO	0	**3.3 Vaux Auxiliary Current**
5	RO	1b	**DSI Device Specific Initialization**
4	RO	0	**Reserved**
3	RO	0	**Power Management Event (PME) Clock**
2:0	RO	010b	**Version** Complies with version 1.1

Offset Address: 65-64h (GFX-PCI)

Power Management Control / Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Power Management Event (PME) Status**
14:13	RO	0	**Data Scale**
12:10	RO	0	**Reserved**
9	RO	0	**D1 Select**
8	RO	0	**PME Enable** 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** 00: D0 State 01: D1 State 10: D2 State 11: D3 State

Offset Address: 66-8Fh – Reserved

MSI Configuration Area (90-9Dh)

Offset Address: 91-90h (GFX-PCI)

MSI Capability List Register **Default Value: 0005h**

Bit	Attribute	Default	Description
15:8	RO	0	**Next Capability Pointer**
7:0	RO	05h	**Capability ID**

Offset Address: 93-92h (GFX-PCI)

Message Control Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6:4	RW	000b	**Multiple Message Enable**
3:1	RW	000b	**Multiple Message Capable** A message request
0	RW	0	**MSI Enable** 0: Disable 1: Enable

Offset Address: 9B-94h (GFX-PCI)

Message Address Register **Default Value: 0**

Bit	Attribute	Default	Description
63:2	RW	0	**Message Address** System specified data.
1:0	RO	0	**Reserved**

Offset Address: 9D-9Ch (GFX-PCI)

Message Control Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** System specified data.

Offset Address: 9E-AFh – Reserved

VIA GFX Configuration Area (B0-B2h)

Offset Address: B0h (GFX-PCI)

Memory Base Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Reserved**
4	RO	0	**Reserved**
3	RW	0	**Unlock**
2	RW	0	**S.L. Disable** 0: Enable S.L. 1: Disable S.L.
1	RW	0	**L.L. Disable** 0: Reserved (this chip has no L.L.) 1: Disable L.L.
0	RW	0	**VGA Memory Selection** 0: Reserved (VGA in L.L.) 1: VGA in S.L.

Offset Address: B1h – Reserved

Offset Address: B2h (GFX-PCI)

Memory Base 0 Size (S.L.) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:0	RW	000 0000b	000 0000: 512MB 100 0000: 256MB 110 0000: 128MB 111 0000: 64MB 111 1000: 32MB 111 1100: 16MB 111 1110: 8MB 111 1111: 4MB Others: Reserved

Offset Address: B3-FFh – Reserved

VGA REGISTERS DESCRIPTIONS

This chapter provides VGA I/O register summary table, extended IO register summary table, secondary display IO register summary table and their detailed register descriptions are followed in the subsequent sections.

VGA I/O Registers

These VGA register tables document the I/O port, I/O index, register function and register attribute for each register.

Table 6. VGA I/O Registers

I/O Port (hex)	I/O Index (hex)	Attribute Control Register	Attribute
3C0	-	Address	RW
3C1	00 – 0F	Palette	RW
3C1	10	Mode Control	RW
3C1	11	Overscan Color	RW
3C1	12	Color Plane Enable	RW
3C1	13	Horizontal Pixel Panning	RW
3C1	14	Color Select	RW

I/O Port	I/O Index	General Register	Attribute
3C2	-	Miscellaneous Output	WO
3CC	-	Miscellaneous Output	RO
3C2	-	Input Status 0	RO
3XA	-	Input Status 1	RO
3C3	-	Video Subsystem Enable	RW
46E8	-	Video Adapter Enable	RW

I/O Port	I/O Index	Sequencer Register	Attribute
3C4	-	Address	RW
3C5	00	Reset	RW
3C5	01	Clocking Mode	RW
3C5	02	Map Mask	RW
3C5	03	Character Map Select	RW
3C5	04	Memory Mode	RW

I/O Port	I/O Index	Graphic Controller Register	Attribute
3CE	-	Address	RW
3CF	00	Set / Reset	RW
3CF	01	Enable Set / Reset	RW
3CF	02	Color Compare	RW
3CF	03	Data Rotate	RW
3CF	04	Read Map Select	RW
3CF	05	Mode	RW
3CF	06	Miscellaneous	RW
3CF	07	Color Don’t Care	RW
3CF	08	Bit Mask	RW

I/O Port	I/O Index	CRTC Controller Register	Attribute
3X4	-	Address	RW
3X5	00	Horizontal Total	RW
3X5	01	Horizontal Dipslay End	RW
3X5	02	Start Horizontal Blank	RW
3X5	03	End Horizontal Blank	RW
3X5	04	Start Horizontal Retrace	RW
3X5	05	End Horizontal Retrace	RW
3X5	06	Vertical Total	RW
3X5	07	Overflow	RW
3X5	08	Preset Row Scan	RW
3X5	09	Max Scan Line	RW
3X5	0A	Cursor Start	RW
3X5	0B	Cursor End	RW
3X5	0C	Start Address High	RW
3X5	0D	Start Address Low	RW
3X5	0E	Cursor Location High	RW
3X5	0F	Cursor Location Low	RW
3X5	10	Vertical Retrace Start	RW
3X5	11	Vertical Retrace End	RW
3X5	12	Vertical Display End	RW
3X5	13	Offset	RW
3X5	14	Underline Location	RW
3X5	15	Start Vertical Blank	RW
3X5	16	End Vertical Blank	RW
3X5	17	CRTC Mode Control	RW
3X5	18	Line Compare	RW

Table 7. Extended I/O Registers

I/O Port	I/O Index	Sequencer Extended Register	Attribute
3C5	10	Extended Register Unlock	RW
3C5	11	Configuration Register 0	RO
3C5	12	Configuration Register 1	RO
3C5	13	Configuration Register 2	RO
3C5	14	Frame Buffer Size Control	RO
3C5	15	Display Mode Control	RW
3C5	16	Display FIFO Threshold Control	RW
3C5	17	Display FIFO Control	RW
3C5	18	Display Arbiter Control 0	RW
3C5	19	Power Management Control 0	RW
3C5	1A	PCI Bus Control	RW
3C5	1B	Power Management Control 1	RW
3C5	1C	Horizontal Display Fetch Count Data	RW
3C5	1D	Horizontal Display Fetch Count Control	RW
3C5	1E	Power Management Control 2	RW
3C5	20	Typical Arbiter Control 0	RW
3C5	21	Typical Arbiter Control 1	RW
3C5	22	Display Arbiter Control 1	RW
3C5	26	IIC Serial Port Control 0	RW
3C5	2A	Power Management Control 3	RW
3C5	2B	DVI and LVDS Interrupt Control	RW
3C5	2C	General Purpose I/O Port	RW
3C5	2D	Power Management Control 4	RW
3C5	2E	Power Management Control 5	RW
3C5	31	IIC Serial Port Control 1	RW
3C5	34-32	Reserved	RO
3C5	36-35	Subsystem Vender ID	RW
3C5	38-37	Subsystem ID	RW
3C5	3A-39	BIOS Reserved Register 1-0	RW
3C5	3B	Reserved	RW
3C5	3C	Miscellaneous	RW
3C5	3D	General Purpose I/O Port	RW
3C5	3E	Miscellaneous Register for AGP Mux	RW
3C5	3F	Power Management Control 6	RW
3C5	40	PLL Control	RW
3C5	41	Typical Arbiter Control 1	RW
3C5	42	Typical Arbiter Control 2	RW
3C5	43	Graphics Bonding Option	RO

I/O Port	I/O Index	Clock Synthesizer Register	Attribute
3C5	44	VCK Clock Synthesizer Value 0	RW
3C5	45	VCK Clock Synthesizer Value 1	RW
3C5	46	VCK Clock Synthesizer Value 2	RW
3C5	47	ECK Clock Synthesizer Value 0	RW
3C5	48	ECK Clock Synthesizer Value 1	RW
3C5	49	ECK Clock Synthesizer Value 2	RW
3C5	4A	Secondary Display (LCDCK) Clock Synthesizer Value 0	RW
3C5	4B	Secondary Display (LCDCK) Clock Synthesizer Value 1	RW
3C5	4C	Secondary Display (LCDCK) Clock Synthesizer Value 2	RW
3C5	4D	Preemptive Arbiter Control	RW
3C5	4E	Software Reset Control	RW
3C5	4F	CR Gating Clock Control	RW
3C5	50	AGP Control Register	RW
3C5	51	Display FIFO Control 1	RW
3C5	52	Integrated TV Shadow Register Control	RW
3C5	53	DAC Sense Control Register 1	RW
3C5	54	DAC Sense Control Register 2	RW
3C5	55	DAC Sense Control Register 3	RW
3C5	56	DAC Sense Control Register 4	RW
3C5	57	Display FIFO Control 2	RW
3C5	58	GFX Power Control Register 1	RW
3C5	59	GFX Power Control Register 2	RW
3C5	5A	PCI Bus Control 2	RW
3C5	5B	Device Used Status 0	RO
3C5	5C	Device Used Status 1	RO
3C5	5D	Timer Control Register	RW
3C5	5E	DAC Control Register 2	RW
3C5	60	I2C Mode Control	RW
3C5	61	I2C Host Address	RW
3C5	62	I2C Host Data	RW
3C5	63	I2C Host Control	RW
3C5	64	I2C Status	RW
3C5	65	Power Management Control 7	RW
3C5	66	GTI Control 0	RW
3C5	67	GTI Control 1	RW
3C5	68	GTI Control 2	RW
3C5	69	GTI Control 3	RW
3C5	6A	GTI Control 4	RW
3C5	6B	GTI Control 5	RW
3C5	6C	GTI Control 6	RW
3C5	6D	GTI Control 7	RW
3C5	6E	GTI Control 8	RW
3C5	6F	GTI Control 9	RW
3C5	70	GARB Control 0	RW
3C5	71	Typical Arbiter Control 2	RW
3C5	72	Typical Arbiter Control 3	RW
3C5	73	Typical Arbiter Control 4	RW
3C5	74	Typical Arbiter Control 5	RW
3C5	75	Typical Arbiter Control 6	RW
3C5	76	Backlight Control 1	RW
3C5	77	Backlight Control 2	RW
3C5	78	Backlight Control 3	RW

I/O Port	I/O Index	Clock Synthesizer Register	Attribute
3C5	79	GTI Control 10	RW
3C5	7A	GTI Control 11	RW
3C5	7B	GTI Control 12	RW
3C5	7C	GTI Control 13	RW
3C5	7D	Transmitter Power Control 0	RW
3C5	7E ~ A7	Reserved	RO
3C5	A8	V1 Power Mode Control 0	RW
3C5	A9	V1 Power Mode Control 1	RW
3C5	AA	V1 Power Mode Control 2	RW
3C5	AB	V1 Power Mode Control 3	RW
3C5	AC	V1 Power Mode Control 4	RW
3C5	AD	V1 Power Mode Control 5	RW
3C5	AE	V1 Power Mode Control 6	RW
3C5	AF	V1 Power Mode Control 7	RW

I/O Port	I/O Index	Graphics Controller Extended Register	Attribute
3CF	20	Offset Register Control	RW
3CF	21	Offset Register A	RW
3CF	22	Offset Register B	RW

I/O Port	I/O Index	CRT Controller Extended Register	Attribute
3X5	30	Display Fetch Blocking Control	RW
3X5	31	Half Line Position	RW
3X5	32	Mode Control	RW
3X5	33	HSYNC Adjuster	RW
3X5	34	Starting Address Overflow	RW
3X5	35	Extended Overflow	RW
3X5	36	Power Management Control 8 (Monitor Control)	RW
3X5	37	DAC Control Register	RW
3X5	38	Signature Data B0	RW
3X5	39	Signature Data B1	RW
3X5	3A	Signature Data B2	RW
3C5	3F-3B	Scratch Pad Register 6-2	RW
3X5	40	Test Mode Control 0	RW
3X5	43	IGA1 Display Control	RW
3X5	45	Power Now Indicator Control 3	RW
3X5	46	Test Mode Control 1	RW
3X5	47	Test Mode Control 2	RW
3X5	48	Starting Address Overflow	RW
3X5	49-4F	Reserved	RW

Note: In monochrome mode, the “X” in the above table stands for **“B”**
In color mode, the “X” in the above table stands for **“D”.**

Table 8. Secondary Display I/O Registers

I/O Port	I/O Index	Sequencer Extended Registers	Attribute
3X5	50	Second CRTC Horizontal Total Period	RW
3X5	51	Second CRTC Horizontal Active Data Period	RW
3X5	52	Second CRTC Horizontal Blanking Start	RW
3X5	53	Second CRTC Horizontal Blanking End	RW
3X5	54	Second CRTC Horizontal Blanking Overflow	RW
3X5	55	Second CRTC Horizontal Period Overflow	RW
3X5	56	Second CRTC Horizontal Retrace Start	RW
3X5	57	Second CRTC Horizontal Retrace End	RW
3X5	58	Second CRTC Vertical Total Period	RW
3X5	59	Second CRTC Vertical Active Data Period	RW
3X5	5A	Second CRTC Vertical Blanking Start	RW
3X5	5B	Second CRTC Vertical Blanking End	RW
3X5	5C	Second CRTC Vertical Blanking Overflow	RW
3X5	5D	Second CRTC Vertical Period Overflow	RW
3X5	5E	Second CRTC Vertical Retrace Start	RW
3X5	5F	Second CRTC Vertical Retrace End	RW
3X5	60	Second CRTC Vertical Status 1	RO
3X5	61	Second CRTC Vertical Status 2	RO
3X5	62	Second Display Starting Address Low	RW
3X5	63	Second Display Starting Address Middle	RW
3X5	64	Second Display Starting Address High	RW
3X5	65	Second Display Horizontal Quadword Count Data	RW
3X5	66	Second Display Horizontal Offset	RW
3X5	67	Second Display Color Depth and Horizontal Overflow	RW
3X5	68	Second Display Queue Depth and Read Threshold	RW
3X5	69	Second Display Interrupt Enable and Status	RW
3X5	6A	Second Display Channel and LCD Enable	RW
3X5	6B	Channel 1 and 2 Clock Mode Selection	RW
3X5	6C	TV Clock Control	RW
3X5	6D	Horizontal Total Shadow	RW
3X5	6E	End Horizontal Blanking Shadow	RW
3X5	6F	Vertical Total Shadow	RW
3X5	70	Vertical Display Enable End Shadow	RW
3X5	71	Vertical Display Overflow Shadow	RW
3X5	72	Start Vertical Blank Shadow	RW
3X5	73	End Vertical Blank Shadow	RW
3X5	74	Vertical Blank Overflow Shadow	RW
3X5	75	Vertical Retrace Start Shadow	RW
3X5	76	Vertical Retrace End Shadow	RW
3X5	77	LCD Horizontal Scaling Factor	RW
3X5	78	LCD Vertical Scaling Factor	RW
3X5	79	LCD Scaling Control	RW
3X5	7A	LCD Scaling Parameter 1	RW
3X5	7B	LCD Scaling Parameter 2	RW
3X5	7C	LCD Scaling Parameter 3	RW
3X5	7D	LCD Scaling Parameter 4	RW
3X5	7E	LCD Scaling Parameter 5	RW
3X5	7F	LCD Scaling Parameter 6	RW
3X5	80	LCD Scaling Parameter 7	RW
3X5	81	LCD Scaling Parameter 8	RW
3X5	82	LCD Scaling Parameter 9	RW

I/O Port	I/O Index	Sequencer Extended Registers	Attribute
3X5	83	LCD Scaling Parameter 10	RW
3X5	84	LCD Scaling Parameter 11	RW
3X5	85	LCD Scaling Parameter 12	RW
3X5	86	LCD Scaling Parameter 13	RW
3X5	87	LCD Scaling Parameter 14	RW
3X5	88	LCD Panel Type (See LVDS/DVI Chapter)	RW
3X5	89	Reserved	RO
3X5	8A	LCD Timing Control 1	RW
3X5	8B	LCD Power Sequence Control 0	RW
3X5	8C	LCD Power Sequence Control 1	RW
3X5	8D	LCD Power Sequence Control 2	RW
3X5	8E	LCD Power Sequence Control 3	RW
3X5	8F	LCD Power Sequence Control 4	RW
3X5	90	LCD Power Sequence Control 5	RW
3X5	91	Software Control Power Sequence	RW
3X5	92	Read Threshold 2	RW
3X5	93	Reserved	RO
3X5	94	Expire Number and Display Queue Extend Bit	RW
3X5	95	Extend Threshold Bit	RW
3X5	97	LVDS Channel 2 Function Select 0 (See LVDS/DVI Chapter)	RW
3X5	98	LVDS Channel 2 Function Select 1 (See LVDS/DVI Chapter)	RW
3X5	99	LVDS Channel 1 Function Select 0 (See LVDS/DVI Chapter)	RW
3X5	9A	Reserved	RO
3X5	9B	Digital Video Port 1 Function Select 0	RW
3X5	9C	Reserved	RO
3X5	9D	Power Now Control 1	RW
3X5	9E	Power Now Control 2	RW
3X5	9F	Power Now Control 3	RW
3X5	A0	Horizontal Scaling Initial Value	RW
3X5	A1	Vertical Scaling Initial Value	RW
3X5	A2	Horizontal and Vertical Scaling Enable Bit	RW
3X5	A3	Second Display Starting Address Extended	RW
3X5	A4	Reserved	RO
3X5	A5	Second LCD Vertical Scaling Factor	RW
3X5	A6	Second LCD Vertical Scaling Factor	RW
3X5	A7	Expected IGA1 Vertical Display End	RW
3X5	A8	Expected IGA1 Vertical Display End	RW
3X5	A9	Hardware Gamma Control Register	RW
3X5	AA	FIFO Depth & Threshold Overflow bit	RW
3X5	AB	IGA2 Interlace Half Line Register	RW
3X5	AC	IGA2 Interlace Half Line Register	RW
3X5	AF	P-Arbiter Write Expired Number Register	RW
3X5	B0 ~ CF	Reserved	RO
3X5	D0	LVDS PLL Control Register (See LVDS/DVI Chapter)	RW
3X5	D1	DVI PLL Control Register (See LVDS/DVI Chapter)	RW
3X5	D2	LVDS / DVI Control Register (See LVDS/DVI Chapter)	RW
3X5	D3	Second Power sequence Control Register 0 (See LVDS/DVI Chapter)	RW

I/O Port	I/O Index	Sequencer Extended Registers	Attribute
3X5	D4	Second Power sequence Control Register 1 (See LVDS/DVI Chapter)	RW
3X5	D5	LVDS Setting Mode Control Register (See LVDS/DVI Chapter)	RW
3X5	D6	DCVI Control Register 0	RW
3X5	D7	DCVI Control Register 1	RW
3X5	D8	PLL control register	RW
3X5	D9	Scaling Down Source Data Offset Control	RW
3X5	DA	Scaling Down Source Data Offset Control	RW
3X5	DB	Scaling Down Source Data Offset Control	RW
3X5	DC	Scaling Down Horizontal Scale Control	RW
3X5	DD	Scaling Down Horizontal Scale Control	RW
3X5	DE	Scaling Down Vertical Scale Control	RW
3X5	DF	Scaling Down Vertical Scale Control	RW
3X5	E0	Scaling Down Destination Frame Buffer Starting Address 0	RW
3X5	E1	Scaling Down Destination Frame Buffer Starting Address 0	RW
3X5	E2	Scaling Down Destination Frame Buffer Starting Address 0	RW
3X5	E3	Scaling Down Destination Frame Buffer Starting Address 0	RW
3X5	E4	Scaling Down SW Source Frame Buffer Stride	RW
3X5	E5	Scaling Down Destination Frame Buffer Starting Address 1	RW
3X5	E6	Scaling Down Destination Frame Buffer Starting Address 1	RW
3X5	E7	Scaling Down Destination Frame Buffer Starting Address 1	RW
3X5	E8	Scaling Down Destination Frame Buffer Starting Address 1	RW
3X5	E9	Scaling Down Destination Frame Buffer Starting Address 2	RW
3X5	EA	Scaling Down Destination Frame Buffer Starting Address 2	RW
3X5	EB	Scaling Down Destination Frame Buffer Starting Address 2	RW
3X5	EC	IGA1 Down Scaling Destination Control Register	RW
3X5	F0	SNAPSHOP Mode – Starting Address of Display Data	RW
3X5	F1	SNAPSHOP Mode – Starting Address of Display Data	RW
3X5	F2	SNAPSHOP Mode – Starting Address of Display Data	RW
3X5	F3	SNAPSHOP Mode Control	RW
3X5	F4	SNAPSHOP Mode Control	RW
3X5	F5	SNAPSHOP Mode Control	RW
3X5	F6	SNAPSHOP Mode Control	RW
3X5	F7	Internal Spread Spectrum Control CH0	RW
3X5	F8	Reserved (Internal SSCG CH1 for dual channel)	RW
3X5	F9	V1 Power Control 0	RW
3X5	FA	V1 Power Control 1	RW
3X5	FB	IGA2 Interlace Vsync Timing register	RW
3X5	FC	IGA2 Interlace Vsync Timing register	RW

Extended I/O Space Register Descriptions

Sequencer Extended Registers

IO Port / Index: 3C5.10
Extended Register Unlock **Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	1b	**Unlock Accessing of I/O Space** 0: Disable 1: Enable

IO Port / Index: 3C5.11
Configuration Register 0 **Default Value: 58h**

Bit	Attribute	Default	Description
7	RO	0	**VGA Port Select** 0: 3C3 1: 46E8
6	RO	1b	**PC AT Space Disable** 0: Disable VGA & memory space: A0000h-BFFFFh 1: IBM VGA standard space
5	RO	0	**Reserved.** Always reads 0.
4:3	RO	11b	**Bus Type** 00: Reserved 01: Reserved 10: Reserved 11: 1x, 2x, 4x (8x) side band AGP Bus
2:0	RO	0	**Reserved**

IO Port / Index: 3C5.12
Configuration Register 1 (3C5.5A[0]=0) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RO	0	**Panel Type ID (Reflects Strapping from Signal VCPD[3:0])** 0~8: VIA Generic Type 9~F: Customers' Request

IO Port / Index: 3C5.12
Shadow Configuration Register 1 (3C5.5A[0]=1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0000b	**Video Capture Port 1 Type Select (Reflects Strapping from Signals DVP1D[7:4])** 0000: CAP 8-bit CCIR656 0001: CAP 8-bit CCIR601 0010: CAP 8-bit VIP 1.1 0011: CAP 8-bit VIP 2.0 0100: CAP 16-bit CCIR656 0101: CAP 16-bit CCIR601 0110: CAP 16-bit VIP 1.1 0111: CAP 16-bit VIP 2.0 1xxx: TS 8-bit
3:0	RO	0000b	**Video Capture Port 0 Type Select (Reflects Strapping from Signals DVP1D[3:0])** 0000: CAP 8-bit CCIR656 0001: CAP 8-bit CCIR601 0010: CAP 8-bit VIP 1.1 0011: CAP 8-bit VIP 2.0 0100: CAP 16-bit CCIR656 0101: CAP 16-bit CCIR601 0110: CAP 16-bit VIP 1.1 0111: CAP 16-bit VIP 2.0 1xxx: TS 8-bit

IO Port / Index: 3C5.13
Configuration Register 2 (3C5.5A[0]=0) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	0	**DVP1 Output Select (Reflects Strapping from Signal VCPD13)** See bit [2:1] for bit value description detail.
5:3	RO	0	**Reserved**
2:1	RO	0	**DVP1 Output Select (Reflects Strapping from Signal VCPD12 / VCPD11)** **Bit [6, 2, 1] / Description** 00x: DVP-TV output 01x: DVP with alpha output 100: DCVI 10-bit data output 101: DCVI 8-bit data output 110: DCVI 20-bit data output 111: DCVI 16-bit data output
0	RO	0	**Reserved**

IO Port / Index: 3C5.13
Configuration Register 2 (3C5.5A[0]=1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	00b	**Reserved**
2:0	RO	000b	**First DAC (CRT/TV) Output Mode Select (Reflects Strapping from Signal DVP1D10/09/08)** 0xx: DAC A/B/C = R/G/B for CRT 100: DAC A/B/C = C/Y/CVBS for TV 101: DAC A/B/C = C/Y/Y for TV 110: DAC A/B/C = R/G/B for TV 111: DAC A/B/C = Pr/Y/Pb for TV

IO Port / Index: 3C5.14
Frame Buffer Size Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**LCD Reference Clock Select** 0: Normal 1: LCD reference clock tie to 0 (Gate off)

IO Port / Index: 3C5.15
Display Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**8/6 Bits LUT** 0: 6-bit 1: 8-bit
6	RW	0	**Text Column Control** 0: 80 column 1: 132 column
5	RW	0	**Wrap Around Disable** 0: Disable (For Mode 0-13) 1: Enable
4	RW	0	**Hi Color Mode Select** 0: 555 1: 565
3:2	RW	00b	**Display Color Depth Select** 00: 8bpp 01: 16bpp 10: 30bpp 11: 32bpp
1	RW	0	**Extended Display Mode Enable** 0: Disable 1: Enable
0	RO	0	**Reserved**

IO Port / Index: 3C5.16
Display FIFO Threshold Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:0	RW	0	**Display FIFO Normal Threshold**

IO Port / Index: 3C5.17
Display FIFO Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Display FIFO Depth Select** See also Rx3C5.51[2].

IO Port / Index: 3C5.18
Display Arbiter Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Force The PREQ Always Higher Than TREQ** 0: Disable 1: Enable
5:0	RW	0	**Display FIFO High Reg Threshold**

IO Port / Index: 3C5.19
Power Management Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**MIU/AGP Interface Clock Control** 0: Clocks always on 1: Enable clock gating
5	RW	0	**P-Arbiter Interface Clock Control** 0: Clocks always on 1: Enable clock gating
4	RW	0	**AGP Interface Clock Control** 0: Clocks always on 1: Enable clock gating
3	RW	0	**Typical Arbiter Interface Clock Control** 0: Clocks always on 1: Enable clock gating
2	RW	0	**MC Interface Clock Control** 0: Clocks always on 1: Enable clock gating
1	RW	0	**Display Interface Clock Control** 0: Clocks always on 1: Enable clock gating
0	RW	0	**CPU Interface Clock Control** 0: Clocks always on 1: Enable clock gating

IO Port / Index: 3C5.1A

PCI Bus Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Read Cache Enable** 0: Disable 1: Enable
6	RW	0	**Software Reset for 3D ECK** 0: Default value 1: Reset
5	RW	0	**DVI Sense - *Refer to LVDS / DVI chapter for details***
4	RW	0	**Second DVI Sense - *Refer to LVDS / DVI chapter for details***
3	RW	0	**Extended Mode Memory Access Enable** 0: Disable 1: Enable
2	RW	0	**PCI Burst Write Wait State Select** 0: 0 Wait state 1: 1 Wait state
1	RW	0	**ECK Software Reset** 0: Default value 1: Reset
0	RW	0	**LUT Shadow Access** 0: 3C6/3C7/3C8/3C9 addresses map to Primary Display's LUT 1: 3C6/3C7/3C8/3C9 addresses map to Secondary Display's LUT

IO Port / Index: 3C5.1B

Power Management Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Secondary Display Engine (Gated Clock <LCK>)** 0x: Clock always off 10: Clock always on 11: Clock on/off according to the Power Management Status (PMS)
5:4	RW	00b	**Primary Display Engine (Gated Clock <VCK>)** 0x: Clock always off 10: Clock always on 11: Clock on/off according to the PMS
3:2	RO	0	**Reserved**
1	RW	0	**Reserved**
0	RW	0	**Primary Display's LUT On/Off** 0: On 1: Off

IO Port / Index: 3C5.1C

Horizontal Display Fetch Count Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Display Fetch Count Data [7:0]** Unit: 16 bytes

IO Port / Index: 3C5.1D

Horizontal Display Fetch Count Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RW	0	**Horizontal Display Fetch Count Data Bits [9:8]** Used in conjunction with Rx3C5.1C register.

IO Port / Index: 3C5.1E
Power Management Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Video Capture Port Power Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS
5:4	RW	00b	**Digital Video Port 1 Power Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS
3	RW	0	**Spread Spectrum On/Off** 0: Off 1: On
2	RW	0	**Reserved**
1	RW	0	**Replace ECK by MCK** For BIST purpose.
0	RW	0	**On/Off ROC ECK** 0: Off 1: On

IO Port / Index: 3C5.20
Typical Arbiter Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:0	RW	0	**Typical Request Max. Queuing Number for Channel 0** Min: 0 Max: 30 (The recommended value is 4.)

IO Port / Index: 3C5.21
Typical Arbiter Control 1 **Default Value: 0Eh**

Bit	Attribute	Default	Description
7:0	RW	0	**Typical Request Track FIFO Number for Channel 0**

IO Port / Index: 3C5.22
Display Arbiter Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Display Queue Request Expire Number** Hardware multiples this register value by 4 to handle the FIFO control.

IO Port / Index: 3C5.26
IIC Serial Port Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**CRTSPCLK Pin Control** 0: Driven low 1: Tri-Stated
4	RW	0	**CRTSPD Pin Control** 0: Driven low 1: Tri-Stated
3	RO	0	**CRTSPCLK Pin Status**
2	RO	0	**CRTSPD Pin Status**
1	RW	0	**CRTSPCLK Wait State Enable** 0: Disable 1: Enable (Drive DDCSCL low upon receipt of serial port start).
0	RW	0	**Serial Port Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.2A
Power Management Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Spread Spectrum Type Control** 0: Original Type 1: FIFO Type
5:4	RW	0	**Reserved**
3:2	RW	00b	**LVDS Channel 2 I/O Pad Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS
1:0	RW	00b	**LVDS Channel 1 and DVI I/O Pad Control** 0x: Pad always off 10: Depend on the other control signal 11: Pad on/off according to the PMS

IO Port / Index: 3C5.2B
DVI and LVDS Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVI Sense Interrupt Enable** - ***Refer to LVDS / DVI chapter for details***
6	RW1C	0	**DVI Sense Interrupt Status** - ***Refer to LVDS / DVI chapter for details***
5	RW	0	**LVDS Sense Interrupt Enable** - ***Refer to LVDS / DVI chapter for details***
4	RW1C	0	**LVDS Sense Interrupt Status** - ***Refer to LVDS / DVI chapter for details***
3	RW	0	**CRT Sense Interrupt Enable** 0: Disable 1: Enable
2	RW1C	0	**CRT Sense Interrupt Status**
1	RW	0	**CRT Hot Plug Detection Function Enable** 0: Disable 1: Enable Please wait at least 2 frames to enable interrupt, when this function is enabled.
0	RW1C	0	**MSI Pending Interrupt Re-trigger Bit** When SW wants to exit interrupt service, please clear the bit. HW may send out interrupt again if pending interrupt exists. The funciton is enabled when MSI Enable = 1'b1.

IO Port / Index: 3C5.2C
General Purpose I/O Port **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**VGPIO2 Output Enable** 0: Disable 1: Enable
6	RW	0	**VGPIO3 Output Enable** 0: Disable 1: Enable
5	RW	0	**VGPIO2 Output Data**
4	RW	0	**VGPIO3 Output Data**
3	RO	0	**VGPIO2 Pin Status**
2	RO	0	**VGPIO3 Pin Status**
1	RW	0	**VGPIO Port Enable** 0: HW controlled 1: SW controlled
0	RW	0	**Spectrum IO Selected** 0: VGPIO[2,3] as VGPIO port 1: VGPIO2 as DISPCLKI0, VGPIO3 as DISPCLKO0

IO Port / Index: 3C5.2D

Power Management Control 4 **Default Value: 2Ah**

Bit	Attribute	Default	Description
7:6	RW	00b	**E3_ECK_N Selection** 00: E3_ECK_N (Inverted 3D Engine Clock) 01: E3_ECK (3D Engine Clock) 10: Delayed E3_ECK_N 11: Delayed E3_ECK
5:4	RW	10b	**VCK (Primary Display Clock) PLL Power Control** 0x: PLL power-off 10: PLL always on 11: PLL on/off according to the PMS
3:2	RW	10b	**LCK (Secondary Display Clock) PLL Power Control** 0x: PLL power-off 10: PLL always on 11: PLL on/off according to the PMS
1:0	RW	10b	**ECK (Engine Clock) PLL Power Control** 0x: PLL power-off 10: PLL always on 11: PLL on/off according to the PMS

IO Port / Index: 3C5.2E

Power Management Control 5 **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RW	10b	**Capturer Clock Gating Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
5:4	RW	10b	**Video Processor Clock Gating Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
3:2	RW	10b	**PCI Master/DMA Clock Gating Control (Gated Clock <ECK/CPUCK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
1:0	RW	10b	**Video Playback Engine Clock Gating Control (V3/V4 Gated Clock <VCK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status

IO Port / Index: 3C5.31

IIC Serial Port Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**DVPSPCLK Pin Control** 0: DVPSPCLK driven low 1: DVPSPCLK tri-stated
4	RW	0	**DVPSPD Pin Control** 0: DVPSPD driven low 1: DVPSPD tri-stated
3	RO	0	**DVPSPCLK Pin Status** 0: DVPSPCLK driven low 1: DVPSPCLK tri-stated
2	RO	0	**DVPSPD Pin Status** 0: DVPSPD driven low 1: DVPSPD tri-stated
1	RW	0	**DVPSPCLK Wait State Enable** 0: Disable 1: Enable (Drive DVPSPCLK low upon receipt of serial port start).
0	RW	0	**Serial Port Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.35
Subsystem Vendor ID 0 **Default Value: 06h**

Bit	Attribute	Default	Description
7:0	RW	06h	**Subsystem Vendor ID [7:0]**

IO Port / Index: 3C5.36
Subsystem Vendor ID 1 **Default Value: 11h**

Bit	Attribute	Default	Description
7:0	RW	11h	**Subsystem Vendor ID [15:8]**

IO Port / Index: 3C5.37
Subsystem ID 0 **Default Value: 22h**

Bit	Attribute	Default	Description
7:0	RW	22h	**Subsystem ID [7:0]**

IO Port / Index: 3C5.38
Subsystem ID 1 **Default Value: 51h**

Bit	Attribute	Default	Description
7:0	RW	51h	**Subsystem ID [15:8]**

IO Port / Index: 3C5.39
BIOS Reserved Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**BIOS Reserved Register 0**

IO Port / Index: 3C5.3A
BIOS Reserved Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**BIOS Reserved Register 1**

IO Port / Index: 3C5.3C
Miscellaneous **Default Value: 01h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:5	RW	00b	**PLL Frequency Division Select for Testing** 00: Original 01: 1/2 10: 1/4 11: 1/8
4	RO	0	**ECK PLL Locked Detect** 0: Unlocked 1: Locked
3	RO	0	**VCK PLL Locked Detect** 0: Unlocked 1: Locked
2	RO	0	**LCDCK PLL Locked Detect** 0: Unlocked 1: Locked
1	RW	0	**Switch 3 PLLs to Prime Output** 0: Disable 1: Enable
0	RW	1b	**AGP Bus Back Door** 0: ACP2.0 Spec 1: ACP3.0 Spec

IO Port / Index: 3C5.3D
General Purpose I/O Port **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**VGPIO4 Output Enable** 0: Disable 1: Enable
6	RW	0	**VGPIO5 Output Enable** 0: Disable 1: Enable
5	RW	0	**VGPIO4 Output Data**
4	RW	0	**VGPIO5 Output Data**
3	RO	0	**VGPIO4 Pin Status**
2	RO	0	**VGPIO5 Pin Status**
1	RO	0	**Reserved**
0	RW	0	**Spectrum IO Selected** 0: VGPIO[4,5] as VGPIO Port 1: VGPIO4 as DISPCLKI1, VGPIO5 as DISPCLKO1

IO Port / Index: 3C5.3E
Miscellaneous Register for AGP Mux **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVI Sense Interrupt Enable** - ***Refer to LVDS / DVI chapter for details***
6	RW1C	0	**DVI Sense Interrupt Status** - ***Refer to LVDS / DVI chapter for details***
5	RW	0	**Inside DVI Sense** - ***Refer to LVDS / DVI chapter for details***
4	RO	0	**Reserved**
3	RW	0	**PCIe Capability Control Back Door** - ***Refer to LVDS / DVI chapter for details***
2	RO	0	**Reserved**
1	RW	0	**Multi-function Selection** - ***Refer to LVDS / DVI chapter for detail***
0	RW	0	**Second DVIDET Sense Signal Source** - ***Refer to LVDS / DVI chapter for details***

IO Port / Index: 3C5.3F
Power Management Control 6 **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RW	10b	**CR Clock Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
5:4	RW	10b	**3D Clock Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
3:2	RW	10b	**2D Clock Control (Gated Clock <ECK/CPUCK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to the engine IDLE status
1:0	RW	10b	**DVD Clock Control (Gated Clock <ECK>)** 0x: Clock off 10: Clock always on 11: Clock on/off according to each engine IDLE status

IO Port / Index: 3C5.40

PLL Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CRT Sense Enable** Hardware sends constant value to DAC for sense. 0: Disable 1: Enable. When enabled, send pattern 24'h555555 to DAC.
6	RW	0	**Reserved**
5:4	RW	00b	**Free Run ECK Frequency Within the Idle Mode** 00: No change 01: 1/2 ECK 10: 1/4 ECK 11: 1/8 ECK
3	RW	0	**LVDS and DVI Interrupt Method** - ***Refer to LVDS / DVI chapter for details***
2	RW	0	**Reset LCDCK PLL**
1	RW	0	**Reset VCK PLL**
0	RW	0	**Reset ECK PLL**

IO Port / Index: 3C5.41

Typical Arbiter Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Typical Request T-Hold**
3:0	RO	0	**Typical Request Pre-T-Hold**

IO Port / Index: 3C5.42

Typical Arbiter Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Linear Addressing Mode Enable** 0: Force all engine use linear addressing mode 1: The addressing mode is decided by engine itself
6	RO	0	**P_ARB Request Attribute** 1: Supports Fetch Cycle With Length (2) Capability
5	RO	0	**P_ARB Arbitration Type** 0: Run-robin Like 1: Fix
4:0	RO	0	**Typical Request Max. Queuing Number**

IO Port / Index: 3C5.43

Graphics Bonding Option **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW1C	0	**IGA2 Display FIFO Underflow Flag**
4	RW1C	0	**IGA1 Display FIFO Underflow Flag**
3	RW1C	0	**Typical Channel 0 Arbiter Read Back Data Overwrite Flag**
2	RW1C	0	**Typical Channel 1 Arbiter Read Back Data Overwrite Flag**
1	RO	0	**Reserved**
0	RO	0	**Notebook Used Flag** 1: Notebook 0: Desktop

Clock Synthesizer Registers

IO Port / Index: 3C5.44
Primary Display (VCK) Clock Synthesizer Value 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DM[7:0]**

IO Port / Index: 3C5.45
Primary Display (VCK) Clock Synthesizer Value 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[0], 2'b00, DR[2:0], DM[9:8]}**

IO Port / Index: 3C5.46
Primary Display (VCK) Clock Synthesizer Value 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[1], DN[6:0]}**

IO Port / Index: 3C5.47
ECK Clock Synthesizer Value 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DM[7:0]**

IO Port / Index: 3C5.48
ECK Clock Synthesizer Value 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[0], 2'b00, DR[2:0], DM[9:8]}**

IO Port / Index: 3C5.49
ECK Clock Synthesizer Value 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[1], DN[6:0]}**

IO Port / Index: 3C5.4A
Secondary Display (LCDCK) Clock Synthesizer Value 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DM[7:0]**

IO Port / Index: 3C5.4B
Secondary Display (LCDCK) Clock Synthesizer Value 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[0], 2'b00, DR[2:0], DM[9:8]}**

IO Port / Index: 3C5.4C

Secondary Display (LCDCK) Clock Synthesizer Value 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**{DTZ[1], DN[6:0]}**

Note:
1. DTZ[1:0]: Select charge-pump current. Default value = 00b.
2. DGAIN[1:0] is for testing purpose and must be 00b in normal mode.
3. New naming of VT3409 GFXPLL spec:
   PLL1: for VCK
   PLL2: for ECK
   PLL3: for LCDCK
   PLLN[9:0]: DM[9:0], GFXPLL Feedback Divider
   PLLD[6:0]: DN[6:0], GFXPLL Pre-Divider
   PLLP[2:0]: DR[2:0], GFXPLL Output Divider
   PLLICP[1:0]: DTZ[1:0], Select the GFXPLL Charge-Pump Current
4. Frequency equations: the following two equations must be asserted

Internal Working Frequency

Fvco = Fref * (DM) / (DN) and 300MHz <= Fvco <= 600MHz

True Output Frequency

Fout = Fref * (DM) / [(DN) (2^{DR})]

IO Port / Index: 3C5.4D

Preemptive Arbiter Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Ypical Arbiter Tracking FIFO Type** 0: 64 levels 1: 128 levels (only single channel can use)
6	RO	0	**Reserved**
5:4	RW	00b	**P Arbiter Length Control** 0x: 2 quad words 10: 4 quad words 11: 8 quad words
3:0	RO	0	**Reserved**

IO Port / Index: 3C5.4E

Software Reset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	00b	**CR Reset Control** 01: Engine reset (high active) 10: Register reset (high active)
5:4	RW	00b	**3D Reset Control** 01: Engine reset (high active) 10: Register reset (high active)
3:2	RW	00b	**2D Reset Control** 01: Engine reset (high active) 10: Register reset (high active)
1:0	RW	00b	**HQV/DVD/Capture Reset Control** 01: Engine reset (high active) 10: Register reset (high active)

IO Port / Index: 3C5.4F

CR Gating Clock Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Threshold Value of Engine Idle for Gating Engine Clock**

IO Port / Index: 3C5.50
AGP Control Register **Default Value: 1Bh**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**AGP Request Attribute** 0: Only support length 1 1: Support length 2
5:0	RW	63h	**AGP Track FIFO Number**

IO Port / Index: 3C5.51
Display FIFO Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**NB FIFO Clock Control** 0: Disable 1: Enable
6	RW	0	**IGA1 Request Using New Method** 0: Original method 1: New method
5	RW	0	**Reserved**
4	RO	0	**Reserved**
3:1	RW	0	**Reserved**
0	RW	0	**NB FIFO Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.52
Integrated TV Shadow Register Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:1	RW	00b	**Integrated TV Shadow Memory Window** 00: A0000 01: A8000 10: B0000 11: B8000
0	RW	0	**Integrated TV Shadow Register Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.53
DAC Sense Control Register 1 **Default Value: 00h**

Bit	Attribut	Default	Description
7:0	RW	0	**Vertical Line Count for Sense Bits[7:0]** Indicates the line to be programmed that can assert HW_SENSE

IO Port / Index: 3C5.54
DAC Sense Control Register 2 **Default Value: 00h**

Bit	Attribut	Default	Description
7:0	RW	0	**Horizontal Pixel Count for Sense Start Bits[7:0]** Indicates the pixel to be programmed that can assert HW_SENSE

IO Port / Index: 3C5.55
DAC Sense Control Register 3 **Default Value: 00h**

Bit	Attribut	Default	Description
7:0	RW	0	**Horizontal Pixel Count for Sense End Bits7:0]** Indicates the pixel to be programmed that can assert HW_SENSE

IO Port / Index: 3C5.56
DAC Sense Control Register 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Horizontal Pixel Count for Sense End Bit[8]** Indicates the pixel to be programmed that can assert HW_SENSE
3	RW	0	**Horizontal Pixel Count for Sense Start Bit[8]** Indicates the pixel to be programmed that can assert HW_SENSE
2:0	RW	0	**Vertical Line Count for Sense Bits[10:8]** Indicates the line to be programmed that can assert HW_SENSE

IO Port / Index: 3C5.57
Display FIFO Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Display Queue Request Expire Number Bit [5]**
5	RW	0	**NB FIFO Delay Mode** 0: Original 1: Delay 1 cycle
4	RW	0	**Display FIFO Threshold Select Bit [7]**
3	RW	0	**Display FIFO Depth Select Bit [8]**
2	RW	0	**Display FIFO Threshold High Select Bit [7]**
1	RW	0	**NB FIFO Extended Source Select** 0: IGA1 (IGA: Integrated Graphics Accelerator) 1: IGA2
0	RW	0	**NB FIFO Length Extended Control** 0: Disable 1: Enable

IO Port / Index: 3C5.58
GFX Power Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Display FIFO Low Threshold Select** HW will multiply the value by 4 to handle. For IGA2, HW only uses bit[4:3]; to program bit[7:5][2:0] is useless.

IO Port / Index: 3C5.59
GFX Power Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1 Enable** When IGA1 engine is active, this bit need to set to 1
6	RO	0	**Reserved**
5	RW	0	**IGA Low Threshold Enable** 0: Disable 1: Enable
4	RW	0	**GFX-NM (Graphics-North Module) IGA Vertical Blanking Enable** 0: Disable 1: Enable
3	RW	0	**GFX-NM PCIC Dynamic Clock Enable** 0: Disable 1: Enable
2	RW	0	**GFX-NM GMINT (Graphics-Memory Interface) Channel 1 Dynamic Clock Enable** 0: Disable 1: Enable
1	RW	0	**GFX-NM GMINT Channel 0 Dynamic Clock Enable** 0: Disable 1: Enable
0	RW	0	**GFX-NM AGP Dynamic Clock Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.5A

PCI Bus Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Scratch Pad Register Shadow Access** 0: This bit controls Rx3X5.49-4F, Rx3C5.39/3A, Rx3X5.3B-3F (total 14) addresses map to original registers 1: This bit controls Rx3X5.49-4F, Rx3C5.39/3A, Rx3X5.3B-3F (total 14) addresses map to secondary registers

IO Port / Index: 3C5.5B

Device Used Status 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**DCVI Source Selection Flag** 0: Graphic 1 :TV
6	RO	0	**DAC0 User Flag** 0: Graphic 1: TV
5	RO	0	**DAC0 Used IGA1 Source Flag** 0: No use 1: Use
4	RO	0	**DAC0 Used IGA2 Source Flag** 0: No use 1: Use
3	RO	0	**LVDS0 Used IGA1 Source Flag** - ***Refer to LVDS / DVI chapter for details***
2	RO	0	**LVDS0 Used IGA2 Source Flag** - ***Refer to LVDS / DVI chapter for detail***
1	RO	0	**LVDS1 Used IGA1 Source Flag** - ***Refer to LVDS / DVI chapter for details***
0	RO	0	**LVDS1 Used IGA2 Source Flag**- ***Refer to LVDS / DVI chapter for details***

IO Port / Index: 3C5.5C

Device Used Status 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	0	**DAC1 User Flag** 0: Graphic 1: TV
5	RO	0	**DAC1 Used IGA1 Source Flag** 0: No use 1: Use
4	RO	0	**DAC1 Used IGA2 Source Flag** 0: No use 1: Use
3:2	RO	0	**Reserved**
1	RO	0	**DVP1 Used IGA1 Source Flag** 0: No use 1: Use
0	RO	0	**DVP1 Used IGA2 Source Flag** 0: No use 1: Use

IO Port / Index: 3C5.5D

Timer Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Timer Status** When the bit is asserted, it means the timer is reached.
6:0	RW	0	**Timer Step Setting** Countdown step value for timer. (one step is about 10us (8.9us)

IO Port / Index: 3C5.5E
DAC Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**DAC3 Off (B)**
2	RW	0	**DAC2 Off (G)**
1	RW	0	**DAC1 Off (R)**
0	RW	0	**CRT DACOFF setting** When this bit is 1, CRT DACOFF signal will be controlled by screen off register (Rx3C5.01[5]).

IO Port / Index: 3C5.60
I2C Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I2C Byte Count** This field is programmed with the data transfer count (a value between 0 and 15).
3	RW	0	**Internal Timer Count using Clock Divided by 2** 0: Counter using original clock 1: Counter using clock divided by 2
2	RW	0	**NO STOP Command Generation** When this bit is enabled, master controller finishes the transaction without STOP.
1	RW	0	**I2C Mode** 0: Standard mode 1: Fast mode
0	RW	0	**I2C Master Interrupt Enable** 0: Disable interrupt generation 1: Enable generation of interrupts on completion of the current transaction

IO Port / Index: 3C5.61
I2C Host Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**I2C Host Address** This field contains the 7 bit address of the targeted slave device.
0	RW	0	**I2C Read/Write Control** 0: Write 1: Read

IO Port / Index: 3C5.62
I2C Host Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**I2C Host Data** Hardware supports the queue of 2-byte data. Reads and writes to this register are used to access the 2-byte data queue. An internal index pointer is used to address the queue. It is reset to 0 by reads of the I2C Host Control register and incremented automatically by each access to this register.

IO Port / Index: 3C5.63
I2C Host Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Software Reset** 0: Normal function 1: Reset I2C master controller
6	RW	0	**No Active Driving to High before Release the Bus** 0: Driving to high 1: No driving to high
5	RO	0	**Reserved**
4	RW	0	**I2C Master Clock Control** 0: Disable 1: Enable
3:2	RW	00b	**Which Port I2C Master Process** 00: 31h 01: 2Ch 10: 26h 11: 25h
1	RW	0	**Kill Transaction in Progress** 0: Normal master controller operation 1: Stop transaction currently in progress
0	RW	0	**Fire** 0: No effect 1: Writing one to this bit causes master controller to start transaction

IO Port / Index: 3C5.64
I2C Status **Default Value: 40h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	1b	**Queue Empty Status** When this bit is one, it means hardware queue is empty.
4	RW1C	0	**I2C Data Transferred Status**
3	RW1C	0	**I2C Transaction Done Status**
2	RW1C	0	**I2C Abnormal Status**
1	RW	0	**Queue Full Status** When this bit is one, it means hardware queue is full.
0	RW	0	**Master Busy Status** When this bit is one, it means master controller is busy processing a command.

IO Port / Index: 3C5.65
Power Management Control 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	00b	**DVP1 Clock Pads Driving Select** 00 (Low) ←→ 11 (high)
1:0	RW	00b	**DVP1 Data Pads Driving Select** 00 (Low) ←→ 11 (high)

IO Port / Index: 3C5.66
GTI Control 0 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**Typical Request Kill Number for Channel 0**

IO Port / Index: 3C5.67
GTI Control 1 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**3D Request Kill Number for Channel 0**

IO Port / Index: 3C5.68
GTI Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Size of System Local Frame Buffer (S.L.)** 00h: 512MB 80h: 256MB C0h: 128MB E0h: 64MB F0h: 32MB F8h: 16MB FCh: 8MB FEh: 4MB FFh: 2MB

IO Port / Index: 3C5.69
GTI Control 3 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**GTI Request Kill Number for Channel 0**

IO Port / Index: 3C5.6A
GTI Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Base Address [19:12] of RTSF in SL**

IO Port / Index: 3C5.6B
GTI Control 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Base Address [27:20] of RTSF in SL**

IO Port / Index: 3C5.6C
GTI Control 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**GART Table Write Protect Enable** Enable to avoid hardware write. 0: Disable 1: Enable
6	RW	0	**GARB Sample GFX1 Data**
5	RW	0	**GTI Sample GFX0 Data**
4:1	RO	0	**Reserved**
0	RW	0	**Base Address [28] of RTSF in SL**

IO Port / Index: 3C5.6D
GTI Control 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Base Address [28:21] of SL in System Memory**

IO Port / Index: 3C5.6E
GTI Control 8 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Base Address [36:29] of SL in System Memory**

IO Port / Index: 3C5.6F
GTI Control 9 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**GTI Cache Flush** Set by SW and reset by GTI.
6:0	RW	0	**Base Address [43:37] of SL in System Memory**

IO Port / Index: 3C5.70
GARB Control 0 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**GARB Request Kill Number for Channel 1**

IO Port / Index: 3C5.71
Typical Arbiter Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:0	RW	0	**Typical Request Max. Queuing Number for Channel 1** Min: 0 Max: 30 (The recommended value is 4.)

IO Port / Index: 3C5.72
Typical Arbiter Control 3 **Default Value: 1Dh**

Bit	Attribute	Default	Description
7:0	RW	0	**Typical Request Track FIFO Number for Channel 1**

IO Port / Index: 3C5.73
Typical Arbiter Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**Typical Request Max. Burst Length to GTI for Channel 1** 00: 1 01: 2 10: 2 11: 4
3:2	RO	0	**Reserved**
1:0	RW	00b	**Typical Request Max. Burst Length to GTI for Channel 0** 00: 1 01: 2 10: 2 11: 4

IO Port / Index: 3C5.74
Typical Arbiter Control 5 **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:0	RW	1Fh	**Typical Request Max. ACK Number Minus One for Channel 1** 00h: Disable the function

IO Port / Index: 3C5.75
Typical Arbiter Control 6 **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:0	RW	1Fh	**Typical Request Max. ACK Number Minus One for Channel 0** 00h: Disable the function

IO Port / Index: 3C5.76
Backlight Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Debug Port Group Selection**
3	RW	0	**Debug Port Group0/Group1 Selection**
2:1	RW	0	**Bonding Option for ECK 166MHz, 250MHz, and 275MHz** 00: 250MHz 01: 166MHz 10: 275MHz 11: Reserved
0	RW	0	**Backlight Control Enable** 0: Disable 1: Enable

IO Port / Index: 3C5.77
Backlight Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**PWM Level Indicator** Total 256 level from 0% ~ 100%.

IO Port / Index: 3C5.78
Backlight Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**South Module Pad Share Enable** 0: Disable 1: Enable
6	RW	0	**Inverse IGA2 HSYNC to LVDS** - ***Refer to LVDS / DVI chapter for details***
5	RW	0	**Inverse IGA2 VSYNC to LVDS** - ***Refer to LVDS / DVI chapter for details***
4	RW	0	**Inverse IGA1 HSYNC to LVDS** - ***Refer to LVDS / DVI chapter for details***
3	RW	0	**Inverse IGA1 VSYNC to LVDS** - ***Refer to LVDS / DVI chapter for details***
2:1	RW	00b	**Clock Source Selection** 00: 14.318 MHz / 128 01: 14.318 MHz / 256 10: 14.318 MHz / 512 11: 14.318 MHz / 1024
0	RW	0	**Backlight Control Fire** 1: Fire (3C5.76[0] must be 1)

IO Port / Index: 3C5.79
GTI Control 10 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**SL/SF Request Kill Number 0** Indicates the Kill number set by SW, which is used when there is high P-ARB request.

IO Port / Index: 3C5.7A
GTI Control 11 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**SL/SF Request Kill Number 1** Indicates the Kill number set by SW, which is used when there is not high P-ARB request.

Note: the kill number0 can be set to small value to service display ASAP, and kill number1 can be set to larger value to service SL/SF request much time.

IO Port / Index: 3C5.7B
GTI Control 12 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**

IO Port / Index: 3C5.7C
GTI Control 13 **Default Value: C8h**

Bit	Attribute	Default	Description
7:0	RW	C8h	**CBU Request Kill Number** Kill number set by SW

IO Port / Index: 3C5.7D
Transmitter Power Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Real PD1 Polarity - *Refer to LVDS / DVI chapter for details***
6	RW	0	**Real PD2 Polarity - *Refer to LVDS / DVI chapter for details***
5	RW	0	**Real PD3 Polarity - *Refer to LVDS / DVI chapter for details***
4	RW	0	**Add a Protect Flag to Prevent All Snapshot State Fail**
3	RW	0	**The Source Clock Selection of Internal SSCG** 0: FIFO type 1: Original type
2	RW	0	**SSCG Selection of Original Type** 0: External SSCG 1: Internal SSCG
1	RW	0	**The Source Clock Selection of External SSCG (For Original Type)** 0: VCKSRC 1: LCDCK_SRC0
0	RW	0	**SSCG selection of FIFO type** 0: External SSCG 1: Internal SSCG

IO Port / Index: 3C5.A8
V1 Power Mode Control 0 (For C0) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Gate Off ROC ECK (ROC Engine Clock)** 0: Clock on 1: Gated off
6:2	RW	0	**Reserved**
1	RW	0	**Disable Gate Off ECK (Engine Clock) in Snapshot Mode** 0: Enable gate off 1: Disable Gated off
0	RW	0	**Reserved**

IO Port / Index: 3C5.A9
V1 Power Mode Control 1 (For C2) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Gate Off ROC ECK (ROC Engine Clock)** 0: Clock on 1: Gated off
6:0	RW	0	**Reserved**

IO Port / Index: 3C5.AA
V1 Power Mode Control 2 (For C4) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Gate Off ROC ECK (ROC Engine Clock)** 0: Clock on 1: Gated off
6:0	RW	0	**Reserved**

IO Port / Index: 3C5.AB
V1 Power Mode Control 3 (For C3) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Gate Off ROC ECK (ROC Engine Clock)** 0: Clock on 1: Gated off
6:0	RW	0	**Reserved**

IO Port / Index: 3C5.AC

V1 Power Mode Control 4 (For S3) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Gate Off ROC ECK (ROC Engine Clock)** 0: Clock on 1: Gated off
6:0	RW	0	**Reserved**

IO Port / Index: 3C5.AD

V1 Power Mode Control 5 (For V1 at S1 Snapshot) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Gate Off ROC ECK (ROC Engine Clock)** 0: Clock on 1: Gated off
6:0	RW	0	**Reserved**

IO Port / Index: 3C5.AE

V1 Power Mode Control 6 (For C4P) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Gate Off ROC ECK (ROC Engine Clock)** 0: Clock on 1: Gated off
6:0	RW	0	**Reserved**

IO Port / Index: 3C5.AF

V1 Power Mode Control 7 (Reserved State) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Gate Off ROC ECK (ROC Engine Clock)** 0: Clock on 1: Gated off
6:0	RW	0	**Reserved**

Graphics Controller Extended Register

This section describes the graphics controller extended register definitions in detail.

IO Port / Index: 3CF.20
Offset Register Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Offset Register A Overflow Bit 9**
5	RW	0	**Offset Register A Overflow Bit 8**
4	RW	0	**Offset Register B Overflow Bit 8**
3:2	RO	0	**Reserved**
1	RW	0	**Offset Read/Write Control** 0: Offset A (Rx3CF.21) and B (Rx3CF.22) as read/write 1: Offset A as write and offset B as read
0	RW	0	**Offset Configuration** 0: Offset A and B configured as 64KB 1: Offset A and B configured as 16KB

IO Port / Index: 3CF.21
Offset Register A **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Offset A**

IO Port / Index: 3CF.22
Offset Register B **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Offset B**

CRT Controller Extended Registers

This section provides detailed CRT controller extended register bit definitions. The "X" contained within the I/O port address stands for **"B"** during monochrome mode and is changed to **"D"** in color mode. For example, the I/O index for Mode Control register will be **Rx3B5.32** in monochrome mode and **Rx3D5.32** in color mode.

IO Port / Index: 3X5.30

Display Fetch Blocking Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1 Digital Interface Test Enable** 0: Disable 1: Enable
6	RW	0	**Convert Primary Display Data From RGB TO YcbCr** 0: Disable 1: Enable
5	RW	0	**Reserved**
4:3	RW	0	**DR. DAC Speed Enhancement**
2	RW	0	**Power Now Signals in Primary Path** 0: Disable (Off) 1: Enable (On)
1:0	RW	00b	**Block T_REQ Path** 0x: Disable 10: Block request within the vertical & horizontal display area 11: Block request within the vertical display area

IO Port / Index: 3X5.31

Half Line Position **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Half Line Position**

IO Port / Index: 3X5.32

Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	000b	**HSYNC Delay Number by VCLK** 000: No delay 001: Delay + 4 VCKs 010: Delay + 8 VCKs 011: Delay + 12 VCKs 100: Delay + 16 VCKs 101: Delay + 20 VCKs Others: Undefined
4	RO	0	**Reserved**
3	RW	0	**CRT SYNC Driving Selection** 0: Low 1: High
2	RW	0	**Display End Blanking Enable** 0: Disable 1: Enable
1	RW	0	**Digital Video Port (DVP) Grammar Correction** If the Grammar correction of primary display is turned on, the grammar correction in DVP can be enabled/disabled by this bit. 0: Disable 1: Enable
0	RW	0	**Real-Time Flipping** 0: Flip by the frame 1: Flip by each scan line

IO Port / Index: 3X5.33
HSYNCH Adjuster **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Primary Display Gamma Correction** 0: Disable 1: Enable
6	RW	0	**Primary Display Interlace Mode**
5	RW	0	**Horizontal Blanking End Bit [6]**
4	RW	0	**HSYNC Start Bit [8]**
3	RW	0	**Prefetch Mode** 0: Disable 1: Enable
2:0	RW	000b	**The value will shift the HSYNC to be early than planned** 000: Shift to early time by 3 character (VGA mode suggested value; default value) 001: Shift to early time by 4 character 010: Shift to early time by 5 character 011: Shift to early time by 6 character 100: Shift to early time by 7 character 101: Shift to early time by 0 character (Non-VGA mode suggested value) 110: Shift to early time by 1 character 111: Shift to early time by 2 character

IO Port / Index: 3X5.34
Starting Address Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Starting Address Overflow Bits [23:16]**

IO Port / Index: 3X5.35
Extended Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Offset Bits [10:8]**
4	RW	0	**Line Compare Bit [10]**
3	RW	0	**Vertical Blanking Start Bit [10]**
2	RW	0	**Vertical Display End Bit [10]**
1	RW	0	**Vertical Retrace Start Bit [10]**
0	RW	0	**Vertical Total Bit [10]**

IO Port / Index: 3X5.36
Power Management 8 (Monitor Control) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DPMS VSYNC Output** Used when 3X5.36[5:4] is in standby state 0: Pin CRT_VSYNC of this chip will be at low level 1: Pin CRT_VSYNC of this chip will be at high level
6	RW	0	**DPMS HSYNC Output** Used when 3x5.36[5:4] is in standby state 0: Pin CRT_HSYNC of this chip will be at low level 1: Pin CRT_HSYNC of this chip will be at high level
5:4	RW	00b	**Simulate the behavior of DPMS** 00: On 01: Standby state 10: Standby state 11: Standby state
3	RW	0	**Horizontal Total Bit [8]**
2:1	RO	0	**Reserved**
0	RW	0	**PCI Power Management Control** 0: Disable 1: Enable

IO Port / Index: 3X5.37
DAC Control Register **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**DAC Power Save Control 1** 0: Depend on Rx3X5.37[5:4] setting 1: DAC always goes into power save mode
6	RW	0	**DAC Power Down Control** 0: Depend on Rx3X5.47[2] setting 1: DAC never goes to power down mode
5:4	RW	00b	**DAC Power Save Control 2** 00: DAC never goes to power save mode 01: DAC goes to power save mode by line 10: DAC goes to power save mode by frame 11: DAC goes to power save mode by line and frame
3	RW	0	**DAC Current Control** 0: Not set 1: Set a minimum level during non-blanking period to increase Iout
2:0	RW	100b	**DAC Factor**

IO Port / Index: 3X5.38
Signature Data Register B0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Signature Data Register B0**

IO Port / Index: 3X5.39
Signature Data Register B1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Signature Data Register B1**

IO Port / Index: 3X5.3A
Signature Data Register B2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Signature Data Register B2**

IO Port / Index: 3X5.3B
Scratch Pad Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 2**

IO Port / Index: 3X5.3C
Scratch Pad Register 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 3**

IO Port / Index: 3X5.3D
Scratch Pad Register 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 4**

IO Port / Index: 3X5.3E
Scratch Pad Register 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 5**

IO Port / Index: 3X5.3F
Scratch Pad Register 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Pad Register 6**

IO Port / Index: 3X5.40
Test Mode Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Test Group Select**
3	RW	0	**Test Mode Control** 0: Disable 1: Enable
2	RW	0	**Signature Test Source** 0: Primary display 1: Secondary display
1	RW	0	**Signature Test Enable** 0: Disable 1: Enable
0	RW	0	**DAC Test Mode Control Enable** 0: Disable 1: Enable Data come from MDI[23:0].

IO Port / Index: 3X5.43
IGA1 Display Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**IGA1 10 Bit Gamma Algorithm LUT256 Index 0 for Color 0** 0: Color 0 always output 10'b0 1: Color 0 output value from index 0' data
2	RW	0	**IGA1 Address Mode Selection** 0: Linear 1: Tile
1	RW	0	**IGA1 Hardware 10 Bit Gamma Enable** 0: Disable 1: Enable
0	RW	0	**IGA1 Extend 10 Bit Mode LSB Selection** 0: Always 00b 1: MSB bits

IO Port / Index: 3X5.45
Power Now Indicator Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Display FIFO Threshold for Power Now Indicator Bit [7]**

IO Port / Index: 3X5.46
Test Mode Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Load a Value to the Vertical Counter**

IO Port / Index: 3X5.47

Test Mode Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IGA1 Timing Plus 2 VCK**
6	RW	0	**IGA1 Timing Plus 4 VCK**
5	RW	0	**Peep at the PCI Bus** 0: Disable 1: Enable
4	RW	0	**CRT Timing Register Protect**
3	RW	0	**IGA1 Timing Plus 6 VCK**
2	RW	0	**DACOFF Backdoor Register**
1	RW	0	**LCD Simultaneous Mode Backdoor Register for 8/9 Dot Clocks**
0	RW	0	**LCD Simultaneous Mode Backdoor Register for Clock Select**

IO Port / Index: 3X5.48

Starting Address Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**IGA1 Channel Selection** 1x: L.L. 00: S.L.
5	RO	0	**Reserved**
4:0	RW	0	**Starting Address Overflow Bits[28:24]**

Secondary Display Registers

This section describes the secondary display I/O register bit definitions. The "X" contained within the I/O port address stands for **"B"** during monochrome mode and is changed to **"D"** in color mode. For example, the I/O index for the Second CRTC horizontal Total Period register will be **Rx3B5.50** in monochrome mode and **Rx3D5.50** in color mode.

IO Port / Index: 3X5.50
Second CRT Horizontal Total Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Total Period Bits [7:0]**

IO Port / Index: 3X5.51
Second CRT Horizontal Active Data Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Active Data Period Bits [7:0]**

IO Port / Index: 3X5.52
Second CRT Horizontal Blanking Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second CRT Horizontal Blanking Start Bits [7:0]**

IO Port / Index: 3X5.53
Second CRT Horizontal Blanking End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second CRT Horizontal Blanking End Bits [7:0]**

IO Port / Index: 3X5.54
Second CRT Horizontal Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Horizontal Retrace Start Bits [9:8]**
5:3	RW	0	**Horizontal Blanking End Bits [10:8]**
2:0	RW	0	**Horizontal Blanking Start Bits [10:8]**

IO Port / Index: 3X5.55
Second CRT Horizontal Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Horizontal Active Data Period Bits [10:8]**
3:0	RW	0	**Horizontal Total Period Bits [11:8]**

IO Port / Index: 3X5.56
Second CRT Horizontal Retrace Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Retrace Start Bits [7:0]**

IO Port / Index: 3X5.57
Second CRT Horizontal Retrace End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Retrace End**

IO Port / Index: 3X5.58
Second CRT Vertical Total Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Total Period Bits [7:0]**

IO Port / Index: 3X5.59
Second CRT Vertical Active Data Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Active Data Period Bits [7:0]**

IO Port / Index: 3X5.5A
Second CRT Vertical Blanking Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Blanking Start Bits [7:0]**

IO Port / Index: 3X5.5B
Second CRT Vertical Blanking End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Blanking End Bits [7:0]**

IO Port / Index: 3X5.5C
Second CRT Vertical Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Horizontal Retrace Bit [10]**
6	RW	0	**Horizontal Retrace End Bit [8]**
5:3	RW	0	**Vertical Blanking End Bits [10:8]**
2:0	RW	0	**Vertical Blanking Start Bits [10:8]**

IO Port / Index: 3X5.5D
Second CRT Vertical Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Horizontal Retrace Start Bit [11]**
6	RW	0	**Horizontal Blanking End Bit [11]**
5:3	RW	0	**Vertical Active Data Period Bits [10:8]**
2:0	RW	0	**Vertical Total Period Bits [10:8]**

IO Port / Index: 3X5.5E
Second CRT Vertical Retrace Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Retrace Start Bits [7:0]**

IO Port / Index: 3X5.5F
Second CRT Vertical Retrace End **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Vertical Retrace Start Bits [10:8]**
4:0	RW	0	**Vertical Retrace End**

IO Port / Index: 3X5.60
Second CRT Vertical Status 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Vertical Count Number Bits[7:0]**

IO Port / Index: 3X5.61
Second CRT Vertical Status 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Vertical Retrace Status** 1: Retrace Period
6	RO	0	**Vertical Active Data Status** 1: Active Data Period
5	RO	0	**Flip Flag**
4	RO	0	**Power Sequence Flag 0** 0: Invalid 1: Valid
3	RO	0	**Power Sequence Flag 1** 0: Invalid 1: Valid
2:0	RO	0	**Vertical Count Number Bits[10:8]**

IO Port / Index: 3X5.62
Second Display Starting Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Second Display Starting Address Bits[9:4]** This is 2-quadword boundary.
1	RO	0	**Reserved**
0	RW	0	**Second Display Address Mode Selection** 0: Linear mode 1: Tile mode

IO Port / Index: 3X5.63
Second Display Starting Address - Middle **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Starting Address Bits[17:10]**

IO Port / Index: 3X5.64
Second Display Starting Address - High **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Starting Address Bits[25:18]**

IO Port / Index: 3X5.65
Second Display Horizontal Quadword Count Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Horizontal 2-Quadword Count Data Bits[7:0]**

IO Port / Index: 3X5.66
Second Display Horizontal Offset **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Horizontal Offset Bits[7:0] or** **Horizontal Synchronous Point**

IO Port / Index: 3X5.67

Second Display Color Depth and Horizontal Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Color Depth** 00: 8bpp 01: 16bpp 10: 30bpp 11: 32bpp
5	RW	0	**Second Display Interlace Mode**
4	RW	0	**IGA2 Extend 10 Bit Mode LSB Selection** 0: 2'b00 1: MSB[7:6]
3:2	RW	0	**Second Display Horizontal 2-Quadword Count Data Bits[9:8]**
1:0	RW	0	**Second Display Horizontal Offset Bits[9:8]**

IO Port / Index: 3X5.68

Second Display Queue Depth and Read Threshold **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Display Queue Depth [3:0]** Unit: 8 levels (Depth[5:4] on Rx3X5..95[7] and Rx3X5..94[7]) HW only uses Depth[3:1]; to program Depth[5:4][0] is useless.
3:0	RW	0	**Display Queue Read Threshold 1** Unit: 4 levels (Threshold[6:4] on Rx3X5.95[6:4]) HW only uses Threshold[4:3]; to program Threshold[6:5][2:0] is useless.

IO Port / Index: 3X5.69

Second Display Interrupt Enable and Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	***For Write:*** **Interrupt Clear** Write 1 to clear. ***For Read:*** **Interrupt Status** 0: No interrupt 1: Interrupt period
6	RW	0	**Interrupt Enable** 0: Disable 1: Enable
5:0	RO	0	**Reserved**

IO Port / Index: 3X5.6A

Second Display Channel and LCD Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Second Display Channel Enable** 0: Disable 1: Enable
6	RW	0	**Second Display Channel Reset** 0: Reset
5	RW	0	**Second Display 8/6 Bits LUT** 0: 6-bit 1: 8-bit
4	RW	0	**Second Display Channel Clock Mode Selection. Same with 3X5.6B[5]** 0: Normal 1: Division by 2
3	RW	0	**First Hardware Power Sequence** - ***Refer to LVDS / DVI chapter for details***
2	RW	0	**Second Display Channel Vertical Clear** Write 1 to clear.
1	RW	0	**LCD Gamma Enable** 0: Disable 1: Enable
0	RW	0	**LCD Pre-fetch Mode Enable** 0: Disable 1: Enable

IO Port / Index: 3X5.6B

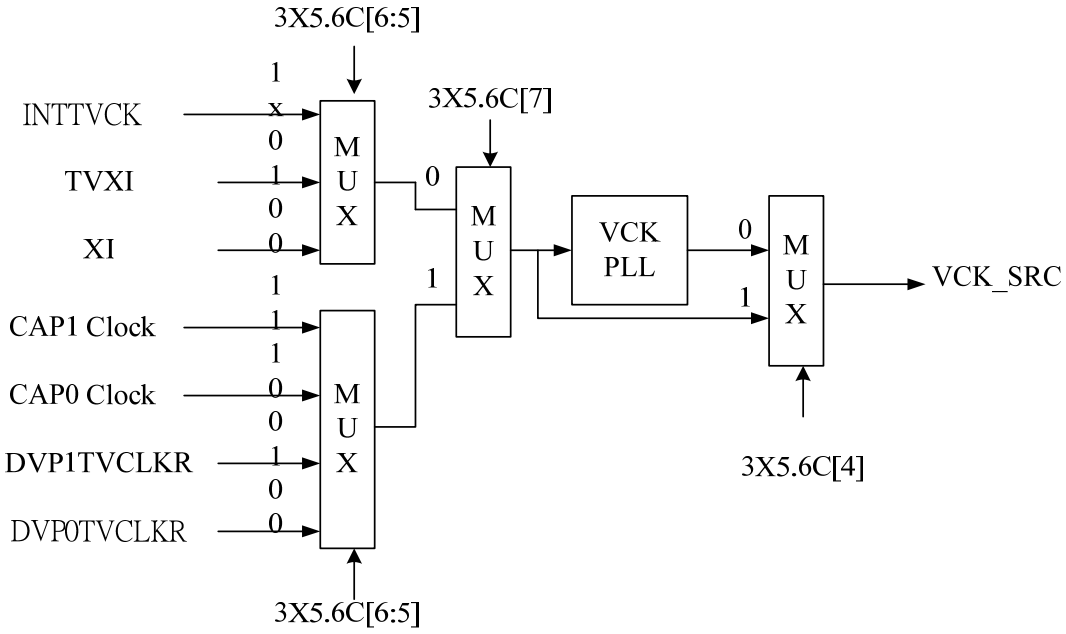
Channel 1 and 2 Clock Mode Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**First Display Channel Clock Mode Selection** 0x: Normal 1x: Division by 2
5:4	RW	00b	**Second Display Channel Clock Mode Selection** 0x: Normal 1x: Division by 2
3	RW	0	**Simultaneous Display Enable** 0: Disable 1: Enable
2	RW	0	**IGA2 Screen Off** 0: Normal 1: Screen off
1	RW	0	**IGA2 Screen Off Selection Method** 0: IGA2 screen off 1: IGA1 screen off
0	RO	0	**Reserved**

IO Port / Index: 3X5.6C
TV CLK Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	000b	**VCK PLL Reference Clock Source Selection** 000: From XI pin 001: From TVXI 01x: From TVPLL 100: Reserved 101: DVP1TVCLKR 110: CAP0 Clock 111: CAP1 Clock
4	RW	0	**VCK Source Selection** 0: VCK PLL output clock 1: VCK PLL reference clock
3:1	RW	000b	**LCDCK PLL Reference Clock Source Selection** 000: From XI pin 001: From TVXI 01x: From TVPLL 100: Reserved 101: DVP1TVCLKR 110: CAP0 Clock 111: CAP1 Clock
0	RW	0	**LCDCK Source Selection** 0: LCDCK PLL output clock 1: LCDCK PLL reference clock

VCK Example:



IO Port / Index: 3X5.6D
Horizontal Total Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Total Bits[7:0]**

IO Port / Index: 3X5.6E
End Horizontal Blanking Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**End Horizontal Blanking Bits[7:0]**

IO Port / Index: 3X5.6F
Vertical Total Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Total Bits[7:0]**

IO Port / Index: 3X5.70
Vertical Display Enable End Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Display Enable End Bits[7:0]**

IO Port / Index: 3X5.71
Vertical Display Overflow Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Second Display Horizontal Offset Bit [13]**
6:4	RW	0	**Vertical Display Enable End Bits[10:8]**
3	RW	0	**Horizontal Total Bit [8]**
2:0	RW	0	**Vertical Total Bits[10:8]**

IO Port / Index: 3X5.72
Start Vertical Blank Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Start Vertical Blanking Bits[7:0]**

IO Port / Index: 3X5.73
End Vertical Blank Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**End Vertical Blanking Bits[7:0]**

IO Port / Index: 3X5.74
Vertical Blank Overflow Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**For 6-bit LUT** 0: Send back original 8 bits data 1: Send back transformed 8 bits data
6:4	RW	0	**Start Vertical Blanking Bits[10:8]**
3	RO	0	**Reserved**
2:0	RW	0	**End Vertical Blanking Bits[10:8]**

IO Port / Index: 3X5.75
Vertical Retrace Start Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Retrace Start Bits[7:0]**

IO Port / Index: 3X5.76
Vertical Retrace End Shadow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Vertical Retrace Start Bits[10:8]**
3:0	RW	0	**Vertical Retrace End**

IO Port / Index: 3X5.77
LCD Horizontal Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Scaling Factor Bits[9:2]**

IO Port / Index: 3X5.78
LCD Vertical Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Scaling Factor Bits[8:1]**

IO Port / Index: 3X5.79
LCD Scaling Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Vertical Scaling Factor Bits[10:9]**
5:4	RW	0	**Horizontal Scaling Factor Bits[11:10]**
3	RW	0	**Vertical Scaling Factor Bit [0]**
2	RO	0	**Reserved**
1	RW	0	**Horizontal Scaling Selection** 0: Duplication 1: Interpolation
0	RW	0	**LCD Scaling Enable** 0: Disable 1: Enable

IO Port / Index: 3X5.7A
LCD Scaling Parameter 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 1**

IO Port / Index: 3X5.7B
LCD Scaling Parameter 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 2**

IO Port / Index: 3X5.7C
LCD Scaling Parameter 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 3**

IO Port / Index: 3X5.7D
LCD Scaling Parameter 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 4**

IO Port / Index: 3X5.7E
LCD Scaling Parameter 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 5**

IO Port / Index: 3X5.7F
LCD Scaling Parameter 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 6**

IO Port / Index: 3X5.80
LCD Scaling Parameter 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 7**

IO Port / Index: 3X5.81
LCD Scaling Parameter 8 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 8**

IO Port / Index: 3X5.82
LCD Scaling Parameter 9 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 9**

IO Port / Index: 3X5.83
LCD Scaling Parameter 10 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 10**

IO Port / Index: 3X5.84
LCD Scaling Parameter 11 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 11**

IO Port / Index: 3X5.85
LCD Scaling Parameter 12 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 12**

IO Port / Index: 3X5.86
LCD Scaling Parameter 13 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 13**

IO Port / Index: 3X5.87
LCD Scaling Parameter 14 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Parameter 14**

IO Port / Index: 3X5.88
LCD Panel Type **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.8A
LCD Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Adjust FLM**
3	RO	0	**Reserved**
2:0	RW	0	**Adjust LP**

IO Port / Index: 3X5.8B
LCD Power Sequence Control 0 **Default Value: CAh**

Bit	Attribute	Default	Description
7:0	RW	CAh	**TD0 Timer Bits[7:0] (default 32ms)**

IO Port / Index: 3X5.8C
LCD Power Sequence Control 1 **Default Value: CAh**

Bit	Attribute	Default	Description
7:0	RW	CAh	**TD1 Timer Bits[7:0] (default 32ms)**

IO Port / Index: 3X5.8D
LCD Power Sequence Control 2 **Default Value: CAh**

Bit	Attribute	Default	Description
7:0	RW	CAh	**TD2 Timer Bits[7:0] (default 32ms)**

IO Port / Index: 3X5.8E
LCD Power Sequence Control 3 **Default Value: CAh**

Bit	Attribute	Default	Description
7:0	RW	CAh	**TD3 Timer Bits[7:0] (default 32ms)**

IO Port / Index: 3X5.8F
LCD Power Sequence Control 4 **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	1h	**TD1 Timer [11:8]**
3:0	RW	1h	**TD0 Timer [11:8]**

IO Port / Index: 3X5.90

LCD Power Sequence Control 5 **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	1h	**TD3 Timer [11:8]**
3:0	RW	1h	**TD2 Timer [11:8]**

IO Port / Index: 3X5.91

Software Control Power Sequence **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Software Direct On / Off Display Period in the Panel Path** 0: On 1: Off
6	RW	0	**Software On / Off Back Light Directly** 0: On 1: Off
5	RW	0	**Software Direct On / Off Display Period in the Secondary Display Path** 0: On 1: Off
4	RW	0	**Software VDD On** 0: Off 1: On
3	RW	0	**Software Data On** 0: Off 1: On
2	RW	0	**Software VEE On** 0: Off 1: On
1	RW	0	**Software Back Light On** 0: Off 1: On
0	RW	0	**Hardware or Software Control Power Sequence** 0: Hardware control 1: Software control

IO Port / Index: 3X5.92

Read Threshold 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0	**Read Threshold 2** Unit: 4 levels (Threshold[6:4] on Rx3X5.95[2:0]) HW only uses Threshold[4:3]; to program Threshold[6:5][2:0] is useless.

IO Port / Index: 3X5.94

Expire Number and Display Queue Extend Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Display Queue Depth Bit[4]**
6:0	RW	0	**Display2 Expire Number Bits [6:0]**

IO Port / Index: 3X5.95

Extend Threshold Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Display Queue Depth Bit[5]**
6:4	RW	0	**Read Threshold 1 Bits [6:4]**
3	RO	0	**Reserved**
2:0	RW	0	**Read Threshold 2 Bits [6:4]**

IO Port / Index: 3X5.97
LVDS Channel 2 Function Select 0 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.98
LVDS Channel 2 Function Select 1 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.99
LVDS Channel 1 Function Select 0 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.9B
Digital Video Port 1 Function Select 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVP1 ALPHA Enable** 0: Disable 1: Enable
6	RW	0	**DVP1 VSYNC Polarity** 0: Positive 1: Negative
5	RW	0	**DVP1 HSYNC Polarity** 0: Positive 1: Negative
4	RW	0	**DVP1 Data Source Selection 0** 0: Primary Display 1: Secondary Display
3	RW	0	**DVP1 Clock Polarity**
2:0	RW	0	**DVP1 Clock Adjust**

IO Port / Index: 3X5.9D
Power Now Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Specifies the Indicator Ending Reference Point in the Vertical Blanking Period** 0: Use vertical retrace starting position 1: Use bits [6:0] of this register
6:0	RW	0	**Ending Position of Power Now Indicator [6:0]**

IO Port / Index: 3X5.9E
Power Now Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Use Which Condition As The Power Now Indicator** 0: Active in the vertical blanking area 1: Active while display FIFO is almost full (refer bit[6:0])or vertical blanking period
6:0	RW	0	**Display FIFO Threshold for Power Now Indicator** The value must be divided by 4.

IO Port / Index: 3X5.9F
Power Now Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable the Power Now Indicator** 0: Disable 1: Enable
6:2	RO	0	**Reserved**
1:0	RW	0	**Horizontal Scaling Factor Bits [1:0]**

IO Port / Index: 3X5.A0
Horizontal Scaling Initial Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Scaling Initial Value** Add on scaling factor high 8 bits.

IO Port / Index: 3X5.A1
Vertical Scaling Initial Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Scaling Initial Value** Add on scaling factor high 8 bits.

IO Port / Index: 3X5.A2
Scaling Enable Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Horizontal Scaling Enable Bit**
6	RW	0	**Horizontal Scaling Factor Selection** 0: Original 1: Linear Mode
5:4	RO	0	**Reserved**
3	RW	0	**Vertical; Scaling Enable Bit**
2:0	RO	0	**Reserved**

IO Port / Index: 3X5.A3
Second Display Starting Address Extended **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	0	**IGA2 Frame Buffer Selection** 1x: L.L. 00: S.L. 01: S.F.
3	RO	0	**Reserved**
2:0	RW	0	**Second Display Starting Address Bits [28:26]**

IO Port / Index: 3X5.A5
Second LCD Vertical Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Second LCD Vertical Scaling Factor Bits [8:1]**

IO Port / Index: 3X5.A6
Second LCD Vertical Scaling Factor **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Second Vertical Scaling Factor Bit [0]**
1:0	RW	0	**Second Vertical Scaling Factor Bits [10:9]**

IO Port / Index: 3X5.A7
Expected IGA1 Vertical Display End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Expected IGA1 Vertical Display End Bits [7:0]**

IO Port / Index: 3X5.A8
Expected IGA1 Vertical Display End **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**Expected IGA1 Vertical Display End Bits [10:8]**

IO Port / Index: 3X5.A9
Hardware Gamma Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Hardware 10 bit Gamma Enable**
0	RW	0	**10 Bit Gamma Algorithm LUT256 Index 0 for Color 0** 0: Color 0 always output 10'b0

IO Port / Index: 3X5.AA
FIFO Depth & Threshold Overflow Bit **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**

IO Port / Index: 3X5.AB
IGA2 Interlace Half Line Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**IGA2 Interlace Half Line Register Bits [7:0]**

IO Port / Index: 3X5.AC
IGA2 Interlace Half Line Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**IGA2 Interlace Half Line Register Bits [10:8]**

IO Port / Index: 3X5.AF
P-Arbiter Write Expired Number Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**P-Arbiter Write Expired Number Bits [4:0]**

IO Port / Index: 3X5.D0
LVDS PLL Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D1
DVI PLL Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D2
LVDS / DVI Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D3
Second Power Sequence Control Register 0 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D4
Second Power Sequence Control Register 1 **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D5
LVDS Testing Mode Control Register **Default Value: 00h**
Refer to LVDS / DVI chapter for more details

IO Port / Index: 3X5.D6
DCVI (Digital Component Video Interface) Control Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DCVI Data Testing Mode** 0: Disable 1: Enable
6	RW	0	**DCVI Format Selection** 0: 656 or 601 output 1: 20 bit output
5	RW	0	**DCVI Format Source Selection High Bit** 0: Reference Rx3X5.9B[4] 1: P2I mode
4	RO	0	**Reserved**
3	RW	0	**DCVI Output Format Selection** 0: Original 1: TV5 mode
2	RW	0	**DCVI Dither Enable**
1	RW	0	**DCVI Color Space Convert Enable**
0	RW	0	**DCVI Enable** 0: Off 1: On

IO Port / Index: 3X5.D7
DCVI Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**DCVI Output Field Polarity** 0: Original 1: Invert
2:0	RW	0	**DCVI Field Delay Lines After Vertical Blank Start**

IO Port / Index: 3X5.D8
PLL Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**VCO (Voltage Controlled Oscillator) Mode 3 (INTLCDCK)** PLL Output Frequency Select: 1X or 2X 0: 1X 1: 2X
6	RW	0	**VCO Mode 2 (INTECK)** PLL Output Frequency Select: 1X or 2X 0: 1X 1: 2X
5	RW	0	**VCO Mode 1 (INTVCK)** PLL Output Frequency Select: 1X or 2X 0: 1X 1: 2X
4:0	RO	0	**Reserved**

IO Port / Index: 3X5.D9
Scaling Down Source Data Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scaling Down Source Data Horizontal Offset Bits [7:0]** Unit: pixel (2P)

IO Port / Index: 3X5.DA
Scaling Down Source Data Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scaling Down Source Data Vertical Offset Bits [7:0]** Unit: pixel (2P)

IO Port / Index: 3X5.DB
Scaling Down Source Data Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:3	RW	0	**Scaling Down Source Data Vertical Offset Bits [10:8]** Unit : pixel (2P)
2:0	RW	0	**Scaling Down Source Data Horizontal Offset Bits [10:8]** Unit : pixel (2P)

IO Port / Index: 3X5.DC
Scaling Down Horizontal Scale Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Scale Factor Bits [7:0]**

IO Port / Index: 3X5.DD
Scaling Down Horizontal Scale Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DN Flip Select**
6	RW	0	**Horizontal Scale Down Enable** 0: Disable 1: Enable
5:0	RW	0	**Horizontal Scale Factor Bits [13:8]**

IO Port / Index: 3X5.DE

Scaling Down Vertical Scale Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Scale Factor Bits [7:0]**

IO Port / Index: 3X5.DF

Scaling Down Vertical Scale Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Vertical Scale Down Enable** 0: Disable 1: Enable
5:0	RW	0	**Vertical Scale Factor Bits [13:8]**

IO Port / Index: 3X5.E0

Scaling Down Destination Frame Buffer Starting Address 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 0 Bits [10:3]**

IO Port / Index: 3X5.E1

Scaling Down Destination Frame Buffer Starting Address 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 0 Bits [18:11]**

IO Port / Index: 3X5.E2

Scaling Down Destination Frame Buffer Starting Address 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 0 Bits [26:19]**

IO Port / Index: 3X5.E3

Scaling Down Destination Frame Buffer Starting Address 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**RGB Scale Down** 00b: RGB32 01b: RGB8 10b: RGB565 11b: RGB10
5:4	RW	0	**SW Source Frame Buffer Stride Bits [9:8]**
3:2	RW	0	**Reserved**
1:0	RW	0	**Destination Frame Buffer Starting Address 0 Bits [28:27]**

IO Port / Index: 3X5.E4

Scaling Down SW Source Frame Buffer Stride **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SW Source Frame Buffer Stride Bits [7:0]** Unit: 16 bytes

IO Port / Index: 3X5.E5

Scaling Down Destination Frame Buffer Starting Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 1 Bits [10:3]**

IO Port / Index: 3X5.E6

Scaling Down Destination Frame Buffer Starting Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 1 Bits [18:11]**

IO Port / Index: 3X5.E7

Scaling Down Destination Frame Buffer Starting Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 1 Bits [26:19]**

IO Port / Index: 3X5.E8

Scaling Down Destination Frame Buffer Starting Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Which IGA Run Scaling Down** 0:IGA1 1:IGA2
6	RW	0	**Line Flip Enable** 0: Disable 1: Enable
5	RW	0	**Flip** IGA2 can start to get next frame.
4	RW	0	**Scaling Down Enable** 0: Disable 1: Enable
3:2	RW	0	**Destination Frame Buffer Starting Address 2 Bits [28:27]**
1:0	RW	0	**Destination Frame Buffer Starting Address 1 Bits [28:27]**

IO Port / Index: 3X5.E9

Scaling Down Destination Frame Buffer Starting Address 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 2 Bits [10:3]**

IO Port / Index: 3X5.EA

Scaling Down Destination Frame Buffer Starting Address 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 2 Bits [18:11]**

IO Port / Index: 3X5.EB

Scaling Down Destination Frame Buffer Starting Address 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Destination Frame Buffer Starting Address 2 Bits [26:19]**

IO Port / Index: 3X5.EC

IGA1 Down Scaling Destination Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**IGA1 Down Scalar Line Flip**
1	RW	0	**IGA1 Down Scalar Flip**
0	RW	0	**IGA1 Down Scalar Enable**

IO Port / Index: 3X5.F0

Snaphot Mode – Starting Address of Display Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Snapshot Mode TVPK_SRC Bits [11:4]**

IO Port / Index: 3X5.F1

Snapshot Mode – Starting Address of Display Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Snapshot Mode TVPK_SRC Bits [19:12]**

IO Port / Index: 3X5.F2

Snapshot Mode – Starting Address of Display Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Snapshot Mode TVPK_SRC Bits [27:20]**

IO Port / Index: 3X5.F3

Snapshot Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVP1 Device Type Selection** 0: Normal LCD 1: 18-bit TTL LCD
6	RW	0	**Snapshot Mode TVPK_SRC Bit [28]**
5	RW	0	**SW Set NM and GFX Entering Snapshot in C0 State** 0: Disable 1: Enable
4	RW	0	**Snapshot Mode** 0 : Mode 0 1 : Mode 1
3	RO	0	**Snapshot PLL Wakeup Setting** 0: Counter (2ms) 1: PLL_OK
2	RW	0	**Snapshot Mode Enable** 0: Disable 1: Enable GFX support Snapshot mode.
1	RW	0	**Enable GFX PLL Power Off When In Snapshot Mode** 0: Disable 1: Enable
0	RO	0	**The VSYNC and HSYNC of DAC0 Are Tied** 0: VSYNC and HSYNC are normal 1: Tied

IO Port / Index: 3X5.F4

Snapshot Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Reserved**

IO Port / Index: 3X5.F5

Snapshot Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**The VSYNC and HSYNC of DAC1 Are Tied** 0: VSYNC and HSYNC are normal 1: Tied
6:0	RW	0	**Reserved**

IO Port / Index: 3X5.F6
Snapshot Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**The VSYNC Count While Engine Is Idle and SW Enables Snapshot** In C0 state, the idle VSYNC count to disable the Rx3X5.F3[5].

IO Port / Index: 3X5.F7
Internal Spread Spectrum Control CH 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Select Internal/External Clock Source** 0: External 1: Internal
6	RW	0	**Power Down Control** 0: Disable 1: Enable
5:4	RW	0	**Input Clock Frequency Select** See Input Clock Frequency Selection Table below.
3:2	RW	0	**Spreading Range Select** See Modulation Selection Table below.
1	RW	0	**Modulation Rate Select** See Modulation Selection Table below.
0	RW	0	**Spread Spectrum Enable** 0: Disable 1: Enable (3C5.7D[2] or [0] must be 1)

Modulation Selection Table

MF_SEL	SR_SEL[1:0]	Spreading Range	Modulation Rate (KHz)
0	00	± 0.5%	Fin/1152
0	01	± 0.75%	Fin/1152
0	10	± 1.00%	Fin/1152
0	11	± 1.25%	Fin/1152
1	00	Reserved	Reserved
1	01	Reserved	Reserved
1	10	± 1.00%	Fin/1920
1	11	± 1.25%	Fin/1920

Input Clock Frequency Selection Table

Input Clock Range	FREQ_SEL[1:0]
25~40MHz	00
40~65MHz	01
65~110MHz	10
110~135MHz	11

IO Port / Index: 3X5.F9
V1 Power Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**V1 Mode Exit-to-Ready Time Control** The period between NB trigger GFX to exit V1 power mode and GFX really exit V1 power mode. (Unit: frame)

IO Port / Index: 3X5.FA
V1 Power Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**V1 Mode Status** This bit is sent to SB when GFX is in V1 power mode. This bit is set to 1'b1 by HW and reset to 1'b0 by SW.

IO Port / Index: 3X5.FB

IGA2 Interlace VSYNC Timing Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**The Offset Cycle of VSYNC[7:0]**

IO Port / Index: 3X5.FC

IGA2 Interlace VSYNC Timing Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**The Offset Cycle of VSYNC[10:8]**

2D ENGINE REGISTER SPACE

This chapter provides 2D register summary table and detailed graphics engine register descriptions.

2D Engine Register Summary Table

These 2D engine register table documents the MMIO offset , register function and register attribute for each register.

Please note that the actual address equals to MB1 (MMIO Base Address) + Offset Address. MB1 is declared in the register with offset address 17h-14h in the PCI configuration space.

Table 9. Graphics Engine Registers

Offset (hex)	2D Engine Registers	Attribute
03-00	GE Command	RW
07-04	GE Mode and Status	RW
0B-08	Pitch & FB Location	RW
0F-0C	Destination Dimension	RW
13-10	BitBLT Destination Address	RW
17-14	Destination Map Base Address	RW
1B-18	BitBLT Source Address	RW
1F-1C	Source Map Base Address	RW
23-20	Pattern Address	RW
27-24	Mono Pattern Data Port 0 or Style Line Mask	RW
2B-28	Mono Pattern Data Port 1	RW
2F-2C	Error Term of Line Draw	RW
33-30	Color Format Conversion (CFC)	RW
43-40	Clipping Window Top and Left Limit	RW
47-44	Clipping Window Bottom and Right Limit	RW
4B-48	Color Key and Chroma Key Control	RW
4F-4C	Foreground Color or Destination Color Key or Line Color or Rectangle Fill Color	RW
53-50	Background Color or Source Color key or Chroma Key Upper Bound	RW
5B-58	Foreground Color of Pattern or Fix Color of Pattern	RW
5F-5C	Background Color of Pattern	RW
60	3D / 2D ID Control	WO
6C	3D / 2D Wait Control	WO
6D-9F	Reserved	RO
1FF-100	Color Pattern RAM Port 0 – Port 63	WO

Graphics Engine Register Descriptions

This section provides detailed register descriptions for the 2D graphics engine.

Offset Address: 03-00h

GE Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**Raster Operation Code (ROP code)**
23	RW	0	**Quick Start Enable** 0: Disable 1: Enable When enabled, a command will be kicked off when a command writes to register 10h, saving one command write instruction.
22	RW	0	**Pattern Keep** 0: Must get somewhere (bitmap pattern register or frame buffer) to pattern RAM. 1: Current pattern RAM (directly use pattern RAM data without filling it again).
21	RW	0	**Line Draws Major** 0: X major 1: Y major
20	RW	0	**Line Draw Last Pixel Turn On Disable** 0: Enable, draw the last pixel or not. 1: Disable, do not draw the last pixel.
19:18	RW	0	**Monochrome Data Next Line Alignment Type (if Alignments Enable)** 00: Byte 01: Reserved 10: Dword 11: Reserved
17	RW	0	**Monochrome Data Alignment Enable** 0: Disable 1: Enable
16	RW	0	**Monochrome Pattern Transparency Enable** 0: Opaque 1: Transparency
15	RW	0	**Destination X-Direction Select** 0: Increment 1: Decrement
14	RW	0	**Destination Y-Direction Select** 0: Increment 1: Decrement
13	RW	0	**Fix Color Pattern** 0: Normal 1: Fix Color
12	RW	0	**Clipping Enable** 0: Disable 1: Enable
11	RW	0	**Pattern Source Select** 0: Pattern from frame buffer 1: Pattern from pattern register
10	RW	0	**Monochrome Source Transparency Enable** 0: Opaque 1: Transparency
9	RW	0	**Pattern Data Format** 0: Color 1: Monochrome
8	RW	0	**Source Data Format** 0: Color 1: Monochrome
7	RO	0	**Reserved**
6	RW	0	**Source Select** 0: On-screen frame buffer 1: From host
5:4	RW	0	**Reserved**
3:0	RW	0	**GE Command Select** 0000: No operation 0001: Bit BLT 0010: Text (mono, ROP == CC) 0101: Bresenham line draw 1001: Bitblt then rotate 1010: Text (mono, ROP == CC) then rotate Others: Reserved

Offset Address: 07-04h

GE Mode and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:10	RO	0	**Reserved**
9:8	RW	0	**Destination Color Depth Select** 00: 8 bpp 01: 16 bpp 10: Reserved 11: 32 bpp
7:2	RO	0	**Reserved**
1:0	RW	0	**Rotation Angle (Hardware: 90=270, diff. X/YDIR)** 00: Rotate 0 degree. 01: Rotate anticlockwise 90 degree. 10: Rotate anticlockwise 180 degree. 11: Rotate anticlockwise 270 degree.

Offset Address: 0B-08h

Pitch and FB Location **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	0	**Destination FB Location** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
29:27	RO	0	**Reserved**
26:16	RW	0	**Destination Pitch; 64-bit Address (128 Bit Alignment).**
15:14	RW	0	**Pattern FB Location** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
13:12	RW	0	**Source FB Location** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
11	RO	0	**Reserved**
10:0	RW	0	**Source Pitch** 64-bit address (128-bit alignment).

Offset Address: 0F-0Ch

Destination Dimension **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	These bits specify the destination rectangle height (value = height – 1) for the BitBLT operation.
15:12	RO	0	**Reserved**
11:0	RW	0	These bits specify the destination rectangle width (value = width – 1) for the BitBLT operation.

Offset Address: 13-10h

BitBLT Destination Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Destination Tile Add Control** 0: Normal 1: Tile
30:28	RO	0	**Reserved**
27:16	RW	0	**BitBILT Destination Address** For BitBLT, bits [27:16] specify the destination y-position.
15:12	RW	0	**Reserved**
11:0	RW	0	**BitBILT Destination Address** For BitBLT, bits [11:0] specify the destination x-position operation.

Offset Address: 17-14h

Destination Map Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:0	RW	0	**Destination Map Base Address** 64-bit address (128-bit alignment).

Offset Address: 1B-18h

BitBLT Source Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Source Tile Add Control** 0: Normal 1: Tile
30	RO	0	**Reserved**
29:16	RW	0	**BitBILT Source Address** These bits are used for three different commands: 1. For color or mono BitBLT, bits [27:16] specify the source y-position (XY based). 2. For line draw, bits [29:16] specify the axial step (K1 term of Bresenham line draw).
15:0	RW	0	**BitBILT Source Address** These bits are used for three different commands: 1. For color BitBLT, bits [11:0] specify the source x-position (XY based). 2. For mono BitBLT, bits [14:0] specify the source x-position. 3. For line draw, bits [13:0] specify the diagonal step (K2 term of Bresenham line draw).

Offset Address: 1F-1Ch

Source Map Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:0	RW	0	**Source Base Address** 64-bit address (128 bit alignment).

Offset Address: 23-20h

Pattern Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Pattern Offset** Bits [31:29]: Start line(Y) location (0~7) Bits [28:26]: 1. Pattern from frame buffer : Start location(X) in a line (0~7) 2. Pattern from frame host : Dest. start location(X) in a line (0~7)
25:0	RW	0	**Pattern Base Address** These bits are used for the following purpose: For 8x8 pattern, bit [25:0] specify the 8x8 pattern address stored in the off-screen frame buffer, 64-bit address (128 bit alignment).

Offset Address: 27-24h

Mono Pattern Data Port 0 or Style Line Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Pattern 0** For mono pattern, specify the Pattern 0 **Style Line Mask** For line draw, specify the style line

Offset Address: 2B-28h

Mono Pattern Data Port 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Pattern 1**

Offset Address: 2F-2Ch

Error Term of Line Draw **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Error Term for Textured Line** The error term for textured line
15:14	RO	0	**Reserved**
13:0	RW	0	**Error Term** The error term for line

Offset Address: 34-30h

Color Format Conversion (CFC) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Color Format Conversion Enable** When disabled, the engine will ignore Source Color depth (Bit[7:6]), set Source Color depth = Dest. Color depth & set Source Color format = Dest. Color format.
30	RW	0	**CFC Extending Mode (Excluding Alpha)** For Alpha channel, always extended with high color bit 0: Extending with high color bit 1: Extending with zero
29	RW	0	**CFC Dither Mode** 0: Dither Table 1: Rounding
28:10	RO	0	**Reserved**
9:8	RW	0	**Destination Color Format** 16BPP: 00: RGB555 (Bit[14:10] = R, Bit[9:5] = G, Bit[4:0] = B) 01: RGB565 (Bit[15:11] = R, Bit[10:5] = G, Bit[4:0] = B) 1x: Reserved 32BPP: 00: ARGB8888 (Bit[31:24] = A, Bit[23:16] = R, Bit[15:8] = G, Bit[7:0] = B) 01: ARGB2_10_10_10 (Bit[31:30] = A, Bit[29:20] = R, Bit[19:10] = G, Bit[9:0] = B) 1x: Reserved
7:6	RW	0	**Source Color Depth Select** 00: 8bpp 01: 16bpp 10: Reserved 11: 32bpp
5:2	RO	0	**Reserved**
1:0	RW	0	**Source Color Format** *For 16BPP*: 00: RGB555 (Bit[14:10] = R, Bit[9:5] = G, Bit[4:0] = B) 01: RGB565 (Bit[15:11] = R, Bit[10:5] = G, Bit[4:0] = B) 1x: Reserved *For 32BPP:* 00: ARGB8888 (Bit[31:24] = A, Bit[23:16] = R, Bit[15:8] = G, Bit[7:0] = B) 01: ARGB2_10_10_10 (Bit[31:30] = A, Bit[29:20] = R, Bit[19:10] = G, Bit[9:0] = B) 1x: Reserved

Note:

1. Only support ROP = cc (source copy). The engine will transfer ROP code to 8'hcc, when Color Format Conversion enabled.
2. Pattern format is equal to Destination format.
3. Support between 16bpp & 32bpp transfer, not support 8bpp.

32 to 32	No CFC
32 to 16	2_10_10_10 to 555 / 2_10_10_10 to 565 8888 to 555 / 8888 to 565
16 to 32	555 to 2_10_10_10 / 555 to 8888 565 to 2_10_10_10 / 565 to 8888
16 to 16	555 to 565 / 565 to 555

4. When CFC 16bpp to 32Bpp, fill A=8'hFF.

Offset Address: 3F-34h – Reserved

Offset Address: 43-40h

Clipping Window Top and Left Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	For clipping operation, these bits specify the top limit.
15:12	RO	0	**Reserved**
11:0	RW	0	For clipping operation, these bits specify the left limit.

Offset Address: 47-44h

Clipping Window Bottom and Right Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	For clipping operation, these bits specify the bottom limit.
15:12	RO	0	**Reserved**
11:0	RW	0	For clipping operation, these bits specify the right limit.

Offset Address: 4B-48h

Color Key and Chroma Key Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**The Byte Mask of 32 bpp in Rectangle Fill Mode.** 0: Write 1: Not write (mask)
27:16	RO	0	**Reserved**
15	RW	0	**Destination Key Select** 0: Disable 1: Enable
14	RW	0	**Source Key Select** 0: Disable 1: Enable
13:0	RO	0	**Reserved**

Note 1: In color key case:
a) Source color always write if diff/not match,
b) Destination color always write if same/match
c) Always ignore Alpha compare.(Alpha does not be updated to Destination)

Note 2: In transparency case:
a) Source and Pattern always write if same/match
b) Alpha channel update rule is same as RGP channel (Always compare Alpha).

Offset Address: 4F-4Ch

Foreground Color or Destination Color Key or Line Color or Rectangle Fill Color **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	For each bpp mode, bits [bpp-1:0] specify foreground color or destination color key.

Note: Alpha channel always pass key compare in 32BPP

Offset Address: 53-50h

Background Color or Source Color Key or Chroma Key Upper Bound **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	For each bpp mode, bits [bpp-1:0] specify background color or source color key or chroma key upper bound.

Note: Alpha channel always pass key compare in 32BPP

Offset Address: 54-57h – Reserved

Offset Address: 5B-58h

Foreground Color of Pattern or Fix Color of Pattern **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Foreground Color of Mono Pattern** **Or Color of Fix Color Pattern (for Rx03-00[13])**

Offset Address: 5F-5Ch

Background color of Pattern **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Background Color of Mono Pattern**

3D / 2D Control Registers (60-6Ch)

Offset Address: 60h

3D / 2D ID Control - *Refer to CR Chapter's "CR Registers in 2D Register Space" for more details*

Offset Address: 6Ch

3D / 2D Wait Control - *Refer to CR Chapter's "CR Registers in 2D Register Space" for more details*

Offset Address: 9F-6Dh – Reserved

Offset Address: 1FF-100h

Color Pattern RAM Port 0 – Port 63 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	WO	0	**Color Pattern Data**

DMA REGISTERS

This chapter provides detailed DMA register summary table and register descriptions are followed in the sequent section.

DMA Registers

These DMA register tables document the MMIO offset , register function and register attribute for each register.

Table 10. DMA Controller Operation Registers (by Offset)

Offset (Hex)	DMA Controller Operation Registers	Attribute
03-00	Channel 0 Mode (MR0)	RW
07-04	Channel 0 Command / Status (CSR0)	RW
0B-08	Channel 1 Mode (MR1)	RW
0F-0C	Channel 1 Command / Status (CSR1)	RW
13-10	Channel 2 Mode (MR2)	RW
17-14	Channel 2 Command / Status (CSR2)	RW
1B-18	Channel 3 Mode (MR3)	RW
1F-1C	Channel 3 Command / Status (CSR3)	RW
23-20	Memory Address Low Register of Channel 0 (MARL0)	RW
27-24	Memory Address High Register of Channel 0 (MARH0)	RW
2B-28	Channel 0 Device Address (DAR0)	RW
2F-2C	Double Quad-Word Count Register of Channel 0 (DQWCR0)	RW
33-30	Tile Mode Register of Channel 0 (TMR0)	RW
37-34	Descriptor Pointer Low Register of Channel 0 (DPRL0)	RW
3B-38	Descriptor Pointer High Register of Channel 0 (DPRH0)	RW
43-40	Memory Address Low Register of Channel 1 (MARL1)	RW
47-44	Memory Address High Register of Channel 1 (MARH1)	RW
4B-48	Channel 1 Device Address (DAR1)	RW
4F-4C	Double Quad-Word Count Register of Channel 1 (DQWCR1)	RW
53-50	Tile Mode Register of Channel 1 (TMR1)	RW
57-54	Descriptor Pointer Low Register of Channel 1 (DPRL1)	RW
5B-58	Descriptor Pointer High Register of Channel 1 (DPRH1)	RW
63-60	Memory Address Low Register of Channel 2 (MARL2)	RW
67-64	Memory Address High Register of Channel 2 (MARH2)	RW
6B-68	Device Address Register of Channel 2 (DAR2)	RW
6F-6C	Double Quad-Word Count Register of Channel 2 (DQWCR2)	RW
73-70	Tile Mode Register of Channel 2 (TMR2)	RW
77-74	Descriptor Pointer Low Register of Channel 2 (DPRL2)	RW
7B-78	Descriptor Pointer High Register of Channel 2 (DPRH2)	RW
83-80	Memory Address Low Register of Channel 3 (MARL3)	RW
87-84	Memory Address High Register of Channel 3 (MARH3)	RW
8B-88	Channel 3 Device Address (DAR3)	RW
8F-8C	Double Quad-Word Count Register of Channel 3 (DQWCR3)	RW
93-90	Tile Mode Register of Channel 3 (TMR3)	RW
97-94	Descriptor Pointer Low Register of Channel 3 (DPRL3)	RW
9B-98	Descriptor Pointer High Register of Channel 3 (DPRH3)	RW
123-120	Byte Enable Register of Channel 0 (BER0)	RW
127-124	Destination Dimension Register of Channel 0 (DDR0)	RW
12B-128	Pitch Memory Address Low Register of Channel 0 (PMARL0)	RW
12F-12C	Pitch Memory Address High Register of Channel 0 (PMARH0)	RW
133-130	Pitch Device Address Register of Channel 0 (PDAR0)	RW
137-134	Pitch Mode Register of Channel 0 (PMR0)	RW

Offset (Hex)	DMA Controller Operation Registers	Attribute
143-140	Byte Enable Register of Channel 1 (BER1)	RW
147-144	Destination Dimension Register of Channel 1 (DDR1)	RW
14B-148	Pitch Memory Address Low Register of Channel 1 (PMARL1)	RW
14F-14C	Pitch Memory Address High Register of Channel 1 (PMARH1)	RW
153-150	Pitch Device Address Register of Channel 1 (PDAR1)	RW
157-154	Pitch Mode Register of Channel 1 (PMR1)	RW
163-160	Byte Enable Register of Channel 2 (BER2)	RW
167-164	Destination Dimension Register of Channel 2 (DDR2)	RW
16B-168	Pitch Memory Address Low Register of Channel 2 (PMARL2)	RW
16F-16C	Pitch Memory Address High Register of Channel 2 (PMARH2)	RW
173-170	Pitch Device Address Register of Channel 2 (PDAR2)	RW
177-174	Pitch Mode Register of Channel 2 (PMR2)	RW
183-180	Byte Enable Register of Channel 3 (BER3)	RW
187-184	Destination Dimension Register of Channel 3 (DDR3)	RW
18B-188	Pitch Memory Address Low Register of Channel 3 (PMARL3)	RW
18F-18C	Pitch Memory Address High Register of Channel 3 (PMARH3)	RW
193-190	Pitch Device Address Register of Channel 3 (PDAR3)	RW
197-194	Pitch Mode Register of Channel 3 (PMR3)	RW

Note: ***Port Address = (MB1 + 0x0E00 + Offset Address)***
MB1 is declared in the register with offset address 17h-14h in the PCI configuration space.

Table 11. DMA Controller Operation Registers (by Channel)

Register Name	Channel 0		Channel 1		Channel 2		Channel 3	
	Offset	Register	Offset	Register	Offset	Register	Offset	Register
MRn: Channel n Mode	03-00	MR0	0B-08	MR1	13-10	MR2	1B-18	MR3
CSRn: Channel n Command / Status	07-04	CSR0	0F-0C	CSR1	17-14	CSR2	1F-1C	CSR3
MARLn: Memory Address Low Register of Channel n	23-20	MARL0	43-40	MARL1	63-60	MARL2	83-80	MARL3
MARHn: Memory Address High Register of Channel n	27-24	MARH0	47-44	MARH1	67-64	MARH2	87-84	MARH3
DARn: Channel n Device Address	2B-28	DAR0	4B-48	DAR1	6B-68	DAR2	8B-88	DAR3
DQWCRn: Double Quad-Word Count Register of Channel n	2F-2C	DQWCR0	4F-4C	DQWCR1	6F-6C	DQWCR2	8F-8C	DQWCR3
TMRn: Tile Mode Register of Channel n	33-30	TMR0	53-50	TMR1	73-70	TMR2	93-90	TMR3
DPRLn: Descriptor Pointer Low Register of Channel n	37-34	DPRL0	57-54	DPRL1	77-74	DPRL2	97-94	DPRL3
DPRHn: Descriptor Pointer High Register of Channel n	3B-38	DPRH0	5B-58	DPRH1	7B-78	DPRH2	9B-98	DPRH3
BERn: Byte Enable Register of Channel n	123-120	BER0	143-140	BER1	163-160	BER2	183-180	BER3
DDRn: Destination Dimension Register of Channel n	127-124	DDR0	147-144	DDR1	167-164	DDR2	187-184	DDR3
PMARLn: Pitch Memory Address Low Register of Channel n	12B-128	PMARL0	14B-148	PMARL1	16B-168	PMARL2	18B-188	PMARL3
PMARHn: Pitch Memory Address High Register of Channel n	12F-12C	PMARH0	14F-14C	PMARH1	16F-16C	PMARH2	18F-18C	PMARH3
PDARn: Pitch Device Address Register of Channel n	133-130	PDAR0	153-150	PDAR1	173-170	PDAR2	193-190	PDAR3
PMRn: Pitch Mode Register of Channel n	137-134	PMR0	157-154	PMR1	177-174	PMR2	197-194	PMR3

DMA Operation Registers Description

Following registers are the DMA Operation registers used to control the operation of the DMA controller. Address space mentioned in the following registers is the offset address based on DMA base address.

Offset Address: {MR0 = 00h, MR1 = 08h, MR2 = 10h, MR3 = 18h}
Mode Register (MRn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RO	0	**Reserved**
1	RW	0	**Transfer Done Interrupt Enable (TDIE)** A value of 1 enables the interrupt to be generated when transfer is done.
0	RW	0	**Chaining Mode (CM)** A value of 1 causes the DMA controller to operate in chaining mode.

Offset Address: {CSR0 = 04h, CSR1 = 0Ch, CSR2 = 14h, CSR3 = 1Ch}
Command / Status Register (CSRn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3	RW1C	0	**Transfer Done (TD)** A value of 1 indicates that the transfer of this channel is complete. Writing a 1 will clear this bit and the interrupt due to this event when TDIE is set to 1. This field can ONLY be written from CBU path.
2	RW	0	**Transfer Abort (TA)** Writing a 1 to this bit causes the channel to abort the current transfer. This channel transfer done bit is set when the abort is complete. Reading this bit always gets 0. This field can ONLY be written from CBU path.
1	RW	0	**Transfer Start (TS)** Writing a 1 to this bit causes the channel to start transferring data if the channel is enabled. Reading this bit always gets 0.
0	RW	0	**DMA Enable (DE)** A value of 1 enables this DMA channel.

Offset Address: {MARL0 = 20h, MARL1 = 40h, MARL2 = 60h, MARL3 = 80h}
MAR Low 28-Bit Register (MARLn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RW	0	**Memory Address Lower 28 bits (MAL)** This field indicates the starting memory address (lower 28 bits) of a DMA transfer. The unit is 128-bit.
3:0	RO	0	**Reserved**

Offset Address: {MARH0 = 24h, MARH1 = 44h, MARH2 = 64h, MARH3 = 84h}
MAR High 12-Bit Register (MARHn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:0	RW	0	**Memory Address Higher 12 bits (MAH)** This field indicates the starting memory address (higher 12 bits) of a DMA transfer. The unit is byte.

Offset Address: {DAR0 = 28h, DAR1 = 48h, DAR2 = 68h, DAR3 = 88h}

Device Address Register (DARn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	0	**Device Addressing Type (DAT)** This field indicates the memory translation type of the starting device address of a DMA transfer. 00: System local frame buffer (S.L.) 01: System dynamic frame buffer (S.F.) 10: Reserved (Do not use) 11: Local memory / Local frame huffer (L.L.)
29	RO	0	**Reserved**
28:4	RW	0	**Device Address (DA)** This field indicates the starting device address of a DMA transfer. In the Tile Mode transfer, this filed must point to the starting address of memory tile.
3:0	RO	0	**Reserved**

Offset Address: {DQWCR0 = 2Ch, DQWCR1 = 4Ch, DQWCR2 = 6Ch, DQWCR3 = 8Ch}

Double Quad-word Count Register (DQWCRn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24:0	RW	0	**Double Quad-Word Count (DQWC)** This field indicates the number of 16-byte count to be transferred during a DMA transfer. It will be cleared when the transfer is done by hardware.

Offset Address: {TMR0 = 30h, TMR1 = 50h, TMR2 = 70h, TMR3 = 90h}

Tile Mode Register (TMRn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Tile Mode Enable (TME)** A value of 1 enables tile mode memory mapping for the coming device memory transfer.
30:28	RO	0	**Reserved**
27:24	RW	0	**Tile Mode Index (TMI)** This field indicates the starting location of the current tile for the current transfer descriptor. It will be cleared when the transfer is done by hardware. This filed is used ONLY in the tile mode, otherwise this field is reserved.
23:16	RW	0	**Tile Mode Pitch Count (TMPC)** This field indicates the pitch count for the tile mode transfer. A value of 8'h00 indicates the maximum pitch count, 256. This filed is used ONLY in the tile mode.
15:8	RO	0	**Reserved**
7:0	RW	0	**Tile Mode Horizontal Tile Index (TMHTI)** This field indicates the horizontal tile index for the tile mode transfer. This filed is used ONLY in the tile mode.

Offset Address: {DPRL0 = 34h, DPRL1 = 54h, DPRL2 = 74h, DPRL3 = 94h}

DPR Low 32-Bit Register (DPRLn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RW	0	**Next Descriptor Address Lower 28 bits (NDAL)** This field indicates the lower 28 bits of the double quad-word aligned address of the next descriptor.
3	RW	0	**Direction of Transfer (DT)** A value of 1 indicates transfers from memory to PCI device. A value of 0 indicates transfers from PCI device to memory.
2	RO	0	**Reserved**
1	RW	0	**End of Chain (EC)** A value of 1 indicates the end of chain.
0	RO	0	**Reserved**

Offset Address: {DPRH0 = 38h, DPRH1 = 58h, DPRH2 = 78h, DPRH3 = 98h}
DPR High 12-Bit Register (DPRHn) **Default Value: 000F 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23-20	RW	0	**DMA Transaction Starting Memory Address Lower 4 bits (SB1)** This field indicates the starting memory address (lower 4 bits) of a DMA transfer. The unit is BYTE. Note: The byte-addressing feature can be applied to non-chaining mode DMA transfer ONLY. In chaining-mode DMA, this field must be set to 0.
19-16	RW	Fh	**DMA Transaction Ending Memory Address Lower 4 bits (EB1)** This field indicates the ending memory address (lower 4 bits) of a DMA transfer. The unit is BYTE. Note: The byte-addressing feature can be applied to non-chaining mode DMA transfer ONLY. In chaining-mode DMA, this field must be set to 0Fh.
15:12	RO	0	**Reserved**
11:0	RW	0	**Next Descriptor Address Higher 12 bits (NDAH)** This field indicates the higher 12 bits of the double quad-word aligned address of the next descriptor.

Offset Address: {BER0 = 120h, BER1 = 140h, BER2 = 160h, BER3 = 180h}
Byte Enable Register (BERn) **Default Value: 0000 0F0Fh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:12	RW	0	**DMA Transaction Starting Memory Address Lower 4 bits (SB2)** This field indicates the starting memory address (lower 4 bits) of a DMA destination transfer in unit of BYTE. This filed is used ONLY in the pitch mode.
11:8	RW	Fh	**DMA Transaction Ending Memory Address Lower 4 bits (EB2)** This field indicates the ending memory address (lower 4 bits) of a DMA destination transfer in unit of BYTE. This filed is used ONLY in the pitch mode.
7:4	RW	0	**DMA Transaction Starting Memory Address Lower 4 bits (SB1)** This field indicates the starting memory address (lower 4 bits) of a DMA source transfer in unit of BYTE. This filed is used ONLY in the pitch mode.
3:0	RW	Fh	**DMA Transaction Ending Memory Address Lower 4 bits (EB1)** This field indicates the ending memory address (lower 4 bits) of a DMA source transfer in unit of BYTE. This filed is used ONLY in the pitch mode.

Offset Address: {DDR0 = 124h, DDR1 = 144h, DDR2 = 164h, DDR3 = 184h}
Destination Dimension Register (DDRn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Direction of Moving (DM)** A value of 1 indicates transfers from system memory to frame buffer. A value of 0 indicates transfers from frame buffer to system memory.
30:28	RO	0	**Reserved**
27:16	RW	0	**Destination Rectangle Height (DRH)** The destination rectangle height equals the value in unit of line. When set up this field, BERn must be set first.
15:9	RO	0	**Reserved**
8:0	RW	0	**Destination Rectangle Width (DRW)** The destination rectangle width equals the value in unit of 128-bit. When set up this field, BERn must be set first.

Offset Address: {PMARL0 = 128h, PMARL1 = 148h, PMARL2 = 168h, PMARL3 = 188h}
PMAR Low 28-Bit Register (PMARLn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RW	0	**Pitch Memory Address Lower 28 bits (PMAL)** This field indicates the starting pitch memory address (lower 28 bits) of a DMA transfer in unit of 128 bits.
3:0	RO	0	**Reserved**

Offset Address: {PMARH0 = 12Ch, PMARH1 = 14Ch, PMARH2 = 16Ch, PMARH3 = 18Ch}

PMAR High 12-Bit Register (PMARHn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:0	RW	0	**Pitch Memory Address Higher 12 bits (PMAH)** This field indicates the starting pitch memory address (higher 12 bits) of a DMA transfer in unit of 128 bits.

Offset Address: {PDAR0 = 130h, PDAR1 = 150h, PDAR2 = 170h, PDAR3 = 190h}

Pitch Device Address Register (PDARn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	0	**Pitch Device Addressing Type (PDAT)** This field indicates the memory translation type of the starting pitch device address of a DMA transfer. 00: System local frame buffer (S.L.) 01: System dynamic frame buffer (S.F.) 10: Reserved (Do not use) 11: Local memory / Local frame buffer (L.L.)
29	RO	0	**Reserved**
28:4	RW	0	**Pitch Device Address (PDA)** This field indicates the starting pitch device address of a DMA transfer in unit of 128 bits.
3:0	RO	0	**Reserved**

Offset Address: {PMR0 = 134h, PMR1 = 154h, PMR2 = 174h, PMR3 = 194h}

Pitch Mode Register (PMRn) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Pitch Mode Enable (PME)** A value of 1 enables pitch mode memory mapping for the coming device memory transfer.
30	RW	0	**Pitch support Tile address Mode Enable (PTME)** A value of 1 enables pitch mode memory support tile address mapping for the coming device memory transfer.
29	RO	0	**Reserved**
28	RW	0	**Tile Mode Index of Pitch Destination (DPTMI)** This field indicates the starting location of the current tile for the current transfer descriptor. It will be cleared when the transfer is done by hardware. This filed is used ONLY in the tile mode and move data from system memory to frame buffer, otherwise this field is reserved.
27	RO	0	**Reserved**
26	RW	0	**Tile Mode Index of Pitch Destination (SPTMI)** This field indicates the starting location of the current tile for the current transfer descriptor. It will be cleared when the transfer is done by hardware. This filed is used ONLY in the tile mode and move data from frame buffer to system memory, otherwise this field is reserved.
25	RO	0	**Reserved**
24:16	RW	0	**Destination Pitch Mode Pitch Count (DPMPC)** This field indicates the pitch count for the pitch mode transfer. This filed is used ONLY in the pitch mode.
15	RO	0	**Reserved**
14:11	RW	0	**Frame Buffer Tile Index (FTIX)** This field indicates the index of starting position with frame buffer tile mode.
10:9	RO	0	**Reserved**
8:0	RW	0	**Source Pitch Mode Pitch Count (SPMPC)** This field indicates the pitch count for the pitch mode transfer. This filed is used ONLY in the pitch mode.

CBU ROTATION REGISTERS

This chapter provides detailed CBU register summary table and its detailed register descriptions are followed in the sequent sections.

CBU Registers

The CBU Rotation Function Register Table documents the offset range, register name and register attribute for each Rotate Window Register.

Table 12. CBU Rotation Function Registers

Offset	CDMA Controller Operation Registers	Attribute
1E1F-1E00	Rotate Window Register 0	RW
1E3F-1E20	Rotate Window Register 1	RW
1E5F-1E40	Rotate Window Register 2	RW
1E7F-1E60	Rotate Window Register 3	RW
1E9F-1E80	Rotate Window Register 4	RW
1EBF-1EA0	Rotate Window Register 5	RW
1EDF-1EC0	Rotate Window Register 6	RW
1EFF-1EE0	Rotate Window Register 7	RW
1F1F-1F00	Rotate Window Register 8	RW
1F3F-1F20	Rotate Window Register 9	RW
1F5F-1F40	Rotate Window Register 10	RW
1F7F-1F60	Rotate Window Register 11	RW
1F9F-1F80	Rotate Window Register 12	RW
1FBF-1FA0	Rotate Window Register 13	RW
1FDF-1FC0	Rotate Window Register 14	RW
1FFF-1FE0	Rotate Window Register 15	RW

Note: Rotation Base Address[28:16], Rotation End Address[28:16] and Rotation Source Pitch[21:0] are write-only. Reading these bits always gets 0.

CBU Rotation Registers Description

There are 16 Rotate Window Registers, ranging from Rotate Window Register 0 to Rotate Window Register 15. The table below specifies the standard structure of each Rotate Window Register.

Offset	CDMA Controller Operation Registers	Attribute
03h-00h	Rotate Control 0	RW
07h-04h	Rotate Base Address 0	RW
0Bh-08h	Rotate End Address 0	RW
0Fh-0Ch	Rotate Source Pitch 0	RW
13h-10h	Rotate Pitch 0	RW
17h-14h	Rotate Height and Width 0	RW
1Fh-18h	Reserved	RW

Offset Address: Rotate Window Register Address + (03h-00h)

Rotate Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	0	**Tile Mapping Mode Select** When this bit is set to 1 and bit 6 (Rotate function with tile) is set to 0, 16 x 256 tile mapping mode is used to translate linear address to tiling address. 0: 8 x 256 tile mapping mode 1: 16 x 256 tile mapping mode
6	RW	0	**Rotate Function with Tile** When this bit is set to 1, translated linear address to tiling address within rotation mode is supported.
5	RW	0	**Tile Function Flag** When Rotate Function Enable is set to 1, this bit shows the function which is supported. 0: Rotate function 1: Tile function
4:3	RW	00b	**Rotate Type** 00: No support 01: 90 degrees 10: 180 degrees 11: 270 degrees
2:1	RW	00b	**Rotate Bpp** 00: 8 bpp 01: 16 bpp 1x: 32 bpp
0	RW	0	**Rotate Function Enable** 0: Disable 1: Enable

Offset Address: Rotate Window Register Address + (07h-04h)

Rotate Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:0	RW	0	**Rotate Base Address [28:0]** Bits [3:0] are read only. Unit: byte

Offset Address: Rotate Window Register Address + (0Bh-08h)

Rotate End Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:0	RW	0	**Rotate End Address [28:0]** Bits [3:0] are read only. Unit: byte

Offset Address: Rotate Window Register Address + (0Fh-0Ch)

Rotate Source Pitch **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	**Reserved**
21:0	RW	0	**Rotate Source Pitch Reciprocal** 22 bits (1/source pitch, source pitch unit: pixel) (1/sp = 0.x, for example, source pitch = 256 d, x = 004000h)

Offset Address: Rotate Window Register Address + (13h-10h)

Rotate Pitch **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Rotate Destination Pitch** Unit: pixel Scope: 1 ~ 2048 (0 means 2048)
15:11	RO	0	**Reserved**
10:0	RW	0	**Rotate Source Pitch** Unit: pixel Scope: 1 ~ 2048 (0 means 2048)

Offset Address: Rotate Window Register Address + (17h-14h)

Rotate Height and Width **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Rotate Window Height** Unit: pixel Scope: 1 ~ 2048 (0 means 2048)
15:11	RO	0	**Reserved**
10:0	RW	0	**Rotate Window Width** Unit: pixel Scope: 1 ~ 2048 (0 means 2048)

LVDS / DVI REGISTERS

This chapter is dedicated for detailed LVDS and DVI register descriptions.

IO Port / Index: 3C5.13 [7:6]
Configuration Register 2 (3C5.5A[0]=1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	00b	**Integrated LVDS / DVI Mode Select (Reflects Strapping from Signal DVP1D15/14)** 00: LVDS Channel 1 01: DVI + LVDS2 10: One dual LVDS Channel (high resolution panel) 11: One DVI only (decrease the clock jitter)

IO Port / Index: 3C5.1A [5:4]
PCI Bus Control **Default Value: 00h**

Bit	Attribute	Default	Description
5	RW	0	**DVI Sense** 0: No connection 1: Connected
4	RW	0	**LVDS Sense** 0: No connection 1: Connected

IO Port / Index: 3C5.2B [7:4]
DVI and LVDS Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVI Sense Interrupt Enable** 0: Disable 1: Enable
6	RW1C	0	**DVI Sense Interrupt Status**
5	RW	0	**LVDS Sense Interrupt Enable** 0: Disable 1: Enable
4	RW1C	0	**LVDS Sense Interrupt Status**

IO Port / Index: 3C5.3E
Miscellaneous Register for AGP MUX **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DVI Sense Interrupt Enable** 0: Disable 1: Enable
6	RW1C	0	**DVI Sense Interrupt Status**
5	RW	0	**Inside DVI Sense** 0: No connect 1: Connected
3	RW	0	**PCIe Capability Control Back Door** 0: Capability = 00h 1: Capability = 70h
1	RW	0	**Multi-function Selection** 0: Emulate I2C and DDC bus by GPIO2/3/4 1: Direct ENPVDD/ ENPVEE / ENBLT signals through AGP bus
0	RW	0	**Second DVIDET Sense Signal Source** 0: From LVDS Channel 2 1: From DVP1

IO Port / Index: 3C5.40 [3]
PLL Control **Default Value: 00h**

Bit	Attribute	Default	Description
3	RW	0	**LVDS and DVI Interrupt Method** 0: New method (bypass and low active) 1: Old method

IO Port / Index: 3C5.5B [3:0]
Device Used Status 0 **Default Value: 00h**

Bit	Attribute	Default	Description
3	RO	0	**LVDS0 Use IGA1 Source Flag** 0: Not used 1: Used
2	RO	0	**LVDS0 Use IGA2 Source Flag** 0: Not used 1: Used
1	RO	0	**LVDS1 Use IGA1 Source Flag** 0: Not used 1: Used
0	RO	0	**LVDS1 Use IGA2 Source Flag** 0: Not used 1: Used

IO Port / Index: 3C5.78 [6:3]
Backlight Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
6	RW	0	**Inverse IGA2 HSYNC to LVDS** 0: Disable 1: Enable
5	RW	0	**Inverse IGA2 VSYNC to LVDS** 0: Disable 1: Enable
4	RW	0	**Inverse IGA1 HSYNC to LVDS** 0: Disable 1: Enable
3	RW	0	**Inverse IGA1 VSYNC to LVDS** 0: Disable 1: Enable

IO Port / Index: 3C5.7D [7:5]
Transmitter Power Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Real PD1 Polarity** 0: The real PD3 polarity is the inverse of 3X5.D2[7] 1: The real PD3 polarity is equal to 3X5.D2[7]
6	RW	0	**Real PD2 Polarity** 0: The real PD2 polarity is the inverse of 3X5.D2[6] 1: The real PD2 polarity is equal to 3X5.D2[6]
5	RW	0	**Real PD3 Polarity** 0: The real PD1 polarity is the inverse of 3X5.D2[3] 1: The real PD1 polarity is equal to 3X5.D2[3]

IO Port / Index: 3X5.6A [3]
Second Display Channel and LCD Enable **Default Value: 00h**

Bit	Attribute	Default	Description
3	RW	0	**First Hardware Power Sequence** 0: Off 1: On

IO Port / Index: 3X5.88
LCD Panel Type **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**LVDS First Channel 1 Output Format** 0: Rotation 1: Sequential
5	RW	0	**Flip Strategy** 0: By frame 1: By line
4:1	RO	0	**Reserved**
0	RW	0	**LVDS Channel 1 Output Bits** 0: 24 bits 1: 18 bits

IO Port / Index: 3X5.97
LVDS Channel 2 Function Select 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:5	RW	0	**Reserved**
4	RW	0	**LVDS Channel 2 Data Source Selection** 0: Primary display 1: Secondary display
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.98
LVDS Channel 2 Function Select 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Reserved**
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.99
LVDS Channel 1 Function Select 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**LVDS Channel 1 Data Source Selection** 0: Primary display 1: Secondary display
3:0	RO	0	**Reserved**

IO Port / Index: 3X5.D0
LVDS PLL Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PLL1 Reference Clock Edge Select Bit** 0: PLLCK lock to rising edge of reference clock 1: PLLCK lock to falling edge of reference clock
6:5	RW	0	**PLL1 Charge Pump Current Select Bits** 00: ICH = 12.5 uA 01: ICH = 25.0 uA 10: ICH = 37.5 uA 11: ICH = 50.0 uA
4:3	RO	0	**Reserved**
2:0	RW	0	**Reserved**

IO Port / Index: 3X5.D1

DVI PLL Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RO	0	**Reserved**
1	RO	0	**TX PLL1 Ready** 0: Not ready 1: Ready
0	RW	0	**Reserved**

IO Port / Index: 3X5.D2

LVDS / DVI Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Power Down (Active High) for Channel 1 LVDS** 0: Disable 1: Enable The output polarity is controlled by 3C5.7D[7].
6	RW	0	**Power Down (Active High) for Channel 2 LVDS** 0: Disable 1: Enable The output polarity is controlled by 3C5.7D[6].
5:4	RW	0	**Display Channel Select** 00: LVDS Channel 1 Others: Reserved
3	RW	0	**Enable LVDSENVDD Pad Output** 0: Disable 1: Enable
2	RW	0	**Reserved**
1	RW	0	**LVDS Channel 1 Format Selection** 0: SPWG mode 1: OPENLDI mode
0	RW	0	**Reserved**

IO Port / Index: 3X5.D3

Second Power Sequence Control Register 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Software Direct On / Off Display Period in the Panel Path** 0: On 1: Off
6	RW	0	**Software On / Off Back Light Directly** 0: On 1: Off
5	RW	0	**Software Direct On / Off Display Period on DVP1 Port** 0: On 1: Off
4	RW	0	**Software VDD On**
3	RW	0	**Software Data On**
2	RW	0	**Software VEE On**
1	RW	0	**Software Back Light On**
0	RW	0	**Hardware or Software Control Power Sequence** 1: Software Control

IO Port / Index: 3X5.D4

Second Power Sequence Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LVDS Second Channel2 Output Format** 0: Rotation 1: Sequential
6	RW	0	**LVDS Second Channel2 Output Bits** 0: 24 bits 1: 18 bits
5:2	RO	0	**Reserved**
1	RW	0	**Secondary Power Hardware Power Sequence Enable** 0: Off 1: On
0	RW	0	**Power Sequence Timer Selection** 0: First 1: Second

IO Port / Index: 3X5.D5

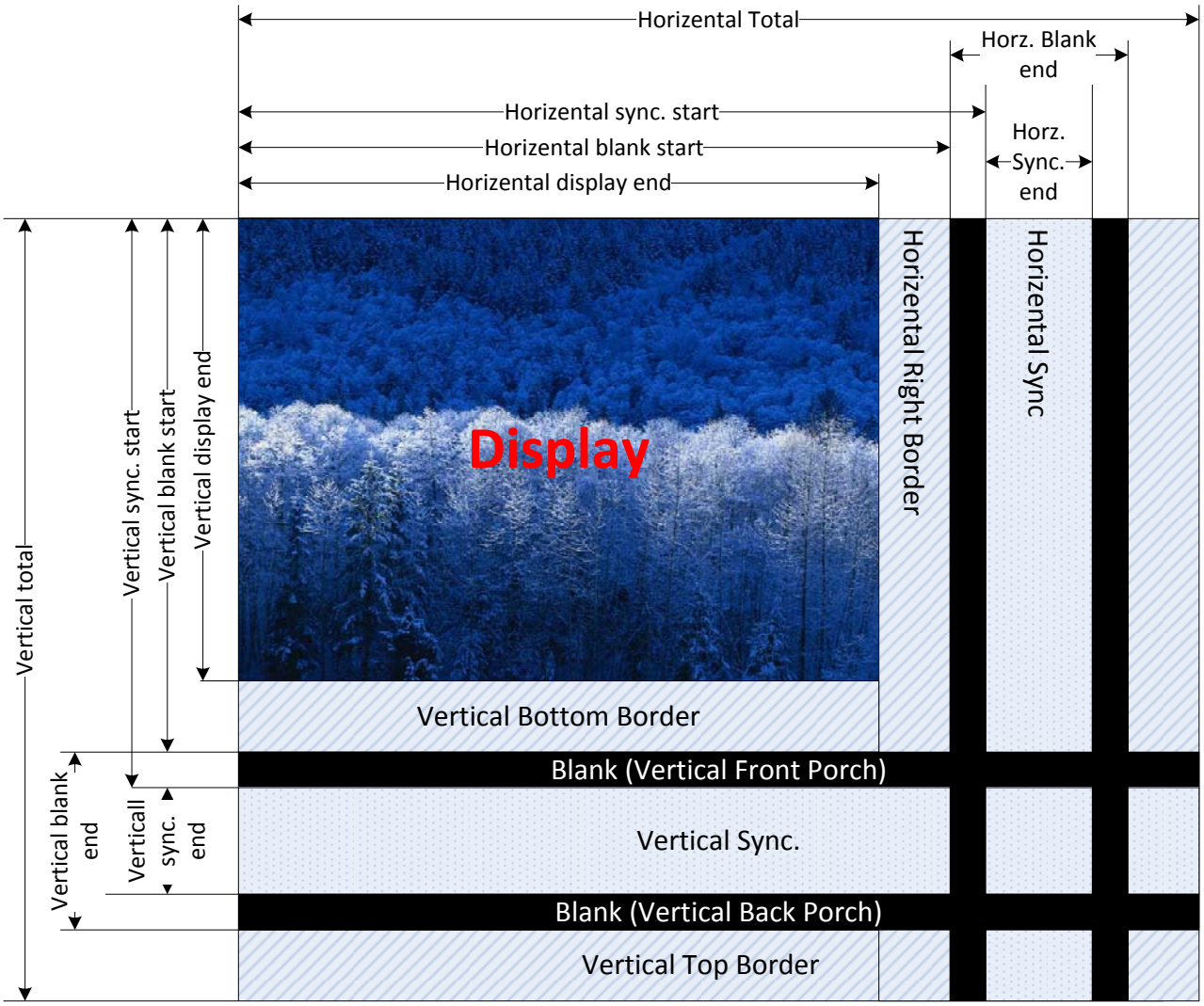
LVDS Testing Mode Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PD1 Enable Selection** 0: Select by register 1: Select by power flag
6	RW	0	**PD2 Enable Selection** 0: Select by register 1: Select by power flag
5	RW	0	**DVI Testing Mode Enable**
4	RW	0	**DVI Testing Format Selection** 0: Half cycle 1: LFSR mode
3	RO	0	Reserved
2	RW	0	**LVDS Testing Mode Enable**
1:0	RW	0	**LVDS Testing Format Selection** 00: Always 0 01: Always 1 1x: 0,1 toggle

APPENDIX A – DISPLAY PARAMETER ADJUSTMENT

Display Parameter

Several parametrers such as the display area and the blank area are relative to display adjustment. The definition of these parameters are shown below.



Primary Display Adjustment

The primary display output follows standard VGA specification in the characteristic unit of parameter adjustment.

Total pixels adjustment

Horizontal total pixels

The values of horizontal total pixels are stored in 9-bit register combination of bit[8]= 3X5.36[3] and bit[7:0]= 3X5.00.

IO Port / Index: 3X5.36
Power Management 8 (Monitor Control) **Default Value: 00h**

Bit	Attribute	Default	Description
3	RW	0	**Horizontal Total Bit [8]**

Vertical total pixels

The values of vertical total pixels are stored in 11-bit register combinatioin of bit[10]=3X5.35[0], bit[9]=3X5.07[5], bit[8]=3X5.07[0] and bit[7:0]=3X5.06.

IO Port / Index: 3X5.35
Extended Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
0	RW	0	**Vertical Total Bit [10]**

Display end position adjustment

Horizontal display end position

The horizontal end position is presented in 8 bits by register 3X5.01.

Vertical display end position

The vertical end postion of display area is presented in 11 bits by register combination of bit[10]=3X5.35[2], bit[9]=3X5.07[6], bit[8]=3X5.07[1] and bit[7:0]=3X5.12.

IO Port / Index: 3X5.35
Extended Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
2	RW	0	**Vertical Display End Bit [10]**

Blank area adjustment

Horozontal blank start

The horizontal starting position of blank area is presented in the total of 8 bits by register 3X5.02.

Horozontal blank end

The horizontal ending position of blank area is presented in the total of 7 bits as register combination of bit[6]=3X5.33[5], bit[5]=3X5.05[7] and bit[4:0]=3X5.03[4:0].

IO Port / Index: 3X5.33
HSYNCH Adjuster **Default Value: 00h**

Bit	Attribute	Default	Description
5	RW	0	**Horizontal Blanking End Bit [6]**

Vertical blank start

The vertical starting position of blank area is presented in 11 bits as register combination of bit[10]=3X5.35[3], bit[9]=3X5.09[5], bit[8]=3X5.07[3], bit[7:0]=3X5.15

IO Port / Index: 3X5.35
Extended Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
3	RW	0	**Vertical Blanking Start Bit [10]**

Vertical blank end

The vertical end position of blank area is presented in 8 bits by register 3X5.16.

Synchronization adjustment

Horozontal synchronization start

The horizontal starting position of synchronization area is presented in 9 bits by register combination of bit[8]=3X5.33[4] and bit[7:0]=3X5.04.

IO Port / Index: 3X5.33
HSYNCH Adjuster **Default Value: 00h**

Bit	Attribute	Default	Description
4	RW	0	**HSYNC Start Bit [8]**

Horozontal synchronization end

The horizontal end position of synchronization area is presented in 5 bits by register 3X5.05[4:0].

Vertical synchronization start

The vertical starting position of synchronization area is presented in 11 bits by register combination of bit[10]=3X5.[1], bit[9]=3X5.07[7], bit[8]=3X5.07[2] and bit[7:0]=3X5.10.

IO Port / Index: 3X5.35
Extended Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
1	RW	0	**Vertical Retrace Start Bit [10]**

Vertical synchronization end

The vertical end position of synbchronization area is presented in 4 bits by register 3X5.11[3:0].

Horizontal offset adjustment

The horizontal offset is presented in 11 bits by registger combination of bit[10:8]=3X5.35[7:5] and bit[7:0]=3X5.13.

IO Port / Index: 3X5.35
Extended Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Offset Bits [10:8]**

Line comparison

The line comparision is presented in 11 bits by register combination of bit[10]=3X5.35[4], bit[9]=3X5.09[6], bit[8]=3X5.07[4] and bit[7:0]=3X5.18.

IO Port / Index: 3X5.35
Extended Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
4	RW	0	**Line Compare Bit [10]**

Alignment

The quad-words alignment is held in horizontal and presented by 10-bit register combination of bit[9:8]=3C5.1D[1:0] and bit[7:0]=3C5.1C[7:0].

IO Port / Index: 3C5.1D
Horizontal Display Fetch Count Control **Default Value: 00h**

Bit	Attribute	Default	Description
1:0	RW	0	**Horizontal Display Fetch Count Data Bits [9:8]** Used in conjunction with Rx3C5.1C register.

IO Port / Index: 3C5.1C
Horizontal Display Fetch Count Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Display Fetch Count Data [7:0]** Unit: 16 bytes

Color Depth Setting

The selection of color depths is presented in 2 bits by register 3C5.15[3:2].

IO Port / Index: 3C5.15
Display Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
3:2	RW	00b	**Display Color Depth Select** 00: 8bpp 01: 16bpp 10: 30bpp 11: 32bpp

Clock Synthesizer

The clock synthsizer of primary display is in the regisers of 3C5.44, 3C5.45 and 3C5.46.

Secondary Display Adjustment

The secondary display output extends the capability to LCD display in the pixel unit of parameter adjustment.

Total pixel adjustment

Horizontal total pixels

The number of horizontal total pixels is presented by the combination of 12-bit register as bit[11:8]=3X5.55[3:0] and bit[7:0]=3X5.50.

IO Port / Index: 3X5.50
Second CRT Horizontal Total Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Total Period Bits [7:0]**

IO Port / Index: 3X5.55
Second CRT Horizontal Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
3:0	RW	0	**Horizontal Total Period Bits [11:8]**

Vertical total pixels

The number of vertical total pixels is presented by the combination of 11-bit register as bit[10:8]=3X5.5D[2:0] and bit[7:0]=3X5.58.

IO Port / Index: 3X5.58
Second CRT Vertical Total Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Total Period Bits [7:0]**

IO Port / Index: 3X5.5D
Second CRT Vertical Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
2:0	RW	0	**Vertical Total Period Bits [10:8]**

Display end position adjustment

Horizontal display end position

The number of horizontal end position is presented by the combination of 11-bit register as bit[10:8]=3X5.55[6:4] and bit[7:0]=3X5.51.

IO Port / Index: 3X5.51
Second CRT Horizontal Active Data Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Active Data Period Bits [7:0]**

IO Port / Index: 3X5.55
Second CRT Horizontal Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
6:4	RW	0	**Horizontal Active Data Period Bits [10:8]**

Vertical display end position

The vertical end postion of display area is presented in 11 bits by register combination of bit[10:8]=3X5.5D[5:3] and bit[7:0]=3X5.59.

IO Port / Index: 3X5.59
Second CRT Vertical Active Data Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Active Data Period Bits [7:0]**

IO Port / Index: 3X5.5D
Second CRT Vertical Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
5:3	RW	0	**Vertical Active Data Period Bits [10:8]**

Blank area adjustment

Horozontal blank start

The horizontal starting position of blank area is presented in the total of 11 bits by register combination of bit[10:8]=3X5.54[2:0] and bit[7:0]=3X5.52.

IO Port / Index: 3X5.54
Second CRT Horizontal Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
2:0	RW	0	**Horizontal Blanking Start Bits [10:8]**

IO Port / Index: 3X5.52
Second CRT Horizontal Blanking Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second CRT Horizontal Blanking Start Bits [7:0]**

Horozontal blank end

The horizontal end position of blank area is presented in the total of 12 bits by register combination of bit[11]=3X5.5D[6], bit[10:8]=3X5.54[5:3] and bit[7:0]=3X5.53.

IO Port / Index: 3X5.53
Second CRT Horizontal Blanking End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second CRT Horizontal Blanking End Bits [7:0]**

IO Port / Index: 3X5.54
Second CRT Horizontal Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
5:3	RW	0	**Horizontal Blanking End Bits [10:8]**

IO Port / Index: 3X5.5D
Second CRT Vertical Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
6	RW	0	**Horizontal Blanking End Bit [11]**

Vertical blank start

The vertical starting position of blank area is presented in 11 bits by register combination of bit[10:8]=3X5.5C[2:0] and bit[7:0]=3X5.5A.

IO Port / Index: 3X5.5A
Second CRT Vertical Blanking Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Blanking Start Bits [7:0]**

IO Port / Index: 3X5.5C
Second CRT Vertical Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
2:0	RW	0	**Vertical Blanking Start Bits [10:8]**

Vertical blank end

The vertical end position of blank area is presented in 11 bits by register combination of bit[10:8]=3X5.5C[5:3] and bit[7:0]=3X5.5B.

IO Port / Index: 3X5.5B
Second CRT Vertical Blanking End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Blanking End Bits [7:0]**

IO Port / Index: 3X5.5C
Second CRT Vertical Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
5:3	RW	0	**Vertical Blanking End Bits [10:8]**

Synchronization adjustment

Horozontal synchronization start

The horizontal starting position of synchronization area is presented in 12 bits by register combination of bit[11]=3X5.5D[7], bit[10]=3X5.5C[7], bit[9:8]=3X5.54[7:6] and bit[7:0]=3X5.56.

IO Port / Index: 3X5.54
Second CRT Horizontal Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Horizontal Retrace Start Bits [9:8]**

IO Port / Index: 3X5.56
Second CRT Horizontal Retrace Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Retrace Start Bits [7:0]**

IO Port / Index: 3X5.5C
Second CRT Vertical Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Horizontal Retrace Bit [10]**

IO Port / Index: 3X5.5D
Second CRT Vertical Period Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Horizontal Retrace Start Bit [11]**

Horozontal synchronization end

The horizontal end position of synchronization area is presented in 9 bits by register combination of bit[8]=3X5.5C[6] and bit[7:0]=3X5.57.

IO Port / Index: 3X5.57
Second CRT Horizontal Retrace End **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Horizontal Retrace End**

IO Port / Index: 3X5.5C
Second CRT Vertical Blanking Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
6	RW	0	**Horizontal Retrace End Bit [8]**

Vertical synchronization start

The vertical starting position of synchronization area is presented in 11 bits by register combination of bit[10:8]=3X5.5F[7:5] and bit[7:0]=3X5.5E.

IO Port / Index: 3X5.5E
Second CRT Vertical Retrace Start **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Vertical Retrace Start Bits [7:0]**

IO Port / Index: 3X5.5F
Second CRT Vertical Retrace End **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Vertical Retrace Start Bits [10:8]**

Vertical synchronization end

The vertical end position of synbchronization area is presented in 5 bits by register 3x5.5F[4:0].

IO Port / Index: 3X5.5F
Second CRT Vertical Retrace End **Default Value: 00h**

Bit	Attribute	Default	Description
4:0	RW	0	**Vertical Retrace End**

Horizontal offset adjustment

The horizontal offset is presented in 10 bits by registger combination of bit[9:8]=3X5.67[1:0] and bit[7:0]=3X5.66.

IO Port / Index: 3X5.66
Second Display Horizontal Offset **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Horizontal Offset Bits[7:0] or Horizontal Synchronous Point**

IO Port / Index: 3X5.67

Second Display Color Depth and Horizontal Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
1:0	RW	0	**Second Display Horizontal Offset Bits[9:8]**

Alignment

Quad-words alignment is held in horizontal and presented the number in 10 bits by register combination of bit[9:8]=3X5.67[3:2] and bit[7:0]=3X5.65.

IO Port / Index: 3X5.65.

Second Display Horizontal Quadword Count Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Second Display Horizontal 2-Quadword Count Data Bits[7:0]**

IO Port / Index: 3X5.67

Second Display Color Depth and Horizontal Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
3:2	RW	0	**Second Display Horizontal 2-Quadword Count Data Bits[9:8]**

Color Depth Setting

The selection of color depths is presented in 2 bits by register 3X5.67[7:6].

IO Port / Index: 3X5.67

Second Display Color Depth and Horizontal Overflow **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Color Depth** 00: 8bpp 01: 16bpp 10: 30bpp 11: 32bpp

Clock Synthesizer

The clock synthsizer of secondary display is in regisers of 3C5.4A, 3C5.4B and 3C5.4C.