Open Graphics Programming Manual

Chrome9 HCM Graphics Processor

VX855 and VX875

Part II: 3D / Video

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TABLE OF CONTENTS

REVISION HISTORY I
TABLE OF CONTENTS II
LIST OF FIGURES IV
LIST OF TABLES IV
INTRODUCTION 1
ABOUT THIS PROGRAMMING GUIDE 1
SUPPORTING PRODUCTS AND FEATURES 3
SYSTEM BLOCK DIAGRAM 4
VIDEO DISPLAY REGISTERS 5
VIDEO DISPLAY REGISTERS 5
VIDEO DISPLAY ENGINE REGISTER DESCRIPTIONS (200-12F0H) 8
DVD / VIDEO CONTROL REGISTER (3260-326CH) 32
VIDEO CAPTURE ENGINE REGISTERS 33
VIDEO CAPTURE ENGINE REGISTERS 33
VIDEO CAPTURE ENGINE REGISTER DESCRIPTIONS (300-35FH) 35
HQV REGISTERS 42
HQV REGISTERS 42
HQV ENGINE REGISTER DESCRIPTIONS (360-3FFH) 44
COMMAND REGULATOR (CR) REGISTERS 56
MEMORY MAPPED I/O REGISTER ADDRESS SPACES 56
DEFINITION OF I/O REGISTERS 57
For Write Mode 57
HPARATYPE 00H: PRIMITIVE VERTEX DATA OR VERTEX INDEX 61
HPARATYPE 10H: COMMANDS FOR COMMAND REGULATOR 62
Sub-Address (Bits [31:24]): 00-7Ch 62
HPARATYPE 11H: COMMANDS FOR FRAME BUFFER SWAPPING AND CR'S MISCELLANEOUS SETTING 69
Sub-Address (Bits [31:24]): 00-ABh 69
CR REGISTERS IN 2D REGISTER SPACE (60-6CH) 75
CR REGISTERS IN VIDEO CONTROL REGISTER SPACE (3260-326CH) 76
3D REGISTERS 77
HPARATYPE 00H: PRIMITIVE VERTEX DATA OR VERTEX INDEX 77
HPARATYPE 01H: ATTRIBUTE OTHER THAN TEXTURE 78
Sub-Address (Bits [31:24]): 00-AAh 78
HPARATYPE 02H: ATTRIBUTE OF TEXTURE STAGE N (HPARASUBTYPE: 00-0FH) 116
Sub-Address (Bits [31:24]): 00-51h 116
HPARATYPE 02H: ATTRIBUTE OF TEXTURE SAMPLE STAGE N (HPARASUBTYPE: 20-2FH) 124

Sub-Address (Bits [31:24]): 00-51h **124**
HPARATYPE 02H: ATTRIBUTE OF TEXTURE STAGE N (HPARASUBTYPE: FEH) **128**
Sub-Address (Bits [31:24]): 00-13h **128**
HPARATYPE 03H: PALETTE (HPARASUBTYPE: 00-22H) **138**
HPARATYPE 04H: VERTEX AND PRIMITIVE SETTING **148**
Sub-Address (Bits [31:24]): 00-AAh **148**
HPARATYPE 10H: COMMANDS FOR COMMAND REGULATOR **166**
HPARATYPE 11H: COMMANDS FOR FRAME BUFFER SWAPPING AND CR'S MISCELLANEOUS SETTING **166**

LIST OF FIGURES

FIGURE 1. THE CHROME9 HCM BLOCK DIAGRAM 4

LIST OF TABLES

TABLE 1. VX855 / VX875 SERIES COMPARISON TABLE 3
TABLE 2. VIDEO DISPLAY ENGINE REGISTERS 5
TABLE 3. GRAPHICS HARDWARE COLOR CURSOR OPERATION 26
TABLE 4. VIDEO CAPTURE ENGINE 33
TABLE 5. HIGH QUALITY VIDEO REGISTERS 42

INTRODUCTION

This document contains detailed graphics registers descriptions and other general information for the Chrome9 HCM graphic engine. The graphics registers for the Chrome9 HCM main features and its underlying subsystems are described explicitly in the following chapters.

About This Programming Guide

The programming manual is organized into 2 volumes (Part I & Part II). A brief description of each chapter is given below:

Part I:

Introduction.

An overview of the Chrome9 HCM design features is given in this chapter, along with block diagram and reference list.

Register Overview

Register specifications for register addressing and I/O space division are shown in this chapter.

PCI Interface Register Descriptions

PCI interface summary table and detailed register descriptions are presented in this chapter.

VGA I/O Register Descriptions

This chapter provides detailed VGA-related register summary and descriptions. The various video modes support by the Chrome9 HCM controller are also included in the configuration section.

2D Engine Register Descriptions

In this chapter provides detailed 2D Engine register summary and descriptions.

DMA Register Descriptions

This chapter provides detailed DMA register summary and descriptions.

CBU Rotation Register Descriptions

This chapter provides detailed CBU rotation register summary and descriptions.

LVDS Register Descriptions

This chapter provides detailed LVDS register summary and descriptions.

Part II:

Video Display Engine Register Descriptions

This chapter provides detailed video display engine register summary and descriptions.

Video Capture Engine Register Descriptions

This chapter provides detailed video capture engine register summary and descriptions.

HQV Register Descriptions

This chapter provides detailed HQV register summary and descriptions.

Command Regulator (CR) Register Descriptions

This chapter provides detailed CR register summary and descriptions.

3D Engine Register Descriptions

This chapter provides detailed 3D Engine register summary and descriptions.

Supporting Products and Features

This document includes all the GFX registers for VIA VX855 and VX875. Please refer to Table 1 for the specification differences of VX855 and VX875 products.

This chip integrates functional modules of the traditional North Bridge and South Bridge chips, plus 3D/2D and Video Processors, Video Decoding Accelerator and controller for external display interface. The register set is partitioned into three blocks: North Module, South Module and Graphics and Video Module; of which, North Module and South Module registers are described in this **System Programming Manual** while graphics and video registers are described in the **Graphics Programming Guide**.

Table 1. VX855 / VX875 Series Comparison Table

Product Model	VX855	VX875
FSB Speed (MHz)	400-800	400-533
Memory Type	DDR2-800 1.5V / 1.8V	DDR2-667 1.5V / 1.8V
Snapshot Memory	Yes	Yes
Core Voltage	1.2V	1.0V
Package Dimension	27x27mm FCBGA 906 balls	21x21mm FCBGA 945 balls

System Block Diagram

The block diagram for the Chrome9 HCM is shown Figure 1.

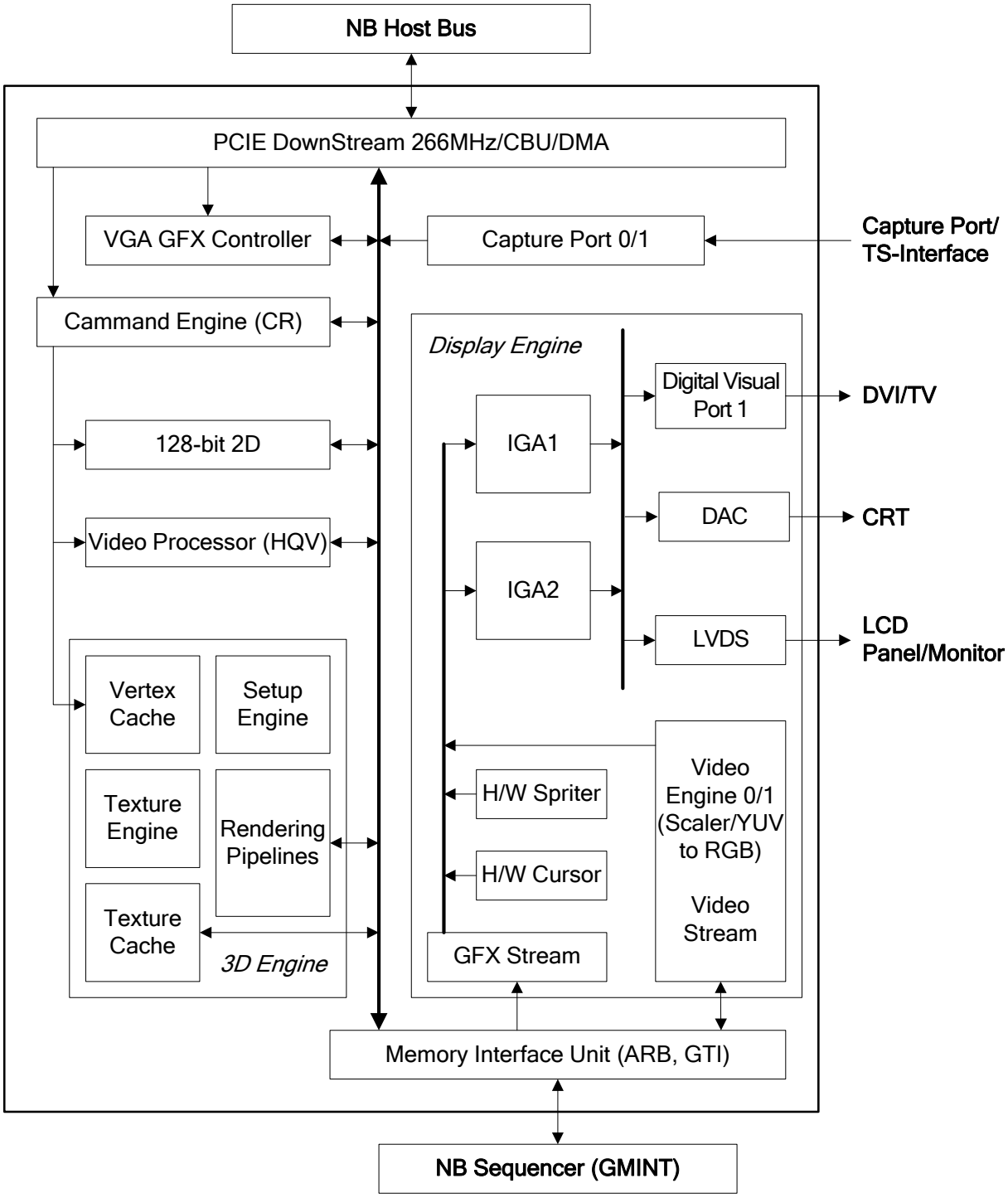

Figure 1. The Chrome9 HCM Block Diagram

VIDEO DISPLAY REGISTERS

This document provides detailed video display engine register summary table. Register descriptions on video play back / blending engine are followed in the sequent sections.

Video Display Registers

The Chrome9 HCM Graphic Engine has an integrated video playback and blending engine. The video playback engine can simultaneously support up to three live video windows, and each video window can be independently scaled. Two blending engines support the graphics-to-video blending, followed by video-to-video blending effect. The blending factor is from constant, alpha stream or is combined with graphics data. Table 2 summarizes the video playback and blending engine registers. Detail register description follows.

Table 2. Video Display Engine Registers

Offset (Hex)	Register Name	Attribute
Video Related Engines Register Space 1 (0x00000200 ~ 0x000003FF)		
203-200	Interrupt Flags & Masks Control	RW
207-204	Address Flip Status	RO
20B-208	Alpha Window / HI (For Second Display) Horizontal and Vertical Location Start	RW
20F-20C	Alpha Window Horizontal and Vertical End & HI (For Second Display) Center Offset	RW
213-210	Alpha Window Control	RW
217-214	CRT Starting Address	RW
21B-218	The Second Display Starting Address	RW
21F-21C	Alpha Stream Frame Buffer Stride	RW
223-220	Primary Display Color Key	RW
227-224	Alpha Window & HI (For Second Display) Frame Buffer Starting Address	RW
22B-228	Chroma Key Lower Bound	RW
22F-22C	Chroma Key Upper Bound	RW
233-230	Video Stream 1 Control	RW
237-234	Video Window 1 Fetch Count	RW
23B-238	Video Window 1 Frame Buffer Y Starting Address 1	RW
23F-23C	Video Window 1 Frame Buffer Stride	RW
243-240	Video Window 1 Horizontal and Vertical Start Location	RW
247-244	Video Window 1 Horizontal and Vertical Ending Location	RW
24B-248	Video Window 1 Frame Buffer Y Starting Address 2	RW
24F-24C	Video Window 1 Display Zoom Control	RW
253-250	Video Window 1 Minify and Interpolation Control	RW
257-254	Video Window 1 Frame Buffer Y Starting Address 0	RW
25B-258	Video 1 FIFO Depth and Threshold Control	RW
25F-25C	Video Window 1 Horizontal and Vertical Starting Location Offset	RW
263-260	HI Control For Second Display	RW
267-264	The Second Display Color Key	RW
26B-268	V3 and Alpha Window FIFO Pre-threshold Control	RW
26F-26C	Video Window 1 Display Count On Screen Control	RW
273-270	HI Transparent Color For Second Display	RW
277-274	HI Inverse Color For Second Display	RW
27B-278	V3 and Alpha Window FIFO Depth and Threshold Control	RW
27F-27C	V3 Display Count On Screen Control	RW
283-280	Primary Display Second Color Key	RW
287-284	V1 Color Space Conversion & Enhancement Control 1	RW

Offset (Hex)	Register Name	Attribute
28B-288	V1 Color Space Conversion & Enhancement Control 2	RW
28F-28C	Reserved	RO
293-290	Alpha Window/HI (For Primary Display) Ending Position	RW
297-294	3D AGP Pause Address MMIO Port	WO
29B-298	Compose Output Modes Select	RW
29F-29C	V3 Frame Buffer Starting Address 2	RW
2A3-2A0	V3 Control	RW
2A7-2A4	V3 Frame Buffer Starting Address 0	RW
2AB-2A8	V3 Frame Buffer Starting Address 1	RW
2AF-2AC	V3 Frame Buffer Stride	RW
2B3-2B0	V3 Horizontal and Vertical Start	RW
2B7-2B4	V3 Horizontal and Vertical End	RW
2BB-2B8	V3 and Alpha Window Fetch Count	RW
2BF-2BC	V3 Display Zoom Control	RW
2C3-2C0	V3 Minify & Interpolation Control	RW
2C7-2C4	V3 Color Space Conversion & Enhancement Control 1	RW
2CB-2C8	V3 Color Space Conversion & Enhancement Control 2	RW
2CF-2CC	Reserved	RO
2D3-2D0	Graphics Hardware Cursor Mode Control	RW
2D7-2D4	Graphics Hardware Cursor Position	RW
2DB-2D8	Graphics Hardware Cursor Origin	RW
2DF-2DC	Graphics Hardware Cursor Background Color	RW
2E3-2E0	Graphics Hardware Cursor Foreground Color	RW
2E7-2E4	Reserved	RO
2EB-2E8	HI for Primary Display FIFO Control Signal	RW
2EF-2EC	HI for Primary Display Transparent color	RW
2F3-2F0	HI for Primary Display Control Signal	RW
2F7-2F4	HI for Primary Display Frame Buffer Starting Address	RW
2FB-2F8	HI for Primary Display Horizontal and Vertical Start	RW
2FF-2FC	HI for Primary Display Center Offset	RW
Video Related Engines Register Space 2 (0x00001200 ~ 0x000013FF)		
1203-1200	Video 1 Gamma R Correction Control	RW
1207-1204	Video 1 Gamma G Correction Control	RW
120B-1208	Video 1 Gamma B Correction Control	RW
120F-120C	HI (For Primary Display) Inverse Color	RW
1223-1220	Video 3 Gamma R Correction Control	RW
1227-1224	Video 3 Gamma G Correction Control	RW
122B-1228	Video 3 Gamma B Correction Control	RW
122F-122C	Video 3 Horizontal and Vertical Starting Location Offset	RW
127F-1230	Reserved	RO
1283-1280	Interrupt Flags and Masks Control	RW
1287-1284	Logic Signature Setting	RW
128B-1288	Reserved	RO
128F-128C	Logic Signature Address Result 0	RW
1293-1290	IGA1 Display Position Counter 0	RO
1297-1294	IGA1 Display Position Counter 1	RO
129B-1298	IGA1 Display Position Counter 2	RW
129F-129C	Logic Signature Data Result 0	RW
12A3-12A0	IGA2 Display Position Counter 0	RO
12A7-12A4	IGA2 Display Position Counter 1	RO
12AB-12A8	IGA2 Display Position Counter 2	RW

Offset (Hex)	Register Name	Attribute
12B3-12B0	Primary Display Data Color Space Conversion and Enhancement Control 1	RW
12B7-12B4	Primary Display Data Color Space Conversion and Enhancement Control 2	RW
12BB-12B8	Primary Display Data Color Space Conversion and Enhancement Control 3	RW
12BF-12BC	Primary Display Data Color Space Conversion and Enhancement Control 4	RW
12FF-12C0	Reserved	RO
Extended Video Engines Register Space 2 (0x00003200 ~ 0x000033FF)		
3260	DVD / Video ID Control	
326C	DVD / Video Wait Control Register	

Note:
1) Port Address: MB1 + Offset Address
MB1 is declared in the register with offset address 17h-14h in the PCI configuration space.

2) There is additional register space to match the above register definition. When write a register to this space, it will be sent to "command regulator" first and then pass to video display engine. However, register read will be same as the original action. The relationship between the additional register space and original register space is:
(The additional register address) = (The original register address) + 16'h2000.

Video Display Engine Register Descriptions (200-12F0h)

Offset Address: 203-200h

Interrupt Flags and Masks Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Interrupt Enable** 0: Disable 1: Enable
30	RW	0	**LVDS Sense Interrupt Enable** 0: Disable 1: Enable
29	RW	0	**Capture 0 VBI Capture End Interrupt Enable** 0: Disable 1: Enable
28	RW	0	**Capture 0 Active Video Data Capture End Enable** 0: Disable 1: Enable
27	RW1C	0	**LVDS Sense Interrupt Status**
26	RW	0	**Capture 1 VBI Capture End Interrupt Enable** 0: Disable 1: Enable
25	RW	0	**First HQV Engine Interrupt Enable** 0: Disable 1: Enable (Refer to 03D0h)
24	RW	0	**Capture 1 Active Video Data Capture End Enable** 0: Disable 1: Enable
23	RW	0	**DMA1 Transfer Done Interrupt Enable** 0: Disable 1: Enable
22	RW	0	**DMA1 Descriptor Done Interrupt Enable** 0: Disable 1: Enable
21	RW	0	**DMA0 Transfer Done Interrupt Enable** 0: Disable 1: Enable
20	RW	0	**DMA0 Descriptor Done Interrupt Enable** 0: Disable 1: Enable
19	RW	0	**VGA VSYNC Interrupt Mask Enable** 0: Disable 1: Enable
18	RW	0	**MC Complete Frame Interrupt Mask Enable** 0: Disable 1: Enable
17	RW	0	**Secondary Display VSYNC Interrupt Enable** 0: Disable 1: Enable
16	RW	0	**DVI Sense Interrupt Enable** 0: Disable 1: Enable
15	RW1C	0	**Secondary Display VSYNC Interrupts Status**
14	RW1C	0	**Capture 1 VBI Capture End Interrupt Status**
13	RW1C	0	**Capture 0 VBI Capture End Interrupt Status**
12	RW1C	0	**Capture 0 Active Video Data Capture End Interrupt Status**
11	RW	0	**Second HQV Engine Interrupt Enable** 0: Disable 1: Enable (Refer to 13D0h for more detail.)
10	RW	0	**Second HQV Engine Interrupt Status** (Refer to 13D0h for more detail.)
9	RW1C	0	**First HQV Engine Interrupt Status** (Refer to 03D0h for more detail.)
8	RW1C	0	**Capture 1 Active Video Data Capture End Interrupt Status**
7	RW1C	0	**DMA 1 Transfer Done Interrupt Status**
6	RW1C	0	**DMA 1 Descriptor Done Interrupt Status**
5	RW1C	0	**DMA 0 Transfer Done Interrupt Status**
4	RW1C	0	**DMA 0 Descriptor Done Interrupt Status**
3	RW1C	0	**VGA VSYNC Interrupt Status**
2	RW1C	0	**MC Complete Frame Interrupt Status**
1	RO	0	**Vertical Blanking Status**
0	RW1C	0	**DVI Sense Interrupt Status**

Offset Address: 207-204h

Address Flip Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11	RO	0	**Video Window 1 SW Flip Status (R)** Write B0+254'h port to clear this bit.
10	RO	0	**Video Window 3 SW Flip Status (R)** Write B0+2A4'h port to clear this bit.
9:6	RO	0	**Reserved**
5	RW1C	0	**CR Interrupt Status**
4	RO	0	**Alpha Window Starting Address Update Status** 0: Updated 1: Not yet updated It will be set as writes Rx224, and be cleared as starting address is updated.
3	RO	0	**Video Window 3 Starting Address Update Status** 0: Updated 1: Not yet updated It will be set as writes Rx2A4, and be cleared as starting address is updated.
2	RO	0	**IGA2 Vertical Blanking Status**
1	RO	0	**Graphics Starting Address Update Status** 0: Updated 1: Not yet updated It will be set as writes Rx214, and be cleared as starting address is updated.
0	RO	0	**Video Window 1 Starting Address Update Status** 0: Updated 1: Not yet updated It will be set as writes Rx254, and be cleared as starting address is updated.

Offset Address: 20B-208h

Alpha Window / Hardware Icon (HI) Horizontal and Vertical Location Start **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	WO	0	***Depend on Hardware Icon Enable (Rx260[0]):*** ***When Rx260[0]=0:*** **Alpha window horizontal (X) starting location** ***When Rx260[0]=1:*** **Hardware icon horizontal (X) starting location** Unit: Pixel
15:11	RO	0	**Reserved**
10:0	WO	0	***When Write: Depend on Hardware Icon Enable (Rx260[0])*** ***When Rx260[0]=0:*** **Alpha window vertical (Y) starting location** ***When Rx260[0]=1:*** **Hardware icon vertical (Y) starting location** Unit: Line ***When Read:*** **Graphic Display Vertical Line Number** Unit: Line

Offset Address: 20F-20Ch

Alpha Window Horizontal and Vertical Location End / Hardware Icon (HI) Center Offset **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RW	0	**Reserved**
26:16	RW	0	***Depend on Hardware Icon Enable (Rx260[0])*** ***When Rx260[0]=0:*** **Alpha window horizontal (X) ending location** ***When Rx260[0]=1:*** **Hardware icon horizontal (X) center offset** Unit: Pixel
15:11	RO	0	**Reserved**
10:0	RW	0	***Depend on Hardware Icon Enable (Rx260[0])*** ***When Rx260[0]=0:*** bits[10:0] = **Alpha window vertical (Y) ending location** ***When Rx260[0]=1:*** bits[6:0] = **Hardware icon vertical (Y) enter offset** Unit: Line

Offset Address: 213-210h

Alpha Window Control **Default Value: 0000 FF00h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20:16	RW	0	**Alpha Stream Request Expire Number** Unit: 4 Requests
15:8	RW	FFh	**Constant Alpha Factor Setting For Graphics Blending**
7:2	RO	0	**Reserved**
1:0	RW	00b	**Graphics Blending Alpha Select (Alpha*VID+(1-Alpha)*GRA)** 00: Blending using constant alpha factor [15:8] 01: Alpha is from alpha stream 10: Alpha is from graphics stream 11: Reserved

Offset Address: 217-214h

CRT Starting Address Shadow **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**IGA1 Down Scaling Flip** Address equivalent to 3X5.EC[1]
30	RW	0	**IGA1 Down Scaling Line Flip Enable**
29	RO	0	**Reserved**
28:0	RW	0	**Primary Display Starting Address or** **IGA1 Down Scaling Source Starting Address (Valid when 3X5.EC[0] = 1)** Address equivalent to: 3X5.48 [4:0] 3X5.34 [7:0] 3X5.0C [7:0] 3X5.0D [7:0]

Note: In monochrome mode, the "X" in the above table stands for **"B".** In color mode, the "X" in the above table stands for **"D".**

Offset Address: 21B-218h

The Second Display Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Display Address Selection** 00: S.L. Others are not supported
28:3	RW	0	**The Second Display Starting Address or** **IGA2 Down Scaling Source Starting Address (Valid when 3X5.E8[4] = 1)** Unit: 8 bytes
2	RO	0	**Reserved**
1	RW	0	**IGA2 Down Scaling Line Flip Enable**
0	RW	0	**IGA2 Down Scaling Flip** Address equivalent to 3X5.E8[5].

Note: This register should be the same with 3X5.5E, 5D and 5C registers.

Offset Address: 21F-21Ch

Alpha Stream Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	RO	0	**Reserved**
12:4	RW	0	**Alpha Stream Frame Buffer Stride** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 223-220h

Primary Display Color Key **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**CRT Color Key** For RGB10 color mode [29]
30	RW	0	**CRT Color Key Enable** 0: Disable 1: Enable
29	RW	0	**CRT Color Key Inverse Control** 0: Display video if color key matches 1: Display video if color key does not match
28:0	RW	0	**CRT Color Key** Bits [28:0]: For RGB10 color mode [28:0] Bits [23:0]: For 32-bit true color mode Bits [15:0]: For 565 high color mode Bits [14:0]: For 555 high color mode Bits [7:0]: For 256 color mode

Offset Address: 227-224h

Alpha Window / Hardware Icon Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:29	RW	00b	**Target of Frame Buffer Starting Address** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:4	RW	0	**Depend On Hardware Icon Enable (Rx260[0])** 0: Frame buffer starting address for alpha window 1: Frame buffer starting address for hardware icon Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 22B-228h

Chroma Key Lower Bound **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Chroma Key Lower for Y/G Bit [1]**
30	RW	0	**Chroma Key Enable** 0: Disable 1: Enable
29	RW	0	**Chroma Key Inverse Control** 0: Display video if chroma key does not match 1: Display video if chroma key matches
28:0	RW	0	**Chroma Key Lower** {[23:16], [31], [28]}: Y/G {[15:8], [27:26]}: U/R {[7:0], [25:24]}: V/B

Offset Address: 22F-22Ch

Chroma Key Upper Bound **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**Chroma Key Select** 1 : Select video 3 0 : Select video 1
29:0	RO	0	**Chroma Key Upper** {[23:16], [29:28]} Y/G {[15:8], [27:26]}: U/R {[7:0], [25:24]}: V/B

Offset Address: 233-230h

Video Stream 1 Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**V1 Display to CRT or the Second Display** 0: CRT 1: Second display
30	RW	0	**V1 Window Pre-fetch Enable**
29	RW	0	**V1 Window Gamma Function Enable**
28	RW	0	**V1 Window De-Gamma Function Enable**
27	RW	0	**V1 Window Adder Tile Mode Enable**
26:25	RW	00b	**V1 Flip Control** 00: SW flip 01: HW flip and triggled by the HQV engine. 10: HW flip and triggled by the Capture Port 0. 11: HW flip and triggled by the Capture Port 1.
24	RW	0	**V1 Frame to Field Enable** 0: Disable 1: Enable If enabled, the stride will be 2 times of original values. This bit is valid at 1. Software flip. 2. HQV flip. 3. Capture frame mode flip. 4. MC frame mode flip.
23	RO	0	**Reserved**
22	RW	0	**V1 De-interlace Mode** If enabled, hardware will add one line to the top of odd (bottom) field. 0: Disable 1: Enable
21	RW	0	**V1 Line Flip Only in Non Video Active Period Enable** 0: Disable 1: Enable
20:16	RW	0	**V1 Request Expire Number** (Unit: 4 requests)
15:10	RO	0	**Reserved**
9	RW	0	**Divided V1 Flip for HQV Engine VSYNC Number to Half Enable** 0: Disable 1: Enable
8	RW	0	**V1 Color Space Conversion Disable** 0: Enable 1: Disable
7	RW	0	**V1 Color Space Conversion Chroma Sign Bits Conversion**
6:5	RO	0	**Reserved**
4:2	RW	000b	**V1 Stream Data Format** 000: YUV422 001: RGB32 010: RGB15 011: RGB16 100: YUV411 101: RGB10 Other : reserved
1	RO	0	**Reserved**
0	RW	0	**V1 Enable** 0: Disable 1: Enable

Offset Address: 237-234h

Video Window 1 Fetch Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**V1 Per Line Fetch Count** It is equal to no-sizing line fetch count / minify times. (Unit: 16 bytes)
19:0	RO	0	**Reserved**

Offset Address: 23B-238h

Video Window 1 Fetch Buffer Y Starting Address 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:29	RW	00b	**Target of The Second Frame Buffer Starting Address** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:3	RW	0	**V1 Packed Mode** The second frame buffer starting address
2:0	RO	0	**Reserved**

Offset Address: 23F-23Ch

Video Window 1 Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13:4	RW	0	**V1 Packed Mode** Frame buffer stride (Unit: 16 bytes)
3:0	RO	0	**Reserved**

Offset Address: 243-240h

Video Window 1 Horizontal and Vertical Starting Location **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Video Window 1 Horizontal (X) Starting Location (-1)**. (Unit: pixel)
15:11	RO	0	**Reserved**
10:0	RW	0	**Video Window 1 Vertical (Y) Starting Location (-1)**. (Unit: Line)

Offset Address: 247-244h

Video Window 1 Horizontal and Vertical Ending Location **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Video Window 1 Horizontal (X) Ending Location (-1)**. (Unit: pixel)
15:11	RO	0	**Reserved**
10:0	RW	0	**Video Window 1 Vertical (Y) Ending Location (-1)**. (Unit: Line)

Offset Address: 24B-248h

Video Window 1 Frame Buffer Y Starting Address 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:29	RW	00b	**Target of The Third Frame Buffer Starting Address** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:3	RW	0	**V1 Packed Mode** The third frame buffer starting address. (Unit: 16 bytes)
2:0	RO	0	**Reserved**

Offset Address: 24F-24Ch

Video Window 1 Display Zoom Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Video Window 1 Horizontal (X) Zoom Enable** 0: Disable 1: Enable
30:27	RO	0	**Reserved**
26:16	RW	0	**Video Window 1 Horizontal (X) Zoom Factor**
15	RW	0	**Video Window 1 Vertical (Y) Zoom Enable** 0: Disable 1: Enable
14:10	RO	0	**Reserved**
9:0	RW	0	**Video Window 1 Vertical (Y) Zoom Factor**

Offset Address: 253-250h

Video Window 1 Minify & Interpolation Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:24	RW	000b	**V1 Horizontal (X) Minify Control** 000: No minify; 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Others: reserved
23:19	RO	0	**Reserved**
18:16	RW	000b	**V1 Vertical (Y) Minify Control** 000: No minify 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Others: reserved
15:3	RO	0	**Reserved**
2	RW	0	**V1 Luma-only Interpolation When the Vertical Interpolation Is Enabled** 0: Only luma values interpolated 1: All YUV/YcbCr values interpolated
1	RW	0	**V1 Horizontal (X) Interpolation Mode Select** 0: Pixel is replicated 1: Enable interpolation
0	RW	0	**V1 Vertical (Y) Interpolation Mode Select** 0: Pixel is replicated 1: Enable interpolation

Offset Address: 257-254h

Video Window 1 Frame Buffer Y Starting Address 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**V1 Play Odd / Even Field Control** This bit is valid when SW Playback and Field Base Picture are selected. 0: Play even field 1: Play odd field
30:29	RO	00b	**Target of The First Frame Buffer Starting Address** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:2	RO	0	**V1 Packed Mode** The first frame buffer starting address. (Unit : 4 bytes)
1:0	RO	0	**Reserved**

Note: In packed mode, we could use Rx254[3:2] to get
1. No minify: 4 bytes alignment. Rx254[3:2] are valid
2. (Minify = 2): 8 bytes alignment. Rx254[3] is valid, and Rx254[2] is omitted.
3. (Minify > 2): 16 bytes alignment. Rx254[3:2] are omitted.

Offset Address: 25B-258h

Video Window 1 FIFO Depth and Threshold Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**V1 FIFO Pre-threshold** Let V1 issue request early. Normally, this value is greater than or equal to V1 FIFO threshold (Rx258[15:8]). (Unit : level)
23:26	RO	0	**Reserved**
15:8	RW	0	**V1 FIFO Threshold** Let V1 request priority from low to high. (Unit: level)
7:0	RW	0	**V1 FIFO Depth (- 1)** (Unit: level)

Note: One level is equal to 16 bytes.

Offset Address: 25F-25Ch

Video Window 1 Horizontal and Vertical Starting Location Offset **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Video Window 1 Horizontal (X) Starting Location Offset** (Unit: 16 bytes)
15:11	RO	0	**Reserved**
10:0	RW	0	**Video Window 1 Vertical (Y) Starting Location Offset** (Unit: Line)

Offset Address: 263-260h

Hardware Icon (HI) Control (Only for Second Display) **Default Value: 000F 00F0h**

Bit	Attribute	Default	Description
31	RW	0	**V4 Display Target Select** 0: Display to CRT 1: Display to secondary display
30	RW	0	**V4 Window Pre-fetch Enable** 0 Disable 1 Enable
29	RW	0	**HI + (1-aplha)*Graphics Mode** 0 Disable 1 Enable
28	RW	0	**Alpha Value Source Select** (Only for the true color Hardware icon) 0: From bits [23:16] 1: From the bits [31:24] of hardware icon
27:26	RW	00b	**HI Window Size** 00: 32x32 01: 64x64 1x: 128x128 Unit: Pixel * line
25:24	RW	00b	**HI Data Stream Format** 00: RGB555 01: RGB565 10: RGB32 11: RGB10
23:20	RO	0	**Reserved**
19:16	RW	Fh	**HI Constant Alpha [3:0] (HIAPA)**
15:12	RW	0	**Alpha Changed Value (HICV) Per Frame As HI Fan In/Out Turn on (When Rx260[8]=1)** ALPHAn[7:0] = ALPHAn-1[7:0] +/- HICV[3:0], where just ALPHAn[7:4] is valid alpha value and ALPHA0 = {HIAPA}.
11:10	RW	0	**DMA1 Descriptor Done Interrupt Enable** 0: Disable 1: Enable
9	RW	0	**HI Fan In / Out Selector** 0: Default 1: Fan in (+)
8	RW	0	**HI Fan In / Out Enable** 0: Disable 1: Enable
7:4	RW	Fh	**HI Constant Alpha[7:4] (HIAPA)** The rest bits are put on [19:16].
3	RO	0	**Reserved**
2	RW	0	**HI Blending Enable** 0: Disable 1: Enable
1	RO	0	**Reserved**
0	RW	0	**HI Enable** 0: Disable 1: Enable

Offset Address: 267-264h

The Second Display Color Key **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**The Second Display Color Key Bit [29] For RGB10 True Color Mode** See also bits [28:0] for detail.
30	RW	0	**Second Display Color Key Enable** 0: Disable 1: Enable
29	RW	0	**Second Display Color Key Inverse Control** 0: Display video if color key matches 1: Display video if color key does not match
28:0	RW	0	**The Second Display Color Key** Bits [31,28:0]: For RGB10 true color mode Bits [23:0]: For 32-bit true color mode Btis [15:0]: For 565 high color mode Bits [14:0]: For 555 high color mode Bits [7:0]: For 256 color mode

Offset Address: 26B-268h

V3 and Alpha Window FIFO Pre-Threshold Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22:16	RW	0	**Alpha Window FIFO Pre-threshold** Let alpha engine issue request early. This value is normally greater than or equal to the alpha engine FIFO threshold (Rx278[30:24]). Unit : Level
15:8	RO	0	**Reserved**
7:0	RW	0	**V3 FIFO Pre-threshold** Let V3 issue request early. This value is normally greater than or equal to V3 FIFO threshold (Rx278[15:8]). Unit: Level

Offset Address: 26F-26Ch

Video Window 1 Display Count On Screen Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:26	RW	0	**V1 Vertical Line Count That Shows On Screen** (Unit: Line)
25:12	RO	0	**Reserved**
11:0	RW	0	**V1 Horizontal Pixel Count That Shows On Screen (-1)** (Unit: Pixel)

Offset Address: 273-270h

Hardware Icon (HI) Transparent Color (Only For Second Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:0	RW	0	**HI Transparent Color** Bits [29:0]: For RGB10 Bits [23:0]: For RGB32 Bits [15:0]: For RGB565 Bits [14:0]: For RGB555

Offset Address: 277-274h

Hardware Icon (HI) Inverse Color (Only For Second Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:0	RW	0	**HI Inverse Color** Bits [29:0]: For RGB10 Bits [23:0]: For RGB32 Bits [15:0]: For RGB565 Bits [14:0]: For RGB555

Offset Address: 27B-278h

V3 and Alpha Window FIFO Depth and Threshold Contorl **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:24	RW	0	**Alpha Window FIFO Threshold** Unit: Level
23	RO	0	**Reserved**
22:16	RW	0	**Alpha Window FIFO Depth (-1)** Unit: Level
15:8	RW	0	**Video Window 3 FIFO Threshold** Unit: Level
7:0	RW	0	**Video Window 3 FIFO Depth (-1)** Unit: Level

Note: One level is equal to 16 bytes.

Offset Address: 27F-27Ch

Video Window 3 Display Count On Screen Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:26	RW	0	**V3 Vertical Line Count That Shows On Screen** (Unit: Line)
15:12	RO	0	**Reserved**
11:0	RW	0	**V1 Horizontal Pixel Count That Shows On Screen (-1)** (Unit: Pixel)

Offset Address: 283-280h

Primary Display Second Color Key **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**CRT Color Key Enable** 0: Disable 1: Enable
29	RW	0	**CRT Color Key Inverse Control** 0: Display video if color key matches 1: Display video if color key does not match
28:24	RO	0	**Reserved**
23:0	RW	0	**Primary Display Color Key** Bits [23:0]: For 32-bit true color mode Bits [15:0]: For 565 high color mode Bits [14:0]: For 555 high color mode Bits [7:0]: For 256 color mode

Offset Address: 287-284h

Video Window 1 Color Space Conversion and Enhancement Control 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**SDTV (BT601) Coefficient Enable** 0: Disable 1: Enable
30	RW	0	**HDTV (BT709) Coefficient Enable** 0: Disable 1: Enable
29	RO	0	**Reserved**
28:24	RW	0	**Coefficient A** X.XXXX From 0 to 1.9375
23:22	RO	0	**Reserved**
21:16	RW	0	**Coefficient B1** SXX.XXX S=1: negative, S=0: positive; from –2.125 to 2.125.
15:14	RO	0	**Reserved**
13:8	RW	0	**Coefficient C1** SXX.XXX S=1: negative, S=0: positive; from –2.125 to 2.125.
7:0	RW	0	**Coefficient D** 2's complement integer; from -128 to 127.

Note: $R = AY+B_1Cb+C_1C_r+D$

Offset Address: 28B-288h

Video Window 1 Color Space Conversion and Enhancement Control 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:24	RW	0	**Coefficient B2** SX.XXX S=1: negative, S=0 positive; from –1.875 to 1.875.
23:21	RO	0	**Reserved**
20:16	RW	0	**Coefficient C2** SX.XXX S=1: negative, S=0 positive; from –1.875 to 1.875.
15:14	RO	0	**Reserved**
13:8	RW	0	**Coefficient B3** SXX.XXX S=1: negative, S=0 positive; from –3.875 to 3.875.
7:6	RO	0	**Reserved**
5:0	RW	0	**Coefficient C3** SXX.XXX S=1: negative, S=0 positive; from –3.875 to 3.875.

Note: $G = AY+B_2Cb+C_2C_r+D$
$B = AY+B_3Cb+C_3C_r+D$

Offset Address: 28F-28Ch – Reserved

Offset Address: 293-290h

Alpha Window / Hardware Icon (For Primary Display) Ending Position **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	**Hardware Icon Horizontal (X) Ending Position**
15:11	RO	0	**Reserved**
10:0	RW	0	**Hardware Icon Vertical (Y) Ending Position** Unit: Line

Offset Address: 297-294h

3D AGP Pause Address MMIO Port **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**3D AGP Pause Address MMIO Port**

Offset Address: 29B-298h

Compose Output Mode Select **Default Value: 0300 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Video 1 Command End, V1 Load New Register Setting** 1: Fire If registers are updated to engine, this bit will be cleared to 0 and the default is set at 0.
30	RW	0	**Video 3 Command End, V3 Load New Register Setting** 1: Fire If registers are updated to engine, this bit will be cleared to 0 and the default is set at 0.
29	RW	0	**Video Register Always Loaded** For hardware simulation and the default is set at 0.
28	RW	0	**Video Register Loaded at Vertical Blanking Without Waiting Source Flip** Need to write bit[31] or bit[30] and default is set at 0.
27	RW	0	**Video 3 Register Always Loaded** For hardware simulation and the default is set at 0.
26	RW	0	**Video 3 Register Loaded at Vertical Blanking Without Waiting Source Flip** Need to write bit[31] or bit[30] and default is set at 0.
25:24	RW	11b	**Interpolation FIFO Clock Select** 00: Not in use 01: V1 HDTV 10: V3 HDTV 11: V1 SDTV and V3 SDTV
23:21	RO	0	**Reserved**
20	RW	0	**Video Output Overlap Control** 0: V1 is on top 1: V3 is on top
19:8	RO	0	**Reserved**
7	RW	0	**MCK Bypass Enable** 0: Disable 1: Enable
6	RO	0	**Reserved**
5	RW	0	**Bypass LCD Horizontal Magnify Function**
4	RW	0	**Bypass LCD Vertical Magnify Function**
3	RW	0	**Video 3 Line Flip Enable** 0: Disable 1: Enable
2	RW	0	**Video 1 Line Flip Enable** 0: Disable 1: Enable
1	RO	0	**Reserved**
0	RW	0	**Video 1 Round Control Enable** 0: Disable 1: Enable

Offset Address: 29F-29Ch

Video Window 3 Frame Buffer Starting Address 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:29	RW	00b	**Target of The Third Frame Buffer Starting Address** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:3	RW	0	**The Third Frame Buffer Starting Address of V3** Unit: 16 bytes
2:0	RO	0	**Reserved**

Offset Address: 2A3-2A0h

Video Stream 3 Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**V3 Window Pre-fetch Enable** 0: Disable 1: Enable
29	RW	0	**V3 Window Gamma Function Enable** 0: Disable 1: Enable
28:27	RO	0	**Reserved**
26:25	RW	00b	**V3 Flip Control** 00: SW flip 01: HW flip and triggered by the HQV engine 10: Reserved 10: HW flip and triggered by the Capture Port 0 11: Reserved 11: HW flip and triggered by the Capture Port 1
24	RW	0	**V3 Frame to Field Enable** 0: Disable 1: Enable If enabled, the stride will be 2 times of original values. This bit is valid when software flip or HQV flip.
23	RO	0	**Reserved**
22	RW	0	**V3 De-interlace Mode** 0: Disable 1: Enable If enabled, hardware will add one line to the top of odd (bottom) field.
21	RW	0	**V3 Line Flip Only in Non Video Active Period Enable** 0: Disable 1: Enable
20:16	RW	0	**V3 Request Expire Number** Unit: 4 requests
15:10	RO	0	**Reserved**
9	RW	0	**Divided V3 Flip for HQV Engine VSYNC Number to Half** 0: Disable 1: Enable
8	RW	0	**V3 Color Space Conversion** 0: Enable 1: Disable
7	RW	0	**V3 Color Space Conversion Chroma Sign Bits Conversion** 0: Normal 1: Inverse
6:5	RO	0	**Reserved**
4:2	RW	000b	**V3 Stream Data Format** x00: YUV422 001: RGB32 x10: RGB15 011: RGB16 Others: Reserved
1	RO	0	**Reserved**
0	RW	0	**V3 Enable** 0: Disable 1: Enable

Offset Address: 2A7-2A4h

Video Window 3 Frame Buffer Starting Address 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**V3 Play Odd / Even Field Control** This bit is valid when SW Playback and Field Base Picture are selected. 0: Play even field 1: Play odd field
30:29	RO	00b	**Target of The First Frame Buffer Starting Address** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:2	RW	0	**The First Frame Buffer Starting Address of V3** Unit: 4 bytes
1:0	RO	0	**Reserved**

Offset Address: 2AB-2A8h

Video Window 3 Frame Buffer Starting Address 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:29	RW	00b	**Target of The Second Frame Buffer Starting Address** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:3	RW	0	**The Second Frame Buffer Starting Address of V3** Unit: 16 bytes
2:0	RO	0	**Reserved**

Offset Address: 2AF-2ACh

Video Window 3 Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13:4	RW	0	**V3 Frame Buffer Stride** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 2B3-2B0h

Video Window 3 Horizontal and Vertical Start **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**V3 Horizontal (X) Starting Location** Unit: Pixel
15:11	RO	0	**Reserved**
10:0	RW	0	**V3 Vertical (Y) Starting Location** Unit: Line

Offset Address: 2B7-2B4h

Video Window 3 Horizontal and Vertical End **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**V3 Horizontal (X) Ending Location** Unit: Pixel
15:11	RO	0	**Reserved**
10:0	RW	0	**V3 Vertical (Y) Ending Location** Unit: Line

Offset Address: 2BB-2B8h

Video Window 3 and Alpha Window Fetch Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**V3 Per Line Fetch Count** Unit: Pixel
19:10	RO	0	**Reserved**
9:0	RW	0	**Alpha Window Per Line Fetch Count** Unit: Line

Offset Address: 2BF-2BCh

Video Window 3 Display Zoom Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**V3 Horizontal (X) Zoom Enable** 0: Disable 1: Enable
30:27	RO	0	**Reserved**
26:16	RW	0	**V3 Horizontal (X) Zoom Factor**
15	RW	0	**V3 Vertical (Y) Zoom Enable** 0: Disable 1: Enable
14:10	RO	0	**Reserved**
9:0	RW	0	**V3 Vertical (Y) Zoom Factor**

Offset Address: 2C3-2C0h

Video Window 3 Minify and Interpolation Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RW	0	**Reserved**
26:24	RW	000b	**V3 Horizontal (X) Minify Control** 000: No minify 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Others: Reserved.
23:19	RO	0	**Reserved**
18:16	RW	000b	**V3 Vertical (Y) Minify Control** 000: No minify 001: Minify by a factor of 2 010: Reserved 011: Minify by a factor of 4 101: Minify by a factor of 8 111: Minify by a factor of 16 Others: Reserved.
15:3	RO	0	**Reserved**
2	RW	0	**V3 Luma-only Interpolation When The Vertical Interpolation Is Enabled** 0: Only luma values interpolated 1: All YUV/YcbCr values interpolated
1	RW	0	**V3 Horizontal (X) Interpolation Mode Select** 0: Pixel is replicated 1: Enable interpolation
0	RW	0	**V3 Vertical (Y) Interpolation Mode Select** 0 Pixel is replicated 1 Enable interpolation Note: V1 and V3 can support interpolation simultaneously when both video source resolutions are lower than 800x600. If anyone exceeds the 800x600 resolution, only one of them can support interpolation. The control bit is defined at 0x298[25:24].

Offset Address: 2C7-2C4h

Video Window 3 Color Space Conversion and Enhancement Control 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**SDTV (BT601) Coefficient Enable** 0: Disable 1: Enable
30	RW	0	**HDTV (BT709) Coefficient Enable** 0: Disable 1: Enable
29	RO	0	**Reserved**
28:24	RW	0	**Coefficient A** X.XXXX from 0 to 1.9375
23:22	RO	0	**Reserved**
21:16	RW	0	**Coefficient B1** SXX.XXX S=1: negative, S=0: positive; from – 2.125 to 2.125.
15:14	RO	0	**Reserved**
13:8	RW	0	**Coefficient C1** SXX.XXX S=1: negative, S=0: positive; from – 2.125 to 2.125.
7:0	RW	0	**Coefficient D[10:3]** 2's complement integer; from -128 to 127.

Note: R=AY+B1Cb+C1Cr+D

Offset Address: 2CB-2C8h

Video Window 3 Color Space Conversion and Enhancement Control 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RW	0	**Coefficient D[2:0]** 2's complement integer; from -128 to 127.
28:24	RW	0	**Coefficient B2** SX.XXX S=1: negative, S=0: positive; from –1.875 to 1.875.
23:21	RO	0	**Reserved**
20:16	RW	0	**Coefficient C2** SX.XXX S=1: negative, S=0: positive; from –1.875 to 1.875.
15:14	RO	0	**Reserved**
13:8	RW	0	**Coefficient B3** SXX.XX S=1: negative, S=0 positive; from 0 to 3.75 .
7:6	RO	0	**Reserved**
5:0	RW	0	**Coefficient C3** SX.XX S=1: negative, S=0: positive; from –3.875 to 3.875.

Note: G = AY+B2Cb+C2Cr+D, B = AY+B3Cb+C3Cr+D

Offset Address: 2CF-2CCh – Reserved

Offset Address: 2D3-2D0h

Graphic Hardware Cursor Mode Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Mono Cursor Display Path** 0: Primary 1: Secondary
30:29	RW	00b	**Target of The Hardware Cursor Buffer Starting Address** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:26	RO	0	**Reserved**
25:8	RW	0	**Hardware Cursor Base Address** Up to 64M bytes For 32x32x2 pattern: Bits [25:8] define the base address For 64x64x2 pattern: Bits [25:10] define the base address
7:2	RO	0	**Reserved**
1	RW	0	**Hardware Cursor Size** 0: 64x64x2 1: 32x32x2
0	RW	0	**Hardware Cursor Enable** 0: Disable 1: Enable

Offset Address: 2D7-2D4h

Graphic Hardware Cursor Position **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Hardware Cursor Position in the X-coordinate**
15:11	RO	0	**Reserved**
10:0	RW	0	**Hardware Cursor Position in the Y-coordinate**

Offset Address: 2DB-2D8h

Graphic Hardware Cursor Origin **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Hardware Cursor Origin in the X-coordinate**
15:11	RO	0	**Reserved**
10:0	RW	0	**Hardware Cursor Origin in the Y-coordinate**

Offset Address: 2DF-2DCh

Graphic Hardware Cursor Background **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RW	0	**For 256 Color Mode** Bits [7:0] specify hardware cursor background color **For 555 High Color Mode** Bits [14:0] specify hardware cursor background color **For 565 High Color Mode** Bits [15:0] specify hardware cursor background color **For 32-bits True Color Mode** Bits [23:0] specify hardware cursor background color

Offset Address: 2E3-2E0h

Graphic Hardware Cursor Foreground **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RW	0	**For 256 Color Mode** Bits [7:0] specify hardware cursor foreground color. **For 555 High Color Mode** Bits [14:0] specify hardware cursor foreground color. **For 565 High Color Mode** Bits [15:0] specify hardware cursor foreground color. **For 32-bits True Color Mode** Bits [23:0] specify hardware cursor foreground color.

Table 3 below shows the hardware color cursor operation. Please be noted this table is only applicable to the graphics modes. For the text modes, the VGA registers control the hardware color cursor.

Table 3. Graphics Hardware Color Cursor Operation

Pixel Operation	AND Plane	XOR Plane
Choose graphics hardware color cursor background color	0	0
Choose graphics hardware color cursor foreground color	0	1
Transparent	1	0
VGA data is inverted	1	1

Offset Address: 2E7-2E4h – Reserved

Offset Address: 2EB-2E8h

HI FIFO Depth and Threshold Control (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**HI FIFO Pre-threshold** Let HI issue request early. Normally, this value is greater than or equal to HI FIFO threshold (Rx2E8[14:8]). (Unit: Level)
23:16	RO	0	**Reserved**
15:8	RW	0	**HI FIFO Threshold** Let HI request priority from low to high. (Unit: Level)
7:0	RO	0	**HI FIFO Depth (- 1)** Unit: Level

Offset Address: 2EF-2ECh

Hardware Icon (HI) Transparent Color (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:0	RW	0	**HI Transparent Color** Bits [29:0]: For RGB10 Bits [23:0]: For RGB32 Bits [15:0]: For RGB565 Bits [14:0]: For RGB555

Offset Address: 2F3-2F0h

Hardware Icon (HI) Control (Only for Primary Display) **Default Value: 000F 00F0h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**HI Window Pre-fetch Enable**
29	RW	0	**HWI + (1-aplha)*Graphics Mode** 0 Disable 1 Enable
28	RW	0	**Alpha Value Come From Where** Only for the true color hardware icon. 0: From bits [7:4] and bits[19:16] 1: From the bits [31:24] of hardware icon
27:26	RW	00b	**HI Window Size** 00: 32 x 32 01: 64 x 64 1x: 128 x 128 Unit: Pixel x line
25:24	RW	00b	**HI Data Stream Format** 00: RGB555 01: RGB565 10: RGB32 11: RGB10
23:20	RO	0	**Reserved**
19:16	RW	Fh	**HI Constant Alpha [3:0] (HIAPA)**
15:12	RW	0	**Alpha Changed Value (HICV) Per Frame as HI Fan In / Out Turn On (When Rx260[8] = 1)** ALPHAn[7:0] = ALPHAn-1[7:0] +/- HICV[3:0], where just ALPHAn[7:4] is valid alpha value and ALPHA0 = {HIAPA}.
11:10	RO	0	**Reserved**
9	RW	0	**HI Fan In / Out Selector** 0: Default 1: Fan in (+)
8	RW	0	**HI Fan In / Out Enable** 0: Disable 1: Enable
7:4	RW	Fh	**HI Constant Alpha[7:4] (HIAPA)** The rest bits are put on bits [19:16].
3	RO	0	**Reserved**
2	RW	0	**HI Blending Enable** 0: Default 1: Enable
1	RO	0	**Reserved**
0	RW	0	**HI Enable** 0: Default 1: Enable

Offset Address: 2F7-2F4h

Hardware Icon Frame Buffer Starting Address (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:29	RW	00b	**Target of The Frame Buffer Starting Address** 00: S.L. 01: S.F. 10: Reserved 11: L.L.
28:4	RW	0	**Frame Buffer Starting Address for Hardware Icon** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 2FB-2F8h

Hardware Icon (HI) Horizontal and Vertical Location Start (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Hardware Icon Horizontal (X) Starting Location** Unit: Pixel
15:11	RO	0	**Reserved**
10:0	RW	0	**Hardware Icon Vertical (Y) Starting Location** Unit: Line

Offset Address: 2FF-2FCh

Hardware Icon (HI) Center Offset (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22:16	RW	0	**Hardware Icon Horizontal (X) Center Offset** Unit: Pixel
15:7	RO	0	**Reserved**
6:0	RW	0	**Hardware Icon Horizontal (Y) Center Offset** Unit: Line

Offset Address: 1203-1200h

Video Gamma Color R Register for Video 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 1207-1204h

Video Gamma Color G Register for Video 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 120B-1208h

Video Gamma Color B Register for Video 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 120F-120Ch

Hardware Icon (HI) Inverse Color (Only For Primary Display) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:0	RW	0	**HI Inverse Color** Bits [29:0]: For RGB10 Bits [23:0]: For RGB32 Btis [15:0]: For RGB565 Bits [14:0]: For RGB555

Offset Address: 1223-1220h

Video Gamma Color R Register for Video 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 1227-1224h

Video Gamma Color G Register for Video 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 122B-1228h

Video Gamma Color B Register for Video 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:16	RW	0	**Color Value After Gamma Function**
15:5	RO	0	**Reserved**
4:0	RW	0	**Color Index Number for Gamma Function Division**

Offset Address: 122F-122Ch

Video Window 3 Horizontal and Vertical Starting Location Offset **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Video Window 3 Horizontal (X) Starting Location Offset** (Unit: 16 bytes)
15:11	RO	0	**Reserved**
10:0	RW	0	**Video Window 3 Vertical (Y) Starting Location Offset** (Unit: Line)

Offset Address: 1283-1280h

Interrupt Flags and Masks Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW1C	0	**MSI Pending Interrupt Re-trigger Bit** When SW wants to exit interrupt service, please clear the bit. HW may send out interrupt again if pending interrupt exists. The function is enabled when MSI Enable = 1'b1.
30:20	RO	0	**Reserved**
19	RW	0	**DMA3 Transfer Done Interrupt Enable** 0: Disable 1: Enable
18	RW	0	**DMA3 Descriptor Done Interrupt Enable** 0: Disable 1: Enable
17	RW	0	**DMA2 Transfer Done Interrupt Enable** 0: Disable 1: Enable
16	RW	0	**DMA2 Descriptor Done Interrupt Enable** 0: Disable 1: Enable
15:5	RO	0	**Reserved**
4	RW1C	0	**CRT Sense Interrupt Status**
3	RW1C	0	**DMA3 Transfer Done Interrupt Status**
2	RW1C	0	**DMA3 Descriptor Done Interrupt Status**
1	RW1C	0	**DMA2 Transfer Done Interrupt Status**
0	RW1C	0	**DMA2 Descriptor Done Interrupt Status**

Offset Address: 1287-1284h

Logic Signature Setting **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3	RW	0	**Signature RD Disable Channel 0**
2	RW	0	**VSYNC Select Signal Channel 0**
1	RW	0	**Signature Enable Channel 0 from T-Arbiter**
0	RW	0	**Signature Enable Channel 0 from P-Arbiter**

Offset Address: 128B-1288h – Reserved

Offset Address: 128F-128Ch

Logic Signature Adder Result 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Logic Signature Adder Result 0**

Offset Address: 1293-1290h

IGA1 Display Position Counter 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**IGA1 Display Line Counter**
15:0	RO	0	**IGA1 Display Frame Counter**

Offset Address: 1297-1294h

IGA1 Display Position Counter 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RO	0	**IGA1 Display Frame Counter**

Offset Address: 129B-1298h

IGA1 Display Position Counter 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RW	0	**IGA1 Display Frame Counter Enable** 0: Disable 1: Enable When this bit is disabled, frame counter always gets 16'h0.

Offset Address: 129F-129Ch

Logic Signature Data Result 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Logic Signature Data Result 0**

Offset Address: 12A3-12A0h

IGA2 Display Position Counter 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**IGA2 Display Line Counter**
15:0	RO	0	**IGA2 Display Frame Counter**

Offset Address: 12A7-12A4h

IGA2 Display Position Counter 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RO	0	**IGA2 Display Frame Counter**

Offset Address: 12AB-12A8h

IGA2 Display Position Counter 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RW	0	**IGA2 Display Frame Counter Enable** 0: Disable 1: Enable When this bit is disabled, frame counter always gets 16'h0.

Offset Address: 12B3-12B0h

Primary Display Data Color Space Conversion and Enhancement Control 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**A1 <= XXXXXXXXXX**
19:10	RW	0	**B1 <= XXXXXXXXXX**
9:0	RW	0	**C1 <= XXXXXXXXXX**

Note: Y = A1R+B1G+C1B+D
Coefficient A1, B1, C1: 10 bits, 0.XXXXXXXX from 0 to 0.99903 Coefficient D: 8 bit positive integer from 16 to 255

Offset Address: 12B7-12B4h

Primary Display Data Color Space Conversion and Enhancement Control 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**A2[9:0] <= XXXXXXXXXX**
19:10	RW	0	**B2[9:0] <= XXXXXXXXXX**
9:0	RW	0	**C2[9:0] <= XXXXXXXXXX**

Note: Cr = A2R+B2G+C2B +128
Coefficient A2, B2, C2: 11 bits S.XXXXXXXX 2's complement from -0.99903 to 0.99903

Offset Address: 12BB-12B8h

Primary Display Data Color Space Conversion and Enhancement Control 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**A3[9:0] <= XXXXXXXXXX**
19:10	RW	0	**B3[9:0] <= XXXXXXXXXX**
9:0	RW	0	**C3[9:0] <= XXXXXXXXXX**

Note: Cr = A3R+B3G+C3B +128
Coefficient A3, B3, C3: 11 bits. S.XXXXXXXX 2's complement from -0.99903 to 0.99903

Offset Address: 12BF-12BCh

Primary Display Data Color Space Conversion and Enhancement Control 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13	RW	0	**A2[10] <= S**
12	RW	0	**B2[10] <= S**
11	RW	0	**C2[10] <= S**
10	RW	0	**A3[10] <= S**
9	RW	0	**B3[10] <= S**
8	RW	0	**C3[10] <= S**
7:0	RW	0	**D**

DVD / Video Control Register (3260-326Ch)

Offset Address: 3260h
DVD / Video ID Control - *Refer toCR Chapter's "CR Registers in Video Control Register Space" for more details*

Offset Address: 326Ch
DVD / Video Wait Control - *Refer toCR Chapter's "CR Registers in Video Control Register Space" for more details*

VIDEO CAPTURE ENGINE REGISTERS

This document provides detailed video capture engine register summary table. Register descriptions on video capture engine registers are followed in the sequent sections.

Video Capture Engine Registers

These video capture engine register tables document the address offset, register name and register attribute for each register.

Table 4. Video Capture Engine

Offset (Hex)	Register Name	Attribute
First Video Capture Engine Register		
303-300	Capture Interrupt Control and Flags	RW
307-304	Reserved	RO
30B-308	Transport Stream Control	RW
30F-30C	Reserved	RO
313-310	Capture Interface Control	RW
317-314	Active Video Horizontal Range (CCIR601 only)	RW
31B-318	Active Video Vertical Range (CCIR601 only)	RW
31F-31C	Active Video Scaling Control	RW
323-320	VBI Data Horizontal Range	RW
327-324	VBI Data Vertical Range	RW
32B-328	First VBI Buffer Starting Address	RW
32F-32C	VBI Buffer Stride	RW
333-330	Ancillary Data Count Setting	RW
337-334	Maximum Data Count of Active Video	RW
33B-338	Maximum Data Count of VBI or ANC	RW
33F-33C	Capture Data Count	RO
343-340	First Active Video Frame Buffer Starting Address	RW
347-344	Second Active Video Frame Buffer Starting Address	RW
34B-348	Third Active Video Frame Buffer Starting Address	RW
34F-34C	Second VBI Buffer Starting Address	RW
353-350	Stride of Active Video Buffer and Coring Function Control	RW
357-354	TS Buffer 0 Error Packet Indicator	RO
35B-358	TS Buffer 1 Error Packet Indicator	RO
35F-35C	TS Buffer 2 Error Packet Indicator	RO
Second Video Capture Engine Registers (Refer to Rx300-35C register descriptions for detail.)		
1303-1300	Capture Interrupt Control and Flags	RW
1307-1304	Reserved	RO
130B-1308	Transport Stream Control	RW
130F-130C	Reserved	RO
1313-1310	Capture Interface Control	RW
1317-1314	Active Video Horizontal Range (CCIR601 only)	RW
131B-1318	Active Video Vertical Range (CCIR601 only)	RW
131F-131C	Active Video Scaling Control	RW
1323-1320	VBI Data Horizontal Range	RW
1327-1324	VBI Data Vertical Range	RW
132B-1328	First VBI Buffer Starting Address	RW
132F-132C	VBI Buffer Stride	RW
1333-1330	Ancillary Data Count Setting	RW
1337-1334	Maximum Data Count of Active Video	RW
133B-1338	Maximum Data Count of VBI or ANC	RW
133F-133C	Capture Data Count	RO

Offset (Hex)	Register Name	Attribute
1343-1340	First Active Video Frame Buffer Starting Address	RW
1347-1344	Second Active Video Frame Buffer Starting Address	RW
134B-1348	Third Active Video Frame Buffer Starting Address	RW
134F-134C	Second VBI Buffer Starting Address	RW
1353-1350	Stride of Active Video Buffer and Coring Function Control	RW
1357-1354	TS Buffer0 Error Packet Indicator	RO
135B-1358	TS Buffer1 Error Packet Indicator	RO
135F-135C	TS Buffer2 Error Packet Indicator	RO
1360-137C	Reserved	RO

Note:
1) Port Address: MB1 + Offset Address
MB1 is declared in the register with offset address 17h-14h in the PCI configuration space.

2) There is additional register space to match the above register definition. When a command is written to that space, it will be sent to "command regulator" first and then pass to video display engine. However, register read will be the same as the original action. The relationship between the additional register space and original register space is
(The additional register address) = (The original register address) + 16'h2000

Video Capture Engine Register Descriptions (300-35Fh)

Offset Address: 303-300h

Capture Interrupt Control and Flags **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10	RW	0	**Current Writing VBI Buffer ID**
9	RW	0	**End of VBI Interrupt Enable**
8	RW	0	**End of Active Video Interrupt Enable** If TS (Transport Stream) is enabled, it defines as TS data over a buffer interrupt enable.
7	RW1C	0	**Video Capture Port Internal FIFO Full Status**
6	RO	0	**Current Active Video Input Field Status** 0: Top field 1: Bottom field
5	RO	0	**Current Input Vsync Status** 0: Vertical blanking 1: Active video
4:3	RO	0	**Current Writing Active Video (or TS Data) Frame Buffer ID**
2	RO	0	**Flipping Active Video Field Status** 0: Top field 1: Bottom field
1	RW1C	0	**Video Capture End-of-VBI Status**
0	RW1C	0	**Video Capture End-of-Active Video Status** If TS is enabled, it defines as TS data over a buffer status.

Offset Address: 30B-308h

Transport Stream Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Serial Input Enable** 0: Enable parallel TS input 1: Enable serial TS input
21	RW	0	**Bit Alignment** Serial input mode only 0: LSB first 1: MSB first
20	RW	0	**Packet Starting Signal Disable** 0:Enable 1:Disable
19	RW	0	**Change Buffer Mode** 0: According to count packet number 1: According to byte count
18:4	RW	0	***When bit 19 = 0*** **Packet_Number_Minus_One** There are (Packet_Number_Minus_One + 1) packets per buffer. ***When bit 19 = 1*** **KBytes_Count** There are KBytes_Count Kbytes per buffer.
3:2	RW	00b	**Method to Move Received TS Data** 0x: Capture engine writes data to FB (Frame Buffer). After filled a buffer, it will trigger an interrupt to driver. 10: Capture engine writes data to FB. After filled a buffer, it will trigger an interrupt to DMA. 11: Capture engine controls DMA to move data. (not via frame buffer)(In mode = 2'b11, set FIFO Threshold Rx310[27:24] to 1)
1	RW	0	**Drop Error Packet** This bit is valid only when TS_DERR pin is available 0: Write all received data out 1: Drop the data of error packet
0	RW	0	**Transport Stream Input Enable** 0: Disable 1: Enable Turn on this bit before enabling capture engine Rx310[0].

Offset Address: 313-310h

Capture Interface Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Capture CLK Enable** 0: Disable 1: Enable This bit should be turned on before setting Rx310[0].
30	RW	0	**Capture FIELD Signal Output Inverted Select** 0: Normal 1: Inverted
29	RW	0	**Vertical Count Starting Reference** 0: Negative edge of VREF 1: Positive edge of VREF
28	RW	0	**Horizontal Count Starting Reference** 0: Negative edge of HREF 1: Positive edge of HREF
27:24	RW	0	**Capture FIFO Threshold** (Unit: level) Once the queuing captured data is more than the threshold, it starts to write data out. Unit of the 1st capture engine is 4-level, the FIFO size is 64-level x 64-bit. Unit of the 2nd capture engine is 2-level, the FIFO size is 32-level x 64-bit.
23	RW	0	**Switch Capture Clock Source** Since there are two capture clock sources, use this bit to switch it. In VIP2.0 while using task bit to differentiate video stream, it needs to switch the clock source as the same one. For 1st Capture Engine: 0: Clock from 1st capture CLK pin 1: Clock from 2nd capture CLK pin For 2nd Capture Engine: 0: Clock from 2nd capture CLK pin 1: Clock from 1st capture CLK pin
22	RW	0	**Capture FIELD Input Inverted Select** 0: Normal 1: Inverted
21	RW	0	**Capture HREF Input Inverted Select** 0: Normal 1: Inverted
20	RW	0	**Capture VREF Input Inverted Select** 0: Normal 1: Inverted
19	RW	0	**Capture CLK Input Inverted Select** 0: Normal 1: Inverted
18:16	RW	000b	**Capture Horizontal Filter Mode Select (2P)** 000: No filtering 001: 2 tap (1,1)/2 010: 3 tap (1,2,1)/4 011: 4 tap (1,3,3,1)/8 100: 5 tap (1,2,2,2,1)/8 101~111:Reserved
15	RW	0	**Capture Flipping Control When Rx310[13:12] Is Set to 2'b11** 0: Capture engine flips to HQV or video engine after captured a frame. 1: Capture engine flips to HQV or video engine after captured a field (HQV or Video should set to frame_to_field).
14	RW	0	**4:2:2 to 4:4:4 Cb, Cr Type Select** 0: Duplication 1: Interpolation
13:12	RW	00b	**Capture De-interlace Mode Select** 00: Capture odd field only, 30fps 01: Capture even field only, 30fps 10: Capture odd / even field, 60fps; place on the same location 11: Capture odd / even field, 30fps; place in interlace fashion doubling the storage space
11	RW	0	**Input FIELD Signal Enable** If TS is enabled, it defines as TS_DERR signal enable. 0: Disable 1: Enable
10	RW	0	**VIP Type** 0: VIP1.1. VBI data region is specified by task bit. 1: VIP2. VBI data region is specified by SAV / EAV during vertical blanking period.

(Continued for Rx310h)

Bit	Attribute	Default	Description
9:8	RW	00b	**Byte Swapping Control** 00: 0123 (no swap: YUYV) 01: 1032 (C, Y swap: UYVY) 10: 0321 (Cr, Cb swap: YVYU) 11: 3012 (Cr, Cb swap and Y swap: VYUY)
7	RW	0	**16 Bit Input Low/High Swap** 0: Not inverted 1: Low/high byte inverted
6	RW	0	**CCIR656-16 Bit Header Decode Mode** 0: Low 8 bits 1: 16 bits all
5:4	RW	00b	**Input Stream Type** 00: CCIR601, 8-bit 01: CCIR656, 8-bit 10: CCIR601, 16-bit 11: CCIR656, 16-bit
3	RW	0	**VIP Enable** 0: Disable 1: Enable
2	RW	0	**Buffer Mode** 0: Double buffers, use starting address 1 and 2 1: Triple buffers, use starting address 1, 2 and 3
1	RW	0	**Bit Stream Selection of VIP2.0** In VIP2.0, task bit to differentiate video stream. For the 1st capture engine: 0: Capture the data of task bit is 0 1: Capture the data of task bit is 1 For the 2nd capture engine: 0: Capture the data of task bit is 1 1: Capture the data of task bit is 0
0	RW	0	**Capture Enable** 0: Disable 1: Enable

Offset Address: 317-314h

Active Video Horizontal Range **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	**Horizontal Ending Cycle (CCIR601 only)** (Unit: Cycle)
15:12	RO	0	**Reserved**
11:0	RW	0	**Horizontal Starting Cycle (CCIR601 only)** (Unit: Cycle)

Offset Address: 31B-318h

Active Video Vertical Range **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Vertical Ending Line (CCIR601 only)** (Unit: Line)
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Starting Line (CCIR601 only)** (Unit: Line)

Offset Address: 31F-31Ch

Active Video Scaling Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
26	RW	0	**Vertical Minify Enable** 0: Disable 1: Enable
25:16	RW	0	**Vertical Minify Factor**
15:12	RO	0	**Reserved**
11	RW	0	**Horizontal Minify Enable** 0: Disable 1: Enable
10:0	RW	0	**Horizontal Minify Factor**

Offset Address: 323-320h

VBI Data Horizontal Range **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:16	RW	0	**Horizontal Ending Cycle** (Unit: Cycle)
15:12	RO	0	**Reserved**
11:0	RW	0	**Horizontal Starting Cycle** (Unit: Cycle)

Offset Address: 327-324h

VBI Data Vertical Range **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Vertical Ending Line** (Unit: Line)
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Starting Line** (Unit: Line)

Offset Address: 32B-328h

First VBI Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**VBI Data Enable** 0: Disable 1: Enable
30	RW	0	**VBI Mode Select** 0: Range depends on SAV/EAV 1: Capture by specific range (defined by register 320h, 324h) When VIP is enabled (Rx310[3]=1), this bit setting would be ignored, capture VBI data is defined as VIP spec.
29	RO	0	**Reserved**
28:4	RW	0	**VBI or ANC Buffer 0 Starting Address** (Unit: 16 bytes)
3:2	RO	0	**Reserved**
1:0	RW	00b	**Buffer Selection** 00: S.L. 01: S.F. 10: S.M. 11: L.L.

Offset Address: 32F-32Ch

VBI Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13	RW	0	**VBI Data Placement Method** 0: Linear, no stride needed 1: With stride
12:4	RW	0	**VBI Buffer Stride** (Unit: 16 bytes)
3:0	RO	0	**Reserved**

Offset Address: 333-330h

Ancillary Data Count Setting **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:15	RO	0	**Reserved**
14	RW	0	**Ancillary Data Type** 0: Type2 – 00-FF-FF-DID-SDID-NN-….-….-CheckSumByte-FillBytes. Total captured data are (8Bytes + NN*4Bytes). 1: Type1 – 00-FF-FF-DID-DBN-NN-….-….-CheckSumByte-FillBytes. Total captured data are (8Bytes + (DBN+NN)*4Bytes).
13	RW	0	**Ancillary Data Enable** 0: Disable 1: Enable
12	RW	0	**Ancillary Data Count Reference Select** 0: By header decoder 1: By register (define by Rx330[11:0])
11:0	RW	0	**Ancillary Data Should Be Capture Length** (Unit: Double-word)

Offset Address: 337-334h

Maximum Data Count of Active Video **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
26:16	RW	0	**Maximum Active Video Line Count In A Field** (Unit: Line) If TS is enabled, it defines as the maximum TS data count of a packet (Unit: Byte).
15:9	RO	0	**Reserved**
8:0	RW	0	**Maximum Active Video QW Count In A Line** (Unit: 8 bytes)

Offset Address: 33B-338h

Maximum Data Count of VBI or ANC **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
26:16	RW	0	**Maximum VBI or ANC Line Count In A Field** (Unit: Line)
15:9	RO	0	**Reserved**
8:0	RW	0	**Maximum VBI or ANC QW Count In A Line** (Unit: 8 bytes)

Offset Address: 33F-33Ch

Capture Data Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Current Active Video Line Counter** (Unit: Line)
15:13	RO	0	**Reserved**
12:0	RW	0	**VBI or ANC Data Length That Has Been Captured** (Unit: 8 bytes)

Offset Address: 343-340h

First Active Video Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Active Video Frame Buffer 0 Starting Address** (Unit: 16 bytes) If TS is enabled, it defines as frame buffer 0 starting address for TS data.
3:2	RO	0	**Reserved**
1:0	RW	00b	**Buffer Selection** 00: S.L. 01: S.F. 10: S.M. 11: L.L.

Offset Address: 347-344h

Second Active Video Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Active Video Frame Buffer 1 Starting Address** (Unit: 16 bytes) If TS is enabled, it defines as frame buffer 1 starting address for TS data.
3:2	RO	0	**Reserved**
1:0	RW	00b	**Buffer Selection** 00: S.L. 01: S.F. 10: S.M. 11: L.L.

Offset Address: 34B-348h

Third Active Video Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Active Video Frame Buffer 2 Starting Address** (Unit: 16 bytes) If TS is enabled, it defines as frame buffer 2 starting address for TS data.
3:2	RO	0	**Reserved**
1:0	RW	00b	**Buffer Selection** 00: S.L. 01: S.F. 10: S.M. 11: L.L.

Offset Address: 34F-34Ch

Second VBI Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**VBI or ANC Buffer 1 Starting Address** (Unit: 16 bytes)
3:2	RO	0	**Reserved**
1:0	RW	00b	**Buffer Selection** 00: S.L. 01: S.F. 10: S.M. 11: L.L.

Offset Address: 353-350h

Stride of Active Video Buffer & Coring Function Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23	RW	0	**Coring Function Enable**
22:16	RW	0	**Coring Function Compare Data (CCD)** If coring function is enabled (Rx350[23]) and (-(CCD+1) <= U, V <= CCD), all of these U and V will be truncated to zero.
15:13	RO	0	**Reserved**
12:4	RW	0	**Stride of Active Video Buffer** (Unit: 8 bytes)
3:0	RO	0	**Reserved**

Offset Address: 357-354h

TS Buffer 0 Error Packet Indicator **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Last Error Packet Indicator** 0: Less than one error packet in this buffer, defined at bits [15:0] 1: More than two error packets, the last error packet ID defined at bits [30:16]
30:16	RO	0	**Last Error Packet ID**
15	RO	0	**First Error Packet Indicator** 0: No error packet in this buffer 1: More than one error packet, the first error packet ID defined at bits [14:0]
14:0	RO	0	**First Error Packet ID**

Offset Address: 35B-358h

TS Buffer 1 Error Packet Indicator **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Last Error Packet Indicator** 0: Less than one error packet in this buffer, defined at bits [15:0] 1: More than two error packets, the last error packet ID defined at bits [30:16]
30:16	RO	0	**Last Error Packet ID**
15	RO	0	**First Error Packet Indicator** 0: No error packet in this buffer 1: More than one error packet, the first error packet ID defined at bits [14:0]
14:0	RO	0	**First Error Packet ID**

Offset Address: 35F-35Ch

TS Buffer 2 Error Packet Indicator **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Last Error Packet Indicator** 0: Less than one error packet in this buffer, defined at bits [15:0] 1: More than two error packets, the last error packet ID defined at bits [30:16]
30:16	RO	0	**Last Error Packet ID**
15	RO	0	**First Error Packet Indicator** 0: No error packet in this buffer 1: More than one error packet, the first error packet ID defined at bits [14:0]
14:0	RO	0	**First Error Packet ID**

Note:
Capture supports 2 input interfaces; therefore, an additional register space is provided to match the above registers definition.
A write to this additional register space will send the data to the second Capture Engine.
The relationship between the additional register space and original register space is
(The additional register address) = (The original register address) + 16'h1000.

HQV REGISTERS

This section provides detailed HQV register summary table. Register descriptions on high quality video registers are followed in the sequent sections.

HQV Registers

These HQV register tables document the I/O port, I/O index and attribute ("Attribute") for each register.

Table 5. High Quality Video Registers

Offset (Hex)	Register Name	Attribute
First HQV (High Quality Video) Engine Registers		
363-360	HQV Color Adjustment Control 1	RW
367-364	HQV Color Adjustment Control 2	RW
36B-368	HQV Color Adjustment Control 3	RW
36F-36C	HQV Color Adjustment Control 4	RW
373-370	HQV Video Start Point Offset Control in Source	RW
377-374	HQV Sub-picture Start Point Offset Control in Source	RW
37B-378	HQV Video End Point Offset Control in Source	RW
37F-37C	HQV Sub-picture End Point Offset Control in Source	RW
383-380	HQV Video Start point Offset Control in Destination	RW
387-384	HQV Sub-picture Start Point Offset Control in Destination	RW
38B-388	HQV Video End Point Offset Control in Destination	RW
38F-38C	HQV Sub-picture End Point Offset Control in Destination	RW
393-390	HQV Parameters of Hardware Tuning Performance/Quality	RW
397-394	HQV Extended Control	RW
39B-398	HQV Static Record Frame Buffer Starting Address	RW
39F-39C	HQV Static Record Frame Buffer Stride	RW
3A3-3A0	HQV Color Adjustment Control 5	RW
3A7-3A4	HQV Color Adjustment Control 6	RW
3AB-3A8	HQV Color Adjustment Control 7	RW
3AF-3AC	HQV Color Adjustment Control 8	RW
3B3-3B0	HQV Video Horizontal Scale Control	RW
3B7-3B4	HQV Video Vertical Scale Control	RW
3BB-3B8	HQV Background Color	RW
3BF-3BC	HQV Segment Residue Pixel Frame Buffer Starting Address	RW
3C3-3C0	HQV Sub-picture Frame Buffer Stride and Control	RW
3C7-3C4	HQV Sub-picture Frame Buffer Starting Address	RW
3CB-3C8	HQV Sub-picture 4 x 16 RAM Table Write Control	RW
3CF-3CC	HQV Background Offset	RW
3D3-3D0	HQV Stream Control and Status	RW
3D7-3D4	HQV SW Source Buffer –Luma or Packed Starting Address	RW
3DB-3D8	HQV SW Source Buffer – Chroma Starting Address	RW
3DF-3DC	HQV Linear/Tile Address Mode, Color Space Conversion, Gamma and De-blocking Control	RW
3E3-3E0	HQV Sub-picture Horizontal Scale Control	RW
3E7-3E4	HQV Motion Adaptive De-interlace Control & Threshold	RW
3EB-3E8	HQV Sub-picture Vertical Scale Control	RW
3EF-3EC	HQV Destination Frame Buffer Starting Address 0	RW
3F3-3F0	HQV Destination Frame Buffer Starting Address 1	RW
3F7-3F4	HQV Destination Frame Buffer Stride	RW
3FB-3F8	HQV Source Frame Buffer Stride	RW
3FF-3FC	HQV Destination Frame Buffer Starting Address 2	RW

Offset (Hex)	Register Name	Attribute
Second HQV Engine Registers (Refer to Rx360-3FC register descriptions for detail)		
1363-1360	HQV Color Adjustment Control 1	RW
1367-1364	HQV Color Adjustment Control 2	RW
136B-1368	HQV Color Adjustment Control 3	RW
136F-136C	HQV Color Adjustment Control 4	RW
1373-1370	HQV Video Start Point Offset Control in Source	RW
1377-1374	HQV Sub-picture Start Point Offset Control in Source	RW
137B-1378	HQV Video End Point Offset Control in Source	RW
137F-137C	HQV Sub-picture End Point Offset Control in Source	RW
1383-1380	HQV Video Start Point Offset Control in Destination	RW
1387-1384	HQV Sub-picture Start Point Offset Control in Destination	RW
138B-1388	HQV Video End Point Offset Control in Destination	RW
138F-138C	HQV Sub-picture End Point Offset Control in Destination	RW
1393-1390	HQV Parameters of Hardware Tuning Performance/Quality	RW
1397-1394	HQV Extended Control	RW
139B-1398	HQV Static Record Frame Buffer Starting Address	RW
139F-139C	HQV Static Record Frame Buffer Stride	RW
13A3-13A0	HQV Color Adjustment Control 5	RW
13A7-13A4	HQV Color Adjustment Control 6	RW
13AB-13A8	HQV Color Adjustment Control 7	RW
13AF-13AC	HQV Color Adjustment Control 8	RW
13B3-13B0	HQV Video Horizontal Scale Control	RW
13B7-13B4	HQV Video Vertical Scale Control	RW
13BB-13B8	HQV Background Color	RW
13BF-13BC	HQV Segment Residue Pixel Frame Buffer Starting Address	RW
13C3-13C0	HQV Sub-picture Frame Buffer Stride and Control	RW
13C7-13C4	HQV Sub-picture Frame Buffer Starting Address	RW
13CB-13C8	HQV Sub-picture 4 x 16 RAM Table Write Control	RW
13CF-13CC	HQV Background Offset	RW
13D3-13D0	HQV Stream Control and Status	RW
13D7-13D4	HQV SW Source Buffer –Luma or Packed Starting Address	RW
13DB-13D8	HQV SW Source Buffer – Chroma Starting Address	RW
13DF-13DC	HQV Linear/Tile Address Mode, Color Space Conversion, Gamma and De-blocking Control	RW
13E3-13E0	HQV Sub-picture Horizontal Scale Control	RW
13E7-13E4	HQV Motion Adaptive De-interlace Control & Threshold	RW
13EB-13E8	HQV Sub-picture Vertical Scale Control	RW
13EF-13EC	HQV Destination Frame Buffer Starting Address 0	RW
13F3-13F0	HQV Destination Frame Buffer Starting Address 1	RW
13F7-13F4	HQV Destination Frame Buffer Stride	RW
13FB-13F8	HQV Source Frame Buffer Stride	RW
13FF-13FC	HQV Destination Frame Buffer Starting Address 2	RW

Note:
1) Port Address: MB1 + Offset Address
MB1 is declared in the register with offset address 17h-14h in the PCI configuration space.

2) There is an additional register space to match the above register definition. When write a register to this space, it will be sent to "command regulator" first and then pass to video display engine. However, register read will be the same as the original action. The relationship between the additional register space and original register space is
(The additional register address) = (The original register address) + 16'h2000

HQV Engine Register Descriptions (360-3FFh)

Offset Address: 363-360h
HQV Color Adjustment Control 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:17	RW	0	**Coefficient D1(s[26:18].[17])** (2P)
16:0	RW	0	**Coefficient C1(s[15:8].[7:0])** (2P)

Offset Address: 367-364h
HQV Color Adjustment Control 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:17	RW	0	**Coefficient D2(s[26:18].[17])** (2P)
16:0	RW	0	**Coefficient C2(s[15:8].[7:0])** (2P)

Offset Address: 36B-368h
HQV Color Adjustment Control 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:17	RW	0	**Coefficient D3(s[26:18].[17])** (2P)
16:0	RW	0	**Coefficient C3(s[15:8].[7:0])** (2P)

Offset Address: 36F-36Ch
HQV Color Adjustment Control 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:17	RO	0	**Reserved**
16:0	RW	0	**Coefficient B1(s[15:8].[7:0])** (2P)

Offset Address: 373-370h
HQV Video Start Point Offset Control in Source **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Horizontal Offset of Start Point for Video Location in Source Picture** Unit: Pixel (2P)
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Offset of Start Point for Video Location in Source Picture** Unit: Pixel (2P)

Offset Address: 377-374h
HQV Sub-picture Start Point Offset Control in Source **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Horizontal Offset of Start Point for Sub-picture Location in Source Picture** Unit: Pixel (2P)
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Offset of Start Point for Sub-picture Location in Source Picture** Unit: Pixel (2P)

Offset Address: 37B-378h

HQV Video End Point Offset Control in Source **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Horizontal Offset of End Point for Video Location in Source Picture** Unit: Pixel (2P)
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Offset of End Point for Video Location in Source Picture** Unit: Pixel (2P)

Offset Address: 37F-37Ch

HQV Sub-picture End Point Offset Control in Source **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Horizontal Offset of End Point for Sub-picture Location in Source Picture** Unit: Pixel (2P)
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Offset of End Point for Sub-picture Location in Source Picture** Unit: Pixel (2P)

Offset Address: 383-380h

HQV Video Start Point Offset Control in Destination **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Horizontal Offset of Start Point for Video Location In Destination Picture** Unit: Pixel (2P) Either video or sub-picture destination data horizontal offset of start point should be set to zero.
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Offset of Start Point for Video Location In Destination Picture** Unit: Line (2P) Either video or sub-picture destination data vertical offset of start point should be set to zero.

Offset Address: 387-384h

HQV Sub-picture Start Point Offset Control in Destination **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Horizontal Offset of Start Point for Sub-picture Location In Destination Picture** Unit: Pixel (2P) Either video or sub-picture destination data horizontal offset of start point should be set to zero.
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Offset of Start Point for Sub-picture Location In Destination Picture** Unit: Line (2P) Either video or sub-picture destination data vertical offset of start point should be set to zero.

Offset Address: 38B-388h

HQV Video End Point Offset Control in Destination **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Horizontal Offset of End Point for Video Location In Destination Picture** Unit: Pixel (2P)
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Offset of End Point for Video Location In Destination Picture** Unit: Line (2P)

Offset Address: 38F-38Ch

HQV Sub-picture End Point Offset Control in Destination **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Horizontal Offset of End Point for Sub-picture Location In Destination Picture** Unit: Byte (2P)
15:11	RO	0	**Reserved**
10:0	RW	0	**Vertical Offset of End Point for Sub-picture Location In Destination Picture** Unit: Line (2P)

Offset Address: 393-390h

HQV Parameters of Hardware Tuning Performance / Quality **Default Value: 4664 8688h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:28	RW	100b	**Threshold of Inter-Field Complexity for Pull Down Detection (x4)** Calculate the difference between current & previous field.
27	RO	0	**Reserved**
26:25	RW	11b	**Factor of Calculating Threshold of Intra-Field Complexity** 00: Threshold = 390[30:28]*4 + 390[30:28]*1 01: Threshold = 390[30:28]*4 + 390[30:28]*2 10: Threshold = 390[30:28]*4 + 390[30:28]*3 11: Threshold = 390[30:28]*4 + 390[30:28]*4
24:23	RO	0	**Reserved**
22:21	RW	11b	**Static Judgment Number (SJN)** As static record number is equal to SJN, then static flag is asserted
20	RW	0	**The Field Number for The Increment of Static Record** 0: 1 field / (static record) 1: 2 fields / (static record)
19:18	RW	01b	**Pull-down Factor 1** Apply this factor while pull-down not yet detected. 00: 2/8 01: 3/8 10: 4/8 11: 5/8
17:16	RW	00b	**Pull-down Factor 2** Apply this factor while pull-down detected 00: 3/8 01: 4/8 10: 5/8 11: 6/8
15:14	RW	10b	**Threshold for Pull Down Detection** (Rx3DC.[10:0]<<Rx390.[15:14]) as the minimum threshold for valid pull-down detection
13:12	RO	0	**Reserved**
11:8	RW	6h	**Threshold for Motion Detection (x2)**
7:4	RW	8h	**Edge Detection Threshold**: **for Degree 90 (x2)**
3:0	RW	8h	**Maximum Difference between Block Boundary (x4)** Apply de-blocking with sin(x) function while the difference between block boundary is greater than this setting.

Offset Address: 397-394h

HQV Extended Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10:8	RW	0	**Constriction Enable** 000: Constriction disable 001~111: Rounding LSB1~LSB7
7	RW	0	**Color Adjustment Enable** 0: Disable 1: Enable
6	RW	0	**Bob de-interlacing method** 0: Line average 1: Line duplication (for TV output)
5	RW	0	**YUV Output Format Control** (2P) 0: YUV422 out 1: YUV444 out This bit is effective when (H or V scaling size) < (1/2 H or V original) size. For the other cases, it just uses YUV422 out.
4	RW	0	**Color Space Conversion Method** 0: BT601 1: BT709
3	RW	0	**Color Format Convert Method** (from YUV420 ➔ YUV422) 0: 4-tap interpolation 1: Method 1 (-1 9 9 –1).
2:1	RW	00b	**Color Format Convert Method** (from YUV422 ➔ YUV444) 00: Method 1 (WMV9 and H.264) 01: Reserved 1x: Method 3 (-1 9 9 –1).
0	RW	0	**Color Format Convert Method** (from YUV444 ➔ YUV422) 0: Method 1 (1 1) 1: Method 2 (Drop) This bit is effective as (no scaling) or (scaling size) > (1/2 original size). For the other cases, it just uses method 2.

Offset Address: 39B-398h

HQV Static Record Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Static Record Frame Buffer Starting Address** Unit: 16 bytes
3:2	RO	0	**Reserved**
1:0	RW	0	**Memory Location**

Offset Address: 39F-39Ch

HQV Static Record Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:15	RW	0	**Coefficient B2(s[30:23].[22:15])** (2P)
14:10	RO	0	**Reserved**
9:4	RW	0	**Static Record Frame Buffer Stride** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 3A3-3A0h

HQV Color Adjustment Control 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:17	RO	0	**Reserved**
16:0	RW	0	**Coefficient B3(s[15:8].[7:0])** (2P)

Note: Y'(R') = A1*Y(R) + B1*Cb(G) + C1*Cr(B) + D1

Offset Address: 3A7-3A4h

HQV Color Adjustment Control 6 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:17	RO	0	**Reserved**
16:0	RW	0	**Coefficient A1(s[15:8].[7:0])** (2P)

Note: Cb'(G') = A2*Y(R) + B2*Cb(G) + C2*Cr(B) + D2

Offset Address: 3AB-3A8h

HQV Color Adjustment Control 7 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:17	RO	0	**Reserved**
16:0	RW	0	**Coefficient A2(s[15:8].[7:0])** (2P)

Note: Cr'(B') = A3*Y(R) + B3*Cb(G) + C3*Cr(B) + D3

Offset Address: 3AF-3ACh

HQV Color Adjustment Control 8 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:17	RO	0	**Reserved**
16:0	RW	0	**Coefficient A3(s[15:8].[7:0])** (2P)

Offset Address: 3B3-3B0h

HQV Video Horizontal Scale Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Horizontal Scale Enable** 1: Enable (2P)
30	RO	0	**Reserved**
29:28	RW	00b	**Horizontal Scale Function** (2P) 00: Scale up. 01: 1~1/4 10: $1/4^{-}$~$1/8^{+}$ 11: <1/8
27:15	RO	0	**Reserved**
14:0	RW	0	**Horizontal Scale Factor [14:12].[11:0]** (2P)

Note: Scale factor:

1. Scale up: source/destination
2. 1~1/4: source/(destination+0.5)
3. $1/4^{-}$~$1/8^{+}$: source/destination
4. <1/8: destination/source

Offset Address: 3B7-3B4h

HQV Video Vertical Scale Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Vertical Scale Enable** 1: Enable (2P)
30:29	RO	0	**Reserved**
28	RW	0	**Vertical Scale Function** (2P) 0: Scale up. 1: Scale down
27:17	RO	0	**Reserved**
16:0	RW	0	**Vertical Scale Factor [16:12].[11:0]** (2P)

Note: Scale factor

1. Scale up: source/destination;
2. Scale down: source/(destination+0.5)

PS:
For all scaling calculation, the final results should be rounded to the nearest integer.
For bi-linear factor, please use 6 binary fraction of factor (need be rounded to the nearest 6^{th} fraction) to do the calculation.

Offset Address: 3BB-3B8h

HQV Background Color **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RO	0	**Reserved**
29:20	RW	0	**Luma(Y) or Red Color Value**
19:10	RW	0	**Chroma(Cb) or Green Color Value**
9:0	RW	0	**Chroma(Cr) or Blue Color Value**

Offset Address: 3BF-3BCh

HQV Segment Residue Pixel Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**HQV Output Field**
30	RO	0	**HQV Current Process Field** 1 to indicate the bottom field.
29	RO	0	**Reserved**
28:4	RW	0	**Segment Residue Pixel Frame Buffer Starting Address** Unit : 16 bytes
3:2	RO	0	**HQV Current Process Destination Buffer ID** 1 to indicate the bottom field.
1:0	RW	0	**Memory Location**

Offset Address: 3C3-3C0h

HQV Sub-picture Frame Buffer Stride and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**MC Flipping Count** ***For MC flip to HQV path:*** Read only ***For SW flip path:*** R/W HQV update read out register data at the beginning of HQV processing a frame.
23:21	RO	0	**Reserved**
20	RW	0	**Sub-picture Blending Option** 0: Blending before scaling 1: Scaling before blending
19	RW	0	**Sub-picture Format** 0: AI44 or IA44 1: AYUV (MSB A(8)-Y(8)-U(8)-V(8) LSB)
18	RW	0	**Inverse Alpha Value in AI44 Mode** 1: Inverse (One's Complement)
17	RW	0	**Alpha, Index Exchange in AI44 Mode** 0: AI44 1: IA44
16	RW	0	**HQV Sub-picture Enable** 1: Enable 0: Disable Only active at HQV source format is YUV.
15:14	RO	0	**Reserved**
13:4	RW	0	**Subpicture Frame Buffer Stride** Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 3C7-3C4h

HQV Sub-picture Frame Buffer Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Sub-picture Frame Buffer Starting Address** (Unit: 16 bytes)
3:2	RO	0	**Reserved**
1:0	RW	0	**Memory Location**

Offset Address: 3CB-3C8h

HQV Sub-picture 4x16 RAM Table Write Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**RAM Table Write Data** V: Bits[31:24] U: Bits[23:16] Y: Bits[15:8]
7:4	RW	0	**RAM Table Read / Write Address** Indicate which entry of palette table will be written or read. Palette table contains 16 entries of palette data. (HQV3C8[7:4] = 0x0000 ~ HQV3C8[7:4] = 0x1111) Need to program HQV3C8[31:8] and HQV3C8[7:4] 16 times to fill the subpicture palette table.
3	RO	0	**Reserved**
2	RW	0	**V Write Enable** 0: Disable 1: Enable
1	RW	0	**U Write Enable** 0: Disable 1: Enable
0	RW	0	**Y Write Enable** 0: Disable 1: Enable

Offset Address: 3CF-3CCh

HQV Background Offset **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26:16	RW	0	**Background Horizontal Offset (-1)** (Unit: Pixel)
15:11	RO	0	**Reserved**
10:0	RW	0	**Background Vertical Offset (-1)** (Unit: Pixel)

Offset Address: 3D3-3D0h

HQV Stream Control and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Video Data Stream Format [3:0]** 0000: RGB32 – (X8R8G8B8) 0001: RGB32 – (X2R10G10B10) 0010: RGB16 – (R5G6B5) 0011: RGB15 – (X1R5G5B5) 0100: YUV444 – (X8Y8U8V8) 0101: V410 – (V10Y10U10X2) 1000: YUV422 – ($V8Y_1 8U8Y_0 8$) 1001: UYVY – ($Y_1 8V8Y_0 8U8$) 1100: YUV420 – (NV12; planar mode) 1101: YUV411 – (NV11; planar mode : $Y_3 8Y_2 8Y_1 8Y_0 8$ $V_0 8U_0 8$ $Y_7 8Y_6 8Y_5 8Y_4 8$ $V_1 8U_1 8$) 1110: P208 – (YUV422 planar mode) Others: Reserved
27	RW	0	**High Quality Video Enable** 0: Disable 1: Enable
26	RW	0	**Buffer Mode** 0: Double destination buffers 1: Triple destination buffers
25:24	RW	00b	**Video Stream Source [1:0]** 00: SW 01: Reserved 10: Capture 0 11: Capture 1
23	RW	0	**Advanced De-interlace Mode Enable** (reference more than one field)
22	RW	0	**Vertical Low Pass Filter Enable** 0: Disable 1: Enable
21	RO	0	**Reserved**

20	RW	0	**Planar Mode Chrominance Source Data Format** 0: Source Chrominance is saved by frame picture 1: Source Chrominance is saved by field picture
19	RW	0	**Inverse Input Field** 0: Non-inversed 1: Inversed
18	RW	0	**Frame To Field** 0: No action 1: Frame base source, extract a field from a frame.
17	RW	0	**Field To Frame** 0: No action 1: Field source, de-interlace to progressive frame.
16	RO	0	**Reserved**
15	RW	0	**Sub-Picture Flip** Software writes 1 to this bit indicates a new sub-picture need to blend. After blending completes, hardware clears it to 0. Software can read this bit to check the status if hardware completes blending.
14:13	RO	0	**Reserved**
12	RO	0	**HQV Flip FIFO Full Status** The FIFO depth defined in Rx3F8 [17:16]
11	RO	0	**Reserved**
10:8	RO	0	**State Machine Status of HQV Flip Module**
7	RW	0	**HQV Interrupt Enable** 0: Disable HQV interrupt. 1: HQV send interrupt signal after done a frame Relative setting: Rx3D0[0].
6	RW	0	**Single Destination Buffer** 0: Not used 1: Single buffer used Rx3D0[26] would be ignored.
5	RW	0	**Field of Software Source Input** 0: Top 1: Bottom
4	RW	0	**Software Source Flip** Software writes 1 to flip a image to HQV. (Rx3D0[25:24] should be 00b) After processing completes, hardware clears it to 0. Software reads this bit to check flip status.
3	RO	0	**HQV Engine Idle State** 0: Busy 1: Idle
2:1	RO	0	**HQV Output Buffer ID** HQV destination buffer ID
0	RW1C	0	**HQV End of Frame Status** 0: Frame not ready 1: HQV has been output an image. (Software writes 1 to clear this bit) After HQV done an image, this bit will be pulled high, and it will be pulled down only whent software writes 1b to it.

Offset Address: 3D7-3D4h

HQV SW Source Buffer – Luma or Packed Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**SW Source Buffer Y or Packed Mode Starting Address** (Unit: 16 bytes)
3:2	RO	0	**Reserved**
1:0	RW	0	**Memory Location**

Offset Address: 3DB-3D8h

HQV SW Source Buffer – Chroma Starting Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**SW Source Buffer U, V Starting Addresses** (Unit: 16 bytes)
3:2	RO	0	**Reserved**
1:0	RW	0	**Memory Location**

Offset Address: 3DF-3DCh

HQV Linear / Tile Address Mode, Color Space Conversion, Gamma, De-blocking Control Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RW	00b	**Linear / Tile Address Mode Control** (Tile address is valid only at source data from MC, 3D0[25:24]=01) 00: Linear 01: 256 bits x 8 tile mode (Addr = SA + (Y[10:3]*PTH*8) + {X[7:1],Y[2:0],X[0]}) 10: 256 bits tile mode (Addr = SA + (Y[10:4]*PTH*16) + {X[6:1],Y[3:0],X[0]}) 11: 512 bits tile mode (Addr = SA + (Y[10:4]*PTH*16) + {X[6:2], Y[3:0],X[1:0]}) Where unit of X is 128-bit; unit of Y is line.
29	RW	0	**HQV Output Data Pack In 32-bits Mode.** 0: 16 bits (RGB565) 1: 32 bits (RGB888) Only valid when the source is YUV and color space conversion is enabled.
28	RW	0	**Color Space Conversion Enable** 0: Disable 1: Enable
27	RW	0	**De-blocking Enable**
26:25	RO	0	**Reserved**
24:20	RW	0	**HQV Output FIFO Threshold for Write Request Control** (Unit: level) HQV output FIFO has 64 levels, once the data in output FIFO touch the threshold (32+3DC.[24:20]), the write request would be triggered.
19:16	RO	0	**Reserved**
15	RW	0	**Constant Alpha of RGB32 Format** 0: Alpha = 00 1: Alpha = FF
14	RW	0	**Enable Synchronization Flipping Field with Interlaced IGA** 0: Disable 1: Enable
13	RW	0	**IGA Field Inverse** 0: Not inversed 1: Inverse
12:11	RO	0	**Reserved**
10:0	RW	0	**Image Size / 1024** Used for pull-down detection.

Offset Address: 3E3-3E0h

HQV Sub-picture Horizontal Scale Control Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	**Horizontal Scale Enable** 0: Disable 1: Enable
30	RO	0	**Reserved**
29:28	RW	0	**Horizontal Scale Function; (2P)** 00: Scale up 01: 1~1/4 10: $1/4^{-}$~$1/8^{+}$ 11: <1/8
27:15	RO	0	**Reserved**
14:0	RW	0	**Horizontal Scale Factor [14:12].[11] (2P)** Scale up : source/destination 1~1/4 : source/(destination + 0.5) $1/4^{-}$~$1/8^{+}$: source/destination <1/8 : destination/source

Offset Address: 3E7-3E4h

HQV Motion Adaptive De-interlace Control & Threshold **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**2:2 Pull Down Sequence Detection Enable** 0: Disable 1: Enable Relative setting: Rx3DC[10:0]
30:28	RO	0	**Reerved**
27	RW	0	**3:2 Pull Down Sequence Detection Enable** 0: Disable 1: Enable Relative setting: Rx3DC[10:0]
26:25	RO	0	**Reerved**
24	RW	0	**2:3:3:2 Pull Down Sequence Detection Enable** 0: Disable 1: Enable Relative setting: Rx3DC[10:0]
23:13	RO	0	**Reserved**
12:8	RW	0	**Motion Detection Enable** 0: Disable 1: Enable
7	RO	0	**2:2 Pull Down Detection Status** 0: Not detected 1: Detected
6	RO	0	**3:2 Pull Down Detection Status** 0: Not detected 1: Detected
5	RO	0	**2:3:3:2 Pull Down Detection Status** 0: Not detected 1: Detected
4:1	RO	0	**Reserved**
0	RW	0	**Edge Detection Enable** 0: Disable 1: Enable

Offset Address: 3EB-3E8h

HQV Sub-picture Vertical Scale Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Vertical Scale Enable** 0: Disable 1: Enable
30:29	RO	0	**Reserved**
28	RW	0	**Vertical Scale Function; (2P)** 0: Scale up 1: Scale down
27:17	RO	0	**Reserved**
16:0	RW	0	**Vertical Scale Factor [14:12].[11] (2P)** Scale up : source/destination Scale down : source/(destination + 0.5)

Offset Address: 3EF-3ECh

HQV Destination Frame Buffer Starting Address 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**HQV Output Data Pack In 32 Bits xRGB2-10-10-10 Format After HQV's Color Space Conversion** 0: Disbale 1: Enable Note: Only one of {Rx3EC[31], Rx3DC[29]} can be set to 1.
30	RW	0	**Enable Output In Tile Mode** 0: Disbale 1:Enable Addr = ST_ADDR[28:4] + Y[10:3]*{PITCH[10:0], 3'b0} + {X[10:1], Y[2:0], X[0]}
29	RO	0	**Reserved**
28:4	RW	0	**Destination Frame Buffer Starting Address 0** Unit: 16 bytes
3:2	RO	0	**Reserved**
1:0	RW	0	**Memory Location**

Offset Address: 3F3-3F0h

HQV Destination Frame Buffer Starting Address 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Destination Frane Buffer Starting Address 1** Unit: 16 bytes
3:2	RO	0	**Reserved**
1:0	RW	0	**Memory Location**

Offset Address: 3F7-3F4h

HQV Destination Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13:4	RW	0	**Destination Frame Buffer Stride** (2P) Unit: 16 bytes
3:0	RO	0	**Reserved**

Offset Address: 3FB-3F8h

HQV Source Frame Buffer Stride **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Load Starting Address Rx3D4[25:4], Rx3D8[25:4] for Advanced De-interlacing** 0: Not used. Hardware keeps the starting address. 1: Load starting address to current field Note: Command sequence Step1: Write Rx3D4, Rx3D8 Step2: Write Rx3F8; new address to PN Step3: Write Rx3D4, Rx3D8 Step4: Write Rx3F8; PN to PC; new address to PN Step5: Write Rx3D4, Rx3D8 Step6: Write Rx3F8; PC to PP; PN to PC; new address to PN
30	RW	0	**SJN Reset** Write 1 to reset static judgment number
29	RW	0	**Pull Down Detection Low-Threshold Value**
28	RW	0	**Pull Down Detection Error Sequence Check One Time** 0: Disbale 1: Enable
27:26	RW	0	**Reserved**
25	RW	0	**Not Check Size** 0: Check size 1: Not check size
24:21	RW	0	**Reserved**
20	RW	0	**Software Flip Queue Enable** 0: Pull Rx3D0[4] low at frame done. 1: Pull Rx3D0[4] low at beginning of processing frame
19	RW	0	**Reserved**
18	RO	0	**Reserved**
17:16	RW	00b	**FIFO Depth of HQV Flip Control Engine** For hardware flip only. (Rx3D0[25:24] ! = 00b) Only supports 2 stages FIFO queuing hardware flipping. 00: Pull "FIFO full status Rx3D0[12]" high, while both two stage are queuing. Drop current processing frame while both two stage are queuing. 01: Pull "FIFO full status Rx3D0[12]" high, while one stage is queuing. Drop current processing frame while both two stage are queuing. 10: Pull "FIFO full status Rx3D0[12]" high, while both two stage are queuing. Never drop current processing frame. 11: Pull "FIFO full status Rx3D0[12]" high, while one stage is queuing. Never drop current processing frame.
15:14	RO	0	**Reserved**
13:4	RW	0	**Source Frame Buffer Stride** (Unit: 16 bytes)
3:0	RO	0	**Reserved**

Offset Address: 3FF-3FCh

HQV Destination Frame Buffer Starting Address 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:4	RW	0	**Destination Frame Buffer Starting Address 2** Unit: 16 bytes
3:2	RO	0	**Reserved**
1:0	RW	0	**Memory Location**

Note: HQV supports 2 Video Streams; therefore, an additional register space is provided to match the above registers definition. Writing a register to this space, it will write to the second HQV, which output to V3 and source is from the second MC engine.

The relationship between the additional register space and the original register space is
(The additional register address) = (The original register address) + 16'h1000.

COMMAND REGULATOR (CR) REGISTERS

This chapter provides detailed Command Regulator register descriptions.

Memory Mapped I/O Register Address Spaces

The following MMIO space is fed into and processed by CR, and then dispatch to related engine.

Memory Range (Note)	Usage
0 ~ 2M-1:	
0x00000000 ~ 0x000001FF	2D Engine Register Space
0x00000200 ~ 0x000003FF	Video Related Engines Register Space 1 (bypass)
0x00000400 ~ 0x000007FF	3D Engine Register Space
0x00000800 ~ 0x00000BFF	Reserved
0x00000C00 ~ 0x00000DFF	Reserved
0x00001200 ~ 0x000013FF	Video Related Engines Register Space 2 (bypass)
0x00002200 ~ 0x000023FF	Extended Video Engines Register Space 1
0x00002E00 ~ 0x00002FFF	DMA(AGP) Register Space 2
0x00003200 ~ 0x000033FF	Extended Video Engines Register Space 2
2M ~ 4M-1	**2D Host BitBLT Space**

Note: These addresses are offset address from PCI Memory Base 1 (MB1).

Definition of I/O Registers

The I/O Register Base Address for 3D/CR is 400h. Offsets Rx1Ch to Rx3Bh are used to set CR registers. These registers are allowed to be set through the starting address Rx1Ch or Rx3Ch with the same HParaType 10h and HparaType 11h. Settings through Rx1Ch would not enable the 3D Engine clock, while settings through Rx3Ch would enable the 3D Engine clock.

For Write Mode

Setting of Command Regulator

<table>
<tr><th>Scope</th><th>Offset</th><th>Description</th><th>Mnemonic</th></tr>
<tr><td rowspan="11">Transmission Setting</td><td>1Ch</td><td>The Beginning of Internal Address for Parameter Programming</td><td>HParaAdr</td></tr>
<tr><td>1Dh</td><td>Offset Setting for Some Special Parameter Types</td><td>HParaOS</td></tr>
<tr><td>1Eh</td><td>Parameter Type

<table><tr><th>HParaType</th><th>Description</th></tr><tr><td>0000 0000b ~ 0000 1111b</td><td>Reserved</td></tr><tr><td>0001 0000b</td><td>Command Decoded in front of Command Regulator</td></tr><tr><td>0001 0001b</td><td>Command for Frame Buffer AutoSwapping and CR’s Miscellaneous Setting</td></tr><tr><td>0001 0010b ~ 1111 1111b</td><td>Reserved</td></tr></table>
For more details for the parameters, please refer to Definition of Parameter section.</td><td>HParaType</td></tr>
<tr><td>1Fh</td><td>Parameter Type Sub-code</td><td>HParaSubType</td></tr>
<tr><td rowspan="5">Transmission Space</td><td>23h-20h</td><td>Parameter 0</td><td>Hpara0</td></tr>
<tr><td>27h-24h</td><td>Parameter 1</td><td>Hpara1</td></tr>
<tr><td>2Bh-28h</td><td>Parameter 2</td><td>Hpara2</td></tr>
<tr><td>…….</td><td>…….</td><td></td></tr>
<tr><td>3Bh-38h</td><td>Parameter 6</td><td>Hpara6</td></tr>
</table>

Setting of 3D Engine

Scope	Offset	Description	Mnemonic
Transmission Setting	3Ch	The Beginning of Internal Address for Parameter Programming	HParaAdr
	3Dh	Offset Setting for Some Special Parameter Types	HParaOS

Scope	Offset	Description	Mnemonic
	3Eh	**Parameter Type**	**HParaType**

HParaType	Description
0000 0000b	**Primitive Vertex Data or Vertex Index**
0000 0001b	**Attribute Other Than Texture**
0000 0010b	**Attribute of Texture n** The setting for texture is divided into 2 kinds of stages: One is defined as Texture Stage with HParaSubType 0nh. n is the number stored in HParaSubType (Rx3Fh): 0000 0000 = Texture 0 0000 0001 = Texture 1 0000 0010 = Texture 2 0000 0011 = Texture 3 0000 0100 = Texture 4 0000 0101 = Texture 5 0000 0110 = Texture 6 0000 0111 = Texture 7 0000 1000 = Texture 8 0000 1001 = Texture 9 0000 1010 = Texture A 0000 1011 = Texture B 0000 1100 = Texture C 0000 1101 = Texture D 0000 1110 = Texture E 0000 1111 = Texture F Another type is Texture Sample Stage with HParaSubType 02nh. n is the number stored in HParaSubType (Rx3Fh): 0010 0000 = Texture sample 0 0010 0001 = Texture sample 1 0010 0010 = Texture sample 2 0010 0011 = Texture sample 3 0010 0100 = Texture sample 4 0010 0101 = Texture sample 5 0010 0110 = Texture sample 6 0010 0111 = Texture sample 7 0010 1000 = Texture sample 8 0010 1001 = Texture sample 9 0010 1010 = Texture sample A 0010 1011 = Texture sample B 0010 1100 = Texture sample C 0010 1101 = Texture sample D 0010 1110 = Texture sample E 0010 1111 = Texture sample F 1111 1110 = General Texture Setting The use of 1111 1111 is prohibited. Others = Reserved
0000 0011b	**Palette** HParaSubType (Rx3Fh) shows the palette type: 0000 0000 = Texture Palette 0 (Only for AI44 and IA44 Video Texture) 0000 1xxx = Reserved 0001 0000 = Base Address Offset of Each Texture 0001 0001 = Texture 4X4 Filter Coefficient Table 0001 0011 = Resreved 0001 0100 = Stipple Palette 0001 0101 = De-Gamma Table for Reading Texture 0001 0110 = Reserved 0001 0111 = Gamma-de-Gamma Table for Writing Destination Color 0010 0000 = Pixel Shader ALU Instruction 0010 0001 = Pixel Shader TAU Instruction 0010 0010 = Pixel Shader Constant Register
0000 0100b	Vertex and Primitive Setting
0000 1111b ~ 0000 0101b	Reserved
0001 0000b	Command Decoded in front of Command Regulator
0001 0001b	Command for Frame Buffer AutoSwapping and CR's Miscellaneous Setting
1111 1101b ~ 0001 0010b	Reserved

For details of the parameters, please refer to Definition of Parameter section.

Scope	Offset	Description	Mnemonic
	3Fh	Parameter Type Sub-code	HParaSubType
Transmission Space	43h-40h	Parameter 0	Hpara0
	47h-44h	Parameter 1	Hpara1
	4Bh-48h	Parameter 2	Hpara2
	…….	…….	
	1F7h-1F4h	Parameter 109	Hpara6D
	1FBh-1F8h	Parameter 110	Hpara6E
	1FFh-1FCh	Parameter 111	Hpara6F
	……	…….	
	2FFh-2FCh	Parameter 175	HparaAF

HParaType 00h: Primitive Vertex Data or Vertex Index

HParaTye 00h is used for Primitive Vertex Data (for Vertex Command Mode) or Vertex Index (for Vertex Buffer Index Mode). There is no sub-address in this ParaType. The steps to fire 3D Engine are as follows:

Step 1: Set the correct value to all the related 3D globe registers through ParaType 01h, 02h, 03h, 04h, 10h, 11h and FEh.

Step 2: Sent Vertex Data or Vertex Index (according to HVertexMode) through ParaType 00h. CR would configure the vertex (according HVFVLEN and HnFVF) and generate fire signal automatically whenever all the vertices of a primitive are ready (according to HVCycle, H2and1VT and HPMType). CR would also generate the PLEND (Primitive List End) signal whenever the entire listed vertexes are finished (according to HVTXnum), or receive a “Stop Command”.

For next primitive list, repeat the two steps above.

HParaType 10h: Commands for Command Regulator

Sub-Address (Bits [31:24]): 00-7Ch

HParaType = 10h, Sub-Address = 00h
PCI Command Setting

Bits [23:0]	Attribute	Default	Description
23:9	WO	xxh	**Reserved**
8	WO	xxh	**Enable of Packaging the PCI Command in front of CR** 0: Disable 1: Enable
7:0	WO	xxh	**Number of ECLK Cycle for PCI Command Packaging Time Out**

HParaType = 10h, Sub-Address = 02h
Read Register Back Command Setting

Bits [23:0]	Attribute	Default	Description
23:21	WO	xxh	**Reserved**
20:12	WO	xxh	**Reading-Back Register to Debug Port** Address [10:2] for Reading-Back Register to Debug port; will be multiplexed with HI2CR_RADR[8:2].
11	WO	xxh	**Enable Reading-Back Register to Debug Port** 0: Disable 1: Enable
10:8	WO	xxh	**Reserved**
7:0	WO	xxh	**ID for Reading-Back Register** 0000 0000: Reading the RB registers from CR 0000 0001: Reading the RB registers from FE (including VP, CL and SE) 0000 0010: Reading the RB registers from PE (including RZ and CZ) 0000 0011: Reading the RB registers from RC 0000 0100: Reading the RB registers from PS 0000 0101: Reading the RB registers from XE 0000 0110: Reading the RB registers from BE (including GEMI) 0000 0111: Reading the RB registers for Performance Profile Counters Others: Reserved

HParaType = 10h, Sub-Address = 03h
Address for Reading-Back Register

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Address for Reading-Back Register** This address setting will read back E32CR_WBREG[127:0]. Bits[23:16]: HParaSubType Bits[15:8]: HParaType Bits[7: 0]: Sub-Address

HParaType = 10h, Sub-Address = 04h
Interrupt State Buffer Control 1

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Lower 24-bit of Interrupt State Buffer Base Address <HIRSBBas Lower Bits>** It is A[23:0] with 128-bit alignment, while A[3:0] is useless.
3:2	WO	xxh	**Reserved**
1:0	WO	xxh	**Interrupt State Buffer Location** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S..M.) 11: Reserved

HParaType = 10h, Sub-Address = 05h
Interrupt State Buffer Control 2

Bits [23:0]	Attribute	Default	Description
23:9	WO	xxh	**Reserved**
8	WO	xxh	**Store 3D Engine's Register Setting in State Buffer <HIRSB4E3>** 0: Disable. It is not necessary to store 3D's register setting (default). 1: Enable. Store 3D's register setting into the State Buffer.
7:0	WO	xxh	**Higher 8-bit of Interrupt State Buffer Base Address <HIRSBBas Higher Byte>** It is A[31:24].

HParaType = 10h, Sub-Address = 06h
Left Vertex Data Threshold

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Threshold Value of the Left Vertex Data within One DIP in CR <HIRFthStop>** When the left vertex data in CR are more than HIRFthStop and HIRStop (see Sub-Address 07: bit [0] below) is set, CR would stop 3D immediately. Otherwise, CR would stop 3D at the end of DIP. Unit: Dword.

HParaType = 10h, Sub-Address = 07h
Interrupt Command

Bits [23:0]	Attribute	Default	Description
23:2	WO	xxh	**Reserved**
1	WO	xxh	**Interrupt Request for Pause <HIRPause>** Force CR into "Pause State" until this bit is cleared. When in "Pause State", CR just holds and not sends any command or data to the Video engine, 2D engine or 3D engine
0	WO	xxh	**Interrupt Request for Stop <HIRStop>** When this register is set, CR would interrupt the GPU and wait new Command triggered.

Note: HIRPause and HIRStop can not be set at the same time.

HParaType = 10h, Sub-Address = 10h
VMR Control

Bits [23:0]	Attribute	Default	Description
23:1	WO	xxh	**Reserved**
0	WO	xxh	**VMR ID Buffer Status Reset**

HParaType = 10h, Sub-Address = 60h
AGP Command Setting 1

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Lower 3 Bytes of AGP Buffer Start Address** ***<HAGPBst Low Bytes>*** It is A[23:0] with 128-bit alignment, where A[3:0] is useless.
3:2	WO	xxh	**Reserved**
1:0	WO	xxh	**AGP Buffer Location** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S.M.) 11: Reserved

HParaType = 10h, Sub-Address = 61h
AGP Command Setting 2

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Higher Byte of AGP Buffer Start Address** ***<HAGPBst High Byte>*** It is A[31:24].

HParaType = 10h, Sub-Address = 62h
AGP Command Setting 3

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 bytes of AGP Buffer End Address** It is A[23:0] with128-bit alignment, where A[3:0] is useless.

HParaType = 10h, Sub-Address = 63h
AGP Command Setting 4

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Higher Byte of AGP Buffer End Address** It is A[31:24].

HParaType = 10h, Sub-Address = 64h
AGP Command Setting 5

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of AGP Buffer Pause Address** It is A[31:0] with 128-bit alignment, where A[3:0] is useless.

HParaType = 10h, Sub-Address = 65h
AGP Command Setting 6

Bits [23:0]	Attribute	Default	Description
23:10	WO	xxh	**Reserved**
9:8	WO	xxh	**AGP Buffer Pause Address ID** 00: HAGPBp (see bits 7:0) is the Pause Address of AGP Command Fetch. If AGP Command Fetcher wants to continuously fetch AGP Command again, it will start on the next address after HAGPBp. 01: HAGPBp is the End Address of a portion of AGP Command Block. When AGP Command Fetcher reaches this address, it will start to fetch next AGP Command addressed by HAGPBst without waiting. 10: HAGPBp is the AGP Command Stop Address. Whenever, AGP Command Fetcher reach this address, the AGP Command Fetching is finished. If we want to do another AGP Command Fetching, we have to set HAGPBTrig as 1. 11: Reserved
7:0	WO	xxh	**Higher Byte of AGP Buffer Pause Address** ***<HAGPBp High Byte>*** It is A[31:24].

HParaType = 10h, Sub-Address = 66h
AGP Command Setting 7

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 bytes of AGP Buffer Jump Address** It is A[23:0] with 128-bit alignment, where A[3:0] is useless.

HParaType = 10h, Sub-Address = 67h
AGP Command Setting 8

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Higher Byte of AGP Buffer Jump Address** It is A[31:24].

HParaType = 10h, Sub-Address = 68h
AGP Command Setting 9

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**Threshold Value of Read AGP Command** Default value is 8.
15:5	WO	xxh	**Reserved**
4	WO	xxh	**Clear Fence Queue**
3	WO	xxh	**Clear AGP Cycle**
2	WO	xxh	**Trigger Restore AGP Command Cycle** Hardware will only restore AGP command.
1	WO	xxh	**Trigger Restore 3D Register Cycle**
0	WO	xxh	**Trigger AGP Cycle** The Trig signal of AGP command.

HParaType = 10h, Sub-Address = 69h
Branch Command Setting

Bit [23:0]	Attribute	Default	Description
23:1	WO	xxh	**Reserved**
0	WO	xxh	**Default is On** 0: Disable AGP Branch. Branched AGP Header (FE8x) is forbidden. 1: Enable AGP Branch

HParaType = 10h, Sub-Address 6Ch
Restore Command Setting 1

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Lower 3 Bytes of Interrupt State Buffer Restore Start Address** It is A[23:4] with 128-bit alignment.
3:2	WO	xxh	**Reserved**
1:0	WO	xxh	**Interrupt State Buffer Restore Location** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S.M.) 11: Reserved

HParaType = 10h, Sub-Address 6Dh
Restore Command Setting 2

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Higher Byte of Interrupt State Buffer Restore Start Address** It is A[31:24] with 128-bit alignment.

HParaType = 10h, Sub-Address 6Eh
Restore Command Setting 3

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Lower 3 bytes of AGP Buffer Restore Start Address** It is A[23:0] with128-bit alignment where A[3:0] is useless.
3:0	WO	xxh	**Reserved**

HParaType = 10h, Sub-Address 6Fh
Restore Command Setting 4

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Higher Byte of AGP Buffer Restore Start Address** It is A[31:24] with 128-bit alignment.

HParaType = 10h, Sub-Address 70h
CMDQ Setting 1

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Lower 3 Bytes of Command Queue Start Address** It is A[23:0] with 128-bit alignment, where A[3:0] is useless.
3:2	WO	xxh	**Reserved**
1:0	WO	xxh	**Command Queue Location** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S.M.) 11: Reserved

HParaType = 10h, Sub-Address 71h
CMDQ Setting 2

Bit [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Command Queue End Address** It is A[23:0] with 128-bit alignment, where A[3:0] is useless.

HParaType = 10h, Sub-Address = 72h
CMDQ Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:8	WO	xxh	**Higher Byte of Command Queue End Address** 128-bit alignment.
7:0	WO	xxh	**Higher Byte of Command Queue Start Address** 128-bit alignment.

HParaType = 10h, Sub-Address = 73h
CMDQ Setting 4

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Length of Command Queue** The minimum value is 24'h800 in unit of 128 bits.

HParaType = 10h, Sub-Address = 74h
CMDQ Setting 5

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**Threshold Value of Write Command Queue FIFO**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**Threshold Value of Read Command Queue FIFO**
7:4	WO	xxh	**Control Setting for CMDQ Read Request Interrupting Write Request** 0000: Never interrupt. CMDQ handles Read request only after CMDQ Write finished. 0001: Interrupt CMDQ Write request whenever CMDQ Read request arrived 1000: Interrupt whenever 16 CMDQ Write requests accepted 1001: Interrupt whenever 32 CMDQ Write requests accepted 1100: Interrupt whenever 32 CMDQ Write request cycles completed 1101: Interrupt whenever 64 CMDQ Write request cycles completed Others: Reserved
3	WO	xxh	**Reserved**
2	WO	xxh	**CMDQ Is Used for Command from AGP or PCI** 0: Store Command from PCI 1: Store Command from AGP
1	WO	xxh	**Enable Request Length for CMDQ of Command Regulator** 0: Disable. Always use 1 128-bit command in one request. 1: Enable. Allow having 1, 2, or 4 128-bit commands within one request.
0	WO	xxh	**Enable Command Queue** 0: Disable 1: Enable

HParaType = 10h, Sub-Address = 78h
CMDQ Setting 6

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Lower 3 Bytes of Command Queue Start Address for 2D/3D Command** It is A[23:0] where A[3:0] is useless.
3:2	WO	xxh	**Reserved**
1:0	WO	xxh	**Command Queue Location for 2D/3D Command** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S.M.) 11: Reserved

HParaType = 10h, Sub-Address = 79h
CMDQ Setting 7

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Command Queue End Address for 2D/3D Command** It is A[23:0] where A[3:0] is useless.

HParaType = 10h, Sub-Address = 7Ah
CMDQ Setting 8

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:8	WO	xxh	**Higher Byte of Command Queue End Address for 2D/3D Command**
7:0	WO	xxh	**Higher Byte of Command Queue Start Address for 2D/3D Command.**

HParaType = 10h, Sub-Address = 7Bh
CMDQ Setting 9

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Length of Command Queue for 2D/3D Command** The minimum value is 24'h800 in unit of 128 bits.

HParaType = 10h, Sub-Address = 7Ch
CMDQ Setting 10

Bits [23:0]	Attribute	Default	Description
23:14	WO	xxh	**Reserved**
13:8	WO	xxh	**Threshold Value of Read Command Queue FIFO for 2D/3D Command**
7:4	WO	xxh	**Control Setting for CMDQ Read Request Interrupting Write Request for 2D/3D Command** 0000: Never interrupt. CMDQ handles Read request only after CMDQ Write finished. 0001: Interrupt CMDQ Write request whenever CMDQ Read request arrived. 1000: Interrupt whenever 16 CMDQ Write requests accepted 1001: Interrupt whenever 32 CMDQ Write requests accepted 1100: Interrupt whenever 32 CMDQ Write request cycles completed 1101: Interrupt whenever 64 CMDQ Write request cycles completed Others: Reserved
3	WO	xxh	**Reserved**
2	WO	xxh	**CMDQ Is Used for Command from AGP or PCI for 2D/3D Command** 0: Store command from PCI 1: Store command from AGP
1	WO	xxh	**Enable Request Length for CMDQ of Command Regulator for 2D/3D Command** 0: Disable. Always use 1 128-bit command in one request. 1: Enable. Allow having 1, 2, or 4 128-bit commands within one request.
0	WO	xxh	**Enable Command Queue for 2D/3D Command** 0: Disable 1: Enable

HParaType 11h: Commands for Frame Buffer Swapping and CR's Miscellaneous Setting

Sub-Address (Bits [31:24]): 00-ABh

HParaType = 11h, Sub-Address = 00h
CR's Miscellaneous Setting

Bits [23:0]	Attribute	Default	Description
23:17	WO	xxh	**Reserved**
16	WO	xxh	**Enable 2D/3D Request Lock Control** 0: Disable. When one of 3D/2D engines is busy, CR will not send commands to another engine. 1: Enable. When one of 3D/2D engines is busy, CR sent commands to another engine but another engine does not access memory. Only one of the 2D and 3D engine is working in one time. However, E3FIRE can be sent to 3D engine when 2D engine is busy. Also, E2FIRE can be sent to 2D engine when 3D engine is busy. In the first case, Command Regulator will set CRLock3D before issuing E3FIRE and reset CRLock3D after 3D engine is idle. Similarly, CRLock2D is working in the same way.
15:11	WO	xxh	**Reserved**
10:8	WO	010b	**The Depth N of FIFO 1 in CR** 000: n = 16 001: n = 24 010: n = 32 (default) 011: n = 48 100: n = 64 Others: Reserved
7:5	WO	010b	**The Depth N of FIFO 2 in CR** 000: n = 16 001: n = 24 010: n = 32 (default) 011: n = 48 100: n = 64 Others: Reserved
4:2	WO	010b	**The Depth N of FIFO 3 in CR** 000: n = 16 001: n = 24 010: n = 32 (default) 011: n = 48 100: n = 64 Others: Reserved
1	WO	xxh	**Reserved**
0	WO	xxh	**Enable to Treat Followed CMDs as "Critical"(Not Breakable)** 0: The Command Queue can be broken by an "Interrupt command" 1: The Command Queue can not be broken. The "STOP" procedure is executed only after this bit is cleared.

HParaType = 11h, Sub-Address = 04h
Fence Command 1

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	**Reserved**
19:0	WO	xxh	**Higher Bits of Fence Command Base Address** If HFCMode[2]=1 (see Sub-Address:07 [19:16] below), it is the higher 20-bit Fence Command Base address for PCI Master Write (A[43:24]). If HFCMode[2]=0, it is the higher 12-bit Fence Type (FenceType[31:20]).

HParaType = 11h, Sub-Address = 05h
Fence Command 2

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Lower Bits of Fence Command Base Address** If HFCMode[2]=1, it is the lower 24-bit Fence Command Base address for PCI Master Write (A[23:4]). If HFCMode[2]=0, it is the lower 24-bit Fence Type (FenceType [19:0]).
3:0	WO	xxh	**Reserved**

HParaType = 11h, Sub-Address = 06h
Fence Command 3

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 24-bit Fence Command ID <HFCID – Lower Bytes>**

HParaType = 11h, Sub-Address = 07h
Fence Command 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22	WO	xxh	**Fence Command Queue Full Skip** Active at First CR Command (for HFCMode with Writes Fence Queue &generate interrupt signal) 0: CR command (41Ch/420h) is paused until Fence Command Queue has space (default) 1: CR keeps running, overwrite Fence_ID to current write point in Fence queue
21	WO	xxh	**Fence Command Interrupt Wait** For HFCMode with Writes Fence Queue & generate interrupt signal 0: CR keeps running when CR_INT active, and write Fence_ID to Fence queue (default) 1: CR is paused until CR_INT is cleared by Fence queue empty (not 204[5]).
20	WO	xxh	**Fence Command Trigger**
19:16	WO	xxh	**Fence Command Mode <HFCMode>** 0000: Just record the HFCID (Sub-Address 07[15:8], 06[23:0]) 0001: Record the HFCID when all engines are idle 0010: Just write Fence Queue, generate interrupt signal and record the HFCID 0011: Write Fence Queue, generate interrupt signal and record the HFCID when all engines are idle 0100: Just write out HFCID to System Memory and record the HFCID 0101: Write out HFCID to System Memory and record the HFCID when all engines are idle 0110: Just write out HFCID to System Memory, write Fence Queue, generate interrupt signal and record the HFCID 0111: Write out HFCID to System Memory, write Fence Queue, generate interrupt signal and record the HFCID when all engines are idle Others: Reserved
15:8	WO	xxh	**Higher 8-bit Fence Command ID <HFCID – Higher Byte>**
7:0	WO	xxh	**Reserved**

HParaType = 11h, Sub-Address = 08h
Save Command 1

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Lower 24-bit of Save Buffer Start Base Address <HSvBSt Lower Bits>** It is A[23:0] with128-bit alignment, where A[3:0] is useless.
3:2	WO	xxh	**Reserved**
1:0	WO	xxh	**Save Buffer Location** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S.M.) 11: Reserved

HParaType = 11h, Sub-Address = 09h
Save Command 2

Bits [23:0]	Attribute	Default	Description
23:9	WO	xxh	**Reserved**
8	WO	xxh	**Store 3D Engine's Register Write Enable <HSvWTEn>** 0: Disable. It is not necessary to store 3D's register. **(default)** 1: Enable. Store 3D's register.
7:0	WO	xxh	**Higher 8-bit of Save Buffer Start Base Address <HSvBSt Higher Byte>** It is A[31:24].

HParaType = 11h, Sub-Address = 0Bh
Save Command 3

Bits [23:0]	Attribute	Default	Description
23:1	WO	xxh	**Reserved**
0	WO	xxh	**Save Trig for Save 3D Write Back Registers** When this register is set, CR saves 3D write back registers and then keep running.

Note:
Priority HIRSB4E3 > HSvWTEn, if HIRSB4E3=1, all 3D save register will save to HIRSBBas not HSvBSt.
HIRSB4E3: HparaType 10h, Sub-Address 05h, bit [8]
HSvWTEn: HparaType 11h, Sub-Address 05h, bit [8]
HIRSBBas: HparaType 10h, Sub-Address 05h, bits [7:0] and HparaType 10h, Sub-Address 04h, bits [23:4]
HIRSBBas: HparaType 11h, Sub-Address 09h, bits [7:0] and HparaType 11h, Sub-Address 08h, bits [23:4]

HParaType = 11h, Sub-Address = 10h
Frame Buffer Automatic Swapping 1

Bits [23:0]	Attribute	Default	Description
23:3	WO	xxh	**Lower 3 Bytes of Display Frame Buffer Base Address of IGA1**
2	WO	xxh	**Reserved**
1:0	WO	xxh	**Display Frame Buffer Location** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S.M.) 11: Reserved

HParaType = 11h, Sub-Address = 11h
Frame Buffer Automatic Swapping 2

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Frame Flip Count of IGA1**
7:0	WO	xxh	**Higher Byte of Display Frame Buffer Base Address of IGA1**

HParaType = 11h, Sub-Address = 12h
Frame Buffer Automatic Swapping 3

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Reserved**
3	WO	xxh	**Enable Frame Buffer Automatic Swapping for IGA1**
2	WO	0	**Skip to Wait Blank When Automatic Swapping for IGA1** (default=0)
1:0	WO	xxh	**Reserved**

HParaType = 11h, Sub-Address = 13-17h: Reserved (for Frame Buffer Automatic Swapping)

HParaType = 11h, Sub-Address = 18h
Frame Buffer Automatic Swapping 4

Bits [23:0]	Attribute	Default	Description
23:3	WO	xxh	**Lower 3 Bytes of Display Frame Buffer Base Address of IGA2**
2	WO	xxh	**Reserved**
1:0	WO	xxh	**Display Frame Buffer Location of IGA2** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S.M.) 11: Reserved

HParaType = 11h, Sub-Address = 19h
Frame Buffer Automatic Swapping 5

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Frame Flip Count of IGA2**
7:0	WO	xxh	**Higher Byte of Display Frame Buffer Base Address of IGA2**

HParaType = 11h, Sub-Address = 1Ah
Frame Buffer Automatic Swapping 6

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Reserved**
3	WO	xxh	**Enable Frame Buffer Automatic Swapping for IGA2**
2	WO	0	**Skip to Wait Blank When Automatic Swapping for IGA2.** (default=0)
1:0	WO	xxh	**Reserved**

HParaType = 11h, Sub-Address = 1B-2Fh: Reserved (for Frame Buffer Automatic Swapping)

HParaType = 11h, Sub-Address = 30h
Frame Buffer Automatic Swapping 7

Bits [23:0]	Attribute	Default	Description
23:3	WO	xxh	**Lower 3 Bytes of Display Frame Buffer Base Address of IGA Duo-view Control**
2	WO	xxh	**Reserved**
1:0	WO	xxh	**Display Frame Buffer location of IGA** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S.M.) 11: Reserved

HParaType = 11h, Sub-Address = 31h
Frame Buffer Automatic Swapping 8

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Frame Flip Count of IGA**
7:0	WO	xxh	**Higher Byte of Display Frame Buffer Base Address of IGA**

HParaType = 11h, Sub-Address = 32h
Frame Buffer Automatic Swapping 9

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Reserved**
3	WO	xxh	**Enable Frame Buffer Automatic Swapping for IGA**
2	WO	0	**Skip to Wait blank When Automatic Swapping for IGA** (default=0)
1:0	WO	xxh	**Reserved**

HParaType = 11h, Sub-Address = 33-34h: Reserved (for Frame Buffer Automatic Swapping)

HParaType = 11h, Sub-Address = 68h
First Branch Command Setting 1

HparaType 11, Sub-Address 68-6Bh are active only in "AGP format" command.

Bits [23:0]	Attribute	Default	Description
23:1	WO	xxh	**Reserved**
0	WO	xxh	**Branch Type** 0: Branch for Normal (default). Branch commands are independent on previous command. Insert Branch commands in CR command queue. 1: Branch for Restore. Wait the completion of all previous commands before Branch header (FE8x), and then activate Branch request.

HParaType = 11h, Sub-Address = 69h
First Branch Command Setting 2

Bits [23:0]	Attribute	Default	Description
23:1	WO	xxh	**Lower 3 Bytes of Branch Buffer Start Address** It is A[23:1] where A[0] is useless. (Unit: Word, 16-bit alignment) Note to Driver and hardware: 1. The branch buffer address is modified to be alignment with 16 bits because of this address points to the vertex index in vertex buffer. 2. Branch for 3D vertex index in vertex buffer (16bits aligned) is only from Header3 (Do not set in Header 2). 3. DWcount of header = valid vertex data DWcount + invalid vertex data DWcount before valid vertex data (ex: HAGPBranchL[3:1]=2 , i.e. invalid vertex data(16-bit alignment) DWcount before valid vertex data = 1)
0	WO	xxh	**Reserved**

HParaType = 11h, Sub-Address = 6Ah
First Branch Command Setting 3

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Branch Buffer Location** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S.M.) 11: Reserved
21:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Higher Byte of Branch Buffer Start Address** It is A[31:24].

Note: For Sub-Address 6Ah, branch command trigger is hidden in AGP header (FE8x). "NESTED" branch buffer is forbidden.

HParaType = 11h, Sub-Address = 6Bh
First Branch Command Setting 4

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Size of Branch Buffer** In unit of 16 bytes (128 bits).

HParaType = 11h, Sub-Address 6Ch: Reserved (for Second Branch Command Setting)

HParaType = 11h, Sub-Address 6Dh
Second Branch Command Setting 1

T11A6C-6F (HparaType 11, Sub-Address 6C-6Fh) are active only in "AGP format" command.

Bits [23:0]	Attribute	Default	Description
23:1	WO	xxh	**Lower 3 Bytes of Branch Buffer Start Address** It is A[23:1] where A[0] is useless. (Unit: Word, 16-bit alignment) Note to Driver and hardware: 1. The branch buffer address is modified to be alignment with 16 bits because of this address points to the vertex index in vertex buffer. 2. Branch for 3D vertex index in vertex buffer (16bits aligned) is only from Header3 (Do not set in Header 2).
0	WO	xxh	**Reserved**

HParaType = 11h, Sub-Address 6Eh
Second Branch Command Setting 2

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Branch Buffer Location** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: System Memory (S.M.) 11: Reserved
21:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Higher Byte of Branch Buffer Start Address** It is A[31:24].

Note: For Sub-Address 6Eh, branch command trigger is hidden in AGP header (FE8x). "NESTED" branch buffer is forbidden.

HParaType = 11h, Sub-Address 6Fh
Second Branch Command Setting 3

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Size of Branch Buffer** In unit of 16 bytes (128 bits).

HParaType = 11h, Sub-Address AAh
SW Inspection (R/W) 1

Bits [23:0]	Attribute	Default	Description
23:0	RW	xxh	**Software Event TAG for Software Inspection**

HParaType = 11h, Sub-Address ABh
SW Inspection (R/W) 2

Bits [23:0]	Attribute	Default	Description
23:0	RW	xxh	**Software Event TAG for Software Inspection**

CR Registers in 2D Register Space (60-6Ch)

For detailed 2D register descriptions, please refer to 2D chapter.

Offset Address: 60h
3D / 2D ID Control

Bit	Attribute	Default	Description
31	WO	xxh	**Reserved**
30	WO	xxh	**3D / 2D Command Force Start (Software Must Fill Zero)**
29:28	WO	xxh	**3D / 2D Command Status** 00: 3D / 2D command start 01: 3D / 2D command end 10: 3D / 2D command end and wait 3D idle 11: 3D / 2D command end and wait 2D idle
27	WO	xxh	**3D / 2D Command Stream Kinds**
26:24	WO	xxh	**3D / 2D Working Buffer Number**
23:16	WO	xxh	**Reserved for Hardware Use**
15:0	WO	xxh	**3D / 2D Working ID**

Offset Address: 6Ch
3D / 2D Wait Control

Bit	Attribute	Default	Description
31	WO	xxh	**Wait HQV0 Idle**
30	WO	xxh	**Wait HQV1 Idle**
29	WO	xxh	**Wait MC Idle**
28:24	WO	xxh	**Wait Idle Count**
23	WO	xxh	**Wait 3D Idle – for 3D / 2D Command Path**
22	WO	xxh	**Wait 2D Idle – for 3D / 2D Command Path**
21	WO	xxh	**Wait DMA Channel 3 Idle**
20	WO	xxh	**Wait DMA Channel 2 Idle**
19	WO	xxh	**Wait DMA Channel 1 Idle**
18	WO	xxh	**Wait DMA Channel 0 Idle**
17	WO	xxh	**Wait LCD DN Idle**
16:14	WO	xxh	**Reserved**
13	WO	xxh	**Command Wait Later IGA VBLK Interval to Start to Work**
12	WO	xxh	**Command Wait Former IGA VBLK Interval to Start to Work**
11	WO	xxh	**Command Wait Later IGA VBLK End Pulse to Start to Work**
10	WO	xxh	**Command Wait Former IGA VBLK End Pulse to Start to Work**
9	WO	xxh	**Command Wait Later IGA VBLK Start Pulse to Start to Work**
8	WO	xxh	**Command Wait Former IGA VBLK Start Pulse to Start to Work**
7:6	WO	xxh	**Reserved**
5	WO	xxh	**Command Wait IGA2 VBLK Interval to Start to Work**
4	WO	xxh	**Command Wait IGA1 VBLK Interval to Start to Work**
3	WO	xxh	**Command Wait IGA2 VBLK End Pulse to Start to Work**
2	WO	xxh	**Command Wait IGA1 VBLK End Pulse to Start to Work**
1	WO	xxh	**Command Wait IGA2 VBLK Start Pulse to Start to Work**
0	WO	xxh	**Command Wait IGA1 VBLK Start Pulse to Start to Work**

CR Registers in Video Control Register Space (3260-326Ch)

For detailed video register descriptions, please refer to Video Overlay Engine chapter.

Offset Address: 3260h
DVD / Video ID Control

Bit	Attribute	Default	Description
31	WO	xxh	**Reserved**
30	WO	xxh	**DVD / Video Command Force Start (Software Must Fill Zero)**
29:28	WO	xxh	**DVD / Video Command Status** 00: DVD / Video command start 01: DVD / Video command end 10: DVD / Video command end and wait DVD idle 11: DVD / Video command end and wait Video idle
27	WO	xxh	**DVD / Video Command Stream Kinds**
26:24	WO	xxh	**DVD / Video Working Buffer Number**
23:16	WO	xxh	**Reserved for Hardware Use**
15:0	WO	xxh	**DVD / Video Working ID**

Offset Address: 326Ch
DVD / Video Wait Control

Bit	Attribute	Default	Description
31	WO	xxh	**Wait 3D Idle – for Video Command Path**
30	WO	xxh	**Wait 2D Idle – for Video Command Path**
29:25	WO	xxh	**Wait Idle Count**
24:22	WO	xxh	**Reserved**
21	WO	xxh	**Wait HQV1 Starting Address Load**
20	WO	xxh	**Wait HQV1 Fire Bit**
19	WO	xxh	**Wait HQV1 HW Flip FIFO Full**
18	WO	xxh	**Wait HQV1 Subpicture / Updateoverlay Flip**
17	WO	xxh	**Wait HQV1 SW Flip**
16	WO	xxh	**Wait HQV1 Finish a Frame**
15	WO	xxh	**Wait DMA Channel 3 Idle**
14	WO	xxh	**Wait DMA Channel 2 Idle**
13	WO	xxh	**Wait DMA Channel 1 Idle**
12	WO	xxh	**Wait DMA Channel 0 Idle**
11:6	WO	xxh	**Reserved**
5	WO	xxh	**Wait HQV0 Starting Address Load**
4	WO	xxh	**Wait HQV0 Fire Bit**
3	WO	xxh	**Wait HQV0 Hardware Flip FIFO Full**
2	WO	xxh	**Wait HQV0 Subpicture / Updateoverlay Flip**
1	WO	xxh	**Wait HQV0 Software Flip**
0	WO	xxh	**Wait HQV0 Finish a Frame**

3D REGISTERS

This chapter provides detailed 3D register descriptions. Please also refer to Chapter “Commnad Regulator”, Section “Definition of I/O Register” for basic introduction on 3D/CR operations and 3D/CR register summary table.

HParaType 00h: Primitive Vertex Data or Vertex Index

HParaTye 00h is used for Primitive Vertex Data (for Vertex Command Mode) or Vertex Index (for Vertex Buffer Index Mode). There is no sub-address in this ParaType. The steps of how to fire 3D Engine are as follows:

Step 1: Set the correct value to all the related 3D globe registers through ParaType 01h, 02h, 03h, 04h, 10h, 11h and FEh.

Step 2: Sent Vertex Data or Vertex Index (according to HVertexMode) through ParaType 00h. CR would configure the vertex (according HVFVLEN and HnFVF) and generate fire signal automatically whenever all the vertices of a primitive are ready (according to HVCycle, H2and1VT and HPMType). CR would also generate the PLEND (Primitive List End) signal whenever the entire listed vertexes are finished (according to HVTXnum), or receive a “Stop Command”.

For next primitive list, repeat the two steps above.

HParaType 01h: Attribute Other Than Texture

Sub-Address (Bits [31:24]): 00-AAh

HParaType = 01h, Sub-Address = 00-0Fh
Enable Setting 1

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22	WO	xxh	**Inverse Enable (Disable) BE's 32-byte (Adjacent 128-bit) Packing** 0: Enable 1: Disable
21	WO	xxh	**Inverse Enable (Disable) BE's Smart Packing** 0: Enable 1: Disable
20	WO	xxh	**Enable Alpha Test Result of RT0 for All Render Targets (RTn)** 0: The success or failure of alpha test for RTn depends on its own alpha test result and HenATMRTn, where n = 0 .. 3. 1: Execution of the alpha test for RT0 and all render targets depend on the result to be killed or not. HenATMRT0, HenATMRT1, HenATMRT2 & HenATMRT3 are ignored
19	WO	xxh	**Enable Alpha Test for Render Target 3 <*HenATMRT3*>** 0: Disable 1: Enable
18	WO	xxh	**Enable Alpha Test for Render Target 2 <*HenATMRT2*>** 0: Disable 1: Enable
17	WO	xxh	**Enable Alpha Test for Render Target 1 <*HenATMRT1*>** 0: Disable 1: Enable
16	WO	xxh	**Enable Alpha Test for Render Target 0 <*HenATMRT0*>** 0: Disable 1: Enable
15	WO	xxh	**Enable Specula Color for Render Target 3** 0: Disable 1: Enable
14	WO	xxh	**Enable Specula Color for Render Target 2** 0: Disable 1: Enable
13	WO	xxh	**Enable Specula Color for Render Target 1** 0: Disable 1: Enable
12	WO	xxh	**Enable Specula Color for Render Target 0** 0: Disable 1: Enable
11	WO	xxh	**Enable Fog for Render Target 3** 0: Disable 1: Enable
10	WO	xxh	**Enable Fog for Render Target 2** 0: Disable 1: Enable
9	WO	xxh	**Enable Fog for Render Target 1** 0: Disable 1: Enable
8	WO	xxh	**Enable Fog for Render Target 0** 0: Disable 1: Enable
7	WO	xxh	**Enable Alpha Blending for Render Target 3** 0: Disable 1: Enable
6	WO	xxh	**Enable Alpha Blending for Render Target 2** 0: Disable 1: Enable
5	WO	xxh	**Enable Alpha Blending for Render Target 1** 0: Disable 1: Enable
4	WO	xxh	**Enable Alpha Blending for Render Target 0** 0: Disable 1: Enable
3	WO	xxh	**Enable Dither for Render Target 3** 0: Disable 1: Enable
2	WO	xxh	**Enable Dither for Render Target 2** 0: Disable 1: Enable
1	WO	xxh	**Enable Dither for Render Target 1** 0: Disable 1: Enable
0	WO	xxh	**Enable Dither for Render Target 0** 0: Disable 1: Enable

HParaType = 01h, Sub-Address = 01h

Enable Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Enable Line Drawing from Up/Left to Down/Right** 0: Draw line from vertex a to vertex b. 1: For vertical line, draw from up vertex to down vertex. For horizontal line, draw from left vertex to right vertex.
22	WO	xxh	**Enable Diamond Rule for Line Drawing** 0: Disable 1: Enable
21	WO	xxh	**Enable Point Sprite** 0: Disable 1: Enable This setting is only available for PMType "point" and "triangle point". All Points have sizes (default is 1.0), and Point Sprite only affects the texture coordinate. ***If non-PointSprite points:*** All the texture coordinates of point 4 vertexes are all those from FVF. ***If PointSprite points:*** Texture coordinate of the upper-left corner is (0, 0, 0, 1). Texture coordinate of the upper-right corner is (1, 0, 0, 1). Texture coordinate of the lower-left corner is (0, 1, 0, 1). Texture coordinate of the lower-right corner is (1, 1, 0, 1).
20	WO	xxh	**Enable Clipping Coordinate to Screen Coordinate Transformation** 0: Disable 1: Enable
19	WO	xxh	**Enable Fog Perspective Correction** 0: Disable 1: Enable
18	WO	xxh	**Enable Spectra Color Perspective Correction** 0: Disable 1: Enable
17	WO	xxh	**Enable Diffuse Color Perspective Correction** 0: Disable 1: Enable
16:14	WO	xxh	**Number of Render Target** 000: Only RT0 001: RT0 & RT1 010: RT0, RT1 and RT2 011: RT0, RT1, RT2 and RT3 1xx: Reserved
13	WO	xxh	**Enable of Coarse Z Test** 0: Disable 1: Enable Note that Coarse Z Test is only available for triangles, not the lines.
12	WO	xxh	**Enable Vertex Cache** 0: Disable 1: Enable
11	WO	xxh	**Enable Clipping Engine** 0: Disable 1: Enable
10	WO	xxh	**Enable Pixel Shader** 0: Disable (Texture map is also disabled) 1: Enable
9	WO	xxh	**Enable Writing Coarse Z Buffer** 0: Do not update the Coarse Z Buffer 1: Enable
8	WO	xxh	**Enable Texture Cache** 0: Disable Texture Cache and Clear Texture Cache 1: Enable
7	WO	xxh	**Enable Back Face Culling** ***<HenBFCull>*** 0: Disable 1: Enable
6	WO	xxh	**Enable Color Write** 0: Disable 1: Enable
5	WO	xxh	**Enable Anti-Aliasing** 0: Disable 1: Enable
4	WO	xxh	**Enable Stencil Test** 0: Disable (Always pass) 1: Enable (Depth buffer must contain stencil bits)
3	WO	xxh	**Enable Z Test** 0: Disable (Always pass) 1: Enable
2	WO	xxh	**Enable Z Write** 0: Disable 1: Enable
1	WO	xxh	**Enable Stipple Pattern** 0: Disable 1: Enable
0	WO	xxh	**Enable Line Pattern** 0: Disable 1: Enable

HParaType = 01h, Sub-Address = 02h
Enable Setting 3

Bits [23:0]	Attribute	Default	Description
23:2	WO	xxh	**Reserved**
1	WO	xxh	**Clear Read-Color Cache (RC Cache)** RC Cache will be cleared while this bit is set to 1.
0	WO	xxh	**Enable Read-Color Cache** 0: Disable 1: Enable

HParaType = 01h, Sub-Address = 03-0Fh: Reserved (for Enable Setting)

HParaType = 01h, Sub-Address = 10h
Z Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**ZW Buffer Base Address** In unit of 256 bytes.

HParaType = 01h, Sub-Address = 11h
Z Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:13	WO	xxh	**ZW Buffer Pitch** ***<HZWBPit>*** In unit of 32 bytes for linear mode. In unit of tile (256 bytes) for tile mode.
12	WO	xxh	**Enable Reading-Z Cache** 0: Disable 1: Enable
11	WO	xxh	**Clear Reading-Z Cache**
10	WO	xxh	**Mode of Reading-Z Cache** 0: 128-bit mode 1: 256-bit mode
9	WO	xxh	**Z and Stencil Value are written through to BE directly** 0: Fully data path from PERZ through PS and RC, and then to BE 1: Short data path from PERZ to BE directly
8:2	WO	xxh	**Reserved**
1:0	WO	xxh	**Location Setting of Z Buffer** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved

HParaType = 01h, Sub-Address = 12h

Z Setting 3

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**ZW Buffer Type** 0: ZW buffer stores Z value 1: ZW buffer stores W value (PP replaces Z by W)
22	WO	xxh	**Reserved**
21	WO	xxh	**Force the Z Value from 1.0 to 1.0- (from 1.00000000h to 0.FFFFFFFFh)** 0: Keep the original 1.0 1: Force to 1.0- whenever Z equals to 1.0 This register is only useful for fixed-point format.
20	WO	xxh	**Clamp the Z Value is over 1.0 to 1.0- (from 1.xxxxxxxxh to 0.FFFFFFFFh)** 0: Keep the original value over 1.0 1: Clamp to 1.0- whenever Z is over 1.0 This register is only useful for fixed-point format.
19	WO	xxh	**Clamp the Z Value is Negative to Zero- (from –x.xxxxxxxxh to 0.00000000 h)** 0: Keep the original negative value 1: Clamp to 0.0- whenever Z is negative Note: These clamping registers do not affect the test of nearby or distant plane. The test of the nearby or distant plane is by the original biased and un-clamped Z value with floating format.
18:16	WO	xxh	**ZW Buffer Format** For Z Buffer 000: 16-bit fixed-point format, 0.0 ≤ Z < 1.0 001: 16-bit floating format s[5].10 from +2^31*1.FFFF to –2^31*1.FFFF 010: Reserved 011: Reserved 100: 32-bit fixed-point format, 0.0 ≤ Z < 1.0 101: 32-bit fixed-point format s[8].23 110: 24-bit fixed-point format Z, 0.0 ≤ Z < 1.0, and Stencil Z is located in bit [31:8], Stencil is located in bit [7:0]
15:7	WO	xxh	**Reserved**
6:5	WO	xxh	**Location Setting of Separated Stencil Buffer** 00: Syntem Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
4	WO	xxh	**Write Stencil Value of the Separated Stencil Buffer to the Z Buffer** 0: Normal 1: Force “STVALID” as true and stencil operation as “Keep”, so the stencil value in the separated buffer can be filled into Z buffer.
3	WO	xxh	**Synchronized with the Separated Stencil Value in Z Buffer** Indidate whether the stencil value in the separated stencil buffer is synchronized with the stencil value in Z buffer. 0: No synchronization. Hardware just updates the stencil value in the separated stencil buffer, which may not be synchronized to the stencil value in Z buffer. 1: The stencil value in the separated stencil buffer is synchronized to the stencil value in Z buffer. Hardware would update the separated stencil buffer and Z buffer.
2	WO	xxh	**Existence of Separated Stencil Buffer** 0: No separated stencil buffer 1: There is a separated stencil buffer
1	WO	xxh	**Extend for Z Format Transformation** 0: Do nothing. For Z with 32-bit floating s[8].23 and mantissa as 1.Z[22:0],it will be extended to 1.{Z[22:0], 8’h00} and transformed to fixed-format. 1: Extend mantissa to 32 bits before format transformation. Consider Z with 32-bit floating s[8].23 and mantissa as 1.Z[22:0], it will be extended to 1.{Z[22:0], 1’b1, Z[22:16]} and transformed to fixed format.
0	WO	xxh	**Memory Mode of ZW Buffer** 0: Linear mode 1: Tile mode

HParaType = 01h, Sub-Address = 13h
Z Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Source Z is Generated by Pixel Shader Instead of Shading** *<HZSrcPS>* 0: Source Z is generated by normal shading 1: Source Z is generated in PS, RZ module should pipe the Zdst to PE. The Zdst and Zsrc for depth test come from BE.
22:19	WO	xxh	**Reserved**
18:16	WO	xxh	**ZW Test Mode** ***<HZWTMD>*** 000: Z or W test never pass 001: Z or W test pass if Znew < Zdst 010: Z or W test pass if Znew = Zdst 011: Z or W test pass if Znew ≤ Zdst 100: Z or W test pass if Znew > Zdst 101: Z or W test pass if Znew ≠ Zdst 110: Z or W test pass if Znew ≥ Zdst 111: Z or W test always pass Where Znew is the calculated Z value and Zdst is the Z stored in the Z buffer.
15:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Z Normalization Factor** The range is from 0 to 255. By definition, Z can be divided by a value of power of 2. Thus, it allows the input Z free from the constrain of Z < 1. Z Normalization is $Z = Zin / 2^{HZNF}$

HParaType = 01h, Sub-Address = 14h
Z Setting 5

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of ZW Clear Data**

HParaType = 01h, Sub-Address = 15h
Z Setting 6

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Negative of Mask to the Zsrc's Last 16-bit Mantissa** Note that this mask is just implemented to the rendered Z value for format transformation, then a Z test is conducted and wrote-back to Z buffer. Consider the generated Z value "Zsrc[31:0]" with floating s[8].23: Step1: Zsrc[15:0] = Zsrc[15:0] & ~HZWMMSK_N[15:0] Step2: Format transform Zsrc according to HZWFM Step3: Z test Step4: Updated Z buffer with the format transformed Zsrc if Z test is passed
7:0	WO	xxh	**Highest Byte of ZW Clear Data**

HParaType = 01h, Sub-Address = 16h
Z Setting 7

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Z Bias Offset** With 32-bit floating format, since Z format transformation is between fixed and floating, and HZBiasOffset description is suggested to be modified as below: *If (HZWBFM == 32-bit fixed)* *HZBiasOffset = HZBiasOffset * (2^32 – 1) / 2^32* *Else if (HZWBFM == 24-bit fixed)* *HZBiasOffset = HZBiasOffset * (2^24 – 1) / 2^24* *Else if (HZWBFM == 16-bit fixed)* HZBiasOffset = HZBiasOffset * (2^16 – 1) / 2^16

HParaType = 01h, Sub-Address = 17h
Z Setting 8

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Bias Scale with 32-bit Floating Format**
15:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Highest Byte of Z Bias Offset** SEZbias = max(Zdx, Zdy) * HZBiasScale + HZBias Offset

HParaType = 01h, Sub-Address = 18h
Z Setting 9

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Z Bias Scale With 32-bit Floating Format**

HParaType = 01h, Sub-Address = 19h
Z Setting 10

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Low 23 Bits of Low Boundary to Clamp the Z Bias** With format of 32-bit floating.

HParaType = 01h, Sub-Address = 1Ah
Z Setting 11

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Low 23 Bits of High Boundary to Clamp the Z Bias** With format of 32-bit floating.

HParaType = 01h, Sub-Address = 1Bh
Z Setting 12

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Enhance Z's Precision During PE Rendering** 0: Disable 1: Enable
22:16	WO	xxh	**Reserved**
15:8	WO	xxh	**High 8 Bits of High Boundary to Clamp the Z Bias** With format of 32-bit floating.
7:0	WO	xxh	**High 8 Bits of Low Boundary to Clamp the Z Bias** With format of 32-bit floating.

HParaType = 01h, Sub-Address = 1Ch
Z Setting 13

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Low 24 Bits Occlusion Count of both Z Test and Stencil Test Result**

HParaType = 01h, Sub-Address = 1Dh
Z Setting 14

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7:0	WO	xxh	**High 8 Bits Occlusion Count of Both Z Test and Stencil Test Result**

HParaType = 01h, Sub-Address = 1Eh
Z Setting 15

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 24 Bits of Clip Plane's Far Value**

HParaType = 01h, Sub-Address = 1Fh
Z Setting 16

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 24 Bits of Clip Plane's Near Value**

HParaType = 01h, Sub-Address = 20h
Z Setting 17

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:8	WO	xxh	**Higher 8 Bits of Clip Plane's Far Value** With format of 32-bit floating.
7:0	WO	xxh	**Higher 8 Bits of Clip Plane's Near Value** With format of 32-bit floating. Check each pixel's Z value before depth testing, and remove this pixel if it's out of the range. If (Z > HZClipFar | Z < HZClipNear) Drop this pixel Else Do Depth Testing Note that this check is in higher priority than "Z Window".

HParaType = 01h, Sub-Address = 21h
Z Setting 18

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Low 24 Bits of Video Memory Address to Address to Write the "HZOcclusionCNT"** ***<HZOcclusionAdrL>*** In a unit of 4 bytes. Note for Driver: Whenever a non-zero value is set to this register, the "HZOcclusionCNT" would be written back to the video memory with the address of "HZOcclusionAdr". Since the address is separated into 2 sub-addresses, please set driver "HZOcclusionAdrL" and then "HZOcclusionAdrH" in order. Whenever decoding the "HZOcclusionAdrH", hardware would check if the address (HZOcclusionAdrH and HZOcclusionAdrL cascaded) is zero or not.

HParaType = 01h, Sub-Address = 22h
Z Setting 19

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Location Setting of Z Occlusion Counter (HZOcclusionCNT)** 00: Syntem Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
21:8	WO	xxh	**Reserved**
7:0	WO	xxh	**High 8 Bits of Video Memory Address to Address** ***<HZOcclusionAdrH>*** For writing the "HZOcclusionCNT", in the unit of 4 bytes.

HParaType = 01h, Sub-Address = 23h

Stencil Setting 1

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Stencil Test Reference Value for Clock-Wise Face** ***<HSTCWREF>*** This value is a positive 8-bit fixed point number with range from 0 to 255, which is used for Stencil Test as the comparison result between Stencil and HSTCWREF.
15:8	WO	xxh	**Stencil Test Operation Mask for Clock-Wise Face** ***<HSTCWOPMSK>*** Indicates the comparison result between (Stencil & HSTCWOPMSK) and (HSTCWREF & HSTCWBMSK).
7:0	WO	xxh	**Stencil Buffer Bit Mask for Clock-Wise Face** ***<HSTCWBMSK>*** If this bit = 0, the corresponding bit in the stencil buffer cannot be changed. Otherwise, it can be changed.

HParaType = 01h, Sub-Address = 24h

Stencil Setting 2

Bits [23:0]	Attribute	Default	Description
23:19	WO	xxh	**Reserved**
18:16	WO	xxh	**Stencil Test Mode for Clock-Wise Face** 000: Stencil Test never pass 001: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) < (Stencil & HSTCWOPMSK) 010: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) = (Stencil & HSTCWOPMSK) 011: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) ≤ (Stencil & HSTCWOPMSK) 100: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) > (Stencil & HSTCWOPMSK) 101: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) ≠ (Stencil & HSTCWOPMSK) 110: Stencil Test pass if (HSTCWREF & HSTCWOPMSK) ≥ (Stencil & HSTCWOPMSK) 111: Stencil Test always pass
15:9	WO	xxh	**Reserved**
8:6	WO	xxh	**Stencil Operation for Stencil Test Fail for Clock-Wise Face** 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR
5:3	WO	xxh	**Stencil Operation for Stencil Test Pass and Z Test Fail for Clock-Wise Face** 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR
2:0	WO	xxh	**Stencil Operation for Stencil Test Pass and Z Test Pass for Clock-Wise Face** 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR

HParaType = 01h, Sub-Address = 25h

Stencil Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Stencil Test Reference Value for Counter-Clock-Wise Face <*HSTCCWREF*>** This value is a positive 8-bit fixed point number with range from 0 to 255, which is used for Stencil Test as the comparison result between Stencil and HSTCCWREF.
15:8	WO	xxh	**Stencil Test Operation Mask for Counter-Clock-Wise Face <*HSTCCWOPMSK*>** Indicates the comparison result between (Stencil & HSTCCWOPMSK) and (HSTCCWREF & HSTCCWBMSK).
7:0	WO	xxh	**Stencil Buffer Bit Mask for Counter-Clock-Wise Face <*HSTCCWBMSK*>** If this bit = 0, the corresponding bit in the stencil buffer cannot be changed. Otherwise, it can be changed.

HParaType = 01h, Sub-Address = 26h

Stencil Setting 4

Bits [23:0]	Attribute	Default	Description
23:19	WO	xxh	**Reserved**
18:16	WO	xxh	**Stencil Test Mode for Counter-Clock-Wise Face** 000: Stencil Test never pass 001: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) < (Stencil & HSTCCWOPMSK) 010: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) = (Stencil & HSTCCWOPMSK) 011: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) ≤ (Stencil & HSTCCWOPMSK) 100: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) > (Stencil & HSTCCWOPMSK) 101: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) ≠ (Stencil & HSTCCWOPMSK) 110: Stencil Test pass if (HSTCCWREF & HSTCCWOPMSK) ≥ (Stencil & HSTCCWOPMSK) 111: Stencil Test always pass
15:9	WO	xxh	**Reserved**
8:6	WO	xxh	**Stencil Operation for Stencil Test Fail for Counter-Clock-Wise Face** 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR
5:3	WO	xxh	**Stencil Operation for Stencil Test Pass and Z Test Fail for Counter-Clock-Wise Face** 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR
2:0	WO	xxh	**Stencil Operation for Stencil Test Pass and Z Test Pass for Counter-Clock-Wise Face** 000: KEEP 001: ZERO 010: REPLACE 011: INCRSAT 100: DECRSAT 101: INVERT 110: INCR 111: DECR

HParaType = 01h, Sub-Address = 27h
Setting for Fast-Z-Clear 1

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:12	WO	xxh	**Index of ZW Buffer for Current Scene**
11:8	WO	xxh	**Length of HZWBIdx in Unit of Bit** 0000: Disable ZW buffer index 0001: Use the LSB 1 bit as ZW buffer index 0010: Use the LSB 2 bits as ZW buffer index 0011: Use the LSB 3 bits as ZW buffer index 0100: Use the LSB 4 bits as ZW buffer index 1111 ~ 0101: Reserved
7:1	WO	xxh	**Reserved**
0	WO	xxh	**Enable Fast-Z-Clear** 0: Disable 1: Enable

HParaType = 01h, Sub-Address = 28h
Setting for Fast-Z-Clear 2

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Stencil Buffer's Base Address** ***<HSTBas>*** In unit of 256 bytes. The pitch of the separated stencil buffer is just the setting of the Z buffer pitch. Since there is only Z24S8 format for the stencil value, the Z must be 32 bpp wnen separated stencil buffer is enabled. No matter Z buffer is in linear or tile mode, the HZWBPit is just (W+7) >> 3, where W is the screen coordinate. E3R(W)STADR = HSTBas*256 + Y[10:3]*HZWBPit*64 + X[10:3]*64 + Y[2:1]*16

HParaType = 01h, Sub-Address = 29h
Setting for Coarse Z Test Function 1

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Force CZ Retest If Original Is "Reject" and the Related Primitive Is Clock-Wise** Force the CZ result as "ReTEST" if original is "REJECT" and the related primitive is Clock-Wise. 0: Normal CZ test 1: Never reject
22	WO	xxh	**Force CZ Retest If Original Is "Pass" and the Related Primitive Is Clock-Wise** Force the CZ result as "ReTEST" if original is "Pass" and the related primitive is Clock-Wise. 0: Normal CZ test 1: Never pass
21:20	WO	xxh	**Coarse Z Buffer Location Setting** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
19:18	WO	xxh	**Reserved**
17	WO	xxh	**Inverse Mode for CZ Test** 0: Smaller Z value as nearer and larger Z value as farer, for HZWTMD is LESS or LESSEQUAL 1: Larger Z value as nearer and smaller Z value as farer, for HZWTMD is GREATER or GREATEREQUAL
16	WO	xxh	**Coarse Z Write Back Mode** 0: Whenever the CZTAG_CNT is "0" and CZTAG_UPDATED, write the CZ in cache back to video memory 1: Whenever the cell is selected for new CZ value and CZTAG_UPDATED, write the old CZ in cache back to video memory, and then read the new CZ value.
15	WO	xxh	**Reset of CZ Cache's TAG** Instead of having software to clear this setting, it would be auto-cleared by hardware. 0: Normal 1: Rest
14	WO	xxh	**Reserved**
13:12	WO	xxh	**Coarse Z Test by Using Conservative Mode** 00: Use optimized merging rule 01: Use Conservative Merging Rule and only update both "MIN" value and "MAX" value 10: Use Conservative Merging Rule and only update "MIN" value 11: Reserved

11	WO	xxh	**Force CZ Retest If Original Is "Reject" and the Related Primitive Is Counter-Clock-Wise** Force the CZ result as "ReTEST" if original is "REJECT" and the related primitive is Counter-Clock-Wise. 0: Normal CZ test 1: Never reject
10	WO	xxh	**Force CZ Retest If Original Is "Pass" and the Related Primitive Is Counter-Clock-Wise** Force the CZ result as "ReTEST" if original is "REJECT" and the related primitive is Counter-Clock-Wise. 0: Normal CZ test 1: Never reject
9	WO	xxh	**Force ReTest as the Result of HZ Test** 0: Normal 1: Force
8:0	WO	xxh	**Coarse Z Buffer's Pitch** In unit of 32 bytes.

HParaType = 01h, Sub-Address = 2Ah
Setting for Coarse Z Test Function 2

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Coarse Z Buffer's Base Address** In unit of 256 bytes. E3R(W)CZADR = HCZBas*256 + Y*HCZPit*32 + (2*X)*16

HParaType = 01h, Sub-Address = 33h
Alpha Setting 1

Bits [23:0]	Attribute	Default	Description
23:15	WO	xxh	**Reserved**
14:12	WO	xxh	**Alpha Test Mode** 000: Alpha test never pass 001: Alpha test pass if Anew < HATREF (bits [10:0]) 010: Alpha test pass if Anew = HATREF 011:A lpha test pass if Anew ≤ HATREF 100: Alpha test pass if Anew > HATREF 101: Alpha test pass if Anew ≠ HATREF 110: Alpha test pass if Anew ≥ HATREF 111: Alpha test always pass
11	WO	xxh	**Reserved**
10:0	WO	xxh	**Alpha Test Reference Value** ***<HATREF>*** Positive fixed-point from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 34h
Alpha Setting 2

Alpha Blending Equation of RGB:
Equation of RGB: Cout = ((AB_FCa * AB_Ca) AB_Cop (AB_FCb * AB_Cb))
If (HABLCsat = false) Clamp Cout to 1.0 to 0.0

<table>
<tr><th>Bits [23:0]</th><th>Attribute</th><th>Default</th><th>Description</th></tr>
<tr><td>23:17</td><td>WO</td><td>xxh</td><td>Reserved</td></tr>
<tr><td>16</td><td>WO</td><td>xxh</td><td>RGB Saturation Control of Alpha Blending Calculation <HABLCsat>
0: Cout will be clamp to 0.0 ~ 1.0
1: Cout will not be clamp to 0.0 ~ 1.0</td></tr>
<tr><td>15:10</td><td>WO</td><td>xxh</td><td>Ca of Alpha Blending Equation <HABLCa>
<table>
<tr><th>HABLCa[3:0]</th><th>R_of_OPCa</th><th>G_of_OPCa</th><th>B_of_OPCa</th></tr>
<tr><td>0001</td><td>Rsrc</td><td>Gsrc</td><td>Bsrc</td></tr>
<tr><td>0001</td><td>Rdst</td><td>Gdst</td><td>Bdst</td></tr>
<tr><td>0101</td><td>R of HABLRca</td><td>G of HABLRCa</td><td>B of HABLRCa</td></tr>
<tr><td>0110</td><td>min (Rsrc, Rdst)</td><td>min (Gsrc, Gdst)</td><td>min (Bsrc, Bdst)</td></tr>
<tr><td>0111</td><td>max (Rsrc, Rdst)</td><td>max (Gsrc, Gdst)</td><td>max (Bsrc, Bdst)</td></tr>
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<tr><td>9:4</td><td>WO</td><td>xxh</td><td>FCa of Alpha Blending Equation <HABLFCa>
<table>
<tr><th>HABLFCa[5:4]</th><th>R of AB_Fca</th><th>G of AB_FCa</th><th>B of AB_FCa</th></tr>
<tr><td>00</td><td>R_of_OPFCa</td><td>G_of_OPFCa</td><td>B_of_OPFCa</td></tr>
<tr><td>01</td><td>1.0 - R_of_OPFCa</td><td>1.0 - G_of_OPFCa</td><td>1.0 - B_of_OPFCa</td></tr>
<tr><td>11</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table>
<table>
<tr><th>HABLFCa[3:0]</th><th>R_of_OPFCa</th><th>G_of_OPFCa</th><th>B_of_OPFCa</th></tr>
<tr><td>0000</td><td>Rsrc</td><td>Gsrc</td><td>Bsrc</td></tr>
<tr><td>0001</td><td>Rdst</td><td>Gdst</td><td>Bdst</td></tr>
<tr><td>0010</td><td>Asrc</td><td>Asrc</td><td>Asrc</td></tr>
<tr><td>0011</td><td>Adst</td><td>Adst</td><td>Adst</td></tr>
<tr><td>0101</td><td>R of HABLRFCa</td><td>G of HABLRFCa</td><td>B of HABLRFCa</td></tr>
<tr><td>1000</td><td>min (Asrc, 1-Adst)</td><td>min (Asrc, 1-Adst)</td><td>min (Asrc, 1-Adst)</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>WO</td><td>xxh</td><td>Reserved</td></tr>
</table>

HParaType = 01h, Sub-Address = 35h

Alpha Setting 3

<table>
<tr><th>Bits [23:0]</th><th>Attribute</th><th>Default</th><th>Description</th></tr>
<tr><td>23:16</td><td>WO</td><td>xxh</td><td>Reserved</td></tr>
<tr><td>15:14</td><td>WO</td><td>xxh</td><td>Cop of Alpha Blending Equation <HABLCop>
<table>
<tr><th>HABLCop</th><th>Cop</th></tr>
<tr><td>00</td><td>+</td></tr>
<tr><td>01</td><td>-</td></tr>
<tr><td>10</td><td>Max</td></tr>
<tr><td>11</td><td>Min</td></tr>
</table></td></tr>
<tr><td>13:8</td><td>WO</td><td>xxh</td><td>Cb of Alpha Blending Equation <HABLCb>
<table>
<tr><th>HABLCb[3:0]</th><th>R_of_OPCb</th><th>G_of_OPCb</th><th>B_of_OPCb</th></tr>
<tr><td>0000</td><td>Rsrc</td><td>Gsrc</td><td>Bsrc</td></tr>
<tr><td>0001</td><td>Rdst</td><td>Gdst</td><td>Bdst</td></tr>
<tr><td>0101</td><td>R of HABLRCb</td><td>G of HABLRCb</td><td>B of HABLRCb</td></tr>
</table></td></tr>
<tr><td>7:2</td><td>WO</td><td>xxh</td><td>FCb of Alpha Blending Equation <HABLFCb>
<table>
<tr><th>HAB_FCb[5:4]</th><th>R of AB_FCb</th><th>G of AB_FCb</th><th>B of AB_FCb</th></tr>
<tr><td>00</td><td>R_of_OPFCb</td><td>G_of_OPFCb</td><td>B_of_OPFCb</td></tr>
<tr><td>01</td><td>1.0 - (R_of_OPFCb)</td><td>1.0 - (G_of_OPFCb)</td><td>1.0 - (B_of_OPFCb)</td></tr>
</table>
<table>
<tr><th>HAB_FCb[3:0]</th><th>R_of_OPFCb</th><th>G_of_OPFCb</th><th>B_of_OPFCb</th></tr>
<tr><td>0000</td><td>Rsrc</td><td>Gsrc</td><td>Bsrc</td></tr>
<tr><td>0001</td><td>Rdst</td><td>Gdst</td><td>Bdst</td></tr>
<tr><td>0010</td><td>Asrc</td><td>Asrc</td><td>Asrc</td></tr>
<tr><td>0011</td><td>Adst</td><td>Adst</td><td>Adst</td></tr>
<tr><td>0101</td><td>R of HABLRFCb</td><td>G of HABLRFCb</td><td>B of HABLRFCb</td></tr>
<tr><td>1000</td><td>min (Asrc, 1-Adst)</td><td>min (Asrc, 1-Adst)</td><td>min (Asrc, 1-Adst)</td></tr>
</table></td></tr>
<tr><td>1:0</td><td>WO</td><td>xxh</td><td>Reserved</td></tr>
</table>

HParaType = 01h, Sub-Address = 36h
Alpha Setting 4

Equation of A: Aout = ((AB_FAa * AB_Aa) AB_Aop (AB_FAb * AB_Ab))
If (HABLAsat = false) Clamp Aout to 1.0 to 0.0

<table>
<tr><th>Bits [23:0]</th><th>Attribute</th><th>Default</th><th>Description</th></tr>
<tr><td>23:17</td><td>WO</td><td>xxh</td><td>Reserved</td></tr>
<tr><td>16</td><td>WO</td><td>xxh</td><td>Alpha Saturation Control of Alpha Blending Calculation <HABLAsat>
0: Aout will be clamped to 0.0 ~ 1.0
1: Aout will not be clamped to 0.0 ~ 1.0</td></tr>
<tr><td>15:10</td><td>WO</td><td>xxh</td><td>Aa of Alpha Blending Equation <HABLAa>
<table>
<tr><th>HABLAa[5:4]</th><th>AB_Aa</th></tr>
<tr><td>xx</td><td>Reserved</td></tr>
</table>
<table>
<tr><th>HABLAa[3:0]</th><th>OPAa</th></tr>
<tr><td>0000</td><td>0</td></tr>
<tr><td>0001</td><td>Asrc</td></tr>
<tr><td>0010</td><td>Adst</td></tr>
<tr><td>0101</td><td>min (Asrc, Adst)</td></tr>
<tr><td>0111</td><td>max (Asrc, Adst)</td></tr>
<tr><td>1000</td><td>Reserved</td></tr>
<tr><td>1001</td><td>HABLRAa</td></tr>
<tr><td>1111-1010</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>9:4</td><td>WO</td><td>xxh</td><td>FAa of Alpha Blending Equation <HABLFAa>
<table>
<tr><th>HABLFAa[5:4]</th><th>AB_FAa</th></tr>
<tr><td>00</td><td>OPFAa</td></tr>
<tr><td>01</td><td>1 - OPFAa</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>
<table>
<tr><th>HABLFAa[3:0]</th><th>OPFAa</th></tr>
<tr><td>0000</td><td>0</td></tr>
<tr><td>0001</td><td>Asrc</td></tr>
<tr><td>0010</td><td>Adst</td></tr>
<tr><td>1000</td><td>min (Asrc, 1-Adst)</td></tr>
<tr><td>1001</td><td>HABLRFAa</td></tr>
<tr><td>1111-1101</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>WO</td><td>xxh</td><td>Reserved</td></tr>
</table>

HParaType = 01h, Sub-Address = 37h
Alpha Setting 5

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:14	WO	xxh	**Aop of Alpha Blending Equation** *<HABLAop>* **HABLAop** / **AB_Aop** 00 / + 01 / - 10 / Max 11 / Min
13:8	WO	xxh	**Ab of Alpha Blending Equation** *<HABLAb>* **HABLAb[5:4]** / **AB_Ab** **xx** / Reserved **HABLAb[3:0]** / **OPAb** **0000** / 0 **0001** / Asrc **0010** / Adst **1000** / min (Asrc, 1-Adst) **1001** / HABLRAb **1111-1001** / Reserved
7:2	WO	xxh	**FAb of Alpha Blending Equation** *<HABLFAb>* **HABLFAb[5:4]** / **AB_FAb** **00** / OPFAb **01** / 1 – OPFAb **HABLFAb[3:0]** / **OPFAb** **0000** / 0 **0001** / Asrc **0010** / Adst **1000** / min (Asrc, 1-Adst) **1001** / HABLRFAb
1:0	WO	xxh	**Reserved**

HParaType = 01h, Sub-Address = 38h
Alpha Setting 6

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**G of HABLRCa** This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	**Reserved**
10:0	WO	xxh	**B of HABLRCa** This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 39h
Alpha Setting 7

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**R of HABLRFCa** This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	**Reserved**
10:0	WO	xxh	**R of HABLRCa** This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Ah
Alpha Setting 8

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**G of HABLRFCa** This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	**Reserved**
10:0	WO	xxh	**B of HABLRFCa** This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Bh
Alpha Setting 9

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**G of HABLRCb** This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	**Reserved**
10:0	WO	xxh	**B of HABLRCb** This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Ch
Alpha Setting 10

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**R of HABLRFCb** This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	**Reserved**
10:0	WO	xxh	**R of HABLRCb** This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Dh
Alpha Setting 11

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**G of HABLRFCb** This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	**Reserved**
10:0	WO	xxh	**B of HABLRFCb** This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Eh
Alpha Setting 12

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**Constant Register of Aa** This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	**Reserved**
10:0	WO	xxh	**Constant Register of FAa** ***<HABLRFAa>*** This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address = 3Fh
Alpha Setting 13

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**Constant Register of Ab** ***<HABLRAb>*** This is an 11-bit positive fixed-point number from 0.0 to 1.0.
11	WO	xxh	**Reserved**
10:0	WO	xxh	**Constant Register of FAb** *<HABLRFAb>* This is an 11-bit positive fixed-point number from 0.0 to 1.0.

HParaType = 01h, Sub-Address 40-4Fh: Reserved (for Alpha Setting)

HParaType = 01h, Sub-Address = 50h
Destination Setting – Render Target 0 – Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Render Target0's Base Address** In unit of 256 bytes.

HParaType = 01h, Sub-Address = 51h
Destination Setting – Render Target 0 – Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Memory Mode of Render Target 0** 0: Linear mode 1: Tile mode
22	WO	xxh	**Render Target0's Tile Is 16-pixel High** ***<HMRT0TileH16>*** 0: Normal 8-pixel high 1: 16-pixel high
21:20	WO	xxh	**Location Setting of Render Target 0** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
19:0	WO	xxh	**Reserved**

HParaType = 01h, Sub-Address = 52h
Destination Setting – Render Target 0 – Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Render Target0's Format** **For Bit [23:19]:** 00000: Reserved 00001: Reserved 00010: Luminance format 00011: Reserved 00100: Reserved 00101: Reserved 00110: YUV(Video Texture) format 00111-10000: Reserved 10001: ARGB_16bpp format 10010: Reserved 10011: ARGB_32bpp format 10100: Reserved 10101: ABGR_16bpp format 10110: Reserved 10111: ABGR_32bpp format 11000: Reserved 11001: RGBA_16bpp format 11010: Reserved 11011: RGBA_32bpp format 11100: BGRA_16bpp format 11101: BGRA_32bpp format 11110: Floating Color format 11111: Reserved ***If there is NO Alpha channel in the defined format, fill 1.0 as Alpha value.*** **For Bit [18:16]:** ***For Luminance Format:*** 000-100: Reserved 101: AL88 (Bits [15:8] = A, Bits [7:0] = L) 110: L16 (Bits [15:0] = L) For L16 format, post-rendering must be disabled. 111: Reserved ***For YUV Format (Video Texture):*** 000: Package mode (Bits [31:24] = V or Cr, Bits [23:16] = Y1, Bits [15:8] = U or Cb, Bits [7:0] = Y0) Others: Reserved **For reading color**, consider the 8-bit Y as positive 8-bit G, 8-bit U as positive 8-bit R, and 8-bit V as positive 8-bit B. Then extend them to s1.10 according to setting of ***Color Extending Mode*** (see bit 15). **For writing color**, the adjacent 2 pixels are combined into 32 bits and share same 8-bit U and V. Consider an even pixel with R0, G0 & B0 (dithered 8-bit color), and the next odd pixel with R1, G1& B1 (dithered 8-bit color), the packed result is {(B0 + B1)/2, G1, (R0+R1)/2, G0}. Note the (B0+B1)/2 and (R0+R1)/2 are the result of rounding. ***For ARGB_16bpp Format:*** 000: RGB555 (Bits [14:10] = R, Bits [9:5] = G, Bits [4:0] = B) 001: RGB565 (Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B) 010: ARGB1555 (Bit [15] = A, Bits [14:10] = R, Bits [9:5] = G, Bits [4:0] = B) 011: ARGB4444 (Bits [15:12] = A, Bits [11:8] = R, Bits [7:4] = G, Bits [3:0] = B) 100: Reserved 101: RGB565 for write color: Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R. As for read color: Bits [15:11] = B, Bits [10:6] = G, Bits [4:0] = R 11x: Reserved ***For ARGB_32bpp Format:*** 000: ARGB0888 (Bits [23:16] = R, Bits [15:8] = G, Bits [7:0] = B) 001: ARGB8888 (Bits [31:24] = A, Bits [23:16] = R, Bits [15:8] = G, Bits [7:0] = B) 010: ARGB2_10_10_10 (Bits [31:30] = A, Bits [29:20] = R, Bits [19:10] = G, Bits [9:0] = B) 011-1xx: Reserved ***For ABGR_16bpp Format:*** 000: BGR555 (Bits [14:10] = B, Bits [9:5] = G, Bits [4:0] = R) 001: BGR565 (Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R) 010: ABGR1555 (Bit [15] = A, Bits [14:10] = B, Bits [9:5] = G, Bits [4:0] = R) 011: ABGR4444 (Bits [15:12] = A, Bits [11:8] = B, Bits [7:4] = G, Bits [3:0] = R) 100: Reserved 101: BGR565 for write color, Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R.

			As for read color, Bits [15:11] = B, Bits [10:6] = G, Bits [4:0] = R. 11x: Reserved ***For ABGR_32bpp Format:*** 000: ABGR0888 (Bits [23:16] = B, Bits [15:8] = G, Bits [7:0] = R) 001: ABGR8888 (Bits [31:24] = A, Bits [23:16] = B, Bits [15:8] = G, Bits [7:0] = R) 010: ABGR2_10_10_10 (Bits [31:30] = A, Bits [29:20] = B, Bits [19:10] = G, Bits [9:0] = R) 011: G16R16 (Bits [31:16] = G, Bits [15:0] = R). For G16R16 format, post-rendering must be disabled. 1xx: Reserved ***For RGBA_16bpp Format:*** 000: RGB555 (Bits [15:11] = R, Bits [10:6] = G, Bits [5:1] = B) 001: RGB565 (Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B) A = 1.0 010: RGBA1555 (Bits [15:11] = R, Bits [10:6] = G, Bits [5:1] = B, Bit [0] = A) 011: RGBA4444 (Bits [15:12] = R, Bits [11:8] = G, Bits [7:4] = B, Bits [3:0] = A) 100: Reserved 101: RGB565 for write color, Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B. As for read color, Bits [15:11] = R, Bits [10:6] = G, Bits [4:0] = B, A = 1.0. 11x: Reserved ***For RGBA_32bpp Format:*** 000: RGBA8880 (Bits [31:24] = R, Bits [23:16] = G, Bits [15:8] = B) A = 1.0 001: RGBA8888 (Bits [31:24] = R, Bits [23:16] = G, Bits [15:8] = B, Bits [7:0] = A) 010: RGBA10_10_10_2 (Bits [31:22] = R, Bits [21:12] = G, Bits [11:2] = B, Bits [1:0] = R) 011-1xx: Reserved ***For ABGR_16bpp Format:*** 000: BGR555 (Bits [15:11] = B, Bits [10:6] = G, Bits [5:1] = R) A = 1.0 001: BGR565 (Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R) A = 1.0 010: BGRA1555 (Bits [15:11] = B, Bits [10:6] = G, Bits [5:1] = R, Bits [0] = A) 011: BGRA4444 (Bits [15:12] = B, Bits [11:8] = G, Bits [7:4] = R, Bits [3:0] = A) 100: Reserved 101: BGR565 for write color, Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R But for read color, Bits [15:11] = B, Bits [10:6] = G, Bits [4:0] = R A = 1.0 11x: Reserved ***For BGRA_32bpp Format:*** 000: BGRA8880 (Bits [31:24] = B, Bits [23:16] = G, Bits [15:8] = R) A = 1.0 001: BGRA8888 (Bits [31:24] = B, Bits [23:16] = G, Bits [15:8] = R, Bits [7:0] = R) 010: BGRA10_10_10_2 (Bits [31:22] = B, Bits [21:12] = G, Bits [11:2] = R, Bits [1:0] = R) 011-1xx: Reserved ***For Floating Color Format:*** 000: R16F (Bits [15:0] = R) 100: G16FR16F (Bits [31:16] = R, Bits [15:0] = G) 101: R32F (Bits [31:0] = R) For floating color format, post-rendering must be disabled

15	WO	xxh	**Color Extending Mode (Excluding Alpha)** 0: Extending with high color bit Translate to 1.10 format. **10 => 11** $C_{11} = C_{10} * (1024/1023) = C_{10} + (1/1023) * C_{10}$ $C_{10} < 1023$, $C_{11} = 0.xxxxxxxxxx(C_{10})$ $C_{10} == 1023$, $C_{11} = 1.0000000000$ **8 => 11** $C_{11} = C_8 * (1024/255) = 4*C_8 + (4/255)*C_8$ $C_8 < 64$, $C_{11} = 0.C_800$ $64 \leqq C_8 < 128$, $C_{11} = 0.C_801$ $128 \leqq C_8 < 192$, $C_{11} = 0.C_810$ $192 \leqq C_8 < 255$, $C_{11} = 0.C_811$ $C_8 == 255$, $C_{11} = 1.0000000000$ **6 => 11** $C_{11} = C_6 * (1024/63) = 16*C_6 + (16/63)*C_6$ $C_6 < 4$, $C_{11} = 0.C_60000$ $4 \leqq C_6 < 8$, $C_{11} = 0.C_60001$ $8 \leqq C_6 < 12$, $C_{11} = 0.C_60010$ $12 \leqq C_6 < 16$, $C_{11} = 0.C_60011$ $16 \leqq C_6 < 20$, $C_{11} = 0.C_60100$ $20 \leqq C_6 < 24$, $C_{11} = 0.C_60101$ $24 \leqq C_6 < 28$, $C_{11} = 0.C_60110$ $28 \leqq C_6 < 32$, $C_{11} = 0.C_60111$ $32 \leqq C_6 < 36$, $C_{11} = 0.C_61000$ $36 \leqq C_6 < 40$, $C_{11} = 0.C_61001$ $40 \leqq C_6 < 44$, $C_{11} = 0.C_61010$ $44 \leqq C_6 < 48$, $C_{11} = 0.C_61011$ $48 \leqq C_6 < 52$, $C_{11} = 0.C_61100$ $52 \leqq C_6 < 56$, $C_{11} = 0.C_61101$ $56 \leqq C_6 < 60$, $C_{11} = 0.C_61110$ $60 \leqq C_6 < 63$, $C_{11} = 0.C_61111$ $C_6 == 63$, $C_{11} = 1.0000000000$ **5 => 11** $C_{11} = C_5 * (1024/31) = 33C_5 + (1/31)*C_5 = 32*C_5 + C_5 + (1/31)*C_5$ $C_5 < 31$, $C_{11}=0.C_5C_5$ $C_5 == 31$, $C_{11}=1.0000000000$ **4=>11** $C_{11} = C_4 * (1024/15) = 68*C_4 + (4/15)*C_4 = 64*C_4 + 4*C_4 + (4/15)*C_4$ $C_4 < 4$, $C_{11}=C_4C_400$ $4 \leqq C_4 < 8$, $C_{11}=C_4C_401$ $8 \leqq C_4 < 12$, $C_{11}=C_4C_410$ $12 \leqq C_4 < 15$, $C_{11}=C_4C_411$ $C_4 == 15$, $C_{11}=1.0000000000$ 1: Extending with zero Considering 6=>11 as example: C11 = 0. $C_6$0000
14:13	WO	xxh	**Reserved**
12	WO	xxh	**Saturation of PS's Output for Render Target "M"** 0: Clamp PS's output color oCm to related render tager format's range For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0 . For 16-bit floating color format: MINVALUE = 16'hFBFF, MAXVALUE = 16'h7BFF. For 32-bit floating color format: MINVALUE = 32'h7F7FFFFF, MAXVALUE =32'hFF7FFFFF. Clamped Value = min(MAXVALUE, max(oCm, MINVALUE)) *Note if oCm is "NAN", clamped value is MINVALUE.* 1: oCm doesn't clamp
11:10	WO	xxh	**Reserved**
9:0	WO	xxh	**Render Target0's Pitch** In unit of 32 bytes for linear mode. In unit of tile (256 bytes or 512 bytes depend on HMRT0TileH16) for tile mode.

HParaType = 01h, Sub-Address = 53h

Destination Setting – Render Target 0 – Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Render Target0's Y Inverse for Dither** 0: Not inverse 1: Inverse
22:21	WO	xxh	**Render Target0's Y Bias for Dither**
20	WO	xxh	**Render Target0's X Inverse for Dither** 0: Not inverse 1: Inverse
19:18	WO	xxh	**Render Target0's X Bias for Dither**
17	WO	xxh	**Reserved**
16:15	WO	xxh	**Render Target0's Dither Mode** 00: Dither Table with multiplied by (2^n – 1) 10: Rounding with multiplied by (2^n – 1) 01: Dither Table without multiplied by (2^n – 1) 11: Rounding without multiplied by (2^n – 1)
14:12	WO	xxh	**Reserved**
11:8	WO	xxh	**Render Target0's Raster Operation** 0000: BLACK 0 0001: NOT_MERGE_PEN DPon 0010: MASK_NOT_PEN DPna 0011: NOT_COPY_PEN Pn 0100: MASK_PEN_NOT PDna 0101: NOT Dn 0110: XOR_PEN DPx 0111: NOT_MASK_PEN DPan 1000: MASK_PEN DPa 1001: NOT_XOR_PEN DPxn 1010: NOP D 1011: MERGE_NOT_PEN DPno 1100: COPY_PEN P 1101: MERGE_PEN_NOT PDno 1110: MERGE_PEN DPo 1111: WHITE 1
7	WO	xxh	**Reserved**
6	WO	xxh	**DeGamma for Render Target0's Reading Color** 0: Disable 1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.
5:4	WO	xxh	**Render Target0 is SRGB** 00: Gamma 1.0 field. Disable Gamma correction of writing back color. 01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer. 10: Gamme correction enabled. Use Gamma Table "HGTWC" to transform each color channel to a specific color field before written back to color buffer. 11: Reserved
3	WO	xxh	**Mask of Render Target0's Alpha Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
2	WO	xxh	**Mask of Render Target0's Red Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
1	WO	xxh	**Mask of Render Target0's Green Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
0	WO	xxh	**Mask of Render Target0's Blue Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number

HParaType = 01h, Sub-Address = 54 – 57h: Reserved (for Destination Setting – Render Target 0)

HParaType = 01h, Sub-Address = 58h
Destination Setting – Render Target 1 – Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Render Target1's Base Address** In unit of 256 bytes.

HParaType = 01h, Sub-Address = 59h
Destination Setting – Render Target 1 – Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Memory Mode of Render Target 1** 0: Linear mode 1: Tile mode
22	WO	xxh	**Render Target1's Tile is 16-Pexel high** ***<HMRT1TileH16>*** 0: Normal 8-pixel high 1: 16-pixel high
21:20	WO	xxh	**Location Setting of Render Target 1** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
19:0	WO	xxh	**Reserved**

HParaType = 01h, Sub-Address = 5Ah
Destination Setting – Render Target 1 – Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Render Target1's Format** *The definition is same as* ***Render Target0's Format.*** *Please refer to* HParaType 01h, Sub-Address 52h bits [23:16] *for details.*
15	WO	xxh	**Color Extending Mode (Excluding Alpha)** 0: Extending with high color bit 1: Extending with zero *Please refer to* HParaType 01h, Sub-Address 52h bit [15] *for details.*
14:13	WO	xxh	**Reserved**
12	WO	xxh	**Saturation of PS's Output for Render Target "M"** 0: Clamp PS's output color oCm to related render tager format's range For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0 For 16-bit floating color format: MINVALUE = 16'hFBFF, MAXVALUE = 16'h7BFF For 32-bit floating color format: MINVALUE = 32'h7F7FFFFF, MAXVALUE =32'hFF7FFFFF Clamped Value = min(MAXVALUE, max(oCm, MINVALUE)) Note if oCm is "NAN", clamped value is MINVALUE 1: oCm doesn't clamp
11:10	WO	xxh	**Reserved**
9:0	WO	xxh	**Render Target1's Pitch** In unit of 32 bytes for linear mode. In unit of tile (256 bytes or 512 bytes depend on HMRT1TileH16) for tile mode.

HParaType = 01h, Sub-Address = 5Bh

Destination Setting – Render Target 1 – Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Render Target1's Y Inverse for Dither** 0: Not inverse 1: Inverse
22:21	WO	xxh	**Render Target1's Y Bias for Dither**
20	WO	xxh	**Render Target1's X Inverse for Dither** 0: Not inverse 1: Inverse
19:18	WO	xxh	**Render Target1's X Bias for Dither**
17	WO	xxh	**Reserved**
16:15	WO	xxh	**Render Target1's Dither Mode** 00: Dither Table with multiplied by (2^n – 1) 10: Rounding with multiplied by (2^n – 1) 01: Dither Table without multiplied by (2^n – 1) 11: Rounding without multiplied by (2^n – 1)
14:12	WO	xxh	**Reserved**
11:8	WO	xxh	**Render Target1's Raster Operation** 0000: BLACK 0 0001: NOT_MERGE_PEN DPon 0010: MASK_NOT_PEN DPna 0011: NOT_COPY_PEN Pn 0100: MASK_PEN_NOT PDna 0101: NOT Dn 0110: XOR_PEN DPx 0111: NOT_MASK_PEN DPan 1000: MASK_PEN DPa 1001: NOT_XOR_PEN DPxn 1010: NOP D 1011: MERGE_NOT_PEN DPno 1100: COPY_PEN P 1101: MERGE_PEN_NOT PDno 1110: MERGE_PEN DPo 1111: WHITE 1
7	WO	xxh	**Reserved**
6	WO	xxh	**DeGamma for Render Target1's Reading Color** 0: Disable 1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.
5:4	WO	xxh	**Render Target1 is SRGB** 00: Gamma 1.0 field. Disable Gamma correction of writing back color 01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer 10: Gamme correction enabled. Use Gamma Table "HGTWC" to transform each color channel to a specific color field before written back to color buffer 11: Reserved
3	WO	xxh	**Mask of Render Target1's Alpha Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
2	WO	xxh	**Mask of Render Target1's Red Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
1	WO	xxh	**Mask of Render Target1's Green Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
0	WO	xxh	**Mask of Render Target1's Blue Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number

HParaType = 01h, Sub-Address = 5C-5Fh: Reserved (for Destination Setting – Render Target 1)

HParaType = 01h, Sub-Address = 60h
Destination Setting – Render Target 2 – Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Render Target2's Base Address** In unit of 256 bytes.

HParaType = 01h, Sub-Address = 61h
Destination Setting – Render Target 2 – Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Memory Mode of Render Target 2** 0: Linear mode 1: Tile mode
22	WO	xxh	**Render Target2's Tile is 16-pexel high** ***<HMRT2TileH16>*** 0: Normal 8-pixel high 1: 16-pixel high
21:20	WO	xxh	**Location Setting of Render Target 2** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
19:0	WO	xxh	**Reserved**

HParaType = 01h, Sub-Address = 62h
Destination Setting – Render Target 2 – Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Render Target2's Format** *The definition is same as* ***Render Target0's Format.*** *Please refer to* HParaType 01h, Sub-Address 52h bits [23:16] *for details.*
15	WO	xxh	**Color Extending Mode (Excluding Alpha)** 0: Extending with high color bit 1: Extending with zero *Please refer to* HParaType 01h, Sub-Address 52h bit [15] *for details.*
14:13	WO	xxh	**Reserved**
12	WO	xxh	**Saturation of PS's Output for Render Target "M"** 0: Clamp PS's output color oCm to related render tager format's range For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0 For 16-bit floating color format: MINVALUE = 16'hFBFF, MAXVALUE = 16'h7BFF For 32-bit floating color format: MINVALUE = 32'h7F7FFFFF, MAXVALUE =32'hFF7FFFFF Clamped Value = min(MAXVALUE, max(oCm, MINVALUE)) Note if oCm is "NAN", clamped value is MINVALUE 1: oCm doesn't clamp
11:10	WO	xxh	**Reserved**
9:0	WO	xxh	**Render Target2's Pitch** In unit of 32 bytes for linear mode. In unit of tile (256 bytes or 512 byte depend on HMRT2TileH16) for tile mode.

HParaType = 01h, Sub-Address = 63h

Destination Setting – Render Target 2 – Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Render Target2's Y Inverse for Dither** 0: Not inverse 1: Inverse
22:21	WO	xxh	**Render Target2's Y Bias for Dither**
20	WO	xxh	**Render Target2's X Inverse for Dither** 0: Not inverse 1: Inverse
19:18	WO	xxh	**Render Target2's X Bias for Dither**
17	WO	xxh	**Reserved**
16:15	WO	xxh	**Render Target2's Dither Mode** 00: Dither Table with multiplied by (2^n – 1) 10: Rounding with multiplied by (2^n – 1) 01: Dither Table without multiplied by (2^n – 1) 11: Rounding without multiplied by (2^n – 1)
14:12	WO	xxh	**Reserved**
11:8	WO	xxh	**Render Target2's Raster Operation** 0000: BLACK 0 0001: NOT_MERGE_PEN DPon 0010: MASK_NOT_PEN DPna 0011: NOT_COPY_PEN Pn 0100: MASK_PEN_NOT PDna 0101: NOT Dn 0110: XOR_PEN DPx 0111: NOT_MASK_PEN DPan 1000: MASK_PEN DPa 1001: NOT_XOR_PEN DPxn 1010: NOP D 1011: MERGE_NOT_PEN DPno 1100: COPY_PEN P 1101: MERGE_PEN_NOT PDno 1110: MERGE_PEN DPo 1111: WHITE 1
7	WO	xxh	**Reserved**
6	WO	xxh	**DeGamma for Render Target2's Reading Color** 0: Disable 1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.
5:4	WO	xxh	**Render Target2 is SRGB** 00: Gamma 1.0 field. Disable Gamma correction of writing back color 01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer 10: Gamme correction enabled. Use Gamma Table "HGTWC" to transform each color channel to a specific color field before written back to color buffer 11: Reserved
3	WO	xxh	**Mask of Render Target2's Alpha Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
2	WO	xxh	**Mask of Render Target2's Red Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
1	WO	xxh	**Mask of Render Target2's Green Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
0	WO	xxh	**Mask of Render Target2's Blue Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number

HParaType = 01h, Sub-Address = 64-67h: Reserved (for Destination Setting – Render Target 2)

HParaType = 01h, Sub-Address = 68h
Destination Setting – Render Target 3 – Setting 1

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Render Target3's Base Address** In unit of 256 bytes.

HParaType = 01h, Sub-Address = 69h
Destination Setting – Render Target 3 – Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Memory Mode of Render Target 3** 0: Linear mode 1: Tile mode
22	WO	xxh	**Render Target3's Tile is 16-pexel high** ***<HMRT3TileH16>*** 0: Normal 8-pixel high 1: 16-pixel high
21:20	WO	xxh	**Location Setting of Render Target 3** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
19:0	WO	xxh	**Reserved**

HParaType = 01h, Sub-Address = 6Ah
Destination Setting – Render Target 3 – Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Render Target3's Format** *The definition is same as* ***Render Target0's Format.*** *Please refer to* HParaType 01h, Sub-Address 52h bits [23:16] *for details.*
15	WO	xxh	**Color Extending Mode (Excluding Alpha)** 0: Extending with high color bit 1: Extending with zero *Please refer to* HParaType 01h, Sub-Address 52h bit [15] *for details.*
14:13	WO	xxh	**Reserved**
12	WO	xxh	**Saturation of PS's Output for Render Target "M"** 0: Clamp PS's output color oCm to related render tager format's range. For format ARGB and Luminance: MINVALUE = 0.0, MAXVALUE = 1.0 For 16-bit floating color format: MINVALUE = 16'hFBFF, MAXVALUE = 16'h7BFF For 32-bit floating color format: MINVALUE = 32'h7F7FFFFF, MAXVALUE =32'hFF7FFFFF Clamped Value = min(MAXVALUE, max(oCm, MINVALUE)) Note if oCm is "NAN", clamped value is MINVALUE 1: oCm doesn't clamp
11:10	WO	xxh	**Reserved**
9:0	WO	xxh	**Render Target3's Pitch** In unit of 32 bytes for linear mode. In unit of tile (256 bytes or 512 bytes depend on HMRT3TileH16) for tile mode.

HParaType = 01h, Sub-Address = 6Bh

Destination Setting – Render Target 3 – Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Render Target3's Y Inverse for Dither** 0: Not inverse 1: Inverse
22:21	WO	xxh	**Render Target3's Y Bias for Dither**
20	WO	xxh	**Render Target3's X Inverse for Dither** 0: Not inverse 1: Inverse
19:18	WO	xxh	**Render Target3's X Bias for Dither**
17	WO	xxh	**Reserved**
16:15	WO	xxh	**Render Target3's Dither Mode** 00: Dither Table with multiplied by (2^n – 1) 10: Rounding with multiplied by (2^n – 1) 01: Dither Table without multiplied by (2^n – 1) 11: Rounding without multiplied by (2^n – 1)
14:12	WO	xxh	**Reserved**
11:8	WO	xxh	**Render Target3's Raster Operation** 0000: BLACK 0 0001: NOT_MERGE_PEN DPon 0010: MASK_NOT_PEN DPna 0011: NOT_COPY_PEN Pn 0100: MASK_PEN_NOT PDna 0101: NOT Dn 0110: XOR_PEN DPx 0111: NOT_MASK_PEN DPan 1000: MASK_PEN DPa 1001: NOT_XOR_PEN DPxn 1010: NOP D 1011: MERGE_NOT_PEN DPno 1100: COPY_PEN P 1101: MERGE_PEN_NOT PDno 1110: MERGE_PEN DPo 1111: WHITE 1
7	WO	xxh	**Reserved**
6	WO	xxh	**DeGamma for Render Target3's Reading Color** 0: Disable 1: Enable. Use one-by-one mapping to deGamma the readen color from 2.2 to 1.0 color field before alpha blending operation.
5:4	WO	xxh	**Render Target3 is SRGB** 00: Gamma 1.0 field. Disable Gamma correction of writing back color 01: Gamma correction enabled. Use one-by-one mapping to transform the color to gamma 2.2 field before written back to color buffer 10: Gamme correction enabled. Use Gamma Table "HGTWC" to transform each color channel to a specific color field before written back to color buffer 11: Reserved
3	WO	xxh	**Mask of Render Target3's Alpha Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
2	WO	xxh	**Mask of Render Target3's Red Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
1	WO	xxh	**Mask of Render Target3's Green Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number
0	WO	xxh	**Mask of Render Target3's Blue Channel** 0: The relative data bit will remain the same in Frame Buffer 1: The relative data bit will be updated by a new calculated number

HParaType = 01h, Sub-Address = 6C-6Fh: Reserved (for Destination Setting – Render Target 3)

HParaType = 01h, Sub-Address = 70h
Fog Setting 1

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7	WO	xxh	**Fog Factor Sourec From PS** 0: Fog factor is generated in PE (Including vertex, linear or exponential Fog) 1: Fog factor and Fog operation is dealt by the PS Instead of 8-bit fixed Fog factor, PE sends "Fog coordinate" with format floating s[7].10 to PS. ***Note: When this bit is set, HenFOGRT0, HenFOGRT1, HenFOGMRT2 and HenFOGMRT3 should be disabled.***
6	WO	xxh	**Linear Fog Calculation Factor Setting 2 *<HFogLF2>*** 0: Use W or Z to calculate linear Fog by setting of bit 4 1: Use attributre "Fog" as fog coordinate to calculate linear Fog If (HFogLF2 == 1) // this bit Use Fog attribute to calculate linear fog or exponential fog (fog per pixel) Else if (HFogLF == 0) // bit 4 Use Z attribute to calculate linear fog or exponential fog (fog per pixel) Else Use W attribute to calculate linear fog or exponential fog (fog per pixel)
5	WO	xxh	**Fog Factor from Spectra Color's Alpha** 0: Individual Fog attribute 1: Use Spectral (Color 2) Alpha as Fog factor
4	WO	xxh	**Linear Fog Calculation Factor Setting *<HFogLF>*** 0: Use W to calculate linear Fog 1: Use Z to calculate linear Fog
3	WO	xxh	**Fog Equation** 0: Use Fog equation 0: Cout = f * (Cin + Csepc) + (1-f) * HCFog 1: Use Fog equation 1: Cout = (1-f) * (Cin + Cspec) + f * HCFog
2:0	WO	xxh	**Fog Mode** When substituting for vertex Z, Z is calculated in PS (HZSrcPS = 1), linear or non-linear Fog from Z is not allowed. 000: Local Fog 001: Reserved (Global Fog) 010: Linear Fog 011: Reserved 100: Exponential Fog 101: Exponential_2 Fog 11x: Reserved *Note: Setting of 1xx: is for Non-linear Fog (Use Fog Table).*

HParaType = 01h, Sub-Address = 71h
Fog Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**G of HCFogCL** Positive fixed-point from 0 to 1.0
11	WO	xxh	**Reserved**
10:0	WO	xxh	**G of HCFogCL** Positive fixed-point from 0 to 1.0

HParaType = 01h, Sub-Address = 72h
Fog Setting 3

Bits [23:0]	Attribute	Default	Description
23:11	WO	xxh	**Reserved**
10:0	WO	xxh	**R of Fog Color** Positive fixed-point from 0 to 1.0

HParaType = 01h, Sub-Address = 73h
Fog Setting 4

Bits [23:0]	Attribute	Default	Description
23:15	WO	xxh	**Reserved**
14:0	WO	xxh	**Fog Start** Floating-point is used to calculate Fog factor. The format is floating-point [8].7.

HParaType = 01h, Sub-Address = 74h
Fog Setting 5

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Reserved**

HParaType = 01h, Sub-Address = 75h
Fog Setting 6

Bits [23:0]	Attribute	Default	Description
23:4	WO	xxh	**Reserved**
3:0	WO	xxh	**Mantissa Part of the One Over (Fog End - Fog Start)** ***<HFogOOdMF>*** Note: The leading one is not included.

HParaType = 01h, Sub-Address = 76h
Fog Setting 7

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Exponential Part of the One Over (Fog End - Fog Start)** ***<HFogOOdEF>*** Format is IEEE's floating presentation. The value of 1/(Fog End – Fog Start) is (1.HfogOOdMF[1:0] * 2^(HfogOOdEF – 127)) .

HParaType = 01h, Sub-Address = 77h
Fog Setting 8

Bits [23:0]	Attribute	Default	Description
23:15	WO	xxh	**Reserved**
14:0	WO	xxh	**Lower 3 Bytes of Fog End** ***<HFogEnd>*** The format of HFogEnd is floating-point [8].7.

HParaType = 01h, Sub-Address = 78h
Fog Setting 9

Bits [23:0]	Attribute	Default	Description
23:21	WO	xxh	**Reserved**
20:8	WO	xxh	**Fog Density with Positive Floating Format [8].5.**
7:0	WO	xxh	**Reserved**

HParaType = 01h, Sub-Address = 79-7Fh: Reserved (for Fog Setting)

HParaType = 01h, Sub-Address = 80h
Miscellaneous Setting 1

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	**Color Window Top Clipping Value in the Range of 0 to 2048**
11:0	WO	xxh	**Color Window Bottom Clipping Value in the Range of 0 to 2048**

HParaType = 01h, Sub-Address = 81h
Miscellaneous Setting 2

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	**Color Window Left Clipping Value in the Range of 0 to 2048**
11:0	WO	xxh	**Color Window RightClipping Value in the Range of 0 to 2048**

HParaType = 01h, Sub-Address = 82h
Miscellaneous Setting 3

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	**Scissor Window Top Clipping Value in the Range of 0 to 2048**
11:0	WO	xxh	**Scissor Window Bottom Clipping Value in the Range of 0 to 2048**

HParaType = 01h, Sub-Address = 83h
Miscellaneous Setting 4

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	**Scissor Window Left Clipping Value in the Range of 0 to 2048**
11:0	WO	xxh	**Scissor Window Right Clipping Value in the Range of 0 to 2048**

HParaType = 01h, Sub-Address = 84h
Miscellaneous Setting 5

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:0	WO	xxh	**Line Pattern** The Line Pattern bit starts from the LSB.

HParaType = 01h, Sub-Address = 85h
Miscellaneous Setting 6

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Line Pattern Reset** Hardware would reset related repeat counter automatically whenever this register is set to "1". It is NOT necessary for driver to clear this bit. Hardware would clear it after the counter reset.
22:16	WO	xxh	**Reserved**
15:0	WO	xxh	**Line Pattern Repeat Factor** This number denotes how many times that a line pattern bit will be used for several line pixels.

HParaType = 01h, Sub-Address = 86h
Miscellaneous Setting 7 - Lower 3 Bytes of Solid Shading Color *<HSolidCL>*

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**R of Solid Shading Color**
15:8	WO	xxh	**G of Solid Shading Color**
7:0	WO	xxh	**B of Solid Shading Color**

HParaType = 01h, Sub-Address = 87h
Miscellaneous Setting 8 - Highest Byte of Solid Shading Color *<HSolidCH>*

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Alpha of Solid Shading Color**

HParaType = 01h, Sub-Address = 88h
Miscellaneous Setting 9

Bits [23:0]	Attribute	Default	Description
23:13	WO	xxh	**Reserved**
12:0	WO	xxh	**Guard Band Window Left Clipping Value** Format as s12 2'scomplement

HParaType = 01h, Sub-Address = 89h
Miscellaneous Setting 10

Bits [23:0]	Attribute	Default	Description
23:13	WO	xxh	**Reserved**
12:0	WO	xxh	**Guard Band Window Right Clipping Value** Format as s12 2'scomplement

HParaType = 01h, Sub-Address = 8Ah
Miscellaneous Setting 11

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Enhance TX's Precision During PE's Rendering** 0: Disable 1: Enable
22:17	WO	xxh	**Reserved**
16	WO	xxh	**Zero Round Mode for the Texture Coordinate from PE to PS** 0: Round to zero 1: Round to 0^+
15:4	WO	xxh	**Bottom Y Value for PS's Location Register** *<HYB4LocationReg>* As 12 positive integer
3	WO	xxh	**Enable HYB4LocationReg** HYB4LocationReg is defined in bits [15:4]. 0: Disable 1: Enable If ((HPSLocationReg == true) // T01A90[19] and this bit is set) LocationReg.Y = floating(HYB4LocationReg – PEY) ElseLocationReg.Y = floating(PEY)
2	WO	xxh	**PreModulate Color 0 (Diffuse Color) with Ws** 0: Not pre-modulated; multiply C0 and Ws in SE 1: Pre-modulated; **don't** multiply C0 and Ws in WS
1	WO	xxh	**PreModulate Color 1 (Specula Color) with Ws** 0: Not pre-modulated; multiply C1 and Ws in SE 1: Pre-modulated; **don't** multiply C1 and Ws in WS

0	WO	xxh	**PreModulate Fog with Ws** 0: Not pre-modulated; multiply Fog and Ws in SE 1: Pre-modulated; **don't** multiply Fog and Ws in WS
23:0	WO	xxh	**Reserved**

HParaType = 01h, Sub-Address = 8B-8Fh: Reserved (for Miscellaneous Setting)

HParaType = 01h, Sub-Address = 90h

Pixel Shader Setting 1

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Disable the Funtion of Detecting "ALUOut" by Hardware PS** 0: PS would detect the "ALUOut" automaticly 1: "ALUOut" set by software PS code
22	WO	xxh	**Software Sets the HPSDPNTAU_N** 0: Hardware judges dependant TAU instruction by (HPSINAtoT[127:0] != 128'h0 | HPSFIREALU) 1: Software sets HPSDPNTAU_N (bit 21) and hardware followed
21	WO	xxh	**TAU Execute Dependant Instruction Control** *<HPSDPNTAU_N>* 0: There is dependant TAU instruction 1: No dependant TAU instruction
20	WO	xxh	**TAU Excutes Dependant TXKILL Instruction Control** 0: TAU would excute dependant TXKILL instruction 1: TAU would not excute dependant TXKILL instruction Example of "dependant TXKILL" *Example 1* txld r0, t0, s0 ← load texture for CVALID | STVALID mad t1, r0, xx, xx txkill t1 ← effect both CVALID and STVALID Note to SW Driver: Whenever there is any "dependant TXKILL", please keep this register "false". Only WITHOUT any "depandant TXKILL", set "HPSDPNTXkill_N" to "true". For "independand" PS code, "dependant TXKILL" must not exist thus HPSDPNTXkill_N" had better to be set for performance issue.
19	WO	xxh	**Pixel Shader Gets Location Register (X, Y, Z, 1/W) from PE** ***<HPSLocationReg>*** 0: No location Register used in PS 1: Location Register used in PS
18	WO	0	**Pixel Shader Fired by ALU Instruction Initially <*HPSFireALU*>** 0: Disable *(Default)* 1: Enable
17	WO	xxh	**The Contents of PS's Constant Registers with Index 32 to 54 Are the Same as the Contents in Index from 0 to 22** 0: Filled independently 1: Fill the same value to n and (n+32)
16:15	WO	xxh	**Pixel Shader Configure** 00: Normal configure. There are 16 texture registers and 12 temporary registers used for each pixel. 01: Double configure. There are 8 texture registers and 6 temporary registers used for each pixel. 10: Tripple configure. There are 5 texture registers and 4 temporary registers used for each pixel. 11: 4-Time configure. There are 4 texture registers and 3 temporary registers used for each pixel.
14	WO	xxh	**Texture Register 14(t14) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
13	WO	xxh	**Texture Register 13(t13) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
12	WO	xxh	**Texture Register 12(t12) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
11	WO	xxh	**Texture Register 11(t11) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
10	WO	xxh	**Texture Register 10(t10) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
9	WO	xxh	**Texture Register 9(t9) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
8	WO	xxh	**Texture Register 8(t8) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)

7	WO	xxh	**Texture Register 7(t7) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
6	WO	xxh	**Texture Register 6(t6) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
5	WO	xxh	**Texture Register 5(t5) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
4	WO	xxh	**Texture Register 4(t4) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
3	WO	xxh	**Texture Register 3(t3) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
2	WO	xxh	**Texture Register 2(t2) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
1	WO	xxh	**Texture Register 1(t1) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
0	WO	xxh	**Texture Register 0(t0) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)

HParaType = 01h, Sub-Address = 91h

Pixel Shader Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Texture Register 15(t15) As the Input to ALU** 0: None 1: For ALU (Arithmetic unit)
22:16	WO	xxh	**Reserved**
15	WO	xxh	**Texture Register 15(t15) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
14	WO	xxh	**Texture Register 14(t14) As the Input to TAU** 0: None 1: For TAU(Texture address unit)
13	WO	xxh	**Texture Register 13(t13) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
12	WO	xxh	**Texture Register 12(t12) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
11	WO	xxh	**Texture Register 11(t11) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
10	WO	xxh	**Texture Register 10(t10) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
9	WO	xxh	**Texture Register 9(t9) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
8	WO	xxh	**Texture Register 8(t8) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
7	WO	xxh	**Texture Register 7(t7) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
6	WO	xxh	**Texture Register 6(t6) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
5	WO	xxh	**Texture Register 5(t5) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
4	WO	xxh	**Texture Register 4(t4) As the Input to TAU** 0: None 1: For TAU (Texture address unit)

3	WO	xxh	**Texture Register 3(t3) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
2	WO	xxh	**Texture Register 2(t2) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
1	WO	xxh	**Texture Register 1(t1) As the Input to TAU** 0: None 1: For TAU (Texture address unit)
0	WO	xxh	**Texture Register 0(t0) As the Input to TAU** 0: None 1: For TAU (Texture address unit)

HParaType = 01h, Sub-Address = 92h

Pixel Shader Setting 3

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**The Result of SOP' s Special Case Control** 0: The result of SOP's special case such as 1/0 or 1/√0 is "MAX" 1: The result of SOP's special case such as 1/0 or 1/√0 is "INFINITE"
22	WO	xxh	**Reserved**
21:16	WO	xxh	**Length of TAU Instruction**
15	WO	xxh	**Enable Texture Register 12-15 Swapping to Internal Register 0-3 whenever TAU-to-ALU Switches** 0: Disable 1: Enable
14	WO	xxh	**Enable Internal Register 0-3 Swapping to Texture Register 12-15 whenever ALU-to-TAU Switches** 0: Disable 1: Enable
13:9	WO	xxh	**Reserved**
8:0	WO	xxh	**Length of ALU Instruction**

HParaType = 01h, Sub-Address = 93h

Pixel Shader Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Instruction Switch from TAU to ALU after the 23rd TAU Instruction** 0: Operate next TAU instruction 1: Switch to operate ALU instruction
22	WO	xxh	**Instruction Switch from TAU to ALU after the 22ndTAU Instruction**
21	WO	xxh	**Instruction Switch from TAU to ALU after the 21st TAU Instruction**
20	WO	xxh	**Instruction Switch from TAU to ALU after the 20th TAU Instruction**
19	WO	xxh	**Instruction Switch from TAU to ALU after the 19thTAU Instruction**
18	WO	xxh	**Instruction Switch from TAU to ALU after the 18thTAU Instruction**
17	WO	xxh	**Instruction Switch from TAU to ALU after the 17thTAU Instruction**
16	WO	xxh	**Instruction Switch from TAU to ALU after the 16thTAU Instruction**
15	WO	xxh	**Instruction Switch from TAU to ALU after the 15thTAU Instruction**
14	WO	xxh	**Instruction Switch from TAU to ALU after the 14thTAU Instruction**
13	WO	xxh	**Instruction Switch from TAU to ALU after the 13thTAU Instruction**
12	WO	xxh	**Instruction Switch from TAU to ALU after the 12thTAU Instruction**
11	WO	xxh	**Instruction Switch from TAU to ALU after the 11thTAU Instruction**
10	WO	xxh	**Instruction Switch from TAU to ALU after the 10thTAU Instruction**
9	WO	xxh	**Instruction Switch from TAU to ALU after the 9thTAU Instruction**
8	WO	xxh	**Instruction Switch from TAU to ALU after the 8thTAU Instruction**
7	WO	xxh	**Instruction Switch from TAU to ALU after the 7thTAU Instruction**
6	WO	xxh	**Instruction Switch from TAU to ALU after the 6thTAU Instruction**
5	WO	xxh	**Instruction Switch from TAU to ALU after the 5thTAU Instruction**
4	WO	xxh	**Instruction Switch from TAU to ALU after the 4thTAU Instruction**
3	WO	xxh	**Instruction Switch from TAU to ALU after the 3rd TAU Instruction**
2	WO	xxh	**Instruction Switch from TAU to ALU after the 2nd TAU Instruction**
1	WO	xxh	**Instruction Switch from TAU to ALU after the 1st TAU Instruction**
0	WO	xxh	**Instruction Switch from TAU to ALU after the 0th TAU Instruction**

HParaType = 01h, Sub-Address = 94h

Pixel Shader Setting 5

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7	WO	xxh	**Instruction Switch from TAU to ALU after the 31st TAU Instruction**
6	WO	xxh	**Instruction Switch from TAU to ALU after the 30th TAU Instruction**
5	WO	xxh	**Instruction Switch from TAU to ALU after the 29th TAU Instruction**
4	WO	xxh	**Instruction Switch from TAU to ALU after the 28th TAU Instruction**
3	WO	xxh	**Instruction Switch from TAU to ALU after the 27th TAU Instruction**
2	WO	xxh	**Instruction Switch from TAU to ALU after the 26th TAU Instruction**
1	WO	xxh	**Instruction Switch from TAU to ALU after the 25th TAU Instruction**
0	WO	xxh	**Instruction Switch from TAU to ALU after the 24th TAU Instruction**

HParaType = 01h, Sub-Address = 95h

Pixel Shader Setting 6

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Instruction Switch from ALU to TAU after the 23rd ALU Instruction** 0: Operate next ALU instruction 1: Switch to operate TAU instruction
22	WO	xxh	**Instruction Switch from ALU to TAU after the 22nd ALU Instruction**
21	WO	xxh	**Instruction Switch from ALU to TAU after the 21st ALU Instruction**
20	WO	xxh	**Instruction Switch from ALU to TAU after the 20th ALU Instruction**
19	WO	xxh	**Instruction Switch from ALU to TAU after the 19th ALU Instruction**
18	WO	xxh	**Instruction Switch from ALU to TAU after the 18th ALU Instruction**
17	WO	xxh	**Instruction Switch from ALU to TAU after the 17th ALU Instruction**
16	WO	xxh	**Instruction Switch from ALU to TAU after the 16th ALU Instruction**
15	WO	xxh	**Instruction Switch from ALU to TAU after the 15th ALU Instruction**
14	WO	xxh	**Instruction Switch from ALU to TAU after the 14th ALU Instruction**
13	WO	xxh	**Instruction Switch from ALU to TAU after the 13th ALU Instruction**
12	WO	xxh	**Instruction Switch from ALU to TAU after the 12th ALU Instruction**
11	WO	xxh	**Instruction Switch from ALU to TAU after the 11th ALU Instruction**
10	WO	xxh	**Instruction Switch from ALU to TAU after the 10th ALU Instruction**
9	WO	xxh	**Instruction Switch from ALU to TAU after the 9th ALU Instruction**
8	WO	xxh	**Instruction Switch from ALU to TAU after the 8th ALU Instruction**
7	WO	xxh	**Instruction Switch from ALU to TAU after the 7th ALU Instruction**
6	WO	xxh	**Instruction Switch from ALU to TAU after the 6th ALU Instruction**
5	WO	xxh	**Instruction Switch from ALU to TAU after the 5th ALU Instruction**
4	WO	xxh	**Instruction Switch from ALU to TAU after the 4th ALU Instruction**
3	WO	xxh	**Instruction Switch from ALU to TAU after the 3rd ALU Instruction**
2	WO	xxh	**Instruction Switch from ALU to TAU after the 2nd ALU Instruction**
1	WO	xxh	**Instruction Switch from ALU to TAU after the 1st ALU Instruction**
0	WO	xxh	**Instruction Switch from ALU to TAU after the 0th ALU Instruction**

HParaType = 01h, Sub-Address = 96h

Pixel Shader Setting 7

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Instruction Switch from ALU to TAU after the 47th ALU Instruction** 0: Operate next ALU instruction 1: Switch to operate TAU instruction
22	WO	xxh	**Instruction Switch from ALU to TAU after the 46th ALU Instruction**
21	WO	xxh	**Instruction Switch from ALU to TAU after the 45th ALU Instruction**
20	WO	xxh	**Instruction Switch from ALU to TAU after the 44th ALU Instruction**
19	WO	xxh	**Instruction Switch from ALU to TAU after the 43rd ALU Instruction**
18	WO	xxh	**Instruction Switch from ALU to TAU after the 42nd ALU Instruction**
17	WO	xxh	**Instruction Switch from ALU to TAU after the 41st ALU Instruction**
16	WO	xxh	**Instruction Switch from ALU to TAU after the 40th ALU Instruction**
15	WO	xxh	**Instruction Switch from ALU to TAU after the 39th ALU Instruction**
14	WO	xxh	**Instruction Switch from ALU to TAU after the 38th ALU Instruction**
13	WO	xxh	**Instruction Switch from ALU to TAU after the 37th ALU Instruction**
12	WO	xxh	**Instruction Switch from ALU to TAU after the 36th ALU Instruction**
11	WO	xxh	**Instruction Switch from ALU to TAU after the 35th ALU Instruction**
10	WO	xxh	**Instruction Switch from ALU to TAU after the 34th ALU Instruction**
9	WO	xxh	**Instruction Switch from ALU to TAU after the 33th ALU Instruction**
8	WO	xxh	**Instruction Switch from ALU to TAU after the 32th ALU Instruction**
7	WO	xxh	**Instruction Switch from ALU to TAU after the 31st ALU Instruction**
6	WO	xxh	**Instruction Switch from ALU to TAU after the 30th ALU Instruction**
5	WO	xxh	**Instruction Switch from ALU to TAU after the 29th ALU Instruction**
4	WO	xxh	**Instruction Switch from ALU to TAU after the 28th ALU Instruction**
3	WO	xxh	**Instruction Switch from ALU to TAU after the 27th ALU Instruction**
2	WO	xxh	**Instruction Switch from ALU to TAU after the 26th ALU Instruction**
1	WO	xxh	**Instruction Switch from ALU to TAU after the 25th ALU Instruction**
0	WO	xxh	**Instruction Switch from ALU to TAU after the 24th ALU Instruction**

HParaType = 01h, Sub-Address = 97h

Pixel Shader Setting 8

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Instruction Switch from ALU to TAU after the 71st ALU Instruction** 0: Operate next ALU instruction 1: Switch to operate TAU instruction
22	WO	xxh	**Instruction Switch from ALU to TAU after the 70th ALU Instruction**
21	WO	xxh	**Instruction Switch from ALU to TAU after the 69th ALU Instruction**
20	WO	xxh	**Instruction Switch from ALU to TAU after the 68th ALU Instruction**
19	WO	xxh	**Instruction Switch from ALU to TAU after the 67th ALU Instruction**
18	WO	xxh	**Instruction Switch from ALU to TAU after the 66th ALU Instruction**
17	WO	xxh	**Instruction Switch from ALU to TAU after the 65th ALU Instruction**
16	WO	xxh	**Instruction Switch from ALU to TAU after the 64th ALU Instruction**
15	WO	xxh	**Instruction Switch from ALU to TAU after the 63rd ALU Instruction**
14	WO	xxh	**Instruction Switch from ALU to TAU after the 62nd ALU Instruction**
13	WO	xxh	**Instruction Switch from ALU to TAU after the 61st ALU Instruction**
12	WO	xxh	**Instruction Switch from ALU to TAU after the 60th ALU Instruction**
11	WO	xxh	**Instruction Switch from ALU to TAU after the 59th ALU Instruction**
10	WO	xxh	**Instruction Switch from ALU to TAU after the 58th ALU Instruction**
9	WO	xxh	**Instruction Switch from ALU to TAU after the 57th ALU Instruction**
8	WO	xxh	**Instruction Switch from ALU to TAU after the 56th ALU Instruction**
7	WO	xxh	**Instruction Switch from ALU to TAU after the 55th ALU Instruction**
6	WO	xxh	**Instruction Switch from ALU to TAU after the 54th ALU Instruction**
5	WO	xxh	**Instruction Switch from ALU to TAU after the 53rd ALU Instruction**
4	WO	xxh	**Instruction Switch from ALU to TAU after the 52nd ALU Instruction**
3	WO	xxh	**Instruction Switch from ALU to TAU after the 51st ALU Instruction**
2	WO	xxh	**Instruction Switch from ALU to TAU after the 50th ALU Instruction**
1	WO	xxh	**Instruction Switch from ALU to TAU after the 49th ALU Instruction**
0	WO	xxh	**Instruction Switch from ALU to TAU after the 48th ALU Instruction**

HParaType = 01h, Sub-Address = 98h

Pixel Shader Setting 9

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Instruction Switch from ALU to TAU after the 95th ALU Instruction** 0: Operate next ALU instruction 1: Switch to operate TAU instruction
22	WO	xxh	**Instruction Switch from ALU to TAU after the 94th ALU Instruction**
21	WO	xxh	**Instruction Switch from ALU to TAU after the 93rd ALU Instruction**
20	WO	xxh	**Instruction Switch from ALU to TAU after the 92nd ALU Instruction**
19	WO	xxh	**Instruction Switch from ALU to TAU after the 91st ALU Instruction**
18	WO	xxh	**Instruction Switch from ALU to TAU after the 90th ALU Instruction**
17	WO	xxh	**Instruction Switch from ALU to TAU after the 89th ALU Instruction**
16	WO	xxh	**Instruction Switch from ALU to TAU after the 88th ALU Instruction**
15	WO	xxh	**Instruction Switch from ALU to TAU after the 87th ALU Instruction**
14	WO	xxh	**Instruction Switch from ALU to TAU after the 86th ALU Instruction**
13	WO	xxh	**Instruction Switch from ALU to TAU after the 85th ALU Instruction**
12	WO	xxh	**Instruction Switch from ALU to TAU after the 84th ALU Instruction**
11	WO	xxh	**Instruction Switch from ALU to TAU after the 83rd ALU Instruction**
10	WO	xxh	**Instruction Switch from ALU to TAU after the 82nd ALU Instruction**
9	WO	xxh	**Instruction Switch from ALU to TAU after the 81st ALU Instruction**
8	WO	xxh	**Instruction Switch from ALU to TAU after the 80th ALU Instruction**
7	WO	xxh	**Instruction Switch from ALU to TAU after the 79th ALU Instruction**
6	WO	xxh	**Instruction Switch from ALU to TAU after the 78th ALU Instruction**
5	WO	xxh	**Instruction Switch from ALU to TAU after the 77th ALU Instruction**
4	WO	xxh	**Instruction Switch from ALU to TAU after the 76th ALU Instruction**
3	WO	xxh	**Instruction Switch from ALU to TAU after the 75th ALU Instruction**
2	WO	xxh	**Instruction Switch from ALU to TAU after the 74th ALU Instruction**
1	WO	xxh	**Instruction Switch from ALU to TAU after the 73rd ALU Instruction**
0	WO	xxh	**Instruction Switch from ALU to TAU after the 72nd ALU Instruction**

HParaType = 01h, Sub-Address = 99h

Pixel Shader Setting 10

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Instruction Switch from ALU to TAU after the 119th ALU Instruction** 0: Operate next ALU instruction 1: Switch to operate TAU instruction
22	WO	xxh	**Instruction Switch from ALU to TAU after the 118th ALU Instruction**
21	WO	xxh	**Instruction Switch from ALU to TAU after the 117th ALU Instruction**
20	WO	xxh	**Instruction Switch from ALU to TAU after the 116th ALU Instruction**
19	WO	xxh	**Instruction Switch from ALU to TAU after the 115th ALU Instruction**
18	WO	xxh	**Instruction Switch from ALU to TAU after the 114th ALU Instruction**
17	WO	xxh	**Instruction Switch from ALU to TAU after the 113rd ALU Instruction**
16	WO	xxh	**Instruction Switch from ALU to TAU after the 112nd ALU Instruction**
15	WO	xxh	**Instruction Switch from ALU to TAU after the 111st ALU Instruction**
14	WO	xxh	**Instruction Switch from ALU to TAU after the 110th ALU Instruction**
13	WO	xxh	**Instruction Switch from ALU to TAU after the 109th ALU Instruction**
12	WO	xxh	**Instruction Switch from ALU to TAU after the 108th ALU Instruction**
11	WO	xxh	**Instruction Switch from ALU to TAU after the 107th ALU Instruction**
10	WO	xxh	**Instruction Switch from ALU to TAU after the 106th ALU Instruction**
9	WO	xxh	**Instruction Switch from ALU to TAU after the 105th ALU Instruction**
8	WO	xxh	**Instruction Switch from ALU to TAU after the 104th ALU Instruction**
7	WO	xxh	**Instruction Switch from ALU to TAU after the 103rd ALU Instruction**
6	WO	xxh	**Instruction Switch from ALU to TAU after the 102nd ALU Instruction**
5	WO	xxh	**Instruction Switch from ALU to TAU after the 101st ALU Instruction**
4	WO	xxh	**Instruction Switch from ALU to TAU after the 100th ALU Instruction**
3	WO	xxh	**Instruction Switch from ALU to TAU after the 99th ALU Instruction**
2	WO	xxh	**Instruction Switch from ALU to TAU after the 98th ALU Instruction**
1	WO	xxh	**Instruction Switch from ALU to TAU after the 97th ALU Instruction**
0	WO	xxh	**Instruction Switch from ALU to TAU after the 96th ALU Instruction**

HParaType = 01h, Sub-Address = 9Ah
Pixel Shader Setting 11

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Temporary Register 15(r15)'s Initial Setting for Dstination Check Bit**
22	WO	xxh	**Temporary Register 14(r14)'s Initial Setting for Dstination Check Bit**
21	WO	xxh	**Temporary Register 13(r13)'s initial Setting for Dstination Check Bit**
20	WO	xxh	**Temporary Register 12(r12)'s initial Setting for Dstination Check Bit**
19	WO	xxh	**Temporary Register 11(r11)'s initial Setting for Dstination Check Bit**
18	WO	xxh	**Temporary Register 10(r10)'s initial Setting for Dstination Check Bit**
17	WO	xxh	**Temporary Register 9(r9)'s Initial Setting for Dstination Check Bit**
16	WO	xxh	**Temporary Register 8(r8)'s Initial Setting for Dstination Check Bit**
15	WO	xxh	**Temporary Register 7(r7)'s Initial Setting for Dstination Check Bit**
14	WO	xxh	**Temporary Register 6(r6)'s Initial Setting for Dstination Check Bit**
13	WO	xxh	**Temporary Register 5(r5)'s Initial Setting for Dstination Check Bit**
12	WO	xxh	**Temporary Register 4(r4)'s Initial Setting for Dstination Check Bit**
11	WO	xxh	**Temporary Register 3(r3)'s Initial Setting for Dstination Check Bit**
10	WO	xxh	**Temporary Register 2(r2)'s Initial Setting for Dstination Check Bit**
9	WO	xxh	**Temporary Register 1(r1)'s Initial Setting for Dstination Check Bit**
8	WO	xxh	**Temporary Register 0(r0)'s Initial Setting for Dstination Check Bit** 0: It is **not** necessary to check r0's valid bit whenever used as ALU's destination at the 1st ime. 1: It is necessary to check r0's valid bit whenever used as ALU's destination at the 1st time. Note to Driver: Define HPSRnDstChk for PS's temporary register n. The default value is "0". If some temporary register is as both TAU and ALU's destination when 1st used, the HPSRnDstChk must be set as "1". Hardware would check r#'s valid bit to see if data from "txld" is valid or not before the ALU instruction which uses r# as "partial" destination. Here are some examples. txld r0, t0; mov r0.a c0.a; …… or txld r0, t0; txld r1, t1; mov r2, r1 mov r0.a, c0.a: …… The HPSR0DstChk must be set as "1" by driver. It is very, very important, wrong setting would lead to wrong result.
7	WO	xxh	**Instruction Switch from ALU to TAU after the 127th ALU Instruction** 0: Operate next ALU instruction 1: Switch to operate TAU instruction
6	WO	xxh	**Instruction Switch from ALU to TAU after the 126th ALU Instruction**
5	WO	xxh	**Instruction Switch from ALU to TAU after the 125th ALU Instruction**
4	WO	xxh	**Instruction Switch from ALU to TAU after the 124th ALU Instruction**
3	WO	xxh	**Instruction Switch from ALU to TAU after the 123rd ALU Instruction**
2	WO	xxh	**Instruction Switch from ALU to TAU after the 122nd ALU Instruction**
1	WO	xxh	**Instruction Switch from ALU to TAU after the 121st ALU Instruction**
0	WO	xxh	**Instruction Switch from ALU to TAU after the 120th ALU Instruction**

HParaType = 01h, Sub-Address = AAh
Software Inspection

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:0	WO	xxh	**Flag Number for Software Inspection**

HParaType 02h: Attribute of Texture Stage N (HParaSubType: 00-0Fh)

The register table in this section is used for following HParaSubTypes (from 00h to 0Fh).

- HParaSubType = 0000 0000 (00h) -- For Texture 0
- HParaSubType = 0000 0001 (01h) -- For Texture 1
- HParaSubType = 0000 0010 (02h) -- For Texture 2
- HParaSubType = 0000 0011 (03h) -- For Texture 3
- HParaSubType = 0000 0100 (04h) -- For Texture 4
- HParaSubType = 0000 0101 (05h) -- For Texture 5
- HParaSubType = 0000 0110 (06h) -- For Texture 6
- HParaSubType = 0000 0111 (07h) -- For Texture 7
- HParaSubType = 0000 1000 (08h) -- For Texture 8
- HParaSubType = 0000 1001 (09h) -- For Texture 9
- HParaSubType = 0000 1010 (0Ah) -- For Texture A
- HParaSubType = 0000 1011 (0Bh) -- For Texture B
- HParaSubType = 0000 1100 (0Ch) -- For Texture C
- HParaSubType = 0000 1101 (0Dh) -- For Texture D
- HParaSubType = 0000 1110 (0Eh) -- For Texture E
- HParaSubType = 0000 1111 (0Fh) -- For Texture F

Sub-Address (Bits [31:24]): 00-51h

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 00h
Face 0 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Face 0's Level 0 Base Address** This is A31 to A8 in unit of 256 bytes.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 01h
Face 1 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Face 1's Level 0 Base Address** This is A31 to A8 in unit of 256 bytes.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 02h
Face 2 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Face 2's Level 0 Base Address** This is A31 to A8 in unit of 256 bytes. Program it back to 0.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 03h
Face 3 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Face 3's Level 0 Base Address** This is A31 to A8 in unit of 256 bytes.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 04h
Face 4 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Face 4's Level 0 Base Address** This is A31 to A8 in unit of 256 bytes.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 05h

Face 5 Level 0 Base Address

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Face 5's Level 0 Base Address in unit of 256 bytes** This is A31 to A8.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 06-17h: Reserved

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 18h

Texture Control 1

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Force Miss for Texture n's Texture Cache Hit Detection** 0: Detect hit or miss normally 1: Always force to miss
22:18	WO	xxh	**Reserved**
17:16	WO	xxh	**Texture Location of Face0** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
15:14	WO	xxh	**Texture Location of Face0** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
13	WO	xxh	**Reserved**
12	WO	xxh	**Base Address Mode for Texture Sample N** 0: HTXSnLmOffset is not offset related to Level 0, but an independent Base Address of Level m. 1: This mode is for cubic texture and planner mode texture Base Address of Level m = HTXSnFfL0Bas + HTXSnLmOffset
11:8	WO	xxh	**Mode of Texture N** 0000: Reserved 0001: 2 Dimension, both S and T coordinates. 0010: 3 Dimension volume texture. S, T, R coordinates. 0011: Cube texture 1xxx: Projection texture Others: Reserved
7:6	WO	xxh	**Texture Location of Face0** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
5:4	WO	xxh	**Texture Location of Face2 or Cr Buffer for Y-Cb-Cr Format** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
3:2	WO	xxh	**Texture Location of Face1, Cb Buffer for Y-Cb-Cr Format, or Crb Buffer for Y-Crb Format** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
1:0	WO	xxh	**Texture Location of Face0 or Y Buffer for Y-Cb-Cr or Y-Crb Format** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved ***The procedure to determine the location of accessed texture:*** Consider fetch the texture with level "l" of texture stage "n"'s face "f" If (HTXnBaseMode == 1 | HTXnPower2 == 1) {// with offset mode for the base address LOC = HTXnFfLOC } else {// with base mode for the base address If ("l" == 0) { LOC = HTXnF0LOC

```
    } else if ( “l” <= 7 ) {
        LOC = HTXnLlLOC
    } else {// “l” == 8,9,10 or 11
        LOC = HTXnL8LOC
    }
}
```

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 19-1Fh: Reserved (Texture Control)

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 20h
Texture Control 2

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	**Height of Texture Level 0** The height of each level is calculated from HTXSnL0H Height at Level “l” = HTXSnL0H >> l. Maximum is 2048.
11:0	WO	xxh	**Width of Texture Level 0** The Width of each level is calculated from HTXSnL0W Width at Level “l” = HTXSnL0W >> l. Maximum is 2048.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 21h
Texture Control 3

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	**Reserved**
11:0	WO	xxh	**Length of Texture Level 0, Maximum to 2048 (for 3D Volume Texture‘s R Axis)** The Length of each level is calculated from HTXSnL0L Length at Level “l” = HTXSnL0L >> l, but NO MIP for 3D volume texture.

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 22h
Texture Control 4

Bits [23:0]	Attribute	Default	Description
23:18	WO	xxh	**Reserved**
17	WO	xxh	**Memory Mode of Texture N** 0: Linear mode 1: Tile mode
16	WO	xxh	**Texture N’s Tile Is 16-texel High** 0: Normal 8-texel high 1: 16-texel high
15	WO	xxh	**Texture N‘s Width and Height Are Both Power of 2** 0: Non-power of 2 texture 1: Power of 2 texture
14:12	WO	xxh	**Reserved**
11:8	WO	xxh	**Exponential of Length of Texture N Level 0** Maximum is up to 11(2^11).
7:4	WO	xxh	**Exponential of Height of Texture N Level 0** Maximum is up to 11(2^11).
3:0	WO	xxh	**Exponential of Width of Texture N Level 0** Maximum is up to 11(2^11).

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 23-2Fh: Reserved (Texture Control)

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 30h

Texture Control 5

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Texture Format** **Bit [23:19]:** 00000: Reserved 00001: Intensity format R, G, B <= I A <= 1.0 00010: Luminance format R, G, B <= L A <= 1.0 or A 00011: Alpha format R, G, B <= 0.0 A <= A 00100: Reserved 00101: Compressed fexture 00110: YUV (Video texture) format 00111: Format for BumpMaping 11111-01000: Reserved 10000: Reserved 10001: ARGB_16bpp format 10010: Reserved 10011: ARGB_32bpp format 10100: Reserved 10101: ABGR_16bpp format 10110: Reserved 10111: ABGR_32bpp format 11000: Reserved 11001: RGBA_16bpp format 11010: Reserved 11011: RGBA_32bpp format 11100: BGRA_16bpp format 11101: BGRA_32bpp format 11110: Floating Color format 11111: Scale (Said Z format or only one component) ***If there is NO Alpha channel in the defined format, fill 1.0 as Alpha value.*** **Bit [18:16]:** ***For Intensity Format:*** 000: Reserved 001: Reserved 010: T4 (Bits [3:0] = T) 011: T8 (Bits [7:0] = T) 1xx: Reserved ***For Luminance Format:*** 000: Reserved 001: Reserved 010: L4 (Bits [3:0] = L) 011: L8 (Bits [7:0] = L) 100: AL44 (Bits [7:4] = A, Bits [3:0] = L) 101: AL88 (Bits [15:8] = A, Bits [7:0] = L) 110: L16 (Bits [15:0] = L) For L16 Format: A = 1.0f R = G = B = float (L/65536) // if (L = FFFFh) R = G = B = 1.0 // else fill “0” into mantissa 111: Reserved ***For Alpha Format:*** 000: Reserved 001: Reserved 010: A4 (Bits [3:0] = A) 011: A8 (Bits [7:0] = A) R = G = B = 0.0 1xx: Reserved

For Compressed Format:
000: Reserved
001: DXT1, 16-bpp format
010: DXT2, DXT3, 4-bit Alpha format
011: DXT4, DXT5, 3-bit Alpha format
100-101: Reserved
The G8R8_G8B8 can be defined by set as YUV format's package mode and set HTXnYUV2RGBmode to RGB mode

For YUV format (Video Texture):
000: Package mode (Bits [31:24] = V or Cr, Bits [23:16] = Y1, Bits [15:8] = U or Cb, Bits [7:0] = Y0) A = 1.0
001: AYUV (Bits [31:24] = A, Bits [23:16] = Y, Bits [15:8] = U, Bits [7:0] = V)
010: IA44 (Bits [7:4] = I as a 16 entries index to get a Y(R)8U(G)8V(B)8 texel, Bits [3:0] = A. A does not come from palette)
011: AI44 (Bits [7:4] = A. A does not come from palette, Bits [3:0] = I as a 16 entries index to get a Y(R)8U(G)8V(B)8 texel)
100-101: Reserved
111: V410 mode (Bits [31:22] = V or Cr, Bits [21:12] = Y, Bits [11:2] = U or Cb) A = 1.0

For BumpMapping Format (Reserved):
000: VU88 (Bits [15:8] = dV, Bits [7:0] = dU)
001: LVU655 (Bits [15:10] = L, Bits [9:5] = dV, Bits [4:0] = dU)
010: LVU888 (Bits [23:16] = L, Bits [15:8] = dV, Bits [7:0] = dU)
011: QWUV8888 (Bits [31:24] = dQ, Bits [23:16] = dW, Bits [15:8] = dV, Bits [7:0] = dU)
100: VU16 (Bits [31:16] = dV, Bits [15:0] = dU)
101: AWVU2_10_10_10 (Bits [31:30] = A, Bits [29:20] = dW, Bits [19:10] = dV, Bits [9:0] = dU)
110: CVUx88 Reserved
111: Reserved

For ARGB_16bpp Format:
000: RGB555 (Bits [14:10] = R, Bits [9:5] = G, Bits [4:0] = B)
001: RGB565 (Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B) A = 1.0
010: ARGB1555 (Bit [15] = A, Bits [14:10] = R, Bits [9:5] = G, Bits [4:0] = B)
011: ARGB4444 (Bits [15:12] = A, Bits [11:8] = R, Bits [7:4] = G, Bits [3:0] = B)
100: Reserved
101: RGB565 for write color, Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B
But for read color, Bits [15:11] = R, Bits [10:6] = G, Bits [4:0] = B, A = 1.0
11x: Reserved

For ARGB_32bpp Format:
000: ARGB0888 (Bits [23:16] = R, Bits [15:8] = G, Bits [7:0] = B)
001: ARGB8888 (Bits [31:24] = A, Bits [23:16] = R, Bits [15:8] = G, Bits [7:0] = B) A = 1.0
010: ARGB2_10_10_10 (Bits [31:30] = A, Bits [29:20] = R, Bits [19:10] = G, Bits [9:0] = B)
011-111: Reserved

For ABGR_16bpp Format:
000: BGR555 (Bits [14:10] = B, Bits [9:5] = G, Bits [4:0] = R)
001: BGR565 (Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R) A = 1.0
010: ABGR1555 (Bits [15] = A, Bit [14:10] = B, Bits [9:5] = G, Bits [4:0] = R)
011: ABGR4444 (Bits [15:12] = A, Bits [11:8] = B, Bits [7:4] = G, Bits [3:0] = R)
100: Reserved
101: BGR565 for write color: Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R.
But for read color: Bits [15:11] = B, Bits [10:6] = G, Bits [4:0] = R, A = 1.0
11x: Reserved

For ABGR_32bpp Format:
000: ABGR0888 (Bits [23:16] = B, Bits [15:8] = G, Bits [7:0] = R) A = 1.0.
001: ABGR8888 (Bit [31:24] = A, Bits [23:16] = B, Bits [15:8] = G, Bits [7:0] = R)
010: ABGR2_10_10_10 (Bits [31:30] = A, Bits [29:20] = B, Bits [19:10] = G, Bits [9:0] = R)
011: G16R16 (Bits [31:16] = G, Bits [15:0] = R) for this format, A = B = 1.0f, G and R are transformed to s[7].16
1xx: Reserved

For RGBA_16bpp Format:
000: RGB555 (Bits [15:11] = R, Bits [10:6] = G, Bits [5:1] = B)
001: RGB565 (Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B) A = 1.0
010: RGBA1555 (Bits [15:11] = R, Bits [10:6] = G, Bits [5:1] = B, Bit [0] = A)
011: RGBA4444 (Bits [15:12] = R, Bits [11:8] = G, Bits [7:4] = B, Bits [3:0] = A)
100: Reserved
101: RGB565 for write color: Bits [15:11] = R, Bits [10:5] = G, Bits [4:0] = B
But for read color: Bits [15:11] = R, Bits [10:6] = G, Bits [4:0] = B, A = 1.0
11x: Reserved

For RGBA_32bpp Format:

			000: RGBA8880 (Bits [31:24] = R, Bits [23:16] = G, Bits [15:8] = B) A = 1.0 001: RGBA8888 (Bits [31:24] = R, Bits [23:16] = G, Bits [15:8] = B, Bits [7:0] = A) 010: RGBA10_10_10_2 (Bits [31:22] = R, Bits [21:12] = G, Bits [11:2] = B, Bits [1:0] = R) 011-111: Reserved ***For ABGR_16bpp Format:*** 000: BGR555 (Bits [15:11] = B, Bits [10:6] = G, Bits [5:1] = R) A = 1.0 001: BGR565 (Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R) A = 1.0 010: BGRA1555 (Bits [15:11] = B, Bits [10:6] = G, Bits [5:1] = R, Bit [0] = A) 011: BGRA4444 (Bits [15:12] = B, Bits [11:8] = G, Bits [7:4] = R, Bits [3:0] = A) 100: Reserved 101: BGR565 for write color: Bits [15:11] = B, Bits [10:5] = G, Bits [4:0] = R. But for read color: Bits [15:11] = B, Bits [10:6] = G, Bits [4:0] = R, A = 1.0 11x: Reserved ***For BGRA_32bpp Format:*** 000: BGRA8880 (Bits [31:24] = B, Bits [23:16] = G, Bits [15:8] = R), A = 1.0 001: BGRA8888 (Bits [31:24] = B, Bits [23:16] = G, Bits [15:8] = R, Bits [7:0] = R) 010: BGRA10_10_10_2 (Bits [31:22] = B, Bits [21:12] = G, Bits [11:2] = R, Bits [1:0] = R) 011-11: Reserved ***For Floating Color Format (Filter not supported):*** 000: R16F (Bits [15:0] = R) s[5].10 A = G = B = 1.0f, and R is extended to s[7].16 with "0" . 100: G16FR16F (Bits [31:16] = G, Bits [15:0] = R) s[5].10 A = B = 1.0f, R and G are extended to s[7].16 with "0" 101: R32F (Bits [31:0] = R) s[8].23 A = G = B = 1.0f, and R is clamped to s[7].16(saturation) 111: Reserved ***For Z Format:*** 000: 16-bit fixed-point format, 0.0 ≤ Z < 1.0 001: 16-bit floating format s[5].10 from +2^63*1.FFFF to –2^63*1.FFFF. <**Only Nearest*> 010-011: Reserved 100: 32-bit fixed-point format, 0.0 ≤ Z < 1.0. <**Only Nearest*> 101: 32-bit floating format s[8].23. <**Only Nearest*> 110: 24-bit fixed-point format Z, 0.0 ≤ Z < 1.0, and Stencil. <**Only Nearest*> Z is located in D[31:8], Stencil is located in D[7:0] 111: Reserved
15	WO	xxh	**Texture Color Extending Mode (Excluding Alpha)** For Alpha channel, always extend it with high color bit. For YUV format (video texture) and when HTXnYUV2RGBmode set as 0, always extend it with zero. 0: Extending with high color bit
14	WO	xxh	**Inverse the Texel Order in One Byte for Those Texture with 1bpp, 2bpp or 3bpp** 0: Normal Consider Index 1: Bit [7] for tex[8n+7], bit [6] for tex[8n+6]……..bit [0] for tex[8n] Consider Index 2: Bits [7:6] for tex[4n+3], bits [5:4] for tex[4n+2]……..bits [1:0] for tex[4n] Consider Index 4: Bits [7:4] for tex[2n+1], bits [3:0] for tex[2n] 1: Inverse Consider Index 1: Bit [7] for tex[8n], bit [6] for tex[8n+1]……..bit [0] for tex[8n+7] Consider Index 2: Bits [7:6] for tex[4n], bits [5:4] for tex[4n+1]……..bits [1:0] for tex[4n+3] Consider Index 4: Bits [7:4] for tex[2n], bits [3:0] for tex[2n+1]

13:11	WO	xxh	**Mode for Z (Depth) Format Texture** 000: D3D Mode R = 0.0 G = Z B = 0.0 A = 1.0 010: Luminnance mode R = Z G = Z B = Z A = 1.0 100: Intensity mode R = Z G = Z B = Z A = Z 110: Alpha mode R = 0.0 G = 0.0 B = 0.0 A = Z Note to OpenGL Driver: For Depth texture's border color, please set the R, G, B, A component to HTXSnTBR, HTXSnTBG, HTXSnTBB and HTXSnTBA separately. Although ICD defines the 1st component of texture border color as the "Depth" value, HW would just adopts HTXSnTBR, HTXSnTBG, HTXSnTBB and HTXSnTBA, not matter what the HTXnMode's setting is.
10:9	WO	xxh	**Reserved**
8	WO	xxh	**Texture Is as sRGB (Non-gamma 1.0).** The deGamma correction is necessary for deGamma table "HDGTRTX". DeGamma correction is only used to R, G and B component. Any color format cauld be deGammaed just after the filtering (& color space conversation). 0: Disable DeGamma 1: Enable DeGamma
7:2	WO	xxh	**Reserved**
1:0	WO	xxh	**Video Texture Is as BT601(SDTV), BT709(HDTV) or Just RGB** 00: RGB For this format, consider the 8-bit Y as positive 8-bit G, 8-bit U as positive 8-bit R, and 8-bit V as positive 8-bit B. Then extend them to s1.10 according to setting of HTXnCExtend. Then filter the texels. For this setting, YUV2RGB transform is not done in format decoder module or YUV2RGB transformed implemented by PS. 01: BT601(SDTV) R = clip (round (((Y – 16)*1.164383 + (V – 128)*1.596027)*256/255)) G = clip (round (((Y – 16)*1.164383 – (U – 128)*0.391762) – (V – 128)*0.812968))*256/255)) B = clip (round (((Y – 16)*1.164838 + (U – 128)*2.017232)*256/255)) 10: BT709(HDTV) R = clip (round (((Y – 16)*1.164383 – (U – 128)*0.0002) + (V – 128)*1.7927)*256/255)) G = clip (round (((Y – 16)*1.164383 – (U – 128)*0.2132) – (V – 128)*0.5329))*256/255)) B = clip (round (((Y – 16)*1.164838 + (U – 128)*2.2114) – (V – 128)*0.0001))*256/255)) 11: Table For 8-bit YUV *R = clip (round ((Y*A + U*B1 + V *C1 + D)*256/255))* *G = clip (round ((Y*A + U*B2 + V *C2 + D)*256/255))* *B = clip (round ((Y*A + U*B3 + V *C3 + D)*256/255))* For 10-bit YUV *R = clip (round ((Y*A + U*B1 + V *C1 + D)*1024/1023))* *G = clip (round ((Y*A + U*B2 + V *C2 + D)*1024/1023))* *B = clip (round ((Y*A + U*B3 + V *C3 + D)*1024/1023))*

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 50h

Software Inspection for Texture N – 1st Flag Number

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:0	WO	xxh	**Texture N's 1st Flag Number for SW inspetion**

HParaType = 02h (HParaSubType = 00h-0Fh), Sub-Address = 51h

Software Inspection for Texture N – 2nd Flag Number

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:0	WO	xxh	**Texture n's 2nd Flag Number for SW inspetion**

HParaType 02h: Attribute of Texture Sample Stage N (HParaSubType: 20-2Fh)

The register table in this section is used for the following HParaSubTypes (from 20h to 2Fh).

- HParaSubType = 0010 0000 (20h) For Texture Sample 0
- HParaSubType = 0010 0001 (21h) For Texture Sample 1
- HParaSubType = 0010 0010 (22h) For Texture Sample 2
- HParaSubType = 0010 0011 (23h) For Texture Sample 3
- HParaSubType = 0010 0100 (24h) For Texture Sample 4
- HParaSubType = 0010 0101 (25h) For Texture Sample 5
- HParaSubType = 0010 0110 (26h) For Texture Sample 6
- HParaSubType = 0010 0111 (27h) For Texture Sample 7
- HParaSubType = 0010 1000 (28h) For Texture Sample 8
- HParaSubType = 0010 1001 (29h) For Texture Sample 9
- HParaSubType = 0010 1010 (2Ah) For Texture Sample A
- HParaSubType = 0010 1011 (2Bh) For Texture Sample B
- HParaSubType = 0010 1100 (2Ch) For Texture Sample C
- HParaSubType = 0010 1101 (2Dh) For Texture Sample D
- HParaSubType = 0010 1110 (2Eh) For Texture Sample E
- HParaSubType = 0010 1111 (2Fh) For Texture Sample F

Sub-Address (Bits [31:24]): 00-51h

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 00h-2Fh: Reserved

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 30h

Texture Level Control 1

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:12	WO	xxh	**Texture Level 0 Offset** Format: 2's Complement fixed-point number with 5-bit integer and 5-bit fraction. The real Level 0 is (Texture Minimum Level + HTXnL0OS). **Bit [21:17]: 5-bit integer of Texture n Level 0** **Bit [16:12]: 5-bit fraction of Texture n Level 0**
11:6	WO	xxh	**Maximum Texture Level** 000000: Texture n Maximum Level = 0 000001: Texture n Maximum Level = 1 000010: Texture n Maximum Level = 2 000011: Texture n Maximum Level = 3 000100: Texture n Maximum Level = 4 000101: Texture n Maximum Level = 5 000110: Texture n Maximum Level = 6 000111: Texture n Maximum Level = 7 001000: Texture n Maximum Level = 8 001001: Texture n Maximum Level = 9 001010: Texture n Maximum Level = A 001011: Texture n Maximum Level = B Others: Reserved
5:0	WO	xxh	**Minimum Texture Level** 000000: Texture n Minimum Level = 0 000001: Texture n Minimum Level = 1 000010: Texture n Minimum Level = 2 000011: Texture n Minimum Level = 3 000100: Texture n Minimum Level = 4 000101: Texture n Minimum Level = 5 000110: Texture n Minimum Level = 6 000111: Texture n Minimum Level = 7 001000: Texture n Minimum Level = 8 001001: Texture n Minimum Level = 9 001010: Texture n Minimum Level = A 001011: Texture n Minimum Level = B Others: Reserved

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 31h
Texture Filter Control 1

Bits [23:0]	Attribute	Default	Description
23:21	WO	xxh	**Reserved**
20:16	WO	xxh	**Maximum Ratio for Anisotropy (Maximum up to 16)** 00000: Max ratio to 0 (no anisotropy) 00001: Max ratio to 1 (no anisotropy) 00010: Max ratio to 2 00011: Max ratio to 3 00100: Max ratio to 4 …… 01111: Max ratio to 15 10000: Max ratio to 16 Others: Reserved
15:13	WO	xxh	**Texture Filter Setting in S Direction for Texture Enlargement** 000: Nearest 001: Linear 010: Linear Anisotropy 011: 4x4 filter Others: Reserved
12:10	WO	xxh	**Texture Filter Setting in S Direction for Texture Shrinking** 000: Nearest 001: Linear 010: Linear Anisotropy 011: 4x4 filter Others: Reserved
9:7	WO	xxh	**Texture Filter Setting in T Direction for Texture Enlargement** 000: Nearest 001: Linear 010: Linear Anisotropy 011: 4x4 filter Others: Reserved ***HTXSnFLTe & HTXSnFLSe must be the same when Linear Anisotropy is set.***
6:4	WO	xxh	**Texture Filter Setting in T Direction For Texture Shrinking** 000: Nearest 001: Linear 010: Linear Anisotropy 011: 4x4 filter Others: Reserved **** HTXSnFLTs & HTXSnFLSs must be the same when Linear Anisotropy is set.***
3:0	WO	xxh	**Texture Filter Setting in D Direction For Texture Shrinking** 0000: Always uses Texture Level 0 0001: Nearest 0010: Linear 0011: Reserved 0100: Dither Others: Reserved

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 32h
Texture Filter Control 2 & Texture Mapping Control

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:19	WO	xxh	**Texture Filter Setting in R Direction for Texture Enlargement (Only for 3D Volume Texture)** 000: Nearest 001: Linear Others: Reserved
18:16	WO	xxh	**Texture Filter Setting in R Direction For Texture Shrinking (Only for 3D Volume Texture)** 000: Nearest 001: Linear Others: Reserved
15:12	WO	xxh	**Reserved**
11:0	WO	xxh	**Texture Mapping Mode** **Bits [11:9]: Reserved** **Bits [8:6]: R Axis Setting (for 3D Volume texture)** 000: Border Color 001: Clamp 010: Repeat 011: Mirror 110-100: Reserved 111: Mirror Once **Bits [5:3]: T Axis Setting** 000: Border Color 001: Clamp 010: Repeat 011: Mirror 110-100: Reserved 111: Mirror Once **Bits [2:0]: S Axis Setting** 000: Border Color 001: Clamp 010: Repeat 011: Mirror 110-100: Reserved 111: Mirror Once

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 33-34h: Reserved

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 35h
Texture Border Control 1

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	**Red Color or U Component of Texture Border** ***<HTXSnTBR>*** As s1.10 from –1.0 to 1.0
11:0	WO	xxh	**Green Color or Y Component of Texture Border** ***<HTXSnTBG>*** As s1.10 from –1.0 to 1.0

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 36h
Texture Border Control 2

Bits [23:0]	Attribute	Default	Description
23:12	WO	xxh	**Blue Color or V Component of Texture Border <*HTXSnTBB*>** As s1.10 from –1.0 to 1.0
11:0	WO	xxh	**Texture Border Alpha <*HTXSnTBA*>** As s1.10 from –1.0 to 1.0 ***Note for texture border color's usage:*** If any filtered texel is border color { A channel of filter output = HTXSnTBA R channel of filter output = HTXSnTBR G channel of filter output = HTXSnTBG B channel of filter output = HTXSnTBB } else if texel is border color { Use {HTXSnTBR[11:0], HTXSnTBG[11:0]} as border value with format .24 } else { If (the texel is border color) { A channel of filter input of the texel = HTXSnTBA R channel of filter input of the texel = HTXSnTBR G channel of filter input of the texel = HTXSnTBG B channel of filter input of the texel = HTXSnTBB } else { //the texel is just from the texture A channel of filter input of the texel = A after "color extending" R channel of filter input of the texel = R after "color extending" G channel of filter input of the texel = G after "color extending" B channel of filter input of the texel = B after "color extending" } } *Note for YUV format and HTXnYUV2RGBmode is SDTV or HDTV, the border color is not in RGB space any more. It must be inverse transformed to YUV space as HTXSnTBG <= Y, HTXSnTBR <= U & HTXSnTBB <= V. And the HTXSnTBG[1:0], HTXSnTBG[1:0] & HTXSnTBR[1:0] are all zero.*

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 37-40h: Reserved

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 50h
Software Inspection for Texture Sample N – 1st Flag Number

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:0	WO	xxh	**Texture Sample n's 1st Flag Number for SW Inspection**

HParaType = 02h (HParaSubType = 20h-2Fh), Sub-Address = 51h
Software Inspection for Texture Sample N – 2nd Flag Number

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
10:0	WO	xxh	**Texture Sample N's 2nd Flag Number for SW Inspection**

HParaType 02h: Attribute of Texture Stage N (HParaSubType: FEh)

The register tables in this section are used for HParaSubType (FEh).

Sub-Address (Bits [31:24]): 00-13h

HParaType = 02h (HParaSubType = FEh), Sub-Address = 00h

General Texture Attribute Control

Bits [23:0]	Attribute	Default	Description
23:8	WO	xxh	**Reserved**
7:4	WO	xxh	**Number of Texture** n: n Texture, max up to 8
3:2	WO	xxh	**Configuration of Data FIFO for Reading Texture** 00: DFIFO1 is assigned to System memory's 1st T-Arbitrator (SL) DFIFO2 is assigned to System memory's 2nd T-Arbitrator (SF) DFIFO3 is assigned to Local Memory's T-Arbitrator 01: DFIFO1 is assigned to System memory's 1st T-Arbitrator (SL) DFIFO2 is assigned to Local Memory's T-Arbitrator DFIFO3 is assigned to System memory's 2nd T-Arbitrator (SF) 10: DFIFO1 is assigned to Local Memory's T-Arbitrator DFIFO2 is assigned to System memory's 2nd T-Arbitrator (SF) DFIFO3 is assigned to System memory's 1st T-Arbitrator (SL) 11: Reserved
1	WO	xxh	**Fetch Texture 2 QWs (256 bits) or 4 QWs (512 bits) for Each Request** 0: Fetch 4 QWs (512 bits) for tiled-mode texture 1: Fetch 2 QWs (256 bits)
0	WO	xxh	**Clear Texture Cache** 0: Don't care 1: Clear texture cache

HParaType = 02h (HParaSubType = FEh), Sub-Address = 01h

Attribute of Texture 0/1/2

Texture 0 to Texture 7 are defined for Primitive Engine.

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:21	WO	xxh	**Perspective Mode of Texture 2** 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
20:18	WO	xxh	**Source of Texture 2** 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
17:16	WO	xxh	**Dimension of Texture 2** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions;.S, T, R, Q coordinates
15	WO	xxh	**Reserved**
14:13	WO	xxh	**Perspective Mode of Texture 1** 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved

12:10	WO	xxh	**Source of Texture 1** 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
9:8	WO	xxh	**Dimension of Texture 1** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions;.S, T, R, Q coordinates
7	WO	xxh	**Reserved**
6:5	WO	xxh	**Perspective Mode of Texture 0** 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
4:2	WO	xxh	**Source of Texture 0** 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
1:0	WO	xxh	**Dimension of Texture 0** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 02h

Attribute of Texture 3/4/5

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:21	WO	xxh	**Perspective Mode of Texture 5** 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
20:18	WO	xxh	**Source of Texture 5** 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
17:16	WO	xxh	**Dimension of Texture 5** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
15	WO	xxh	**Reserved**
14:13	WO	xxh	**Perspective Mode of Texture 4** 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved

12:10	WO	xxh	**Source of Texture 4** 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
9:8	WO	xxh	**Dimension of Texture 4** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7	WO	xxh	**Reserved**
6:5	WO	xxh	**Perspective Mode of Texture 3** 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
4:2	WO	xxh	**Source of Texture 3** 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
1:0	WO	xxh	**Dimension of Texture 3** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 03h

Attribute of Texture 6/7

Bits [23:0]	Attribute	Default	Description
23:19	WO	xxh	**Threshold Value for Mip-map Linear Mode** Format is positive fixed .5.
18:15	WO	xxh	**Reserved**
14:13	WO	xxh	**Perspective Mode of Texture 7** 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved
12:10	WO	xxh	**Source of Texture 7** 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
9:8	WO	xxh	**Dimension of Texture 7** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7	WO	xxh	**Reserved**
6:5	WO	xxh	**Perspective Mode of Texture 6** 00: Disable 01: Enable perspective correction 10: Enable projection and be implemented to UVD module 11: Reserved

4:2	WO	xxh	**Source of Texture 6** 000: Texture comes from Texture A 001: Texture comes from Texture B 010: Texture comes from Texture C 011: Texture comes from Texture D 100: Texture comes from Texture E 101: Texture comes from Texture F 110: Texture comes from Texture G 111: Texture comes from Texture H
1:0	WO	xxh	**Dimension of Texture 6** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 04h
Texture Coordinate Control

Bits [23:0]	Attribute	Default	Description
23:20	WO	xxh	**Exponential of Width for the Texture Coordinate Replaced by (x, y) *<HTXXYrpSTWE>*** s = x / 2^ HTXXYrpSTWE
19:16	WO	xxh	**Exponential of High for the Texture Coordinate Replaced by (x, y) *<HTXXYrpSTHE>*** t = y / 2^ HTXXYrpSTHE
15:8	WO	xxh	**Reserved**
7:0	WO	xxh	**Use Screen Coordinates (x,y) to Replace (s, t)** *The value of bit[n] is used to control the setting of coresponding Textue[n]. (ex. bit[0] for Texture 0, bit[1] for Texture 1)* 0: Normal (s,t) for Texture n 1: Use (x,y) to replace (s, t) for Texture n

HParaType = 02h (HParaSubType = FEh), Sub-Address = 05h
User Defined Clipping Planes Control - 1st/2nd Groups

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15	WO	xxh	**Enable of 2nd Group of User Defined Clipping Planes *<HTXUCP1Enable>*** 0: Disable. No user defined clipping plane or only 1 texture is used for "User defined Clipping Plane". 1: Enable. A 2nd texture is used for "User defined Clipping Plane".
14	WO	xxh	**Perspective Mode of the Texture for 2nd Group of User Defined Clipping Planes** 0: Disable 1: Enable perspective correction
13:10	WO	xxh	**Source of the Texture for 2nd Group of User Defined Clipping Planes** 0000: Texture comes from Texture A 0001: Texture comes from Texture B 0010: Texture comes from Texture C 0011: Texture comes from Texture D 0100: Texture comes from Texture E 0101: Texture comes from Texture F 0110: Texture comes from Texture G 0111: Texture comes from Texture H 1000: Texture comes from Texture I 1001: Texture comes from Texture J Others: Reserved
9:8	WO	xxh	**Dimension of the Texture for 2nd Group of User Defined Clipping Planes** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7	WO	xxh	**Enable of 1st Group of User Defined Clipping Planes *<HTXUCP0Enable>*** 0: Disable. No user defined clipping plane. 1: Enable. A texture is used for "User defined Clipping Plane".
6	WO	xxh	**Perspective Mode of the Texture for 1st Group of User Defined Clipping Planes** 0: Disable 1: Enable perspective correction

5:2	WO	xxh	**Source of the Texture for 1st Group of User Defined Clipping Planes** 0000: Texture come from Texture A 0001: Texture come from Texture B 0010: Texture come from Texture C 0011: Texture come from Texture D 0100: Texture come from Texture E 0101: Texture come from Texture F 0110: Texture come from Texture G 0111: Texture come from Texture H 1000: Texture come from Texture I 1001: Texture come from Texture J Others: Reserved
1:0	WO	xxh	**Dimension of the Texture for 1st Group of User Defined Clipping Planes** 00: 1 dsimension; only S coordinate 01: 2 dimensions; both S and T coordinate 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates *Note to Driver: It is forbidden to enable HTXUCP1Enable but disable HTXUCP0Enable.*

HParaType = 02h (HParaSubType = FEh), Sub-Address = 06-07h: Reserved

HParaType = 02h (HParaSubType = FEh), Sub-Address = 08h

Texture A-H Control 1

Texture A to Texture H is defined in Vertex Buffer.

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21	WO	xxh	**Texture S Coordinate Input Mode – for Texture B** 0: Un-normalized 1: Normalized
20	WO	xxh	**Texture T Coordinate Input Mode – for Texture B** 0: Un-normalized 1: Normalized
19	WO	xxh	**Texture R Coordinate Input Mode – for Texture B** 0: Un-normalized 1: Normalized
18	WO	xxh	**Texture Q Coordinate Input Mode – for Texture B** 0: Un-normalized 1: Normalized
17:16	WO	xxh	**Dimension of Texture B** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture. S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
15:14	WO	xxh	**Reserved**
13	WO	xxh	**Texture S Coordinate Input Mode – for Texture A** 0: Un-normalized 1: Normalized
12	WO	xxh	**Texture T Coordinate Input Mode – for Texture A** 0: Un-normalized 1: Normalized
11	WO	xxh	**Texture R Coordinate Input Mode – for Texture A** 0: Un-normalized 1: Normalized
10	WO	xxh	**Texture Q Coordinate Input Mode – for Texture A** 0: Un-normalized 1: Normalized
9:8	WO	xxh	**Dimension of Texture A** 00: 1 dimension, only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture. S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7:4	WO	xxh	**Reserved**
3:0	WO	xxh	**Number of Texture in Vertex Buffer** n: n Textures

HParaType = 02h (HParaSubType = FEh), Sub-Address = 09h

Texture A-H Control 2

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21	WO	xxh	**Texture S Coordinate Input Mode – for Texture E** 0: Un-normalized 1: Normalized
20	WO	xxh	**Texture T Coordinate Input Mode – for Texture E** 0: Un-normalized 1: Normalized
19	WO	xxh	**Texture R Coordinate Input Mode – for Texture E** 0: Un-normalized 1: Normalized
18	WO	xxh	**Texture Q Coordinate Input Mode – for Texture E** 0: Un-normalized 1: Normalized
17:16	WO	xxh	**Dimension of Texture E** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
15:14	WO	xxh	**Reserved**
13	WO	xxh	**Texture S Coordinate Input Mode – for Texture D** 0: Un-normalized 1: Normalized
12	WO	xxh	**Texture T Coordinate Input Mode – for Texture D** 0: Un-normalized 1: Normalized
11	WO	xxh	**Texture R Coordinate Input Mode – for Texture D** 0: Un-normalized 1: Normalized
10	WO	xxh	**Texture Q Coordinate Input Mode – for Texture D** 0: Un-normalized 1: Normalized
9:8	WO	xxh	**Dimension of Texture D** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7:6	WO	xxh	**Reserved**
5	WO	xxh	**Texture S Coordinate Input Mode – for Texture C** 0: Un-normalized 1: Normalized
4	WO	xxh	**Texture T Coordinate Input Mode – for Texture C** 0: Un-normalized 1: Normalized
3	WO	xxh	**Texture R Coordinate Input Mode – for Texture C** 0: Un-normalized 1: Normalized
2	WO	xxh	**Texture Q Coordinate Input Mode – for Texture C** 0: Un-normalized 1: Normalized
1:0	WO	xxh	**Dimension of Texture C** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Ah

Texture A-H Control 3

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21	WO	xxh	**Texture S Coordinate Input Mode – for Texture H** 0: Un-normalized 1: Normalized
20	WO	xxh	**Texture T Coordinate Input Mode – for Texture H** 0: Un-normalized 1: Normalized
19	WO	xxh	**Texture R Coordinate Input Mode – for Texture H** 0: Un-normalized 1: Normalized
18	WO	xxh	**Texture Q Coordinate Input Mode – for Texture H** 0: Un-normalized 1: Normalized
17:16	WO	xxh	**Dimension of Texture H** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
15:14	WO	xxh	**Reserved**
13	WO	xxh	**Texture S Coordinate Input Mode – for Texture G** 0: Un-normalized 1: Normalized
12	WO	xxh	**Texture T Coordinate Input Mode – for Texture G** 0: Un-normalized 1: Normalized
11	WO	xxh	**Texture R Coordinate Input Mode – for Texture G** 0: Un-normalized 1: Normalized
10	WO	xxh	**Texture Q Coordinate Input Mode – for Texture G** 0: Un-normalized 1: Normalized
9:8	WO	xxh	**Dimension of Texture G** 00: 1 dimension, only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7:6	WO	xxh	**Reserved**
5	WO	xxh	**Texture S Coordinate Input Mode – for Texture F** 0: Un-normalized 1: Normalized
4	WO	xxh	**Texture T Coordinate Input Mode – for Texture F** 0: Un-normalized 1: Normalized
3	WO	xxh	**Texture R Coordinate Input Mode – for Texture F** 0: Un-normalized 1: Normalized
2	WO	xxh	**Texture Q Coordinate Input Mode – for Texture F** 0: Un-normalized 1: Normalized
1:0	WO	xxh	**Dimension of Texture F** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Bh
Texture A-H Control 4

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15	WO	xxh	**Texture D Wrap Correction along S Coordinate** 0: No wrap 1: Wrap
14	WO	xxh	**Texture D Wrap Correction along T Coordinate** 0: No wrap 1: Wrap
13:12	WO	xxh	**Reserved**
11	WO	xxh	**Texture C Wrap Correction along S Coordinate** 0: No wrap 1: Wrap
10	WO	xxh	**Texture C Wrap Correction along T Coordinate** 0: No wrap 1: Wrap
9:8	WO	xxh	**Reserved**
7	WO	xxh	**Texture B Wrap Correction along S Coordinate** 0: No wrap 1: Wrap
6	WO	xxh	**Texture B Wrap Correction along T Coordinate** 0: No wrap 1: Wrap
5:4	WO	xxh	**Reserved**
3	WO	xxh	**Texture A Wrap Correction along S Coordinate** 0: No wrap 1: Wrap
2	WO	xxh	**Texture A Wrap Correction along T Coordinate** 0: No wrap 1: Wrap
1:0	WO	xxh	**Rserved**

HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Ch
Texture A-H Control 5

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15	WO	xxh	**Texture H Wrap Correction along S Coordinate** 0: No wrap 1: Wrap
14	WO	xxh	**Texture H Wrap Correction along T Coordinate** 0: No wrap 1: Wrap
13:12	WO	xxh	**Reserved**
11	WO	xxh	**Texture G Wrap Correction along S Coordinate** 0: No wrap 1: Wrap
10	WO	xxh	**Texture G Wrap Correction along T Coordinate** 0: No wrap 1: Wrap
9:8	WO	xxh	**Reserved**
7	WO	xxh	**Texture F Wrap Correction along S Coordinate** 0: No wrap 1: Wrap
6	WO	xxh	**Texture F Wrap Correction along T Coordinate** 0: No wrap 1: Wrap
5:4	WO	xxh	**Reserved**
3	WO	xxh	**Texture E Wrap Correction along S Coordinate** 0: No wrap 1: Wrap
2	WO	xxh	**Texture E Wrap Correction along T Coordinate** 0: No wrap 1: Wrap
1:0	WO	xxh	**Rserved**

HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Dh
Texture A-H Control 6

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Exponential of Modulus**
15:8	WO	xxh	**Reserved**
7	WO	xxh	**Do "Modulus of 2^HTXMODE" with Texture H's Coordinate**
6	WO	xxh	**Do "Modulus of 2^HTXMODE" with Texture G's Coordinate**
5	WO	xxh	**Do "Modulus of 2^HTXMODE" with Texture F's Coordinate**
4	WO	xxh	**Do "Modulus of 2^HTXMODE" with Texture E's Coordinate**
3	WO	xxh	**Do "Modulus of 2^HTXMODE" with Texture D's Coordinate**
2	WO	xxh	**Do "Modulus of 2^HTXMODE" with Texture C's Coordinate**
1	WO	xxh	**Do "Modulus of 2^HTXMODE" with Texture B's Coordinate**
0	WO	xxh	**Do "Modulus of 2^HTXMODE" with Texture A's Coordinate**

HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Eh
Texture I/J Control

Bits [23:0]	Attribute	Default	Description
23:14	WO	xxh	**Reserved**
13	WO	xxh	**Texture S Coordinate Input Mode – for Texture J** 0: Un-normalized 1: Normalized
12	WO	xxh	**Texture T Coordinate Input Mode – for Texture J** 0: Un-normalized 1: Normalized
11	WO	xxh	**Texture R Coordinate Input Mode – for Texture J** 0: Un-normalized 1: Normalized
10	WO	xxh	**Texture Q Coordinate Input Mode – for Texture J** 0: Un-normalized 1: Normalized
9:8	WO	xxh	**Dimension of Texture J** 00: 1 dimension; only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture. S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates
7:6	WO	xxh	**Reserved**
5	WO	xxh	**Texture S Coordinate Input Mode – for Texture I** 0: Un-normalized 1: Normalized
4	WO	xxh	**TextureT Coordinate Input Mode – for Texture I** 0: Un-normalized 1: Normalized
3	WO	xxh	**Texture R Coordinate Input Mode – for Texture I** 0: Un-normalized 1: Normalized
2	WO	xxh	**Texture Q Coordinate Input Mode – for Texture I** 0: Un-normalized 1: Normalized
1:0	WO	xxh	**Dimension of Texture I** 00: 1 dimension, only S coordinate 01: 2 dimensions; both S and T coordinates 10: 3 dimensions; volume texture; S, T, R coordinates 11: 4 dimensions; S, T, R, Q coordinates

HParaType = 02h (HParaSubType = FEh), Sub-Address = 0Fh: Reserved

HParaType = 02h (HParaSubType = FEh), Sub-Address = 10h
Coefficient Setting 1

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**YUV422 (Packet Mode) Texture Decode Mode** 0: Even texel in S direction (Ye, U_n, V_n) Odd texel in S direction (Yo, U_n, V_n) 1: Even texel in S direction (Ye, U_n, V_n) Odd texel in S direction (Yo, $(U_n + U_{n+1})/2$, $(V_n + V_{n+1})/2$) Note: If (HTXYUV422DM == true & HTXnFM == 00110 000b & (HTXSnFLSe == nearest for enlarge | HTXSnFLSs == nearest for shrink) & (odd texel in S direction) & (not the rightest texel of texture)) { Y = Yo U = $(U_n + U_{n+1})/2$ V = $(V_n + V_{n+1})/2$ } else { Y = Y U = U_n V = V_n }
22:12	WO	xxh	**Coefficient D of YUV to RGB Conversion** Format as 2's complement s2.8
11	WO	xxh	**Reserved**
10:0	WO	xxh	**Coefficient A of YUV to RGB Conversion** Format as 2's complement s2.8

HParaType = 02h (HParaSubType = FEh), Sub-Address = 11h
Coefficient Setting 2

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**Coefficient C1 of YUV to RGB Conversion** Format as 2's complement s2.8
11	WO	xxh	**Reserved**
10:0	WO	xxh	**Coefficient B1 of YUV to RGB Conversion** Format as 2's complement s2.8

HParaType = 02h (HParaSubType = FEh), Sub-Address = 12h
Coefficient Setting 3

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**Coefficient C2 of YUV to RGB Conversion** Format as 2's complement s2.8
11	WO	xxh	**Reserved**
10:0	WO	xxh	**Coefficient B2 of YUV to RGB Conversion** Format as 2's complement s2.8

HParaType = 02h (HParaSubType = FEh), Sub-Address = 13h
Coefficient Setting 4

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Reserved**
22:12	WO	xxh	**Coefficient C3 of YUV to RGB Conversion** Format as 2's complement s2.8
11	WO	xxh	**Reserved**
10:0	WO	xxh	**Coefficient B3 of YUV to RGB Conversion** Format as 2's complement s2.8

HParaType 03h: Palette (HParaSubType: 00-22h)

HParaType = 03h (HParaSubType = 00h)
Texture Palette 0

Bits	Attribute	Default	Description
31:24	WO	xxh	**Reserved**
23:16	WO	xxh	**Y of Texture Palette N Data**
15:8	WO	xxh	**U of Texture Palette N Data**
7:0	WO	xxh	**V of Texture Palette N Data**

HParaType = 03h (HParaSubType = 01h): Reserved (Texture Palette1 1)

HParaType = 03h (HParaSubType = 02h): Reserved (Texture Palette1 2)

HParaType = 03h (HParaSubType = 03h): Reserved (Texture Palette1 3)

HParaType = 03h (HParaSubType = 04h): Reserved (Texture Palette1 4)

HParaType = 03h (HParaSubType = 05h): Reserved (Texture Palette1 5)

HParaType = 03h (HParaSubType = 06h): Reserved (Texture Palette1 6)

HParaType = 03h (HParaSubType = 07h): Reserved (Texture Palette1 7)

HParaType = 03h (HParaSubType = 08-0Fh): Reserved

HParaType = 03h (HParaSubType = 10h)

Offset or Base Address of Texture from Level 1 to Level 8 for the 16 Texture Samples

Ther are 16 texture samples and each sample can be up to 8 levels, so there should be 16x8 = 128 entries.

- HParaAdr 0 → HTXS0L1Offset
- HParaAdr 1 → HTXS0L2Offset
- …….
- HParaAdr 7 → HTXS0L8Offset
- HParaAdr 8 → HTXS1L1Offset
- HParaAdr 9 → HTXS1L2Offset
- …….
- HParaAdr 15 → HTXS1L8Offset
- HParaAdr 16 → HTXS2L1Offset
- HParaAdr 17 → HTXS2L2Offset
- …….
- HParaAdr 23 → HTXS2L8Offset
- ……..
- ……..
- HParaAdr 118 → HTXSFL1Offset
- HParaAdr 119 → HTXSFL2Offset
- …….
- HParaAdr 127 → HTXSFL8Offset

To sum up, consider HTXS**n**L**m**BasOffset, its entry is (**n***8 + **m**), where **n** is from 0 to Fh, and **m** is from 1 to 8h.

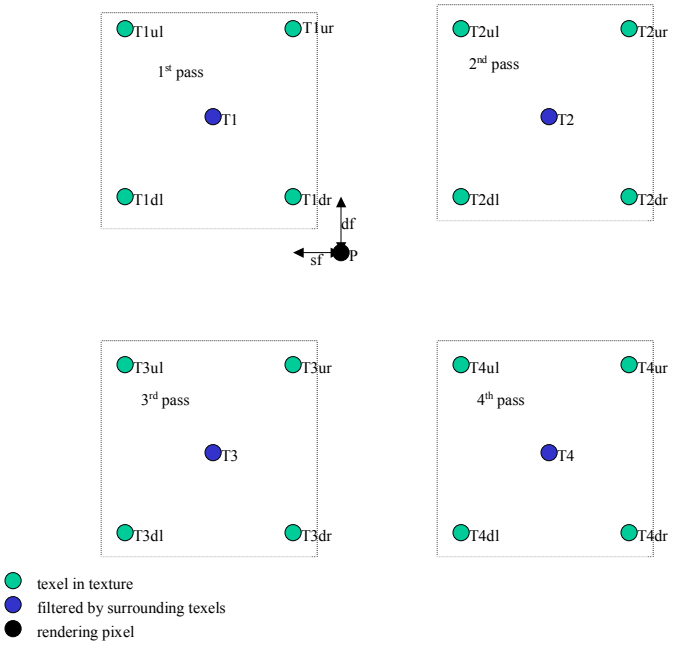
Bits	Attribute	Default	Description
31:30	WO	xxh	**Location of Texture Sample n's Level m** 00: Syntem Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved
29:24	WO	xxh	**Reserved**
23:0	WO	xxh	**Offset Related to Texture Sample n's Level 0 for Level m Base Address** In unit of byte. This must be 256-byte boundary (in unit of 256 bytes or [31:8]).

HParaType = 03h (HParaSubType = 11h)

Texture 4x4 Filter Coeffiecient Table

There are 2^5 = 32 entries. The 5-bit fraction of "sf" or "tf" is the index.

Bits	Attribute	Default	Description
31:22	WO	xxh	**Reserved**
21:16	WO	xxh	**Coefficient Cm for 4x4 Filter** Format as 1.5 positive fixed-point; maximum is 1.0.
15	WO	xxh	**Double the Coefficient Cr** 0: Crd = HTX4X4FltCrd 1: Crd = HTX4X4FltCrd << 1
14:8	WO	xxh	**Coefficient C2 for 4x4 Filter** Format as s1.5 2's complement fixed-point; maximum is 1.0 and minimum is –0.5.
7	WO	xxh	**Double the Coefficient Clu** 0: Clu = HTX4X4FltClu 1: Clu = HTX4X4FltClu << 1
6:0	WO	xxh	**Coefficient Clu for 4x4 Filter** Format as s1.5 2's complement fixed-point; maximum is 1.0 and minimum is –0.5.



Cl = HTX4X4Clu(sf) * 2^HTX4X4CluE(sf)
Cr = HTX4X4Crd(sf) * 2^HTX4X4CrdE(sf)
Csm = HTX4X4Cm(sf)
Cu = HTX4X4Clu(tf) * 2^HTX4X4CluE(tf)
Cd = HTX4X4Crd(tf) * 2^HTX4X4CrdE(tf)
Ctm = HTX4X4Cm(tf)

Cp1 = (1 – Csm)*(1 – Ctm)
Cp2 = Csm*(1 – Ctm)
Cp3 = (1 – Csm)*Ctm
Cp4 = Csm*Ctm

T1 = (1 – Cl)*(1 – Cu)*T1ul + Cl*(1 – Cu)*T1ur + (1 – Cl)*Cu*T1dl + Cl*Cu*T1dr
T2 = (1 – Cr)*(1 – Cu)*T2ul + Cr*(1 – Cu)*T2ur + (1 – Cr)*Cu*T2dl + Cr*Cu*T2dr
T3 = (1 – Cl)*(1 – Cd)*T3ul + Cl*(1 – Cd)*T3ur + (1 – Cl)*Cd*T3dl + Cl*Cd*T3dr
T4 = (1 – Cr)*(1 – Cd)*T4ul + Cr*(1 – Cd)*T4ur + (1 – Cr)*Cd*T4dl + Cr*Cd*T4dr
P = T1*Cp1 + T2*Cp2 + T3*Cp3 + T4*Cp4

HParaType = 03h (HParaSubType = 14h)
Stipple Palette

Bits	Attribute	Default	Description
31:0	WO	xxh	**32-Bit Stipple Palette Data**

HParaType = 03h (HParaSubType = 15h), HParaAdr = 00h
De-Gamma Table for Reading Texture

Bits	Attribute	Default	Description
31:30	WO	xxh	**Rounding Mode** 00: Truncate 01: Rounding 1x: Reserved
29:20	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h0C0**
19:10	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h080**
9:0	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h040**

HParaType = 03h (HParaSubType = 15h), HParaAdr = 01h
De-Gamma Table for Reading Texture

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h180**
19:10	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h140**
9:0	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h100**

HParaType = 03h (HParaSubType = 15h), HParaAdr = 02h
De-Gamma Table for Reading Texture

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h240**
19:10	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h200**
9:0	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h1C0**

HParaType = 03h (HParaSubType = 15h), HParaAdr = 03h
De-Gamma Table for Reading Texture

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h300**
19:10	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h2C0**
9:0	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h280**

HParaType = 03h (HParaSubType = 15h), HParaAdr = 04h
De-Gamma Table for Reading Texture

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h3C0**
19:10	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h380**
9:0	WO	xxh	**De-Gamma Table Value for Reading Texture at C = 10'h340**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 00h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Rounding Mode for R Channel** 00: Truncate 01: Rounding 1x: Reserved
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h001**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h001**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h001**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 01h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Rounding Mode for G Channel** 00: Truncate 01: Rounding 1x: Reserved
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h002**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h002**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h002**

ParaType = 03h (HParaSubType = 17h), HParaAdr = 02h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Rounding Mode for B Channel** 00: Truncate 01: Rounding 1x: Reserved
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h003**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h003**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h003**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 03h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31	WO	xxh	**Instead of Gamma Correction, but deGamma correction for R Channel** 0: Gamma correction 1: de-Gamma correction
30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h004**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h004**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h004**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 04h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31	WO	xxh	**Instead of Gamma Correction, but deGamma correction for G Channel** 0: Gamma correction 1: de-Gamma correction
30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h006**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h006**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h006**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 05h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31	WO	xxh	**Instead of Gamma Correction, but deGamma correction for B Channel** 0: Gamma correction 1: de-Gamma correction
30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h008**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h008**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h008**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 06h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h00C**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h00C**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h00C**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 07h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h010**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h010**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h010**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 08h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h018**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h018**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h018**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 09h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h020**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h020**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h020**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Ah
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h030**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h030**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h030**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Bh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h040**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h040**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h040**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Ch
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h050**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h050**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h050**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Dh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h060**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h060**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h060**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Eh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h070**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h070**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h070**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 0Fh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h080**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h080**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h080**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 10h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h0A0**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h0A0**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h0A0**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 11h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h0C0**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h0C0**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h0C0**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 12h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h0E0**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h0E0**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h0E0**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 13h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h100**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h100**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h100**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 14h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h140**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h140**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h140**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 15h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h180**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h180**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h180**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 16h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h1C0**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h1C0**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h1C0**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 17h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h200**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h200**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h200**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 18h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h240**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h240**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h240**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 19h
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h280**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h280**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h280**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Ah
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h2C0**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h2C0**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h2C0**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Bh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h300**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h300**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h300**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Ch
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h340**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h340**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h340**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Dh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h380**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h380**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h380**

HParaType = 03h (HParaSubType = 17h), HParaAdr = 1Eh
Gamma-de-Gamma Table for Writing Color

Bits	Attribute	Default	Description
31:30	WO	xxh	**Reserved**
29:20	WO	xxh	**Gamma Table Value for Writing R Channel at R = 10'h3C0**
19:10	WO	xxh	**Gamma Table Value for Writing G Channel at G = 10'h3C0**
9:0	WO	xxh	**Gamma Table Value for Writing B Channel at B = 10'h3C0**

HParaType = 03h (HParaSubType = 20h)
Pixel Shader ALU Instruction

Each instruction contains 4 double words. HParaAdr (4n+3) to (4n) are as the n-th instruction. Because of total 96 instructions, there are up to 96*4 (=384) entries.

Bits	Attribute	Default	Description
31:0	WO	xxh	**Pixel Shader ALU Instruction**

HParaType = 03h (HParaSubType = 21h)
Pixel Shader TAU Instruction

There are totally 32 32-bit TAU instructions.

Bits	Attribute	Default	escription
31:0	WO	xxh	**Pixel Shader TAU Instruction**

HParaType = 03h (HParaSubType = 22h)
Pixel Shader Constant Registers

Each constant register contains 4 32-bit components.
HParaAdr (4n) is as the 1st component of the n-th constant register.
HParaAdr (4n+1) is as the 2nd component of the n-th constant register.
HParaAdr (4n+2) is as the 3rd component of the n-th constant register.
HParaAdr (4n+3) is as the 4th component of the n-th constant register.
Where n is from 0 to 22, and 32 to 54.
If HPSDbCnstR is set, the n from 32 to 54 is the same as the n from 0 to 22. And HW would fill n from 32 to 54 automatly.

Bits	Attribute	Default	escription
31:0	WO	xxh	**Pixel Shader's Constant Register as Floating s[8].23** Hardware would automatically transform the 32-bit floating to 24-bit floating format.

HParaType 04h: Vertex and Primitive Setting

Sub-Address (Bits [31:24]): 00-AAh

HParaType = 04h, Sub-Address = 00h
Flexible Vertex Format 1

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Flexibility Vertex Format's (X, Y) Test Mode** 00: Disable 01: If (X or Y is "Not-a-Number) then ignore corresponded ***primitive*** 1x: If (X or Y is "Not-a-Number) then ignore corresponded ***primitive list***
21:20	WO	xxh	**Flexibility Vertex Format's Z Test Mode** 00: Disable 01: If (Z is "Not-a-Number) then ignore corresponded ***primitive*** 1x: If (Z is "Not-a-Number) then ignore corresponded ***primitive list***
19:18	WO	xxh	**Flexibility Vertex Format's W Test Mode** 00: Disable 01: If (W is "Not-a-Number) then ignore corresponded ***primitive*** 1x: If (W is "Not-a-Number) then ignore corresponded ***primitive list***
17	WO	xxh	**Switch the Flexibility Vertex Format's X to Y, and Y to X** 0: Keep 1: Switch
16:15	WO	xxh	**Location of Vertex Buffer** 00: System Local Frame Buffer (S.L.) 01: System Dynamic Frame Buffer (S.F.) 10: Reserved (System Memory) 11: Reserved Note to Driver and HW: All vertex buffers are located in LL, SF, or all in LL.
14:6	WO	xxh	**Reserved**
5:0	WO	xxh	**Length of FVF Vertex Length** In unit of 32 bits

HParaType = 04h, Sub-Address = 01h
Flexible Vertex Format 2

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 3rd FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 2nd FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 1st FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)** 00h: X 01h: Y 02h: Z 03h: W 04h: Point Size 05h: Color 0: Diffuse 06h: Color 1: Specula 07h: Fog Factor 08h: S of TextureA 09h: T of TextureA 0Ah: R of TextureA 0Bh: Q of TextureA 0Ch: S of TextureB 0Dh: T of TextureB 0Eh: R of TextureB 0Fh: Q of TextureB 10h: S of TextureC 11h: T of TextureC 12h: R of TextureC 13h: Q of TextureC 14h: S of TextureD 15h: T of TextureD 16h: R of TextureD 17h: Q of TextureD 18h: S of TextureE 19h: T of TextureE 1Ah: R of TextureE 1Bh: Q of TextureE 1Ch: S of TextureF 1Dh: T of TextureF 1Eh: R of TextureF 1Fh: Q of TextureF 20h: S of TextureG 21h: T of TextureG 22h: R of TextureG 23h: Q of TextureG 24h: S of TextureH 25h: T of TextureH 26h: R of TextureH 27h: Q of TextureH 28h: S of TextureI 29h: T of TextureI 2Ah: R of TextureI 2Bh: Q of TextureI 2Ch: S of TextureJ 2Dh: T of TextureJ 2Eh: R of TextureJ 2Fh: Q of TextureJ 30h: Reserved 31h: Back Face Color0 (BFCdiff) 32h: Back Face Color1 (BFCspec) Others: Reserved

HParaType = 04h, Sub-Address = 02h
Flexible Vertex Format 3

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 6th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 5th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 4th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 03h
Flexible Vertex Format 4

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 9th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 8th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 7th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 04h
Flexible Vertex Format 5

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 12th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 11th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 10th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 05h
Flexible Vertex Format 6

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 15th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 14th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 13th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 06h
Flexible Vertex Format 7

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 18th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 17th FVF Attribute Number (X, Y, … J, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 16th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 07h
Flexible Vertex Format 8

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 21st FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 20th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 19nd FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 08h
Flexible Vertex Format 9

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 24th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 23rd FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 22nd FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 09h
Flexible Vertex Format 10

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 27th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 26th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 25th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 0Ah
Flexible Vertex Format 11

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 30th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 29th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 28th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address 0Bh
Flexible Vertex Format 12

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 33th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 32nd FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 31st FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 0Ch
Flexible Vertex Format 13

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The36th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 35th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 34th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 0Dh
Flexible Vertex Format 14

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Reserved**
21:16	WO	xxh	**The 39th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
15:14	WO	xxh	**Reserved**
13:8	WO	xxh	**The 38th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
7:6	WO	xxh	**Reserved**
5:0	WO	xxh	**The 37th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 0Eh
Flexible Vertex Format 15

Bits [23:0]	Attribute	Default	Description
23:18	WO	xxh	**The 43rd FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
17:12	WO	xxh	**The 42nd FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
11:6	WO	xxh	**The 41st FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
5:0	WO	xxh	**The 40th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 0Fh
Flexible Vertex Format 16

Bits [23:0]	Attribute	Default	Description
23:18	WO	xxh	**The 47th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
17:12	WO	xxh	**The 46th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
11:6	WO	xxh	**The 45th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
5:0	WO	xxh	**The 44th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 10h
Flexible Vertex Format 17

Bits [23:0]	Attribute	Default	Description
23:22	WO	xxh	**Flexible Vertex Format Mask** **Bit [23]: BFCdiff Parameter Mask** 0: Primitive Vertex Parameter does not have Back Face Color0 1: Primitive Vertex Parameter has Back Face Color0 **Bit [22]: BFCspec Parameter Mask** 0: Primitive Vertex Parameter does not have Back Face Color1 1: Primitive Vertex Parameter has Back Face Color1
21:18	WO	xxh	**Reserved**
17:12	WO	xxh	**The 50th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
11:6	WO	xxh	**The 49th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**
5:0	WO	xxh	**The 48th FVF Attribute Number (X, Y, … QJ, BFCdiff, BFCspec)**

HParaType = 04h, Sub-Address = 11-1Fh: Reserved (For Flexible Vertex Format)

HParaType = 04h, Sub-Address = 20h
Vertex Buffer & Primitive Setting 1

There are totally 32 32-bit TAU instructions.

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Disable Clipping for Triangle Point (Just Near Plane)** 0: Enable 1: Disable Note to Driver: This register is only for triangle with fill mode "point". When this register enabled, there might be 2 new points resulted from near plane clipping, and their attributes (such as point size, color, texsture and so on) are interpolated from the original 3 vertices. When disabled (HenCL4TriPoint_N = 1), HW just renders the vertices inside the view volumn.
22:21	WO	xxh	**Reserved**
21:16	WO	xxh	**The Setting of Second or Even One-vertex Triangle** ***<H2nd1VT>*** **Bit [21:20]: Setting of Vertex A** This setting is used for both triangle and line rendering. 00: Vertex a is a new input 01: The Vertex a will be replaced by previous Vertex a. 10: The Vertex a will be replaced by previous Vertex b. 11: The Vertex a will be replaced by previous Vertex c. **Bit [19:18] Setting of Vertex B** This setting is used for both triangle and line rendering. 00: Vertex b is a new input 01: The Vertex b will be replaced by previous Vertex a. 10: The Vertex b will be replaced by previous Vertex b. 11: The Vertex b will be replaced by previous Vertex c. **Bit [17:16] Setting of Vertex C** This setting is used for both triangle and line rendering. 00: Vertex c is a new input 01: The Vertex c will be replaced by previous Vertex a. 10: The Vertex c will be replaced by previous Vertex b. 11: The Vertex c will be replaced by previous Vertex c.

15:8	WO	xxh	**Primitive Render Mode** 00000000: Full Vertex Cycle For Triangle Rendering, this is the 3 vertexes cycle. For Line Rendering, this is the 2 vertexes cycle. 10xxxxxx: Reserved x1xxxxxx: Automatic Fast Primitive Vertex Cycle For Triangle Rendering, this is a fast way to render 3111 Mode For Line Rendering, this is a fast way to render 2111 Mode The first or odd single vertex cycle will use the setting of bit [5:0]. The second or even single vertex cycle will use the setting of H2nd1VT. **Bit [13:12] Setting of Vertex A** This setting is used for both triangle and line rendering. 00: Vertex a is a new input 01: The Vertex a will be replaced by previous Vertex a. 10: The Vertex a will be replaced by previous Vertex b. 11: The Vertex a will be replaced by previous Vertex c. **Bit [11:10] Setting of Vertex B** This setting is used for both triangle and line rendering. 00: Vertex b is a new input 01: The Vertex b will be replaced by previous Vertex a. 10: The Vertex b will be replaced by previous Vertex b. 11: The Vertex b will be replaced by previous Vertex c. **Bit [9:8] Setting of Vertex C** This setting is used for both triangle and line rendering. 00: Vertex c is a new input 01: The Vertex c will be replaced by previous Vertex a. 10: The Vertex c will be replaced by previous Vertex b. 11: The Vertex c will be replaced by previous Vertex c.
7:2	WO	xxh	**Reserved**
1	WO	xxh	**Vertex Buffer Index Mode** 0: 16-bit index 1: 32-bit index
0	WO	xxh	**Vertex Mode** 0: Command mode Vertex 1: Index mode Vertex

HParaType = 04h, Sub-Address = 21h
Vertex Buffer & Primitive Setting 2

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Vertex Buffer Base Address**

HParaType = 04h, Sub-Address = 22h
Vertex Buffer & Primitive Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:8	WO	xxh	**Pitch of Each Vertex in Vertex Buffer**
7:0	WO	xxh	**Higher Byte of Vertex Buffer Base Address**

HParaType = 04h, Sub-Address = 23h
Vertex Buffer & Primitive Setting 4

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15	WO	xxh	**Last Pixel Control for Drawing Line** 0: Discard the last pixel of each line 1: Draw the last pixel of each line
14:12	WO	xxh	**Shading Setting** 000: Solid shading 001: Flat shading via Vertex a 010: Flat shading via Vertex b 011: Flat shading via Vertex c 100: Gouraud shading
11:9	WO	xxh	**Edge Flag** Assume the vertex transmission sequence of a triangle is a, b, then c. 000: Render NO Edge for triangle wire-frame or antialiasing 1xx: Render Edge (a, b) for triangle wire-frame or antialiasing x1x: Render Edge (b, c) for triangle wire-frame or antialiasing xx1: Render Edge (c, a) for triangle wire-frame or antialiasing
8	WO	xxh	**Back Face Mode for "Culling"** 0: If the vertex input is in the order of clockwise, it would be "culled" 1: If the vertex input is in the order of counterclockwise, it would be "culled"
7	WO	xxh	**Back Face Mode for VS's Output "oBFD#"** 0: If the vertex input is in the order of clockwise, "oBFD#" would be selected as the vertex color 1: If the vertex input is in the order of counterclockwise, "oBFD#" would be selected as the vertex color Note to Driver: Whenever the configure of VS's Output Registers contains oBD#, and HenBFCull is false, HW would select oD# or oBFD# as Color 0 and Color1. And the algorithm is as: If (HenBFCull & triangle meets HBFcae4Cull) Drop the triangle Else if ((FVFMask has Back Face Color0 | FVFMask has Back Face Color1)& triangle meet HBFcae4BFD) C0 = Back Face Color 0 C1 = Back Face Color 1 Else C0 = Color 0 C1 = Color 1
6:5	WO	xxh	**Primitive Type for Clockwise Triangle** 00: Triangle Rendering for Hen2FRender enabled and clockwise primitive 01: Reserved 10: Triangle Wire-frame Rendering for Hen2FRender enabled and clockwise primitive 11: Triangle Point Rendering for Hen2FRender enabled and clockwise primitive
4	WO	xxh	**Render Mode (PMType) Is Different for Front-Face and Back-Face Primitive** ***<Hen2FRender>*** The related PMType is "Triangle", "Triangle Wire-Frame" and "Triangle Point". 0: The PMTypes for both front-face and back-face are the same, or only one kind of face is rendered. 1: The PMType is different for front-face and back-face primitive.
3:0	WO	xxh	**Primitive Type** 0000: Point Rendering 0001: Line Rendering 0010: Triangle Rendering for "Hen2Frender" is false, or Hen2Frender enabled and counter-clockwise primitive 0011: Reserved 0100: Rectangle 0101: Reserved 0110: Triangle Wire-frame Rendering for "Hen2Frender" is false, or Hen2Frender enabled and counter-clockwise primitive 0111: Triangle Point Rendering for "Hen2Frender" is false, or Hen2Frender enabled and counter-clock-wise primitive 1xxx: Reserved

HParaType = 04h, Sub-Address = 24
Vertex Buffer & Primitive Setting 5

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Vertexes Number** n: There are n vertexes in current primitive list.

HParaType = 04h, Sub-Address = 25h
Vertex Buffer & Primitive Setting 6

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Vertexes Number** **Bit [23]: X Parameter Mask** 0: Primitive Vertex Parameter does not have X 1: Primitive Vertex Parameter has X **Bit [22]: Y Parameter Mask** 0: Primitive Vertex Parameter does not have Y 1: Primitive Vertex Parameter has Y **Bit [21]: Z Parameter Mask** 0: Primitive Vertex Parameter does not have Z 1: Primitive Vertex Parameter has Z **Bit [20]: W Parameter Mask** 0: Primitive Vertex Parameter does not have W 1: Primitive Vertex Parameter has W **Bit [19]: Point-Size Parameter Mask** 0: Primitive Vertex Parameter does not have Point-Size If the primitive type is point, use HVPointSize. 1: Primitive Vertex Parameter has Point-Size If the primitive type is point, use the value from Vertex Data. **Bit [18]: Cd(C0) Parameter Mask** 0: Primitive Vertex Parameter does not have Diffuse Color, ARGB 1: Primitive Vertex Parameter has Diffuse Color, ARGB **Bit [17]: Cs(C1) Parameter Mask** 0: Primitive Vertex Parameter does not have Specula Color, SR SG SB, and SA 1: Primitive Vertex Parameter has Specula Color, SR SG SB, and SA **Bit [16]: Fog-Factor Parameter Mask** 0: Primitive Vertex Parameter does not have Fog Factor 1: Primitive Vertex Parameter has Fog Factor **Bit [15]: Texture A's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [14]: Texture A's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [13]: Texture A's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [12]: Texture A's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [11]: Texture B's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [10]: Texture B's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [9]: Texture B's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [8]: Texture B's Q Parameter Mask**

			0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [7]: Texture C's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [6]: Texture C's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [5]: Texture C's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [4]: Texture C's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [3]: Texture D's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [2]: Texture D's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [1]: Texture D's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [0]: Texture D's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q

HParaType = 04h, Sub-Address = 26h
Vertex Buffer & Primitive Setting 7

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Flexible Vertex Format Mask** **Bit [23]: Texture I's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [22]: Texture I's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [21]: Texture I's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [20]: Texture I's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [19]: Texture J's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [18]: Texture J's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [17]: Texture J's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [16]: Texture J's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q

15:0	WO	xxh	**Flexible Vertex Format Mask** **Bit [15]: TextureE's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [14]: Texture E's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [13]: Texture E's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [12]: Texture E's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [11]: Texture F's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [10]: Texture F's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [9]: Texture F's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [8]: Texture F's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [7]: Texture G's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [6]: Texture G's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [5]: Texture G's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [4]: Texture G's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [3]: Texture H's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [2]: Texture H's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [1]: Texture H's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [0]: Texture H's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q 1: Primitive Vertex Parameter has Texture Coordinate Q

HParaType = 04h, Sub-Address = 27h
Vertex Buffer & Primitive Setting 8

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Starting Primitive Count**

HParaType = 04h, Sub-Address = 28h
Vertex Buffer & Primitive Setting 9

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Vertex Parameter Mask** *Note that the "(**)" is controlled by HVPDV_XX's Setting* **Bit [23]: X Parameter Mask** 0: Primitive Vertex Parameter does not have X thus use default value 0.0 1: Primitive Vertex Parameter has X **Bit [22]: Y Parameter Mask** 0: Primitive Vertex Parameter does not have Y thus use default value 0.0 1: Primitive Vertex Parameter has Y **Bit [21]: Z Parameter Mask** 0: Primitive Vertex Parameter does not have Z thus use default value (**) 1: Primitive Vertex Parameter has Z **Bit [20]: W Parameter Mask** 0: Primitive Vertex Parameter does not have W thus use default value (**) 1: Primitive Vertex Parameter has W **Bit [19]: Reserved** **Bit [18]: Cd (C0) Parameter Mask** 0: Primitive Vertex Parameter does not have Diffuse Color, ARGB thus use default value (**) 1: Primitive Vertex Parameter has Diffuse Color, ARGB **Bit [17]: Cs (C1) Parameter Mask** 0: Primitive Vertex Parameter does not have Specula Color, SR SG SB, and SA thus use default value (**) 1: Primitive Vertex Parameter has Specula Color, SR SG SB, and SA **Bit [16]: Fog-Factor Parameter Mask** 0: Primitive Vertex Parameter does not have Fog Factor thus use default value (**) 1: Primitive Vertex Parameter has Fog Factor **Bit [15]: Texture 0's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [14]: Texture 0's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [13]: Texture 0's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [12]: Texture 0's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [11]: Texture 1's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [10]: Texture 1's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T

			Bit [9]: Texture 1's R Parameter Mask 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [8]: Texture 1's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [7]: Texture 2's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [6]: Texture 2's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [5]:Texture 2's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [4]: Texture 2's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [3]: Texture 3's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [2]: Texture 3's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [1]: Texture 3's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [0]: Texture 3's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q

HParaType = 04h, Sub-Address = 29h
Vertex Buffer & Primitive Setting 10

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:0	WO	xxh	**Vertex Parameter Mask** *Note that the "(**)" is controlled by HVPDV_XX's Setting* **Bit [15]: Texture 4's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [14]: Texture 4's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [13]: Texture 4's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [12]: Texture 4's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [11]: Texture 5's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [10]: Texture 5's T Parameter Mask**

			0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [9]: Texture 5's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [8]: Texture 5's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [7]: Texture 6's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [6]: Texture 6's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [5]:Texture 6's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [4]: Texture 6's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q **Bit [3]: Texture 7's S Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate S thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate S **Bit [2]: Texture 7's T Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate T thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate T **Bit [1]: Texture 7's R Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate R thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate R **Bit [0]: Texture 7's Q Parameter Mask** 0: Primitive Vertex Parameter does not have Texture Coordinate Q thus use default value (**) 1: Primitive Vertex Parameter has Texture Coordinate Q

HParaType = 04h, Sub-Address = 2Ah
Vertex Buffer & Primitive Setting 11

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Point's Default Width as Floating s[8].15** When point size comes from FVF, this setting is as the maximum value of point size. Point Sprite is not only useful for 3D AP, but also for 2D and vedio AP. This can be considered as just filled a rectangle and make use of all those 3D features at the same time. The maximum value is 2048.0. The minimum value is 1.0. If (HFVFMask of "point size" is "0", and primitive type is point) Point_width = HVPointW Else Point_width = max(HVPointH, min(HVPointW, value from Primitive Vertex data's "point_size")

HParaType = 04h, Sub-Address = 2Bh
Vertex Buffer & Primitive Setting 12

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Point's Default Hight as Floating s[8].15** When point size comes from FVF, this setting is as the minimum value of point size. The maximum value is 2048.0. The minimum value is 1.0.

HParaType = 04h, Sub-Address = 2Ch
Vertex Buffer & Primitive Setting 13

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 24 Bits for Maximum Value of Vertex Buffer's Index**

HParaType = 04h, Sub-Address = 2Dh
Vertex Buffer & Primitive Setting 14

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 24 Bits for Minimum Value of Vertex Buffer's Index**

HParaType = 04h, Sub-Address = 2Eh
Vertex Buffer & Primitive Setting 15

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:8	WO	xxh	**Higher 8 Bits for Maximum Value of Vertex Buffer's Index**
7:0	WO	xxh	**Higher 8 Bits for Minimum Value of Vertex Buffer's Index** If (index of vertex > HVBIndexMax | index of vertex < HVBIndexMin) Ignore this and the followed indices

HParaType = 04h, Sub-Address = 2Fh
Vertex Buffer & Primitive Setting 16

Bits [23:0]	Attribute	Default	Description
23	WO	xxh	**Default Value for Vertex Parameter Z** 0: Default value is 0.0 1: Default value is 1.0
22	WO	xxh	**Default Value for Vertex Parameter W** 0: Default value is 0.0 1: Default value is 1.0
21	WO	xxh	**Default Value for Vertex Parameter Fog** 0: Default value is 0.0 1: Default value is 1.0
20	WO	xxh	**Default Value for Vertex Parameter Color 0** 0: Default value is 0.0 1: Default value is 1.0
19	WO	xxh	**Default Value for Vertex Parameter Alpha 0** 0: Default value is 0.0 1: Default value is 1.0
18	WO	xxh	**Default Value for Vertex Parameter Color 1** 0: Default value is 0.0 1: Default value is 1.0
17	WO	xxh	**Default Value for Vertex Parameter Alpha 1** 0: Default value is 0.0 1: Default value is 1.0
16	WO	xxh	**Default Value for Vertex Parameter Texture Coordinate S** 0: Default value is 0.0 1: Default value is 1.0
15	WO	xxh	**Default Value for Vertex Parameter Texture Coordinate T** 0: Default value is 0.0 1: Default value is 1.0
14	WO	xxh	**Default Value for Vertex Parameter Texture Coordinate R** 0: Default value is 0.0 1: Default value is 1.0
13	WO	xxh	**Default Value for Vertex Parameter Texture Coordinate Q** 0: Default value is 0.0 1: Default value is 1.0
12:10	WO	xxh	**Reserved**

9	WO	xxh	**Point Sprite Enable for Texture J** 0: Disable 1: Enable
8	WO	xxh	**Point Sprite Enable for Texture I** 0: Disable 1: Enable
7	WO	xxh	**Point Sprite Enable for Texture H** 0: Disable 1: Enable
6	WO	xxh	**Point Sprite Enable for Texture G** 0: Disable 1: Enable
5	WO	xxh	**Point Sprite Enable for Texture F** 0: Disable 1: Enable
4	WO	xxh	**Point Sprite Enable for Texture E** 0: Disable 1: Enable
3	WO	xxh	**Point Sprite Enable for Texture D** 0: Disable 1: Enable
2	WO	xxh	**Point Sprite Enable for Texture C** 0: Disable 1: Enable
1	WO	xxh	**Point Sprite Enable for Texture B** 0: Disable 1: Enable
0	WO	xxh	**Point Sprite Enable for Texture A** 0: Disable 1: Enable Note to Driver: There are 2 enable settings for Point Sprite, "HenPSprite" and "HVPenPSpriteTXn", where n is from A to J. For OpenGL, the "HVPenPSpriteTXn" are used to set point sprite for **each** texture. But for D3D, "HenPSprite" is used to set point sprite for **ALL** textures. HW would do point sprite if any one of the 2 registers is true. That is *For (n = A to J):* *If ((PMType is "point or "triangle point") & (HenPSprite | HVPenPSpriteTXn))* *Texture n is setup as "Point Sprite"*

HParaType = 04h, Sub-Address = 30-3Fh: Reserved (for Vertex Buffer & Primitive Setting)

HParaType = 04h, Sub-Address = 40h
Clipping Window to Screen Window Transformation Setting 1

All the transforming coefficients are 32-bit floating-point.

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Scaling for X Transform**

HParaType = 04h, Sub-Address = 41h
Clipping Window to Screen Window Transformation Setting 2

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Offset for X Transform**

HParaType = 04h, Sub-Address = 42h
Clipping Window to Screen Window Transformation Setting 3

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:8	WO	xxh	**Higher Byte of Offset for X Transform**
7:0	WO	xxh	**Higher Byte of Scaling for X Transform**

HParaType = 04h, Sub-Address = 43h
Clipping Window to Screen Window Transformation Setting 4

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Scaling for Y Transform**

HParaType = 04h, Sub-Address = 44h:
Clipping Window to Screen Window Transformation Setting 5

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Offset for Y Transform**

HParaType = 04h, Sub-Address = 45h
Clipping Window to Screen Window Transformation Setting 6

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:8	WO	xxh	**Higher Byte of Offset for Y Transform**
7:0	WO	xxh	**Higher Byte of Scaling for Y Transform**

HParaType = 04h, Sub-Address = 46h
Clipping Window to Screen Window Transformation Setting 7

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Scaling for Z Transform**

HParaType = 04h, Sub-Address = 47h
Clipping Window to Screen Window Transformation Setting 8

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Offset for Z Transform**

HParaType = 04h, Sub-Address = 48h
Clipping Window to Screen Window Transformation Setting 9

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**A Threshold Value For More Accurate Area Calculating** ***<HC2SXYEmax4Area >*** A threshold value of screen coordinate's Exponential part for more accurate area calculation. If any screen coordinate's expomomtial is over "HC2SXYEmax4Area", the area calculating equation would be XbYc – XbYa – XaYc – XcYb +XcYa + XaYb. And add each term in the order from absolute largest to the absolute smallest. Note to HW: The minimum value of HC2SXYEmax4Area is 19+127 (that is 2^19). HW has to check and makes adjustment as Used HC2SXYEmax4Area = max(146, decoded HC2SXYEmax4Area). Thus the original patterns won't be re-generated.
15:8	WO	xxh	**Higher Byte of Offset for Z Transform**
7:0	WO	xxh	**Higher Byte of Scaling for Z Transform**

HParaType = 04h, Sub-Address = 49-4Fh: Reserved (for Clipping Window to Screen Window Transformation Setting)

HParaType = 04h, Sub-Address = 50h
Clipping Window to Screen Window Transformation Setting 10

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Upper Clamping Value for Screen Coordinate**

HParaType = 04h, Sub-Address = 51h
Clipping Window to Screen Window Transformation Setting 11

Bits [23:0]	Attribute	Default	Description
23:0	WO	xxh	**Lower 3 Bytes of Down Clamping Value for Screen Coordinate**

HParaType = 04h, Sub-Address = 52h
Clipping Window to Screen Window Transformation Setting 12

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Maximum Exponential Value Clipped Screen Coordinate** *<HC2SXYEmax4CL>* If the clipped new vertex's screen coordinate is over ±2^ HC2SXYEmax4CL, re-generate this clipped vertex to a smaller screen coordinate.
15:8	WO	xxh	**Higher Byte of Upper Clamping Value for Screen Coordinate**
7:0	WO	xxh	**Higher Byte of Down Clamping Value for Screen Coordinate** If (Xs >= HC2SXYUClamp) Xs = HC2SXYUClamp Else if (Xs <= HC2SXYDClamp) Xs = *HC2SXYDClamp If (Ys >= HC2SXYUClamp) Ys = HC2SXYUClamp Else if (Ys <= HC2SXYDClamp) Ys = HC2SXYDClamp

HParaType = 04h, Sub-Address AAh
Software Inspection

Bits [23:0]	Attribute	Default	Description
23:16	WO	xxh	**Reserved**
15:0	WO	xxh	**Flag Number for SW Inspection**

HParaType 10h: Commands for Command Regulator

Refer to CR Chapter's "HParaType 10h: Commands for Command Regulator" for more details

HParaType 11h: Commands for Frame Buffer Swapping and CR's Miscellaneous Setting

Refer to CR Chapter's "HParaType 11h: Commands for Frame Buffer Swapping and CR's Miscellaneous Setting" for more details.