Provisional

V6377

(EPDC)

■ OUTLINE

The enhanced panel display controller (EPDC) is a high-level display controller with functions for controlling large-capacity flat panel displays (hereinafter simply "panels") and for controlling raster-scanning CRT displays. In addition, since application software written for CRTs can be used as is when the EPDC BIOS is used, portable and transportable computers with panels can be configured easily. (Display switching between CRT and panel as necessary is possible.) This EPDC is completely compatible with the IBM-PC enhanced graphics adapter (EGA). When a standard monitor is used, this compatibility requires no change to the BIOS or software whatsoever. Even if a non-standard monitor is used, compatibility can be achieved by simply setting the values of switches with the EPDC BIOS. There is no need to change the software at all. For example when an IBM monochrome monitor and 2-tone panel are used, color display software can be executed. (Monitors that can not display colors handle this with gray scaling and hatching.)

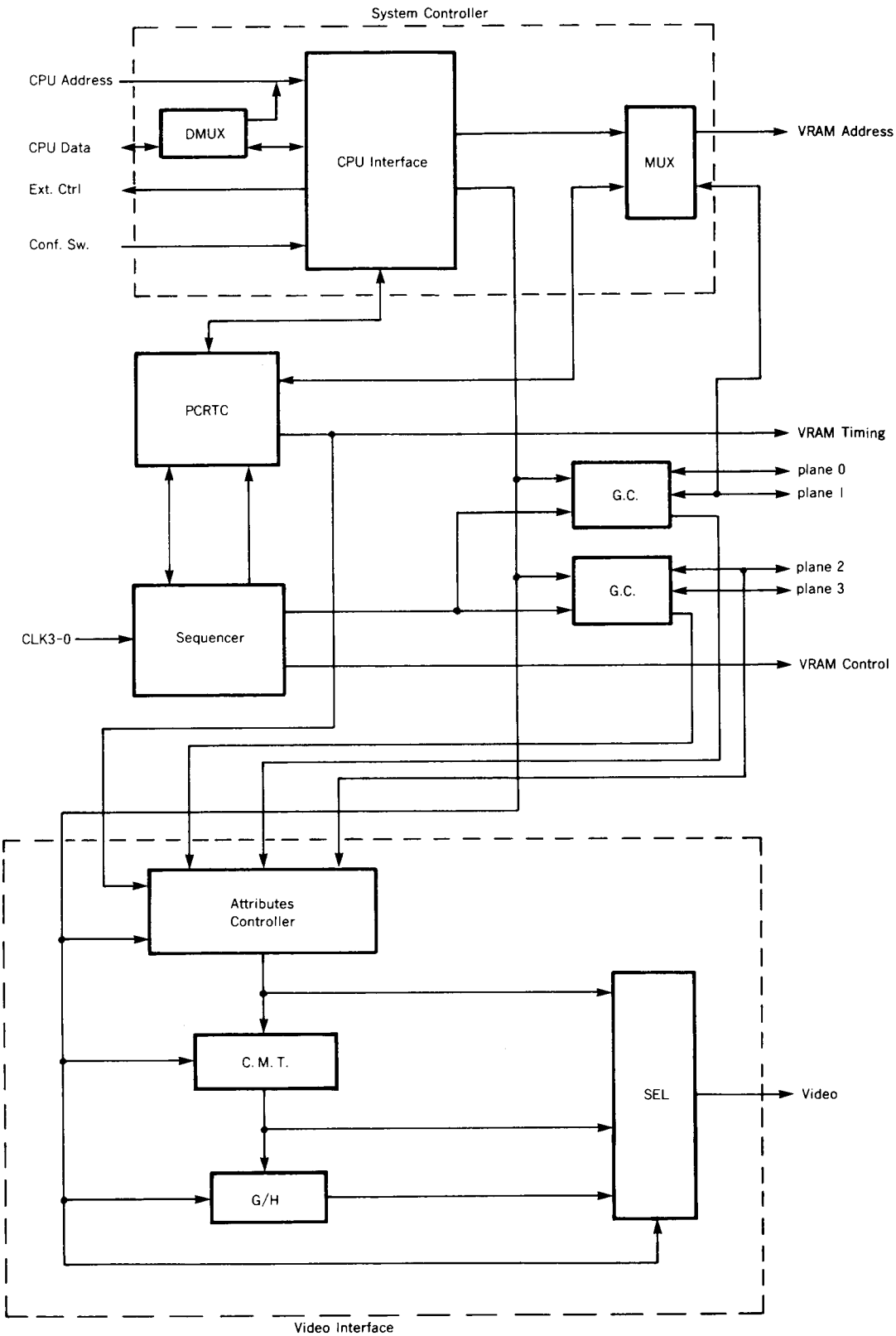
In addition to EGA display capacity, the EPDC has expanded display functions, so it can also display 640 x 480 dots. It can also be easily configured for higher level display systems, with a built-in color look-up table (LUT) for color mapping.

V6377カタログ
CATALOG No. :
1988.5

■ FEATURES

- Since IBM EGA CRT-controller functions have been included, the EGA board function is realized with few parts. Furthermore, LCDs, plasma displays, and EL displays can be controlled as well.
- The EPDC can be connected to the following CRTs:
  - · IBM monochrome display
  - · IBM color display
  - · IBM enhanced color display
  - · NEC Multisync monitor (and models from other manufacturers that have the same functions)
- The EPDC can be connected to panels (LCD, plasma, EL) with the following resolutions:
  - · 640 x 200
  - · 320 x 200
  - · 640 x 400
  - · 640 x 480
- Eight 64K x 4 dynamic RAM chips or eight 32K x 8 static RAM chips can be used for video RAM (for a maximum of 256 KB)
- Up to 16 colors can be displayed for 640 x 480 dots.
- 1-screen panels and 2-screen panels can be used.
- The duty cycle can be set as high as 1/512 when a 2-screen panel is used.
- The AC signal for the LCD panel can be set freely in units of 1Horizontal scan (with a maximum pulse width of 1024H).
- Data can be sent to the panel in parallel 4 or 8 bits at a time or serially.
- Color liquid crystal displays can be used (320 x 200 dots by 8 colors)
- 16-shade display is possible with panels and monochrome monitors. (Of these 16, 9 can be converted into 9 hatching patterns.)
- Screen display position compensation is possible when using panels the same as for CRTs (Screen center can also be adjusted).
- Multi-raster scan function (display taking into account the aspect ratio)
- Built-in look-up table (LUT) for color mapping
- CMOS, 128-pin QFP

■ BLOCK DIAGRAM



■ PIN FUNCTIONS

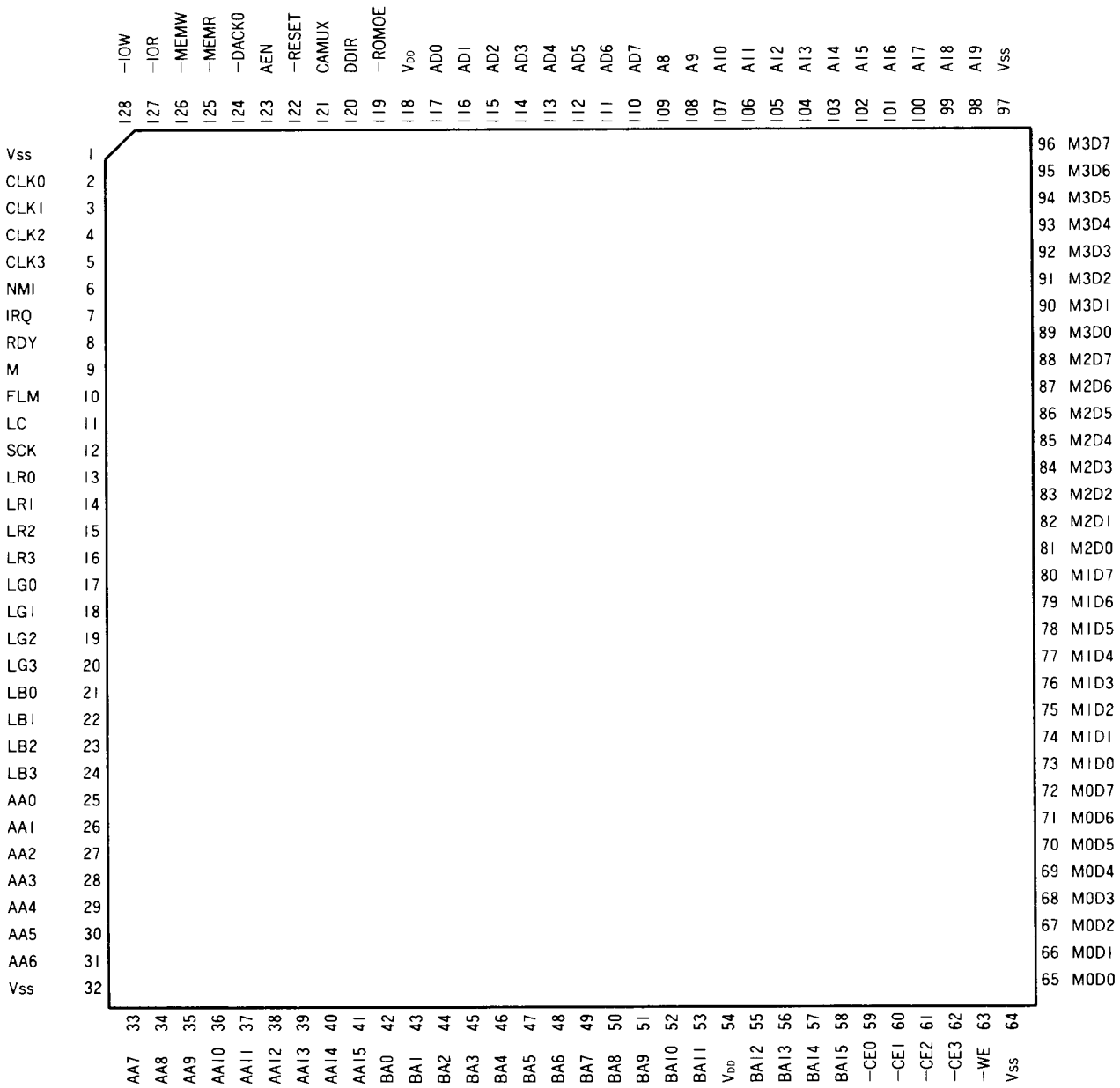
Signal	I/O	Number of pins	Pin function	
A19-8	I	12	CPU Address Bit 19-8	
AD7-0	I/O	8	CPU Address/CPU Data bit 7-0	
CAMUX	I	1	Address and data MUX signal	
DDIR	O	1	Data bus direction control	
–ROMOE	O	1	BIOS ROM read out control	
–DACK0	I	1	CPU refresh timing	
AEN	I	1	Address Enable	
–MEMR	I	1	Control for read out from memory	
–MEMW	I	1	Control for writing to memory	
–IOR	I	1	Control for read out from I/O registers	
–IOW	I	1	Control for writing to I/O registers	
RDY	O	1	Ready	
–RESET	I	1	Power On Reset	
IRQ	O	1	Interrupt Request	
NMI	O	1	Non Maskable Interrupt	
CLK3-0	I	4	Clock input (14 MHz/16 MHz/25 MHz/other)	
VDD	I	2	+5V	
VSS	I	4	Ground	CPU
LB3-0	O	4	Panel display data (blue/top screen)	
LG3-0	O	4	Panel display data (green/bottom screen)	
LR3-0	O	4	Panel display data (red)	
SCK	O	1	Panel shift clock	
LC	O	1	Panel data latch clock	
FLM	O	1	Panel scan start signal	
M	O	1	Panel AC signal	pannel
LB3	O	1	B1: secondary blue/monochrome output	
LB2	O	1	B0: primary blue output	
LB1,0	O	2	Non Connection	
LG3	O	1	G1: secondary green/intensity output	
LG2	O	1	G0: primary green output	
LG1,0	O	2	Non Connection	
LR3	O	1	R1: secondary red output	
LR2	O	1	R0: primary red output	
LR1,0	O	2	Non Connection	
LC	O	1	HSY: horizontal sync signal	
FLM	O	1	VSY: vertical sync signal	
SCK	O	1	Non Connection	
M	O	1	Non Connection	CRT

Signal	I/O	Number of pins	Pin function	
AA15-12	I/O	4	VRAM Address for Plane 0 and 1	
AA11-0	O	12	VRAM Address for Plane 0 and 1	
BA15-12	O	4	VRAM Address for Plane 2 and 3	
BA11-0	I/O	12	VRAM Address for Plane 2 and 3	
—CE3-0	O	4	VRAM Chip Enable for Plane 3-0	
—WE	O	1	VRAM Write Enable	
M0D7-0	I/O	8	VRAM Data for Plane 0	
M1D7-0	I/O	8	VRAM Data for Plane 1	
M2D7-0	I/O	8	VRAM Data for Plane 2	
M3D7-0	I/O	8	VRAM Data for Plane 3	SRAM
AA15	I/O	1	—LPENSW: light pen switch input	
AA14	I/O	1	—LPENIN: light pen optical detection strobe input	
AA13,12	I/O	2	FEAT1,0: Feature Code 1,0	
AA11-8	O	4	Non Connection	
AA7-0	O	8	VRAM Address for Plane 0 and 1	
BA15	O	1	ATRS/-L: Attribute Shift/-Load for Feature Connector	
BA14	O	1	BLANK: Blank for Feature Connector	
BA13	O	1	INTRNL: Disable Internal Video Drives	
BA12	O	1	—CAS: Column Address Strobe	
BA11,10	I/O	2	FC1,0: Feature Control bit 1,0	
BA9	I/O	1	MUX: VRAM data external latch signal	
BA8	I/O	1	CPU: signal showing the DMA in the memory cycle	
BA7-0	I/O	8	VRAM Address for Plane 2 and 3	
—CE3-0	O	4	—RAS3-0: Row Address Strobe for Plane 3-0	DRAM

For power on reset Signal

Signal	I/O	Number of pins	Pin function
BA11-8	I/O	4	Configuration switch input
BA7-0	I/O	8	Set-up switch input

■ PIN LAYOUT



■ ELECTRICAL CHARACTERISTICS

Absolute maximum ratings (with Vss = 0.0V as the standard)

Item	Code	Min.	Max.	Unit
Power supply voltage	VDD	−0.3	7.0	V
Input voltage	VI	−0.3	VDD+0.3	V
Output voltage	VO	−0.2	VDD+0.3	V
Operating ambient temperature	TOP	0	70	°C
Storage temperature	TSTG	−50	125	°C

Recommended operating conditions (with Vss = 0.0V as the standard)

Item	Code	Min.	Standard	Max.	Unit
Power supply voltage	VDD	4.75	5.00	5.25	V
Operating ambient temperature	TOP	0	25	70	°C
Low level input voltage*	VIL			0.8	V
High level input voltage*	VIH	2.0			V

*: except for clock input

Pin capacitance

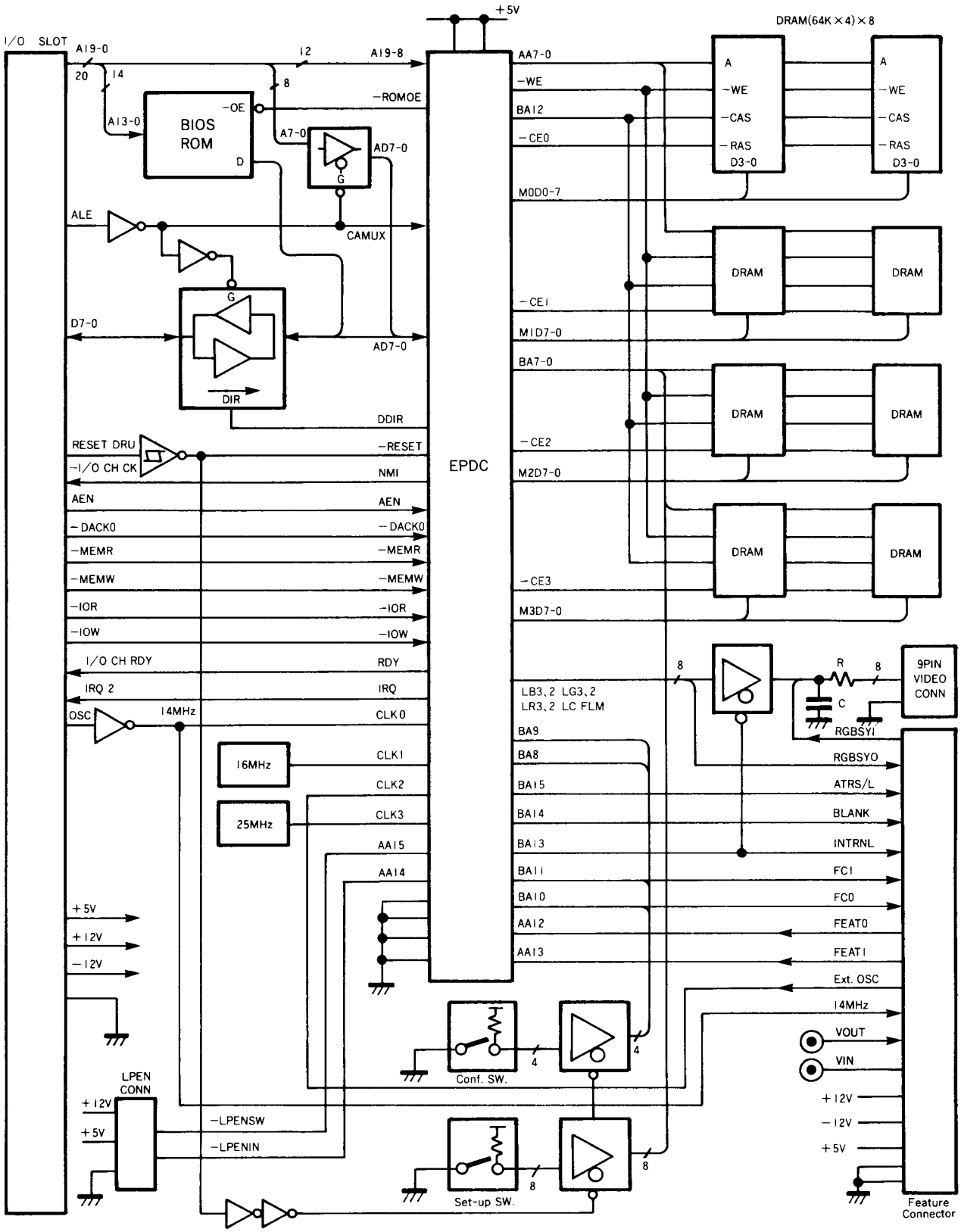
Measurement conditions: Top = 25.0°C VDD = 5.00V
VIH = 2.4Vmin. VIH = 0.8Vmax.
Input signal frequency: 1.0MHz
Except VDD and the pin being measured, perform measurement with connections made to GND.

Item	Code	Min.	Standard	Max.	Unit
Input pin capacitance	CI			8	pF
Output pin capacitance	CO			10	pF
Input/output pin capacitance	CIO			12	pF

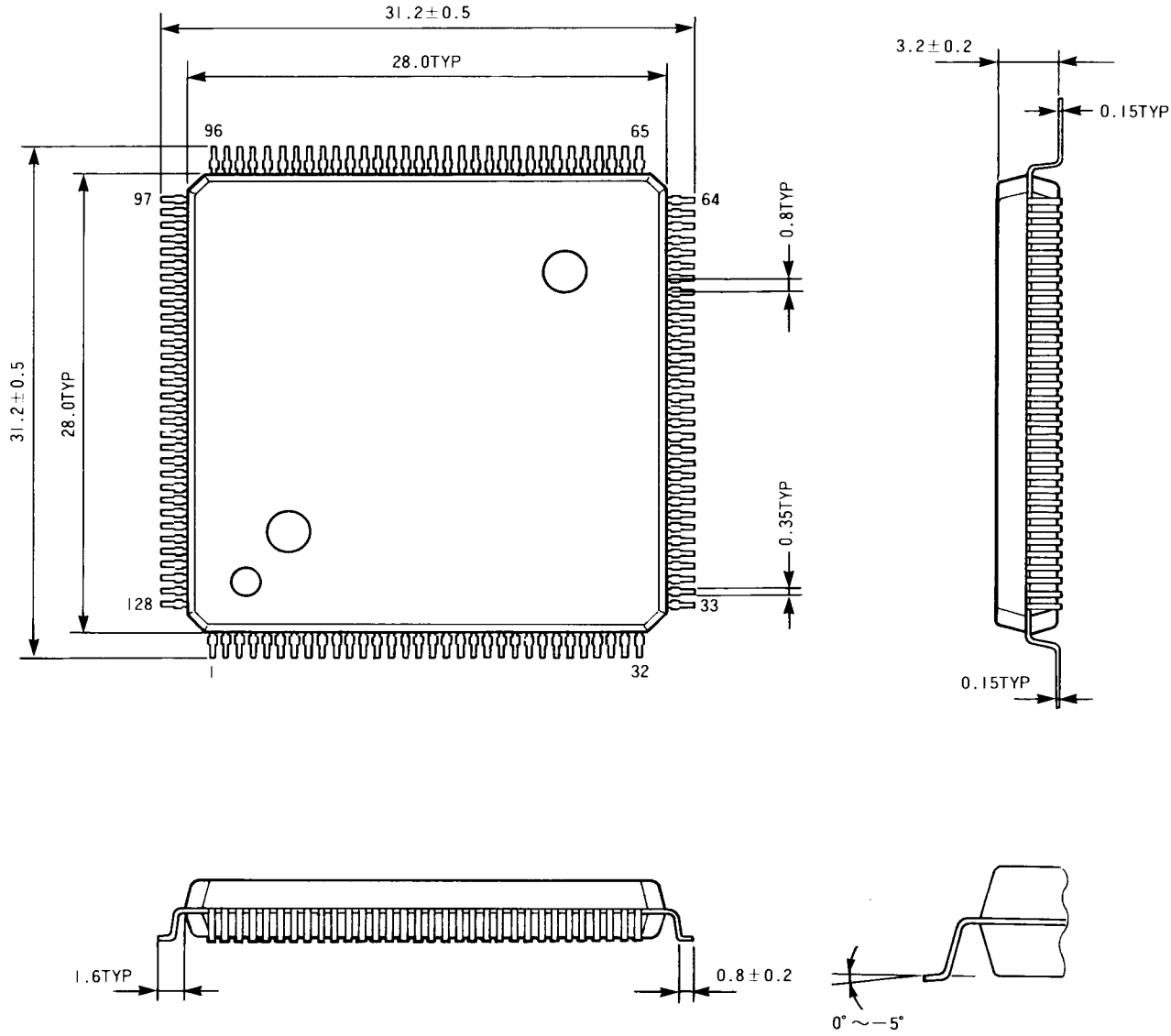
DC characteristics (at recommended operating conditions)

Item	Code	Min.	Standard	Max.	Unit
High level output voltage	VOH	IOH = −80μA	2.4		V
Low level output voltage	VOL	IOL = 1.6mA		0.4	V
Input leak current	IL		−10	10	μA
Power supply current	IDD				mA

■ EXAMPLE OF SYSTEM CONFIGURATION (DRAM AND CRT)



■ EXTERNAL DIAGRAM OF THE PACKAGE



The specifications of this product are subject to improvement changes without prior notice.

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