by Chromatic Research

Mpact™ Media Processor

Preliminary Data Sheet

Features

An Mpact media processor offers a complete multimedia solution for today's mainstream PC system, with the highest performance, integration and flexibility, and the lowest total cost.

- Complete
  - A total hardware solution for all multimedia ports: display monitor, audio, telephone, video and joystick/MIDI
  - Integrated software for all major multimedia functions on an x86 Windows 95 PC
- High Performance
  - Very Long Instruction Word (VLIW) processor with 3 billion operations per second (BOPS) peak in the Mpact /3000 version
  - 5 concurrent I/O and memory controllers
  - 132 MB/s PCI bus interface
  - Concurrent operation with MRK multitasking real-time kernel
  - Dynamically shared processing with x86 host for highest total system efficiency using the MRM resource manager
- Flexible
  - Loadable mediaware modules provide the latest multimedia functionality using evolving APIs and operating system standards, while retaining the same hardware
  - Software programmable hardware interfaces support today's popular RAMDACs, video encoders and decoders, and audio and modem codecs, while allowing future I/O device requirements to be met
- Low Cost
  - High integration interfaces require minimal support circuitry
  - A single low-cost 2-Mbyte Rambus DRAM needed for normal operation
  - Small footprint 240-pin HQFP package
  - Low power 3.3V operation

Description

The Mpact media processor is a high performance coprocessor for Windows 95 based PCs. Loaded with Mpact mediaware modules, the media processor adds or enhances support for all seven multimedia functions:

- Video: MPEG-1 & -2 decode, MPEG-1 encode
- 2D graphics: Full VGA, SVGA support, acceleration of video playback and GUI through GDI and DirectDraw
- 3D graphics: Full 3D acceleration through Direct3D
- Digital Audio: Industry-standard Sound Card compatibility, 3D Audio (SRS) and 3D positional audio effects (DirectSound), Dolby AC-3™ and MPEG-1 decode and Wave Table and Waveguide synthesis
- Fax/modem: Data up to 33.6 kb/s, fax up to 14.4 kb/s and DSVD (Digital Simultaneous Voice and Data)
- Telephony: Full-duplex speakerphone, Voicemail and caller ID
- Videophone: H.324 over POTS and H.320 over ISDN

The Mpact media processor uses an optimized real-time multitasking kernel to simultaneously execute these Mpact mediaware modules. The kernel allows, for example, 2D and 3D graphics, music synthesis audio and modem communications to run concurrently.

The Mpact media processor with its associated Rambus media memory resides on the PCI bus. A display interface supports popular RAMDACs for the RGB display monitor. A digital video interface and a programmable I/O interface support a wide range of peripheral devices. This flexibility makes the Mpact media processor the ideal solution for designing integrated, low cost, multimedia PCs.

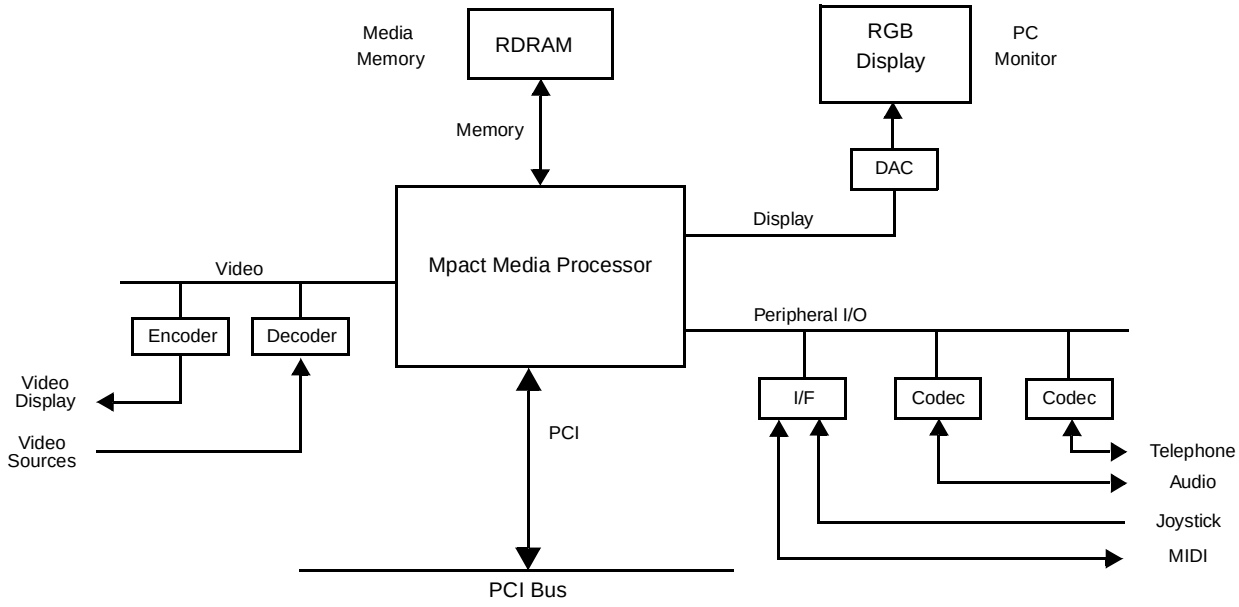


Figure 1. A Single Mpact Media Processor On The PCI Bus Supports All Multimedia Functions.

GENERAL DESCRIPTION

Multimedia On The PC

The functionality and performance of the x86 PC has steadily increased to meet the demands of multimedia. This has been through higher host x86 performance and a variety of peripheral processors and accelerator boards designed for specific media related functions. Commercial success has brought some generally accepted standard functions, hardware interfaces and, importantly with Windows 95, the DirectX family of uniform Application Programming Interfaces (APIs).

The high functional density and speed of submicron integrated circuit technology now allows all of the special multimedia processing to be combined in one programmable processor. Also, Rambus technology now provides low-cost, but high bandwidth dynamic memories to support graphics and video buffer needs. Chromatic Research and its partners have utilized these three trends: a more uniform hardware and software operating environment; large, fast, low-cost memories; and high density VLSI circuits to form a total multimedia solution for the Windows 95 PC. The result is the Mpact media processor with associated Mpact mediaware modules of software.

The Mpact Media Processor

The Mpact media processor is on the host PCI bus for tightly coupled sharing of the multimedia tasks being executed. The arithmetic and display buffer intensive portions of the tasks are done in a very long instruction word (VLIW) central processing unit (CPU) that operates out of a shared eight port SRAM. The Mpact /3000 CPU has five execution units operating in parallel from a single 72-bit instruction word at a peak 3000 million operations per second rate.

Five controllers share the SRAM with the CPU to concurrently support the wide variety of multimedia peripherals shown in Figure 2. These peripherals, the media buffer memory and the PCI bus connect through five distinct interfaces whose signals are summarized in Table 1.

Interfaces

Display

For high resolution 24-bit RGB color RAMDACs and PC monitors.

Video

For YUV digital video from analog or digital sources and to analog or digital displays.

Peripheral I/O

For serial and parallel digital audio and telephony codecs, digital interfaces to joysticks and MIDI, and the BIOS and Plug and Play ROMs. Microprogrammable for flexibility.

Memory

For 9-bit-wide modules of 500 MB/s Rambus media memory. Normal configuration uses one 2-MB RDRAM.

PCI Bus

A 132 MB/s burst connection to the x86 host system.

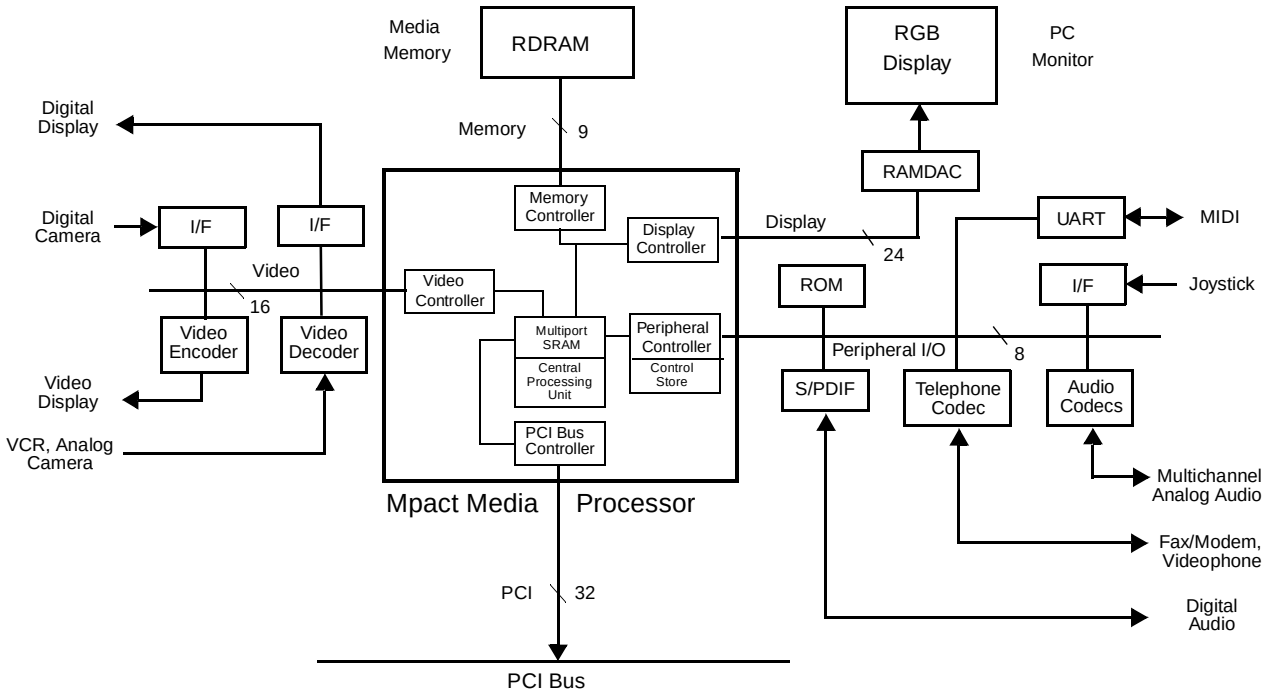


Figure 2. A CPU And Five I/O Controllers Operating Out Of A Multiport SRAM Concurrently Service All Elements Of A Multimedia PC.

Table 1. Interface Signal Summary

NAME	NUMBER	TYPE	DESCRIPTION
Display Interface	**30**		
DDATA[23:0]	24	O	Display Data, RGB
$\overline{DVS}$, $\overline{DCS}$, $\overline{DHS}$	3	O	Display Vertical, Composite and Horizontal Synchronization
$\overline{DBLNK}$	1	O	Display Blanking
DCLKI, DCLKO	2	I, O	Display Clock Input and Output
Video Interface	**22**		
VDATA [15:0]	16	I/O	Video Data, YUV
VVS, VHS, VODD	3	I	Video Vertical and Horizontal Synchronization and field indicator
VCREF, VHREF	2	I/O	Video pixel Clock Reference and Horizontal Reference
VCLK	1	I	Video Clock
Peripheral I/O Interface - Parallel	**19**		
PDATA[7:0]	8	I/O	Peripheral Parallel Data
$\overline{PPIEN}$, $\overline{PPOEN}$	2	O	Peripheral Parallel data Input and Output Enables
$\overline{PJYEN}$, $\overline{PAXEN}$	2	O	Peripheral Parallel Joystick and Auxiliary control input Enables
$\overline{PREQH}$, $\overline{PREQL}$	2	O	Peripheral Parallel Request input Enables, High and Low bytes
PPDCK, PPACK, PCSCK, PCOCK, PJYCK	5	O	Peripheral Parallel Data, Parallel Address, Chip Select, Control and Joystick register Clocks
Peripheral I/O Interface - Serial	**16**		
PSDI[3:0], PSDO[3:0]	8	I, O	Peripheral Serial Data Inputs and Outputs, channels 0-3
PSSYN[3:0]	4	I	Peripheral Serial Synchronization inputs, channels 0-3
PSCLK[3:0]	4	I	Peripheral Serial Clock inputs, channels 0-3
Peripheral I/O Interface - Special	**5**		
PMSD, PMSC	2	I/O	Peripheral Mpact Serial bus Data and Clock
PB0, PB1	2	O	Peripheral Programmed output Bits 0 and 1
PROM	1	I/O	Peripheral system identification ROM, serial input/output
Memory Interface - Rambus	**15**		
MDATA[8:0]	9	I/O	Memory Data
MCTRL, MEN	2	I/O, O	Memory Control and Enable
MCCP, MVREF	2	AI	Memory Current Control Program and Voltage Reference (analog)
MTXCK, MRXCK	2	I	Memory Transmit and Receive Clocks. The processor clock.
PCI Bus Interface	**48**		
AD[31:0]	32	I/O	PCI bus Address and Data
C/$\overline{BE}$[3:0]	4	I/O	PCI bus Command or Byte Enable
PAR	1	I/O	PCI bus Parity
$\overline{DEVSEL}$	1	I/O	PCI bus Device Select
IDSEL	1	I	PCI bus Initialization Device Select
$\overline{REQ}$, $\overline{GNT}$	2	O, I	PCI bus master Request and Grant
$\overline{INTA}$	1	O	PCI bus Interrupt A request
$\overline{FRAME}$	1	I/O	PCI bus Frame transaction
$\overline{IRDY}$, $\overline{TRDY}$	2	I/O	PCI bus Initiator and Target Readies
$\overline{STOP}$	1	I/O	PCI bus Stop transaction
CLK	1	I	PCI bus Clock
$\overline{RST}$	1	I	PCI bus Reset
System Interface	**3**		
Power	**82**		
V_{DD}	41	P	+5 Volt power supply and +3.3 Volt power supply in six groupings
V_{GND}	41	P	Power supply ground in one core and five I/O groupings
TOTAL	**240**		

Mpact Mediaware

Mpact mediaware by Chromatic Research is the software that enables access to the high-performance Mpact media processor on an x86 system. Through support for the latest DirectX APIs, in addition to alternative and earlier component APIs and legacy hardware views, the mediaware provides Mpact's power to DOS and Windows applications running on Windows 95. The system software component parts are shown schematically in a highly simplified form in Figure 4.

System Operation

Applications, when running, invoke various functions through their API or hardware view. These become single or multiple individual tasks related to the I/O port that is involved: video tasks use the Video port, 2D and 3D graphics use the Display port, digital audio tasks use the Audio port, fax/modem, telephony and videoconferencing use the Telephone port and the joystick, MIDI and ancillary functions use the General Port. These five classes of port are an important logical distinction. A port may use more than one electrical interface and is I/O device specific for the system.

Mpact Resource Manager - MRM

Operational tasks are executed on the x86 host, the media processor or both (as shown in Figure 4) as determined by the MRM resource manager operating on the host. MRM performs dynamic real-time task linking and loading based on the resources available as well as providing a backoff or graceful degradation strategy when either is over subscribed.

Mpact Real-time Kernel - MRK

The MRK dynamically schedules and dispatches tasks based on nearest deadlines. It is Mpact media processor resident and can be pre-emptive to meet the nearest deadline requirements.

Mpact Audio Processing Manager - MAPM

Real-time audio related tasks are controlled by a sub-task processing manager to ensure that synchronous audio operations are maintained without interruption. The human ear is more sensitive to time lapses than the eye is to the lapse's visual effects.

Memory Resources

Figure 3 shows the five memories managed by the Mpact Resource Manager. All media processor operations, including the MRK control, are from instructions resident in its multiported SRAM. Task instructions and corresponding SRAM data buffers are kept current from the media memory. The media memory also contains graphic and video display and audio buffers which are maintained directly by the processor and controllers.

The Peripheral I/O controller microcode executes out of its control store RAM. Normally all I/O routines can be resident, with only error handling needing to be downloaded from the media memory on a demand basis.

Boot initialization routines for the media processor and extended BIOS reside in the ROM on the Peripheral I/O interface. All other operational software is resident on the x86 host memory system and managed by the MRM. Mediaware modules are easily updated for new functionality using diskettes, CDROMs or by using on-line services.

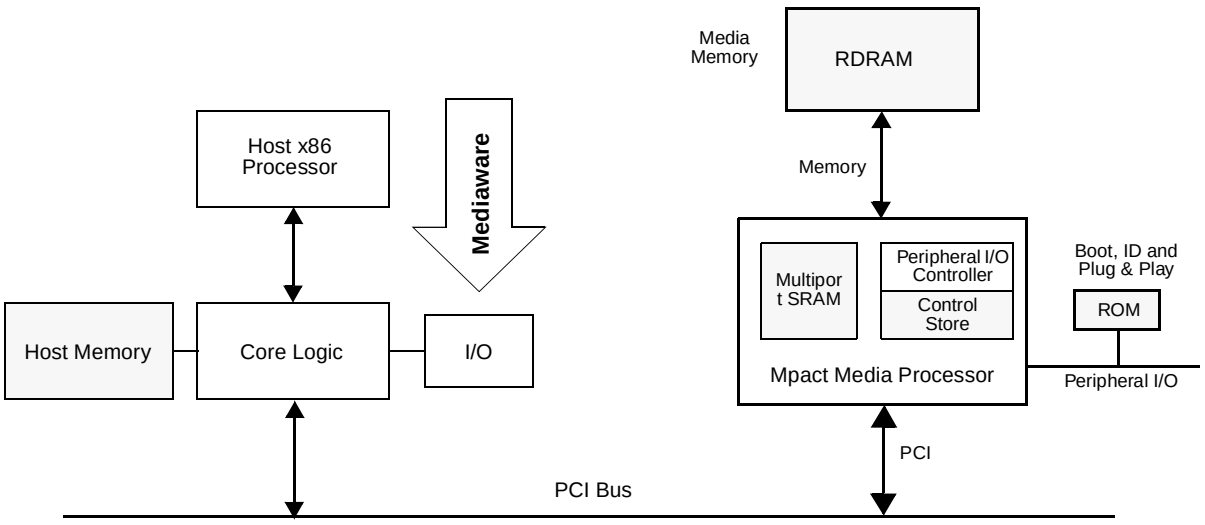


Figure 3. Real-Time Multimedia Operation Utilizes Mpact Mediaware Modules Resident In Five Memories.

Mpact Mediaware Modules

A mediaware module can be thought of as a narrow vertical slice extending from the top to the bottom of Figure 4. Each mediaware module adds a multimedia function generally defined by its primary task. These functions are summarized in Table 4 with primary attributes for the eight functional groups. Of equal importance are the supported APIs at the top that invoke the functions and the devices at the bottom that are supported by an I/O port. Table 4 summarizes the supported APIs and Table 5 in the Input/Output Interface section summarizes the supported devices. Table 4 shows by major API the functions that are enabled.

Video Compression and Decompression

The mediaware video modules support international standards for decompression, including MPEG-1 and MPEG-2 video, audio and system decoding through the DirectVideo, MCI and ActiveMovie APIs. The media processor's patented hardware motion estimation function

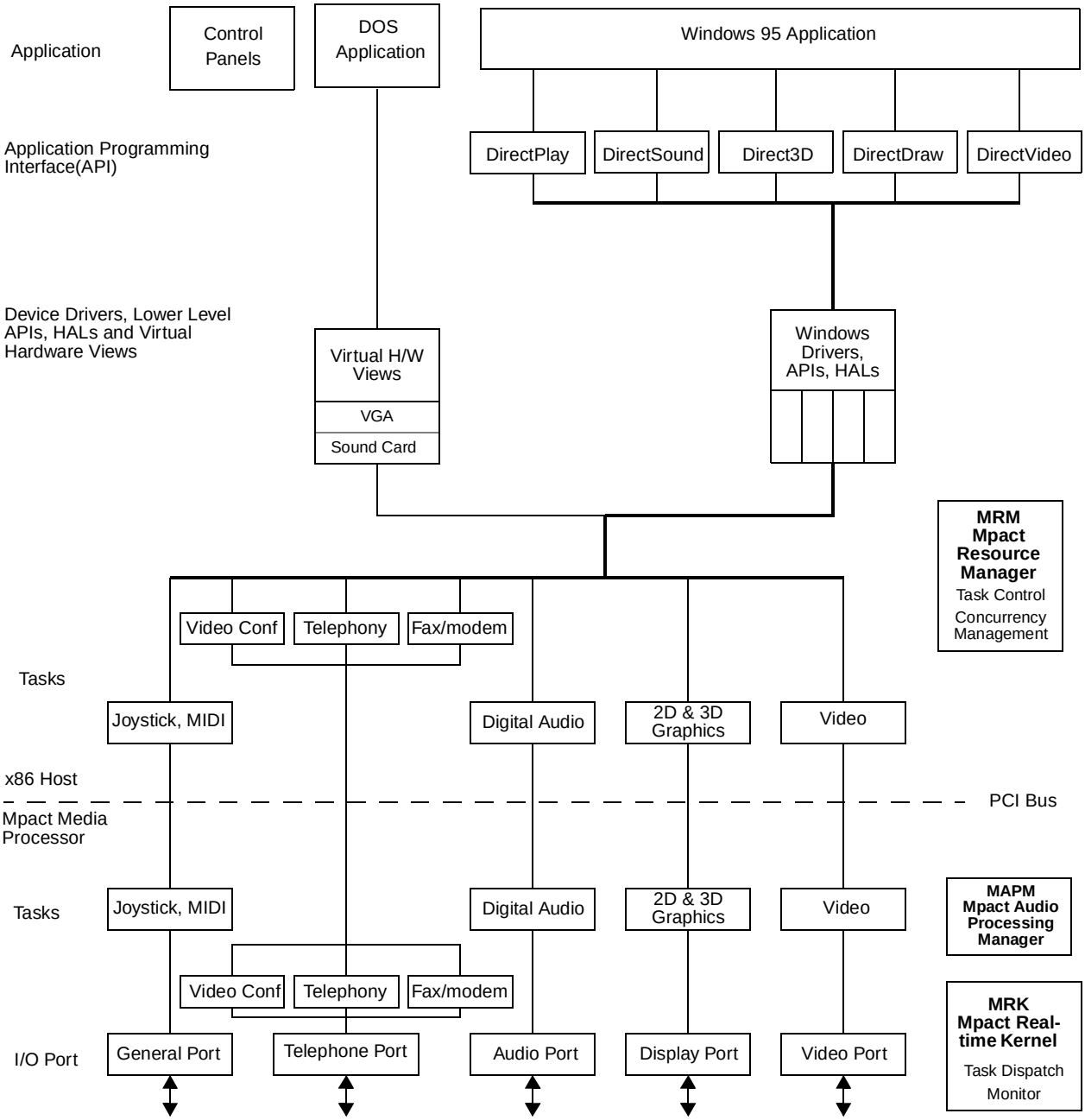


Figure 4. Distribution Of Operating Software Between The Mpact Media Processor And A Windows '95 PC Host.

enables high quality real-time MPEG-1 video, audio and system encoding as well as videoconferencing.

2D Graphics - VGA and GUI Acceleration

The mediaware graphics module provides full VGA compatibility for legacy applications and full SVGA as defined in VESA BIOS extension 2.0. Internal buffers support 8-, 15-, 16-, 24- and 32-bits per pixel views. The special 18-bit Chro-color format provides color depth performance between the 16-bit and 24-bit true-color with greater memory efficiency.

GUI acceleration is optimized for Windows 95 performance with a hardware cursor through the GDI and DirectDraw APIs. Acceleration is provided for solid and pattern fill, font and polygon generation, line draw, scaling and clipping, and color space conversion.

3D Graphics Acceleration

The mediaware 3D graphics module is optimized to fully accelerate 3D rendering for game play through the Direct3D API.

Digital Audio

The mediaware digital audio modules can utilize full 36-bit processing at 48 kHz sampling rates, even for compute-intensive functions like Dolby AC-3 and Waveguide physical modeling music synthesis. Automatic resampling is used so that all processing is at a uniform 48-kHz rate.

Fax/Modem

The mediaware Fax/modem modules support the latest current data and Fax modem standards. For data modulation to 33,600 b/s there is V.34bis, V.32bis, V.22bis, V.21, Bell 212A and Bell 103. For Fax modulation to 14,400 b/s there is V.17, V.29, V.27ter, and V.21.

Telephony

The mediaware telephony modules combine the AT+V command set with various functions like echo-cancelling, DTMF, ADPCM coding and DSVD processing to permit a full range of telephony operations like speakerphone, voicemail, answering machine and voice response.

Videoconferencing

The mediaware videoconferencing modules support international standards over ISDN and standard telephone lines to interface with various ISV's videophone applications.

General

For games and entertainment, the industry standard sound board interfaces to a joystick with buttons and MIDI, the Musical Instrument Digital Interface, are supported in mediaware modules.

Table 2. Mpact Mediaware API Summary By Function.

FUNCTION	APIs
Video	
MPEG Decode:	DirectVideo, MCI, ActiveMovie
MPEG Encode:	ActiveMovie
Graphics - 2D	
Graphics Card:	VGA, SVGA compatible
GUI Acceleration:	DirectDraw, GDI
Graphics - 3D	
3D Acceleration:	Direct3D, OpenGL, RealityLab
Digital Audio	
Sound Card:	Industry Standard with FM
Output:	DirectSound, MCI
Music:	MCI, MIDIout/in, WAVEout/in
Effects:	DirectSound 3D Audio
Fax/Modem	
Fax/Data modem	TAPI, TSPI, VCOMM, DirectPlay
Telephony	
Speakerphone, DSVD, Voicemail	TAPI, TSPI, VCOMM, DirectPlay
Videoconferencing	
	ActiveMovie, Independent Software Vendor's (ISV's)
General	
Joystick/MIDI	Industry Standard Sound Card

Table 3. Mpact Mediaware API Support Summary.

API	FUNCTIONS
DOS	
VGA Compatible	All
SVGA Compatible	All VESA Extension 2.0
Sound Card	All
WINDOWS 95	
DirectVideo	
ActiveMovie	MPEG encode and decode, videoconferencing
DirectDraw	
Direct3D	
DirectSound	
DirectPlay	

Table 4. Mpact Mediaware Functions Summary

FUNCTION	DESCRIPTION
Video	
Encode & Decode:	MPEG-1 Decoder, SIF 352 x 240, 30 f/s
	MPEG-2 Decoder, Main Level, Main Profile, NTSC 720 x 480, 30 f/s or PAL 720 x 576 25 f/s
	MPEG-1 Real-time encode, SIF I frames 30 f/s, 10 Mb/s
	MPEG-1 Non-real-time encode, IBP frames
Graphics - 2D	
Graphics Card:	VGA, all modes, up to 640 x 480 x 4 b/p @ 85 Hz
	SVGA, up to 1280 x 1024 x 18 b/p @ 75 Hz or 1024 x 768 x 24 b/p @ 85 Hz
GUI Acceleration:	Full 256 Ternary ROPs, BitBLT, font acceleration, line draw, polygon engine, YUV color conversion, H/W cursor
Graphics - 3D	
3D Acceleration:	Full rendering with lighting, shading, texturing, anti-aliasing support for rectangle fills, 3D spans and geometric primitives such as lines, triangles and quadrilaterals
Digital Audio	
Sound Card:	Industry Standard with FM synthesis
Encode & Decode:	MPEG-1, Layers 1 & 2
	MPEG-2 AC-3 decode
	Dolby AC-3, 5.1 channel decode
	Dolby ProLogic, 4 channel and stereo decode
	IMA ADPCM for Windows
Music:	FM synthesis
	Wave Table synthesis (32 voices, 32 multitrimbality parts), Synclavier® sample library
	Waveguide synthesis
	General MIDI, 128 instruments +>50 percussion, 64 voices
Effects:	Surround and 3D Sound (SRS), 3D Positional Audio Effects (Direct Sound), reverb, chorus, noise cancellation
Fax/Modem	
Data Rates:	Up to V.34bis @ 33.6 kb/s
Fax Rates:	Up to V.17 @ 14.4 kb/s
Data Protocols:	V.42, V.42bis, MNP 2-4 error correction, compression.
	AT Command set
Fax Protocols:	Class 1 (TIA-578), 2, 2.0 (TIA-592)
Telephony	
	Full-duplex speakerphone, caller ID and answering machine using the IS-101A (AT+V Command set)
	IMA ADPCM encoding/decoding
	Digital simultaneous voice and data (DSVD)
Videoconferencing	
	H.320 over ISDN
	H.324 over POTS
General	
Joystick:	Industry standard connector including MIDI
MIDI:	Industry standard NS16550 UART I/O

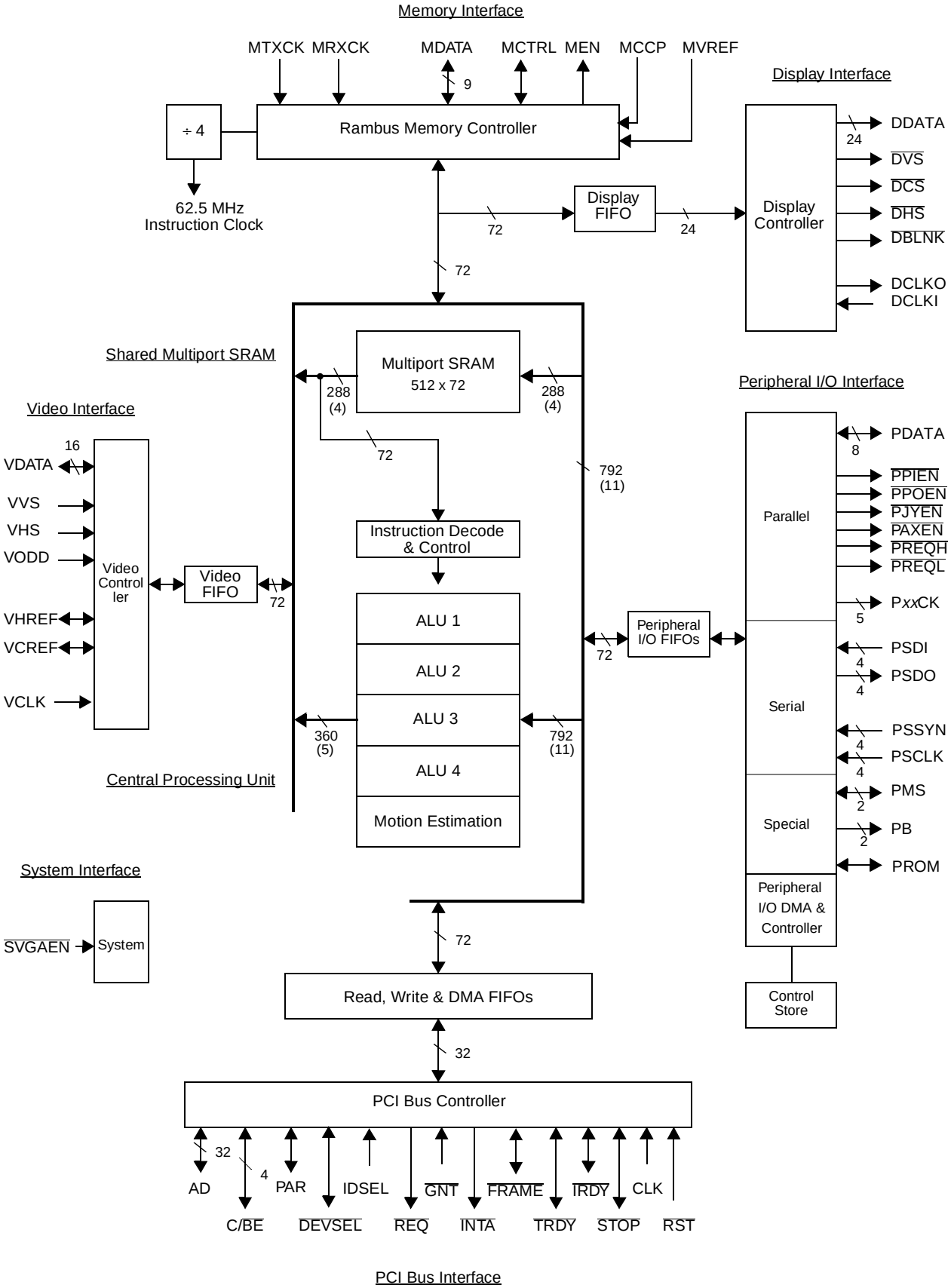


Figure 5. The Mpact /3000 Media Processor Block Diagram

FUNCTIONAL DESCRIPTION

An Mpact /3000 media processor is composed of the interconnected functional hardware units shown in the block diagram of Figure 5. The five interface controllers with their associated memory or FIFOs share the 4 kbyte multiport SRAM with the central processing unit (CPU). The basic bus width is that of a double word of eight 9-bit bytes for a total of 72 bits. Wider buses are shown with multiples of this basic width in parenthesis. Most interconnection is by crossbar connection to a 792-bit bus that allows multiple data sinks for an aggregate bandwidth of 9.0 GB/s. Transfers are controlled by the instructions executed by the CPU in combination with the interface controllers whose operation is setup by the CPU. The FIFOs on the non-memory interfaces ensure steady I/O data flows and a direct link to the display interface from the RDRAM media memory maintains the display.

Shared Multiport SRAM

All CPU instructions are fetched out of the shared multiport SRAM and most data operations are on data stored there. The simultaneous four read and four write ports provide a steady flow of instructions and data to the CPU, allow I/O buffers to be maintained in the SRAM and execute load and store instructions with the RDRAM media memory. The 4 kbytes SRAM is organized as 512 double words of 8 bytes each. The CPU maintains the cache of data and instructions in the SRAM from the RDRAM media memory.

Central Processing Unit (CPU)

The central processing unit consists of four arithmetic/ logic unit (ALU) groups, a motion estimation unit and the instruction decode and control.

Instruction Execution

The Mpact /3000 media processor is a very long instruction word (VLIW) processor where each instruction word is 72 bits. Each word is composed of two instructions that are 3 to 5 bytes in length each. Instructions cause multiple operations within a group and even multiple operations in multiple groups. A single instruction word can cause 8 single-byte operations to be executed on each of the four ALU groups for sustained rates of 2 billion operation per second (2 BOPS). Peak rates can reach 3 BOPS. Instruction memory efficiency is high because of vector and block repeat instructions.

ALU1

Each ALU group operates on double words of 8 bytes which can be 1, 2, 4 or 8 operands. ALU1 is a shift and align group which uses three inputs for extensive crossbar operations to produce two results.

ALU2

ALU2 is a general purpose ALU group with two inputs and a single output result except for special FFT butterfly instructions which produce a sum and difference result.

ALU3 & 4

ALU3 is a general purpose ALU group without the butterfly operations but it is augmented with three inputs for ternary operations that produce two results. ALU4 uses Booth encoders in a Wallace tree structure to produce various precisions of multiply and multiply-add operations in combination with ALU3 which outputs the results.

Motion Estimation Unit

The Mpact /3000 media processor motion estimation unit consists of some 400 arithmetic elements which produce an additional 20 BOPS performance for MPEG motion estimation.

Input/Output Interfaces And Ports

Of the five interfaces on the media processor, three are used for system input/output devices: the Display, the Video and the Peripheral I/O interfaces. A typical I/O device uses signals from more than one interface. The combination of signals from various interfaces to support a particular class of I/O device and its associated media-aware is called a port. There are five classes of ports for display, video, digital audio, telephone and general digital devices. Table 5 lists available ports and the interfaces signals that are used in each. Each port supports different functions and specific commercial devices for that function. These functions and devices are also listed in Table 5 with the Appendix which describes each port's design and operation. Example ports and devices are illustrated in Figure 6. Appendices are also provided for the Rambus Memory and PCI Bus Interfaces, and two alternative implementations for the Peripheral I/O Parallel Bus.

Video Port

The video port is used for direct digital video input or output in the 4:2:2 YUV format of CCIR 601. The video interface signals can be used directly for most digital video cameras, solid-state digital displays or the Zoom Video interface.

Analog video is input through decoders and output through encoders. Data is transferred on the video interface with the Mpact Serial and/or the Peripheral I/O parallel interface used for control functions.

Display Port

The display port is used for the PC monitor's RGB color display or with an encoder for an RGB video color display. Data is transferred on the display interface with the Mpact Serial and/or the Peripheral I/O parallel interface used for control functions.

Digital Audio Port

The digital audio port is used for both analog codecs and digital S/PDIF devices for input and output. Data is transferred on the Peripheral I/O interface along with control.

Telephone Port

The telephone port uses the Peripheral I/O interface for supporting telephony, fax/modem and videoconferencing codecs.

General Port

The general port uses the Peripheral I/O interface for transfers with other digital support devices that are in the typical multimedia system. These include game joysticks, MIDI and the various system ROMs.

Memory And PCI Bus Interfaces

These interfaces are used for standard Rambus media memory and the industry standard 32-bit PCI bus.

Peripheral I/O Parallel Bus

The Peripheral I/O Parallel Bus is formed from Peripheral I/O Interface signals using discrete external buffers or the Mpact System Integration ASIC (MSIA).

Table 5. Mpact Input/Output Ports & Interfaces

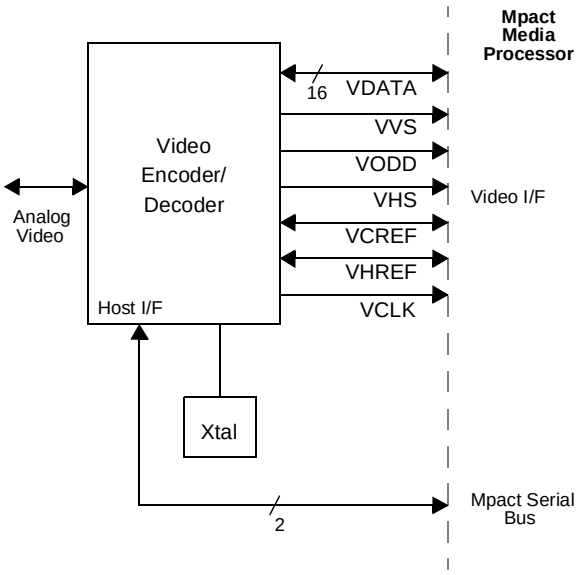
I/O Function	Interface*	I/O Device	A**
Video Port - YUV			
Analog output encoder:			
NTSC/PAL	V, PP, PMS	SAA7187	A11
		AD7176	
Analog input decoder:			
NTSC/PAL/SECAM	V, PP, PMS	SAA7110	A12
NTSC/PAL	V, PP, PMS	KS0122	
Digital I/O:			
CCIR 601 4:2:2 YUV	V		A15
Display Port - RGB			
RGB 24-bit RAMDAC			
1280 x 1024 @ 75 Hz. 8, 16, 18 b/p	D, PP, PMS	ATT 1178AB	A4
		ADV473KP	
Digital Audio Port			
Parallel Codec			
16 bit, 48 KHz, stereo	PP, PB	CS4231A	A5
		AD1845, 48	
Serial Codec			
16 bit, 48 KHz, stereo	PS, PB	CS4216	A13
S/PDIF			
Output	PP, PS, PB	CS8401	A6
Telephone Port			
Fax/Modem/Telephony/H.324 Videoconferencing			
V.34	PP, PS	CSP1027	A7
Fax/Modem/Telephony			
V.32bis	PP, PS	T7525	A14
Videoconferencing			
H.320 for ISDN			A16
General Port			
Joystick	PP	Ind. Std.	A8
MIDI UART	PP, PB	NS16550A	
System ID ROM	PROM	DS2430A	A10
Boot and P&P Flash EPROM	PP	Am29F010	
Boot ROM	PP	Ind. Std.	
Plug & Play serial EEPROM	PP, PB	X84041	
Memory Interface	Memory	Rambus	A1
PCI Bus Interface	PCI Bus	Ind. Std.	A2
Peripheral I/O Parallel Bus			
Discrete components	PP		A3
ASIC	PP		

* V = Video, D = Display, PP = Peripheral I/O Parallel, PS = Peripheral I/O Serial, PMS = Peripheral Mpact Serial, PB = Peripheral Programmed Bits.
** Data Sheet Appendix number.

Video Controller And Interface

The video controller, in combination with the 32-byte video FIFO, inputs or outputs YUV video data on the 16-bit video interface. This programmable interface is bidirectional but transfers are half-duplex. The three input synchronization signals, two bidirectional reference clock signals and an external video clock input can support a wide variety of 16-bit input video sources and output devices in either 8- or 16-bit formats. Industry standard NTSC or PAL encoders and decoders can be used at full scan rates for analog composite or S-video signals. Digital interfaces can be used for Zoom Video or CCIR 601 YUV 4:2:2 digital cameras or displays. Formats can be interlaced or progressive scan. The video controller is capable of horizontal decimation on input or output.

Among the supported devices in the Mpact mediaware modules video port are the SAA7187 and AD7176 encoders and the SAA7110 and KS0122 decoders. Control of the interfaced device is with the Peripheral Mpact Serial bus (the PMSD and PMSC signals) with possible device selection from the Peripheral I/O parallel interface.



Display Controller And Interface

The display controller in combination with the 512-byte display FIFO provides continuous RGB display data to the display interface from buffers in the RDRAM media memory.

The display controller generates all data, synchronization and clock signals to the display RAMDAC (digital-to-analog converter) or display encoder from a single video clock generator input DCLKI. Both 8-bit indexed-color and 24-bit true-color RAMDACs can be supported as well as NTSC and PAL RGB encoders. Possible display resolutions and the pixel clock frequency DCLKO are shown in Table 6.

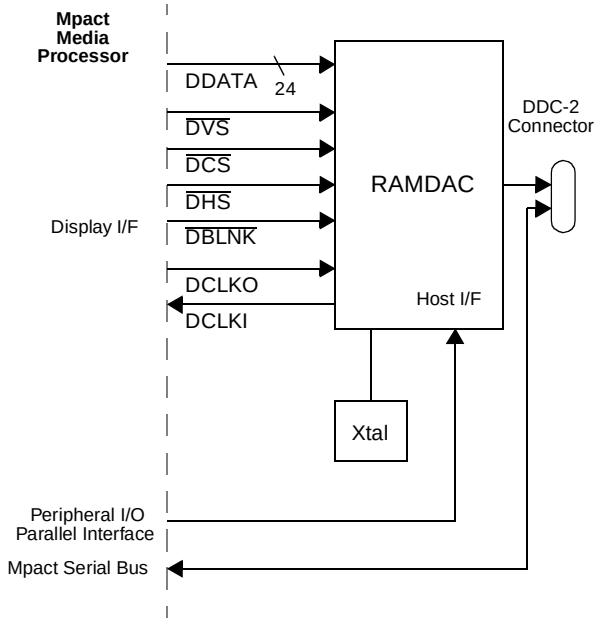
Table 6. Display Resolutions

Display Resolution	Pixel Clock Frequency MHz	Maximum Refresh Rate Hz	Maximum Pixel Depth
1280 x 1024	135	75	8
1152 x 870	121	85	18
1024 x 768	94.5	85	18
800 x 600	56	85	24
640 x 480	36	85	24
NTSC: 720 x 480	14.318	30	24
PAL: 720 x 576	16.250	25	24

Control of the display RAMDAC or encoder is through the use of the Mpact Serial bus and/or the parallel bus in the Peripheral I/O interface.

Display data is stored in the media memory in one-, two- or three-byte formats to support 8, 15, 16, 18 and 24 bits per pixel. The special 18 bits per pixel data Chro-color format provides a 32-bit buffer view yet takes only two bytes in the media memory. The conversion from media memory format to RAMDAC format takes place in the display controller.

Supported devices in the Mpact mediaware modules display port are the ATT 1178AB, Bt473 and ADV473KP.



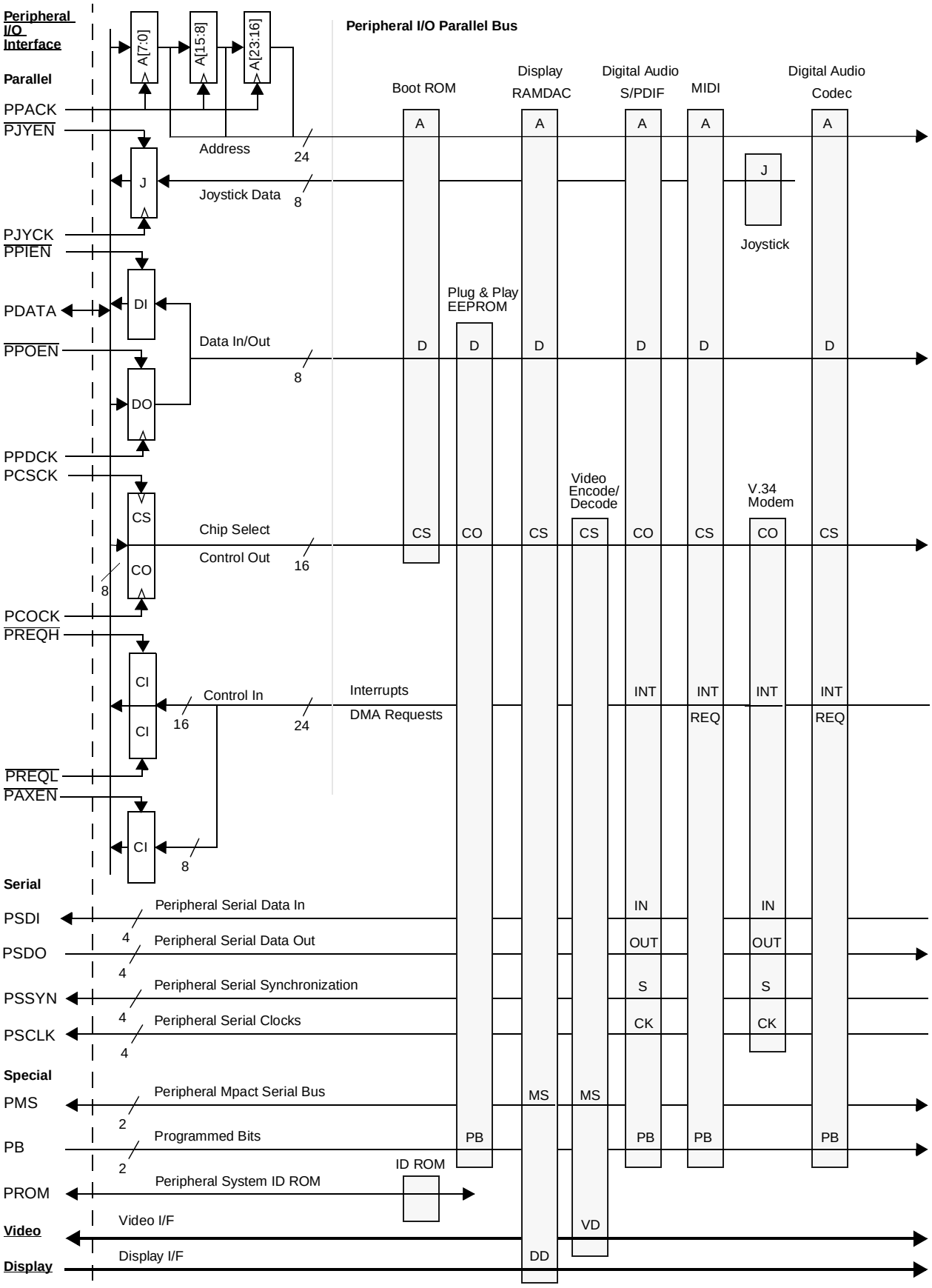


Figure 6. Peripheral I/O Interface External Components And Connections To Example Mediaware Supported I/O Devices.

Peripheral Input/Output Controller And Interface

The Peripheral I/O controller and its associated FIFOs provide the interface to lower bandwidth peripheral components of the multimedia system. This is done with eight generic unidirectional bit-serial data buses, a single generic bidirectional 8-bit parallel data bus and three special buses. The aggregate data rate can be as high as 5 Mbytes/second in the Mpact /3000 media processor. These generic buses become device and function specific ports with the loading of the 96-byte controller microcode RAM and the use of the various mediaware modules. A total of fourteen different transaction ports may be operational at one time, with twelve of them using separate DMAs and 8-byte each FIFOs. Figure 6 shows the interface connections to ten example I/O devices that are supported by mediaware. Signals labelled and shown visibly passing through the block are connected in that block. The device types are listed in Table 5. These serve to illustrate typical interfaces to I/O peripherals.

The Peripheral Input/Output Interface divides naturally into three sections for parallel data, serial data and special transfers.

Parallel Interface

The 8-bit bidirectional PDATA[7:0] bus transfers not only data in and out, but also has specific clocking and control signals to support 24-bit addressing, 8 chip-select outputs, 8 general control signal outputs, 12 interrupt requests and 12 DMA requests. Also, it provides the periodic clock timing for a joystick input. Figure 6 shows the clocking and output enables for the seven 8-bit registers and four input multiplexers. Table 8 summarizes the Peripheral I/O Parallel Bus signals that result.

Table 7. Peripheral I/O Parallel Bus Signals

Signal	Number	Type
Data In/Out [7:0]	8	I/O
Address [23:0]	24	O
Chip Select [7:0]	8	O
Control Out [7:0]	8	O
Interrupt In [11:0]	12	I
DMA Request In [11:0]	12	I
Joystick Data In [7:0]	8	I

This configuration can support most popular I/O peripherals with a parallel data interface today, but because its timing and function is programmable it can easily adapt to the data, address and sequence formats of future devices.

Serial Interface

The bit-serial interface has four input channels 0 - 3 and four output channels 0 - 3. Like numbered input and output channels, PSDI[3:0] and PSDO[3:0], share common data clocks PSCLK[3:0] and frame synchronization signals PSSYN[3:0]. These can support the wide variety of slave mode serial data formats used in audio and telephony codecs as well as the serial control ports of many microprocessor peripherals.

Special Interface

Mpact Serial Bus

Many microprocessor peripherals, including display and video products, use a two-wire bidirectional bus for multimaster control. The peripheral Mpact Serial Bus, PMSD and PMSC, is an enhanced version of the industry standard for support of these devices.

Programmed Bits

The PB[1:0] signals are two outputs without external registering that can be used for peripheral communication without regard to other transfers on the parallel or serial interfaces. They are set and cleared directly by the peripheral I/O controller's microcode.

System Identification ROM

Each Mpact media processor has a unique system identification number read from a one-time-programmable ROM. The bidirectional PROM signal provides a single pin connection to a DS2430A or similar device for this purpose.

Rambus Memory Controller And Interface

The memory controller supports external Rambus DRAM (RDRAM) media memory connected to the memory interface. Media memory is used for both data and instruction storage for transfer to the processor's multiported SRAM as well as for video and display data buffers.

The controller has direct access to the multiported SRAM and the display FIFO for rapid transfers with the RDRAM. All addresses are translated in the controller to provide tiling for greater transfer rates on large video and display buffers. In addition, the controller provides memory refresh and facilitates internal RDRAM register initialization.

The minimum media memory is 2 Mbytes of 9-bit (18-Mbit) RDRAM. Increments of 1 or 2 Mbytes can be added up to a maximum of 8 Mbytes. The interface utilizes the Rambus Signaling Logic (RSL) for transfers on each clock edge at a 500 Mbytes/second peak rate on the Mpact /3000 media processor. The minimum amount of media memory required is a function of the maximum display resolution and associated pixel depth as shown in Table 8.

Table 8. Media Memory Requirements

Display Resolution	Pixel Depth In Bits	Minimum RDRAM Size
1280 x 1024	8	2 MB
1152 x 870	18	4 MB
1152 x 870	8	2 MB
1024 x 768	24	4 MB
1024 x 768	8, 18	2 MB
800 x 600	8, 18, 24	2 MB
640 x 480	8, 18, 24	2 MB

The interconnection of the RDRAM media memory on the Rambus channel is shown in Figure 7. Note that on the Mpact /3000 media processor the external 250 MHz Rambus clock is the main processor system clock. The MCCP analog current input determines drive capability of the memory interface as specified by RSL.

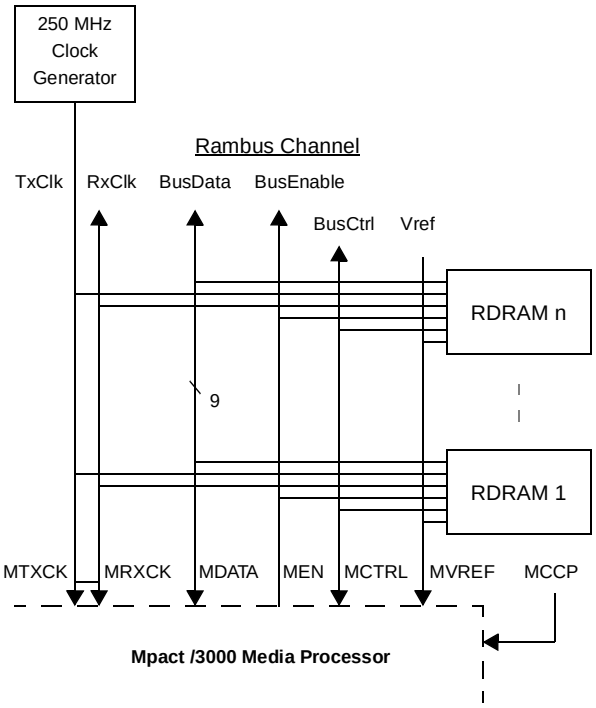


Figure 7. RDRAM Media Memory On The Rambus Channel

PCI Bus Controller And Interface

The PCI bus controller and its three FIFOs manage access between the Mpact media processor and the host x86. The interface is fully compliant with PCI Local Bus Specification, Revision 2.0 with either 3.3- or 5-Volt signaling. Peak transfer rates are 132 MB/second on the 32-bit bus.

The Mpact media processor acts as a target or a bus master with transfers being fully concurrent with the host or memory subsystem at a synchronous 33-MHz rate. Three separate FIFOs provide for variable length read and write burst operation as a target and DMA operation as a master. The DMA FIFO is four 32-bit words, the write FIFO is eight words and the read only a single word buffer.

As determined in the PCI configuration space, the Mpact media processor appears in address space in three forms: as 128 MB of memory, as 128 kB of extension ROM and as specific device compatibility addresses. Autoconfiguration for add-in cards and components is supported.

Correct 5 Volt PCI bus signaling operation is assured by connecting the six V5DD power pins to +5 Volts rather than +3.3 Volts.

System Interface

The Mpact media processor can be configured and tested using signals in the system interface.

The $\overline{\text{SVGAEN}}$ signal allows disabling the Mpact media processor from appearing in PCI configuration space as a VGA device. When asserted the class code is 030000 Hex for VGA Compatible Controller. When not asserted the class code is 048000 Hex for Other Multimedia Device.

The $\overline{\text{SVGAEN}}$ signal did not exist on pre-production versions of the Mpact /3000 media processor with Revision ID numbers below 0A Hex as identified in the PCI configuration space.

The TMS signal puts the media processor in a test mode of operation that changes the function of certain pins. For normal operation it should not be asserted.

SIGNAL DESCRIPTION

Table 9. Signal Description

NAME	NUMBER	TYPE	DESCRIPTION
Display Interface (30)			
DDATA[23:0]	24	O	Display Data, RGB
$\overline{\text{DVS}}$	1	O	Display Vertical Synchronization
$\overline{\text{DCS}}$	1	O	Display Composite Synchronization
$\overline{\text{DHS}}$	1	O	Display Horizontal Synchronization
$\overline{\text{DBLNK}}$	1	O	Display Blanking
DCLKI	1	I	Display Clock Input. Pixel clock source.
DCLKO	1	O	Display Clock Output. Pixel clock.
Video Interface (22)			
VDATA [15:0]	16	I/O	Video Data, YUV
VVS	1	I	Video Vertical Synchronization
VHS	1	I	Video Horizontal Synchronization
VODD	1	I	Video Odd field indicator
VCREF	1	I/O	Video pixel Clock Reference
VHREF	1	I/O	Video Horizontal Reference
VCLK	1	I	Video Clock. Twice the pixel rate.
Peripheral I/O Interface - Parallel (19)			
PDATA[7:0]	8	I/O	Peripheral Parallel Data
$\overline{\text{PPIEN}}$	1	O	Peripheral Parallel data Input Enable. Enables I/O parallel bus onto PDATA.
$\overline{\text{PPOEN}}$	1	O	Peripheral Parallel data Output Enable. Enables DO register onto I/O parallel bus
$\overline{\text{PJYEN}}$	1	O	Peripheral Parallel Joystick input Enable. Enables joystick register onto PDATA.
$\overline{\text{PAXEN}}$	1	O	Peripheral Auxiliary control input Enable. Enables auxiliary control input onto PDATA.
$\overline{\text{PREQH}}$	1	O	Peripheral Parallel Request input Enable, High byte. Enables requests onto PDATA.
$\overline{\text{PREQL}}$	1	O	Peripheral Parallel Request input Enable, Low byte. Enables requests onto PDATA.
PPDCK	1	O	Peripheral Parallel Data register Clock. Clocks PDATA data into DO register.
PPACK	1	O	Peripheral Parallel Address register Clock. Clocks PDATA data into address registers.
PCSCK	1	O	Peripheral Chip Select register Clock. Clocks PDATA data into chip select register.
PCOCK	1	O	Peripheral Control Output register Clock. Clocks PDATA data into control out register.
PJYCK	1	O	Peripheral Joystick register Clock. Clocks joystick data into joystick input register.
Peripheral I/O Interface - Serial (16)			
PSDI[3:0]	4	I	Peripheral Serial Data Inputs, channels 0-3
PSDO[3:0]	4	O	Peripheral Serial Data Outputs, channels 0-3
PSSYN[3:0]	4	I	Peripheral Serial Synchronization inputs, channels 0-3
PSCLK[3:0]	4	I	Peripheral Serial Clock inputs, channels 0-3
Peripheral I/O Interface - Special (5)			
PMSD	1	I/O	Peripheral Mpact Serial bus Data
PMSC	1	I/O	Peripheral Mpact Serial bus Clock
PB[1:0]	2	O	Peripheral Programmed output Bits 1 and 0
PROM	1	I/O	Peripheral system identification ROM, serial input/output

Table 9. Signal Description (Continued)

NAME	NUMBER	TYPE	DESCRIPTION
Memory Interface - Rambus (15)			
MDATA[8:0]	9	I/O	Memory Data to/from the Rambus BusData signal
MCTRL	1	I/O	Memory Control to/from the Rambus BusCtrl signal
MEN	1	O	Memory Enable to the Rambus BusEnable signal
MCCP	1	AI	Memory Current Control Program (CCtlPgm), an analog input derived from V_{term}
MVREF	1	AI	Memory Voltage Reference, an analog input from the Rambus V_{ref}
MTXCK	1	I	Memory Transmit Clock from the Rambus TxClk signal. Transmit from memory.
MRXCK	1	I	Memory Receive Clock from the Rambus RxClk signal. Receive into memory.
PCI Bus Interface (48)			
AD[31:0]	32	I/O	PCI bus Address and Data
C/$\overline{BE}$[3:0]	4	I/O	PCI bus Command or Byte Enable during address transactions
PAR	1	I/O	PCI bus Parity
$\overline{DEVSEL}$	1	I/O	PCI bus Device Select. Target has decoded its address.
IDSEL	1	I	PCI bus Initialization Device Select input
$\overline{REQ}$	1	O	PCI bus master Request
$\overline{GNT}$	1	I	PCI bus master Grant
$\overline{INTA}$	1	O	PCI bus Interrupt A request
$\overline{FRAME}$	1	I/O	PCI bus Frame transaction
$\overline{IRDY}$	1	I/O	PCI bus Initiator Ready
$\overline{TRDY}$	1	I/O	PCI bus Target Ready
$\overline{STOP}$	1	I/O	PCI bus Stop transaction request by target
CLK	1	I	PCI bus Clock
$\overline{RST}$	1	I	PCI bus Reset
System Interface (3)			
$\overline{SVGAEN}$	1	I	System VGA Enable
TMS	1	I	Test Mode Select
Test	1	I	Test
Power (82)			
V_{DD}	16	P	+3.3 Volt power supply, core
$V5_{DD}$	6	P	+5 Volt power supply, I/O. Input clamping level. Should be 5.0 Volts in mixed 5/3.3-Volt supply voltage systems. Maybe 3.3 Volts in 3.3-Volt only supply voltage systems.
$V_{DD}1$	6	P	+3.3 Volt power supply, display interface
$V_{DD}2$	6	P	+3.3 Volt power supply, PCI bus interface
$V_{DD}3$	4	P	+3.3 Volt power supply, peripheral interface
$V_{DD}4$	2	P	+3.3 Volt power supply, video interface
$V_{DD}A$	1	A	+3.3 Volt power supply, analog, memory interface
V_{GND}	22	P	Power supply ground, core
$V_{GND}1$	6	P	Power supply ground, display interface
$V_{GND}2$	6	P	Power supply ground, PCI bus interface
$V_{GND}3$	4	P	Power supply ground, peripheral interface
$V_{GND}4$	2	P	Power supply ground, video interface
$V_{GND}A$	1	A	Power supply ground, analog, memory interface
TOTAL (240)			

SPECIFICATIONS

Packaging - Pinout

Table 10. Pin Number By Signal Name

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
Display Interface (30)							
DDATA23	194	DDATA15	208	DDATA7	220	$\overline{\text{DVS}}$	234
DDATA22	195	DDATA14	209	DDATA6	222	$\overline{\text{DCS}}$	236
DDATA21	197	DDATA13	212	DDATA5	224	$\overline{\text{DHS}}$	237
DDATA20	199	DDATA12	213	DDATA4	225	$\overline{\text{DBLNK}}$	233
DDATA19	201	DDATA11	214	DDATA3	226	DCLKI	239
DDATA18	203	DDATA10	215	DDATA2	227	DCLKO	229
DDATA17	204	DDATA9	217	DDATA1	231		
DDATA16	206	DDATA8	219	DDATA0	232		
Video Interface (22)							
VDATA15	137	VDATA9	127	VDATA3	117	VODD	111
VDATA14	136	VDATA8	126	VDATA2	116	VCREF	112
VDATA13	135	VDATA7	125	VDATA1	115	VHREF	113
VDATA12	133	VDATA6	124	VDATA0	114	VCLK	119
VDATA11	131	VDATA5	123	VVS	110		
VDATA10	129	VDATA4	122	VHS	74		
Peripheral I/O Interface - Parallel (19)							
PDATA7	139	PDATA2	147	$\overline{\text{PJYEN}}$	182	PPACK	184
PDATA6	141	PDATA1	149	$\overline{\text{PAXEN}}$	177	PCSCK	185
PDATA5	143	PDATA0	152	$\overline{\text{PREQH}}$	179	PCOCK	186
PDATA4	144	$\overline{\text{PPIEN}}$	190	$\overline{\text{PREQL}}$	178	PJYCK	183
PDATA3	145	$\overline{\text{PPOEN}}$	192	PPDCK	189		
Peripheral I/O Interface - Serial (16)							
PSDI3	157	PSDO3	160	PSSYN3	156	PSCLK3	158
PSDI2	162	PSDO2	166	PSSYN2	161	PSCLK2	164
PSDI1	168	PSDO1	170	PSSYN1	167	PSCLK1	169
PSDI0	172	PSDO0/TDO	176	PSSYN0	171	PSCLK0	174
Peripheral I/O Interface - Special (5)							
PMSD	155	PB1	188	PROM	153		
PMSC	154	PB0	187				
Memory Interface - Rambus (15)							
MDATA8	106	MDATA4	88	MDATA0	76	MVREF	84
MDATA7	104	MDATA3	82	MCTRL	86	MTXCK	93
MDATA6	100	MDATA2	80	MEN	102	MRXCK	95
MDATA5	98	MDATA1	78	MCCP	108		

Table 10. Pin Number By Signal Name (Continued)

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
PCI Bus Interface (48)							
AD31	7	AD19	28	AD7	58	PAR	44
AD30	9	AD18	29	AD6	59	$\overline{\text{DEVSEL}}$	40
AD29	11	AD17	32	AD5	62	IDSEL	21
AD28	12	AD16	33	AD4	64	$\overline{\text{REQ}}$	6
AD27	14	AD15	47	AD3	66	$\overline{\text{GNT}}$	5
AD26	15	AD14	48	AD2	68	$\overline{\text{INTA}}$	2
AD25	16	AD13	49	AD1	69	$\overline{\text{FRAME}}$	35
AD24	17	AD12	50	AD0	70	$\overline{\text{IRDY}}$	36
AD23	22	AD11	51	C/$\overline{\text{B}}$3	19	$\overline{\text{TRDY}}$	38
AD22	23	AD10	53	C/$\overline{\text{B}}$2	34	$\overline{\text{STOP}}$	42
AD21	25	AD9	55	C/$\overline{\text{B}}$1	46	CLK	4
AD20	27	AD8	56	C/$\overline{\text{B}}$0	57	$\overline{\text{RST}}$	3
Test Interface (3)							
$\overline{\text{SVGAEN}}$, TDI	71	TMS	72	TCLK	73	TDO/PSDO0	176
Power (82)							

Pin Name	Number of Pins	Pin Numbers
V_{DD}	16	24, 37, 60, 79, 90, 92, 97, 101, 109, 128, 150, 163, 173, 200, 216, 240
$V5_{DD}$	6	13, 41, 63, 118, 138, 159
$V_{DD}1$	6	196, 205, 210, 221, 228, 235
$V_{DD}2$	6	8, 18, 30, 43, 52, 65
$V_{DD}3$	4	140, 146, 180, 191
$V_{DD}4$	2	120, 134
$V_{DD}A$	1	96
V_{GND}	22	1, 26, 39, 61, 75, 77, 81, 83, 85, 87, 89, 91, 99, 103, 105, 107, 130, 151, 165, 175, 202, 218
$V_{GND}1$	6	198, 207, 211, 223, 230, 238
$V_{GND}2$	6	10, 20, 31, 45, 54, 67
$V_{GND}3$	4	142, 148, 181, 193
$V_{GND}4$	2	121, 132
$V_{GND}A$	1	94

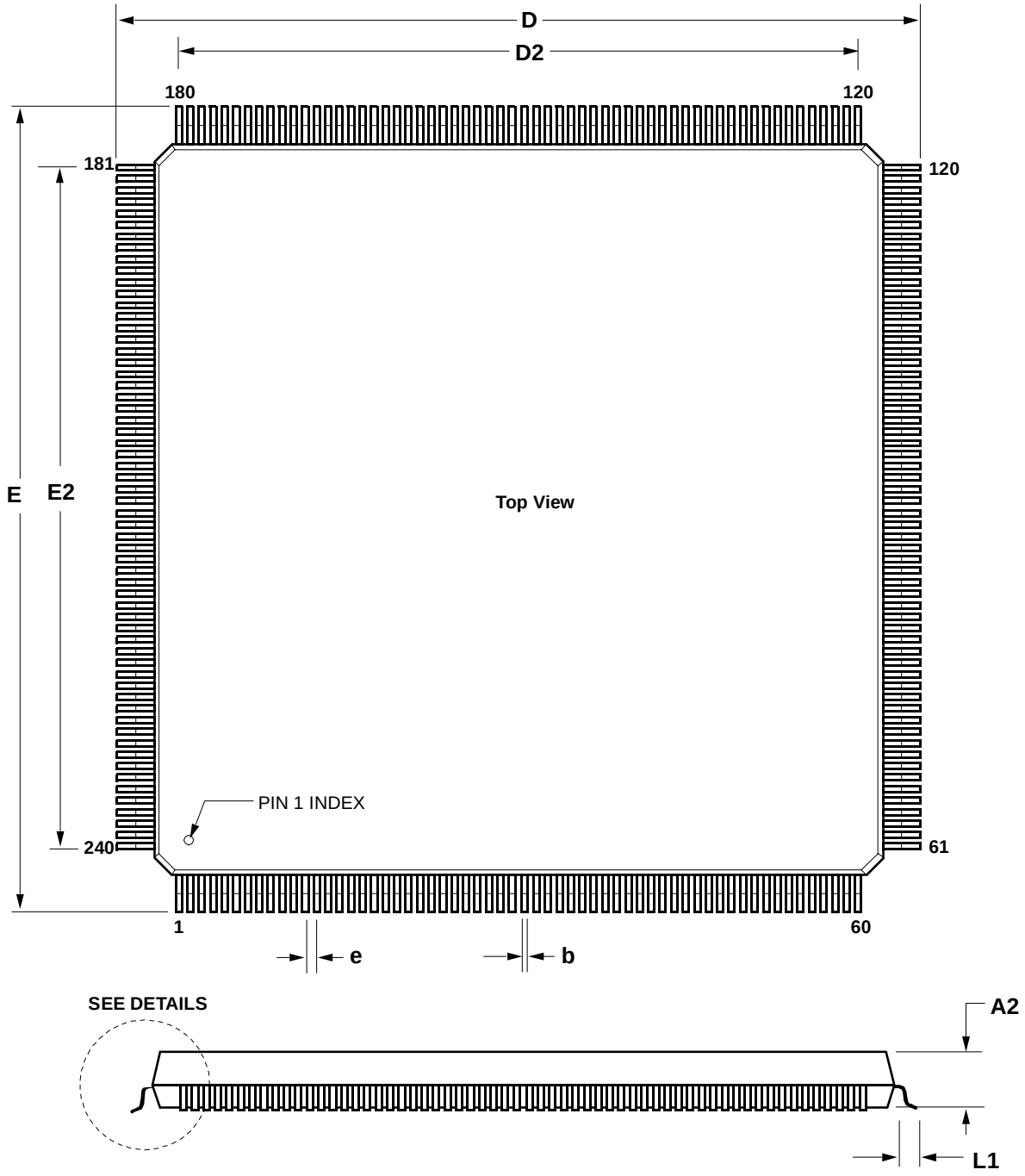
Table 11. Signal Name By Pin Number

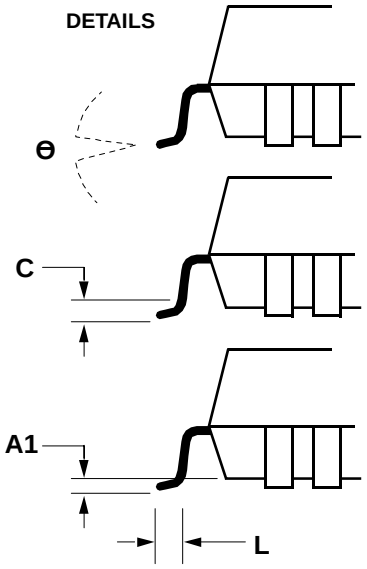
Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	V_{GND}	31	$V_{GND}2$	61	V_{GND}	91	V_{GND}
2	$\overline{INTA}$	32	AD17	62	AD5	92	V_{DD}
3	$\overline{RST}$	33	AD16	63	$V5_{DD}$	93	MTXCK
4	CLK	34	C/$\overline{B}$2	64	AD4	94	V_{GND}A
5	$\overline{GNT}$	35	$\overline{FRAME}$	65	$V_{DD}2$	95	MRXCK
6	$\overline{REQ}$	36	$\overline{IRDY}$	66	AD3	96	V_{DD}A
7	AD31	37	V_{DD}	67	$V_{GND}2$	97	V_{DD}
8	$V_{DD}2$	38	$\overline{TRDY}$	68	AD2	98	MDATA5
9	AD30	39	V_{GND}	69	AD1	99	V_{GND}
10	$V_{GND}2$	40	$\overline{DEVSEL}$	70	AD0	100	MDATA6
11	AD29	41	$V5_{DD}$	71	$\overline{SVGAEN}$, TDI	101	V_{DD}
12	AD28	42	$\overline{STOP}$	72	TMS	102	MEN
13	$V5_{DD}$	43	$V_{DD}2$	73	TCLK	103	V_{GND}
14	AD27	44	PAR	74	VHS	104	MDATA7
15	AD26	45	$V_{GND}2$	75	V_{GND}	105	V_{GND}
16	AD25	46	C/$\overline{B}$1	76	MDATA0	106	MDATA8
17	AD24	47	AD15	77	V_{GND}	107	V_{GND}
18	$V_{DD}2$	48	AD14	78	MDATA1	108	MCCP
19	C/$\overline{B}$3	49	AD13	79	V_{DD}	109	V_{DD}
20	$V_{GND}2$	50	AD12	80	MDATA2	110	VVS
21	IDSEL	51	AD11	81	V_{GND}	111	VODD
22	AD23	52	$V_{DD}2$	82	MDATA3	112	VCREF
23	AD22	53	AD10	83	V_{GND}	113	VHREF
24	V_{DD}	54	$V_{GND}2$	84	MVREF	114	VDATA0
25	AD21	55	AD9	85	V_{GND}	115	VDATA1
26	V_{GND}	56	AD8	86	MCTRL	116	VDATA2
27	AD20	57	C/$\overline{B}$0	87	V_{GND}	117	VDATA3
28	AD19	58	AD7	88	MDATA4	118	$V5_{DD}$
29	AD18	59	AD6	89	V_{GND}	119	VCLK
30	$V_{DD}2$	60	V_{DD}	90	V_{DD}	120	$V_{DD}4$

Table 11. Signal Name By Pin Number (Continued)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
121	$V_{GND}4$	151	V_{GND}	181	$V_{GND}3$	211	$V_{GND}1$
122	VDATA4	152	PDATA0	182	$\overline{PJYEN}$	212	DDATA13
123	VDATA5	153	PROM	183	PJYCK	213	DDATA12
124	VDATA6	154	PMSC	184	PPACK	214	DDATA11
125	VDATA7	155	PMSD	185	PCSCK	215	DDATA10
126	VDATA8	156	PSSYN3	186	PCOCK	216	V_{DD}
127	VDATA9	157	PSDI3	187	PB0	217	DDATA9
128	V_{DD}	158	PSCLK3	188	PB1	218	V_{GND}
129	VDATA10	159	$V5_{DD}$	189	PPDCK	219	DDATA8
130	V_{GND}	160	PSDO3	190	$\overline{PPIEN}$	220	DDATA7
131	VDATA11	161	PSSYN2	191	$V_{DD}3$	221	$V_{DD}1$
132	$V_{GND}4$	162	PSDI2	192	$\overline{PPOEN}$	222	DDATA6
133	VDATA12	163	V_{DD}	193	$V_{GND}3$	223	$V_{GND}1$
134	$V_{DD}4$	164	PSCLK2	194	DDATA23	224	DDATA5
135	VDATA13	165	V_{GND}	195	DDATA22	225	DDATA4
136	VDATA14	166	PSDO2	196	$V_{DD}1$	226	DDATA3
137	VDATA15	167	PSSYN1	197	DDATA21	227	DDATA2
138	$V5_{DD}$	168	PSDI1	198	$V_{GND}1$	228	$V_{DD}1$
139	PDATA7	169	PSCLK1	199	DDATA20	229	DCLKO
140	$V_{DD}3$	170	PSDO1	200	V_{DD}	230	$V_{GND}1$
141	PDATA6	171	PSSYN0	201	DDATA19	231	DDATA1
142	$V_{GND}3$	172	PSDI0	202	V_{GND}	232	DDATA0
143	PDATA5	173	V_{DD}	203	DDATA18	233	$\overline{DBLNK}$
144	PDATA4	174	PSCLK0	204	DDATA17	234	$\overline{DVS}$
145	PDATA3	175	V_{GND}	205	$V_{DD}1$	235	$V_{DD}1$
146	$V_{DD}3$	176	PSDO0/TD0	206	DDATA16	236	$\overline{DCS}$
147	PDATA2	177	$\overline{PAXEN}$	207	$V_{GND}1$	237	$\overline{DHS}$
148	$V_{GND}3$	178	$\overline{PREQL}$	208	DDATA15	238	$V_{GND}1$
149	PDATA1	179	$\overline{PREQH}$	209	DDATA14	239	DCLKI
150	V_{DD}	180	$V_{DD}3$	210	$V_{DD}1$	240	V_{DD}

Packaging - Mechanical





SYMBOL	DIMENSION IN INCHES	DIMENSION IN MM
A1	.010 MIN	0.25 MIN
A2	.134 ± .004	3.40 ± .10
b	.006 MIN	0.16 MIN
	.011 MAX	0.28 MAX
C	0.13 MIN	.005 MIN
	0.25 MAX	.010 MAX
D	1.362 ± .008	34.60 ± 0.20
E	1.362 ± .008	34.60 ± 0.20
e	.020	0.50
D2	1.161	29.50
E2	1.161	29.50
L	.022 ± .004	0.56 ± 0.10
L1	.020 ± .004	.50 ± 0.10
Θ	0° – 7°	0° – 7°

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